CS2600

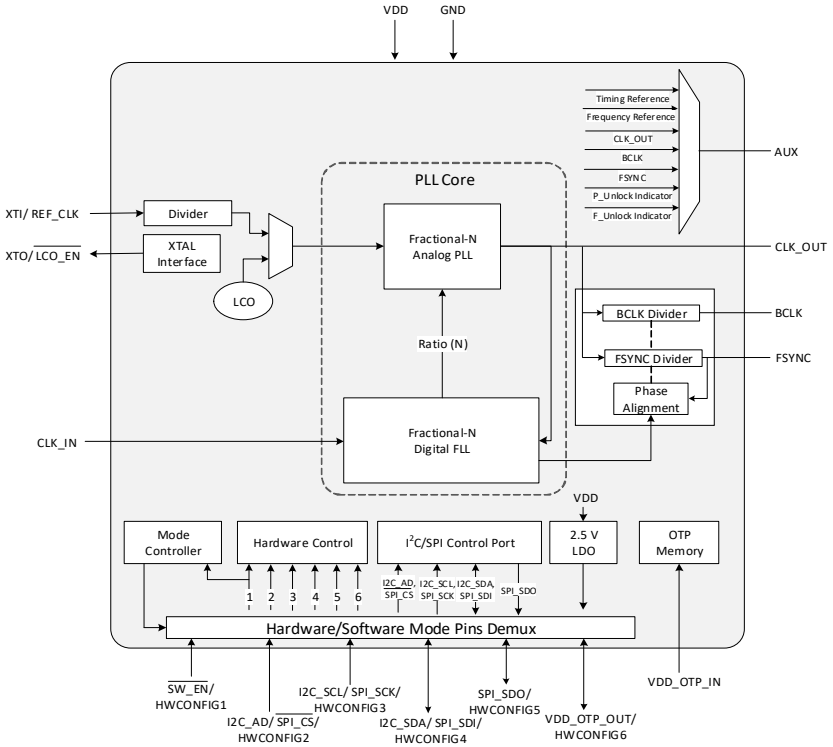
Fractional-N Clock Synthesizer and Clock Multiplier

Features

- Frequency synthesizer based on delta-sigma fractional-N analog PLL
  - Generates a low-jitter 6–75 MHz clock (CLK_OUT) from 8–75 MHz timing reference clock (REF_CLK)
- Clock multiplier and jitter reduction based on hybrid PLL
  - Generates a low-jitter 6–75 MHz clock (CLK_OUT) from a jittery or intermittent 50 Hz–30 MHz input clock source (CLK_IN)
- Highly accurate PLL multiplication factor
  - Less than 1 PPM
- I²C/SPI control port and hardware control mode
- Configurable auxiliary output
- Flexible sourcing of timing reference clock
  - External clock, external crystal, or built-in inductor-capacitor oscillator (LCO)
- Period jitter of 40 ps_{RMS} for REF_CLK and 35 ps_{RMS} for LCO
- Minimal board space required
  - No external analog loop-filter components
- Customer-programmable startup configuration, using integrated One-Time Programmable (OTP) memory
- Automatic rate control for digital audio applications
- BCLK and FSYNC outputs (derived from CLK_OUT) for digital audio applications can be aligned in phase with the clock source
- Glitchless clock outputs derived from an intermittent input clock

Applications

- Digital audio systems
- Network and USB audio interfaces
- IoT sensor and transducer systems
- Embedded systems
- Automotive audio systems



Target Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product.

PB1031R4
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General Description

The CS2600 is a system-clocking device that uses a programmable phase-locked loop (PLL). The hybrid analog/digital PLL architecture comprises a delta-sigma fractional-N analog PLL and a digital frequency-locked loop (FLL). The CS2600 enables frequency synthesis and clock generation from a stable timing reference clock. The device can generate low-jitter clocks from a noisy input clock source at frequencies as low as 50 Hz. The CS2600 outputs can be phase-aligned with the input clock source. An internal LCO can supply the timing reference clock if an external timing reference clock is not available. The CS2600 can be configured using a control interface supporting I²C and SPI modes of operation. The device can also operate in hardware mode, using the pull-up/pull-down resistors, reducing system software overhead.

The automatic rate control feature enables CS2600 to detect the frequency of the input clock among a set of sample rate frequencies. It then updates the PLL configuration to keep a stable output when the input clock dynamically changes.

The CS2600 provides a built-in OTP memory to configure the default operating settings, loaded at boot-up. The OTP memory is optimized and managed to allow for multiple programming cycles.

The CS2600 can be powered from a single 1.8 V or 3.3 V supply. The device combines high performance with low power consumption.

The CS2600 is available in commercial-grade, 16-pin QFN package for operation from –40°C to +85°C. The device is also available in the AEC-Q100-qualified grade-2 package for operation from –40°C to +105°C.

Table of Contents

1 Pin Assignments and Descriptions

These sections show pin assignments and describe pin functions.

1.1 QFN Package Drawing (Top View, Through Package)

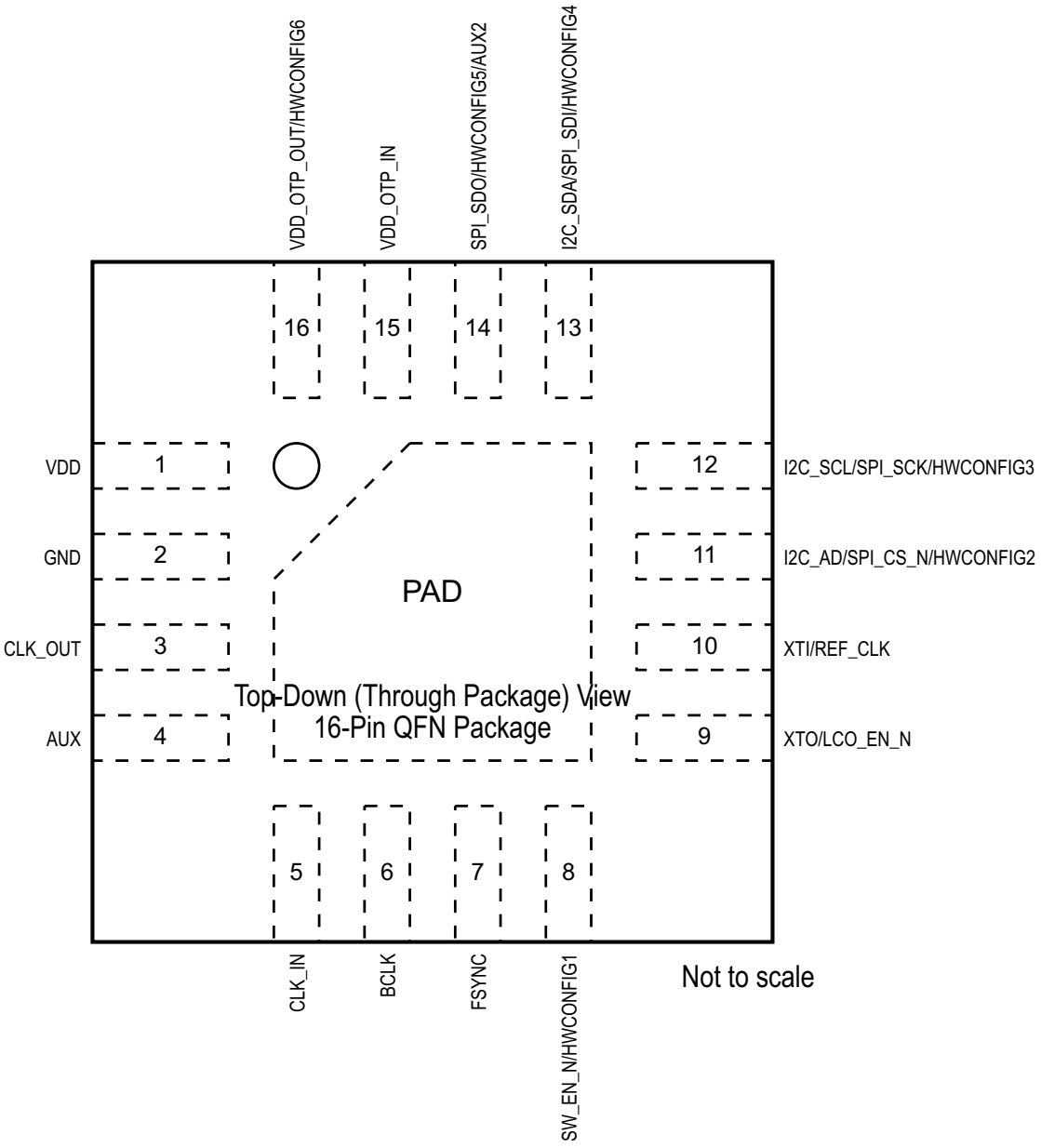


Figure 1-1. QFN 16-Pin Package Assignments (Top View, Through-Package)

1.2 Pin Descriptions

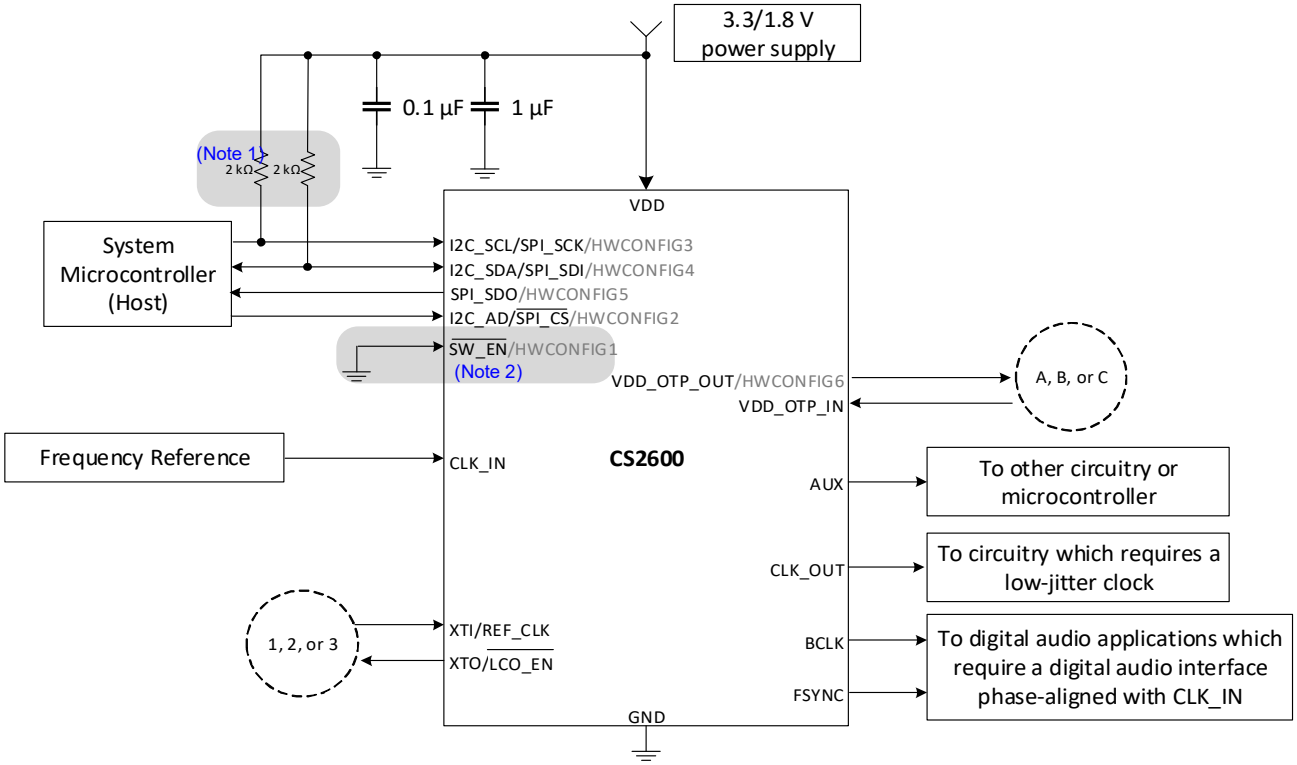
Table 1-1. Pin Descriptions

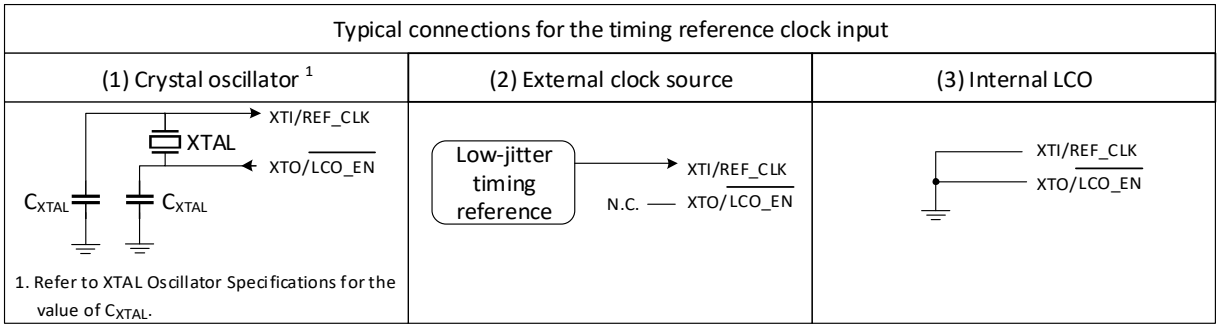
Pin Name	Pin #	Power Supply	I/O	Description	Internal Connection	State at Reset
VDD	1	—	—	**Power Supply.** 3.3 V/1.8 V supply for the digital and analog blocks.	—	—
GND	2, PAD	—	—	**Ground and Pad.** The paddle must be connected to ground plane directly underneath the CS2600.	—	—
CLK_OUT	3	VDD	O	**Clock Output.** PLL clock output.	—	—
AUX	4	VDD	O	**Auxiliary Output.** Configurable input/output clock or status output.	—	—
CLK_IN	5	VDD	I	**Clock Input.** Frequency reference input for the digital PLL.	—	—
BCLK	6	VDD	O	**BCLK Output.** PLL bit clock output (CLK_OUT derived), which can be phase-aligned with CLK_IN.	—	—
FSYNC	7	VDD	O	**FSYNC Output.** PLL frame sync clock output (CLK_OUT derived), which can be phase-aligned with CLK_IN.	—	—
$\overline{\text{SW\_EN}}$/HWCONFIG1	8	VDD	I	**Software Enable.** Active-low software mode enablement input. **Hardware Configuration 1.** Hardware mode configuration input.	—	—
XTO/$\overline{\text{LCO\_EN}}$	9	VDD	I/O	**Crystal Connection.** Output for an external crystal to generate the low-jitter PLL input clock. **Inductor-Capacitor Oscillator Enable.** Connected to ground if the internal LCO is used as the timing reference.	—	—
XTI/REF_CLK	10	VDD	I	**Crystal Connection.** Input for an external crystal to generate the low-jitter PLL input clock. **Reference Clock.** External low-jitter timing reference input clock.	—	—
I2C_AD/$\overline{\text{SPI\_CS}}$/HWCONFIG2	11	VDD	I	**I²C Control-Port Address.** Chip address input for the I²C interface. **SPI Control-Port Chip Select.** Active-low chip select input for the SPI interface. **Hardware Configuration 2.** Hardware mode configuration input.	—	—
I2C_SCL/SPI_SCK/HWCONFIG3	12	VDD	I	**I²C Control-Port Clock.** Clock input for the I²C interface. **SPI Control-Port Clock.** Clock input for the SPI interface. **Hardware Configuration 3.** Hardware mode configuration input.	—	—
I2C_SDA/SPI_SDI/HWCONFIG4	13	VDD	I/O	**I²C Control-Port Data.** Data input/output for the I²C interface. **SPI Control-Port Serial Data In.** SPI data input. **Hardware Configuration 4.** Hardware mode configuration input.	—	—
SPI_SDO/HWCONFIG5	14	VDD	I/O	**SPI Control-Port Serial Data Out.** SPI data output. **Hardware Configuration 5.** Hardware mode configuration input.	—	—
VDD_OTP_IN	15	—	—	**OTP Programming Supply (VDD = 1.8 V).** If VDD = 1.8 V, an external 2.5 V supply is required when writing to the OTP memory.	—	—
VDD_OTP_OUT/HWCONFIG6	16	VDD	I/O	**OTP Programming Supply (VDD = 3.3 V).** If VDD = 3.3 V, an internal LDO generates the required 2.5 V supply when writing to the OTP memory. **Hardware Configuration 6.** Hardware mode configuration input.	—	—

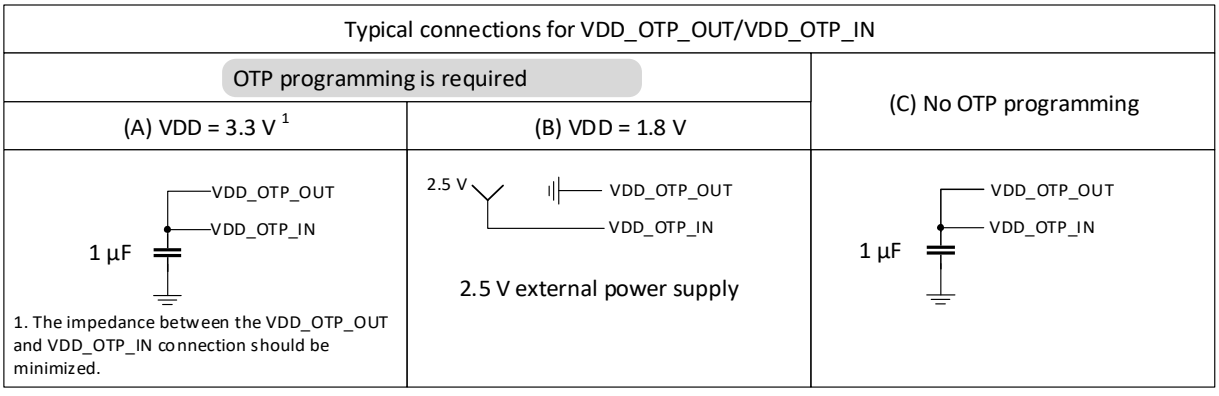
1.3 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS2600 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is to be qualified to current JEDEC ESD standards.

2 Typical Connection Diagrams







Unselected signals as part of multifunction pins are shown in gray.

Figure 2-1. Typical Connection Diagram — Software Mode

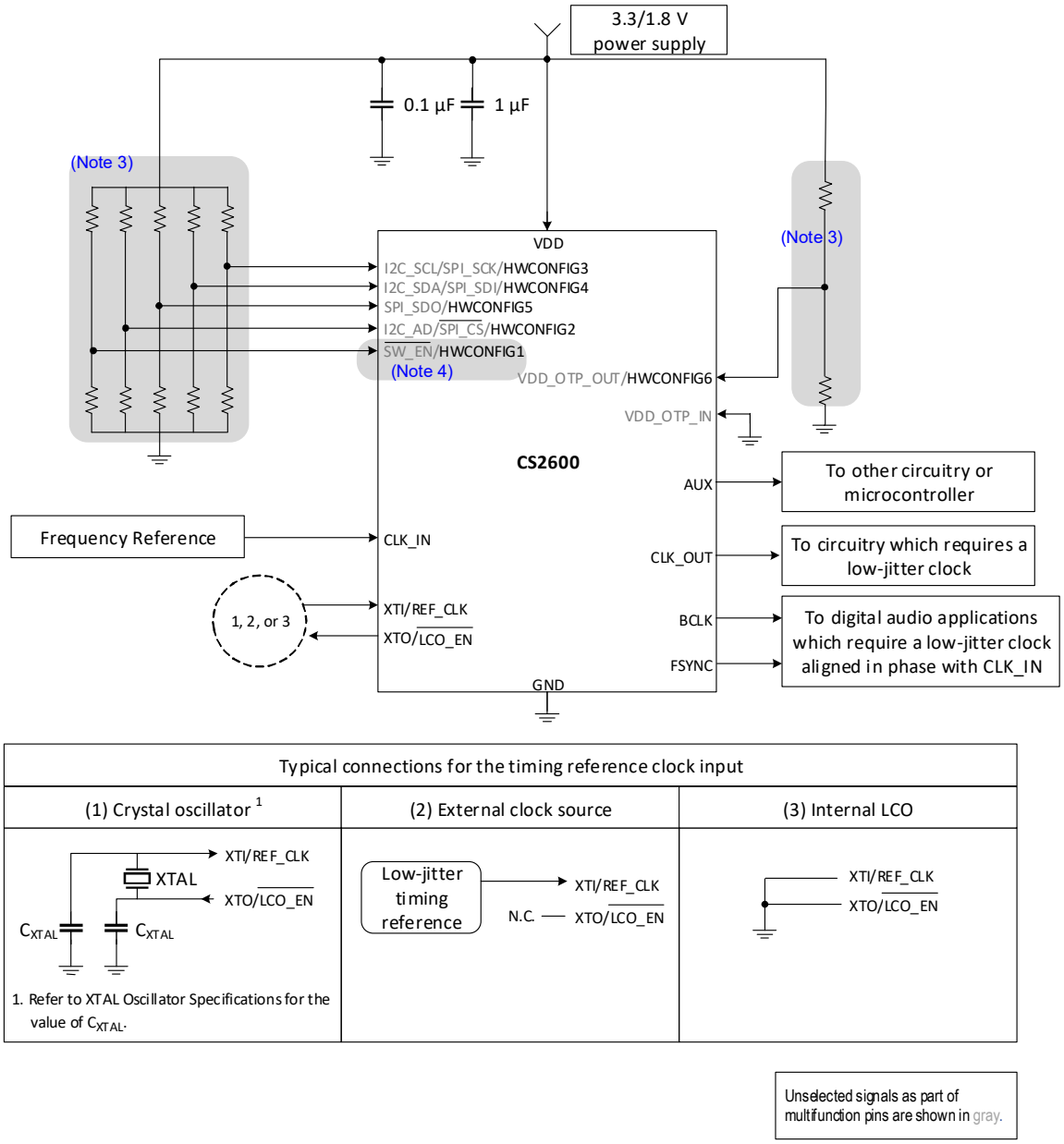


Figure 2-2. Typical Connection Diagram — Hardware Mode

Notes referenced in the typical connection diagrams:

1. The pull-up resistors are required only for I²C operation.
2. To enable the software mode, the $\overline{\text{SW\_EN}}$ pin must be connected to GND.
3. Each hardware pin is configured by connecting it to GND or VDD through a resistor providing up to eight configuration options per pin.
4. To enable the hardware mode, the HWCONFIG1 pin must not be connected to GND through a 0 Ω resistor. The pin should be connected to GND or VDD using the remaining configuration options.

3 Characteristics and Specifications

Table 3-1. Recommended Operating Conditions

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters		Symbol	Min	Typ	Max	Units
DC power supply [1]		VDD	3.13	3.3	3.47	V
			1.77	1.8	1.89	V
OTP write supply [2]		VDD_OTP	2.5	2.63	2.75	V
Supply ramp up/down (all supplies)		t_{PWR-UD}	0.01	—	10	ms
Ambient temperature	Commercial Grade	T_A	–40	—	85	°C
	AEC-Q100 Grade2		–40	—	105	°C

1. The system can be either powered with a 3.3 V or a 1.8 V DC power supply.
2. External supply for programming OTP is only needed for systems using 1.8 V DC power supply.

Table 3-2. Absolute Maximum Ratings

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters	Symbol	Min	Max	Units
DC power supply	VDD	–0.3	4.32	V
External voltage applied to digital input/output	V_{INDI}	–0.3	VDD + 0.3	V
Input current	I_{in}	—	±10	mA
Ambient temperature	T_A	–55	125	°C
Storage temperature	T_{STG}	–65	150	°C

Table 3-3. DC Electrical Characteristics

Test Conditions (unless specified otherwise): VDD = 3.3 V; T_A = 25°C; timing reference = external REF_CLK.

Parameters	Symbol	Min	Typ	Max	Units
Power supply current – unloaded [1]	I_{VDD}	—	3.94	TBD	mA
Power dissipation – unloaded	P_D	—	13	TBD	mW
Input leakage current (per pin)	I_{IN}	—	—	±10	µA
Input capacitance (per pin)	I_C	—	—	5	pF
High-level input voltage	V_{IH}	0.70 × VDD	—	—	V
Low-level input voltage	V_{IL}	—	—	0.30 × VDD	V
High-level output voltage	V_{OH}	0.90 × VDD	—	—	V
Low-level output voltage	V_{OL}	—	—	0.10 × VDD	V

1. To calculate the additional current consumption due to loading (per output pin), multiply clock output frequency by load capacitance (C_L) and power supply voltage (VDD).

Table 3-4. AC Electrical Characteristics

Test Conditions (unless specified otherwise): VDD = 3.3 V; T_A = –40°C to 85°C (commercial grade); T_A = –40°C to 105°C (AEC-Q100 grade-2); Load capacitance (C_L) = 15 pF.

Parameters		Symbol	Min	Typ	Max	Units
Crystal frequency Fundamental mode XTAL	RefClkDiv[1:0] = 10	f_{XTAL}	8	—	18.75	MHz
	RefClkDiv[1:0] = 01		16	—	37.50	MHz
	RefClkDiv[1:0] = 00		32	—	50	MHz
	Drive power		—	—	100	µW
	Negative resistance		500	—	—	Ω
	Maximum capacitance (C_{XTAL})[1]		—	—	50	pF
Reference clock input frequency	RefClkDiv[1:0] = 10	f_{REF_CLK}	8	—	18.75	MHz
	RefClkDiv[1:0] = 01		16	—	37.50	MHz
	RefClkDiv[1:0] = 00		32	—	75	MHz
Reference clock input duty cycle		D_{REF_CLK}	45	—	55	%
Clock input frequency		f_{CLK_IN}	50	—	30 ×10[6]	Hz
Clock input pulse width [2]	$f_{CLK\_IN} < f_{SYS\_CLK} / 96$	pw_{CLK_IN}	2	—	—	UI
	$f_{CLK\_IN} > f_{SYS\_CLK} / 96$		10	—	—	ns
PLL clock output frequency [3]		f_{CLK_OUT}	6	—	75	MHz
BCLK frequency range [4]		f_{BCLK}	$f_{CLK\_OUT} / 48$	—	f_{CLK_OUT}	MHz
FSYNC frequency range [5]		f_{FSYNC}	$f_{CLK\_OUT} / 1536$	—	$f_{CLK\_OUT} / 16$	MHz
PLL clock output duty cycle	Measured at VDD / 2	t_{OD}	45	50	55	%

Table 3-4. AC Electrical Characteristics *(Cont.)*

Test Conditions (unless specified otherwise): VDD = 3.3 V; T_A = –40°C to 85°C (commercial grade); T_A = –40°C to 105°C (AEC-Q100 grade-2); Load capacitance (C_L) = 15 pF.

Parameters		Symbol	Min	Typ	Max	Units
Clock output rise time	20% to 80% of VDD	t_{OR}	—	1.7	3.0	ns
Clock output fall time	80% to 20% of VDD	t_{OF}	—	1.7	3.0	ns
Period jitter [6]	REF_CLK LCO	t_{JIT}	— —	40 35	— —	ps_{RMS} ps_{RMS}
Baseband TIE jitter (100 Hz to 40 kHz) [6, 7]	REF_CLK LCO	—	— —	50 300	— —	ps_{RMS} ps_{RMS}
Wideband TIE jitter (100 Hz Corner) [6, 8]	REF_CLK LCO	—	— —	165 300	— —	ps_{RMS} ps_{RMS}
PLL lock time – CLK_IN [9]	f_{CLK_IN} < 200 kHz f_{CLK_IN} > 200 kHz	t_{LC}	— —	100 1	200 3	UI ms
PLL lock time – REF_CLK	f_{REF_CLK} = 8 to 75 MHz	t_{LR}	—	1	3	ms
Output frequency resolution [6, 10]	High resolution High multiplication	F_{err}	0 0	— —	±0.50 ±112	ppm ppm
LCO frequency		—	—	TBD	—	Hz
LCO frequency accuracy at 25°C		—	—	±1	—	%
LCO thermal frequency drifting at 25°C		—	TBD	50	TBD	ppm/°C
CLK_IN to FSYNC phase error [11]		—	—	—	TBD	ns
CLK_OUT, BCLK, and FYNC phase offset		—	—	—	±1	ns
Phase alignment CLK_IN frequency [12]		—	50	—	1×10^6	Hz
Time to first locked clock output [13]	After boot-up	—	—	—	20	ms
Maximum output frequency deviation [14]		—	—	—	TBD	%

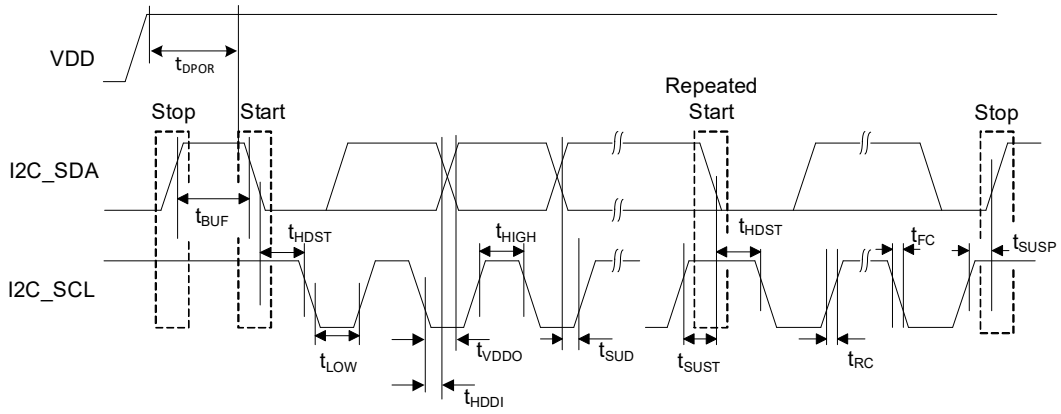
1. Refer to XTAL oscillator specifications for the value of C_{XTAL}.
2. UI (unit interval) corresponds to t_{SYS_CLK} or 1 / f_{SYS_CLK}.
3. f_{CLK_OUT} = 75 MHz is ratio-limited when f_{CLK_IN} is below 72 Hz (high multiplication) or 18.3 kHz (high precision).
4. BCLK output is derived from CLK_OUT using a frequency divider. Available ratios for f_{BCLK} are 1, 1/2, 1/3, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, 1/32, and 1/48.
5. FSYNC output is derived from CLK_OUT using a frequency divider. Available ratios for f_{FSYNC} are 1/16, 1/32, 1/64, 1/128, 1/192, 1/256, 1/512, 1/1024, 1/384, 1/768, and 1/1536.
6. REF_CLK is a 12 MHz timing reference clock. If the phase noise of REF_CLK is 20 dB lower than the output clock's noise across the bandwidth spectrum, the clock is considered jitter-free. The clock output frequency (f_{CLK_OUT}) is 24.576 MHz and sample size is 10000.
7. 3rd order 100 Hz – 40 kHz bandpass filtered according to AES-12id-2020 section 3.4.2.
8. 3rd order 100 Hz high pass filtered according to AES-12id-2020 section 3.4.1.
9. UI corresponds to t_{CLK_IN} or 1 / f_{CLK_IN}.
10. The frequency accuracy of the PLL clock output is directly proportional to the accuracy of the input clocks.
11. This parameter is relevant when CLK_IN to FSYNC phase alignment is enabled.
12. To enable the phase alignment feature, the CLK_IN frequency should be between the specific min and max values.
13. The time to first locked clock o/p is calculated for f_{CLK_IN} = 48 kHz and lock time = 100 UI.
14. This parameter refers to the maximum frequency deviation in the Multiplier mode after the CLK_IN signal is lost and before the dynamic ratio is fixed.

Table 3-5. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise): VDD = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds; T_A = 25°C.

Parameters [1]	Symbol	Min	Max	Units
SCL clock frequency	f_{SCL}	—	1000	kHz
Clock low time	t_{LOW}	500	—	ns
Clock high time	t_{HIGH}	260	—	ns
Start condition hold time (before first pulse clock)	t_{HDST}	260	—	ns
Setup time for repeated start	t_{SUST}	260	—	ns
Rise time of SCL and SDA	t_{RC}	600 180 72	1000 300 120	ns ns ns
Fall time SCL and SDA	t_{FC}	6.5 6.5 6.5	300 300 120	ns ns ns
Rise time variation between SDA and SCL	—	—	1.67	x
Fall time variation between SDA and SCL	—	— — —	100 100 75	ns ns ns
Setup time for stop condition	t_{SUSP}	260	—	ns
SDA setup time to SCL rising	t_{SUD}	50	—	ns
SDA input hold time from SCL falling [2]	t_{HDDI}	0	—	ns
Output data valid (Data/ACK) [2]	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions	t_{BUF}	500	—	ns
SDA bus capacitance	C_B	—	400	pF
SCL/SDA pull-up resistance	R_P	500	—	Ω
Pulse width of spikes to be suppressed	t_{ps}	0	50	ns
Delay from supply voltage stable to control port ready	t_{DPOR}	—	5	ms

1. I²C control-port timing.



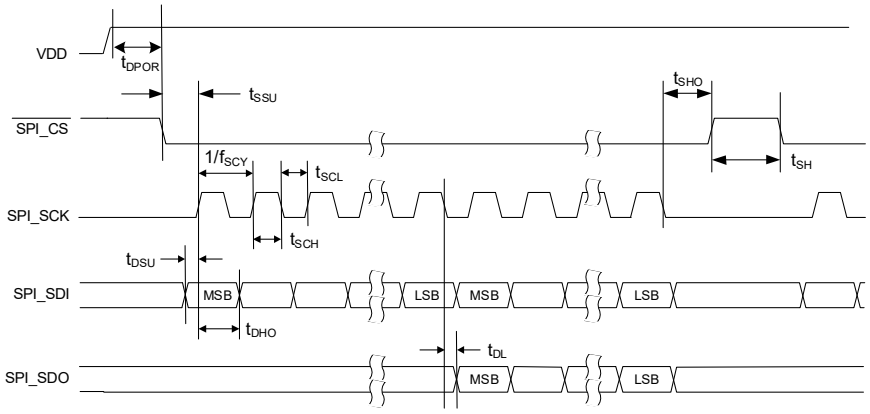
2. Data must be held long enough to bridge the transition time (t_{FC}) of SCL.

Table 3-6. Switching Specifications—SPI Control Port

Test conditions (unless specified otherwise): VDD = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds; T_A = 25°C.

Parameters [1]	Symbol	Min	Max	Units
SCK clock frequency	f_{SCL}	—	24	MHz
$\overline{CS}$ falling edge to SCK rising edge	t_{SSU}	5	—	ns
SCK falling edge to $\overline{CS}$ rising edge	t_{SHO}	0.5	—	ns
SCK pulse width low	t_{SCL}	18.5	—	ns
SCK pulse width high	t_{SCH}	18.5	—	ns
SDI to SCK rising setup time	t_{DSU}	5	—	ns
SDI to SCK hold time	t_{DHO}	2.5	—	ns
SCK falling edge to SDO transition	t_{DL}	0	15	ns
$\overline{CS}$ rising edge to SDO output high-Z	—	0	15	ns
Bus free time between active $\overline{CS}$	—	5	—	ms
Delay from supply voltage stable to control port ready [2]	t_{DPOR}	—	5	ms

1.SPI control-port timing.



2.The supply voltage is considered stable after VDD is within the specified operating conditions (see Table 3-4).

4 Revision History

Table 4-1. Revision History

Revision	Change
R4 JUL 2023	• Initial revision

Important:

Please check to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.