AN300

CS3001/2/11/12 & CS3003/4/13/14 Chopper-stabilized Operational Amplifiers

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1. INTRODUCTION

Cirrus Logic offers a variety of low-voltage CMOS chopper-stabilized amplifiers.

The chopper-stabilized amplifiers designed at Cirrus Logic are unique. These amplifiers offer performance benefits that combine the best features of bipolar amplifiers with the best features of chopper amplifiers. The intent of this application note is to understand Cirrus Logic's unique technology and to see how it can be applied in various measurement applications. But before the applications are discussed, the following provides a brief overview of the concepts involved in a chopper-stabilized amplifier.

2. CHOPPER AMPLIFIER AND CHOPPER-STABILIZED AMPLIFIER BASICS

Not everyone is familiar with chopper amplifiers and chopper-stabilized amplifiers. A look back at some history can help us understand how the chopper-stabilized amplifier operates.

Figure 1 illustrates the block diagram of a chopper-stabilized amplifier. A chopper-stabilized amplifier is a DC amplifier whose offset is stabilized by a chopping amplifier. The basic amplifier diagram in Figure 1 is called the Goldberg configuration, named after E. A. Goldberg, an engineer who designed and patented electron tube-based, chopper-stabilized amplifiers for RCA (Radio Corporation of America) in the 1940s and 1950s.

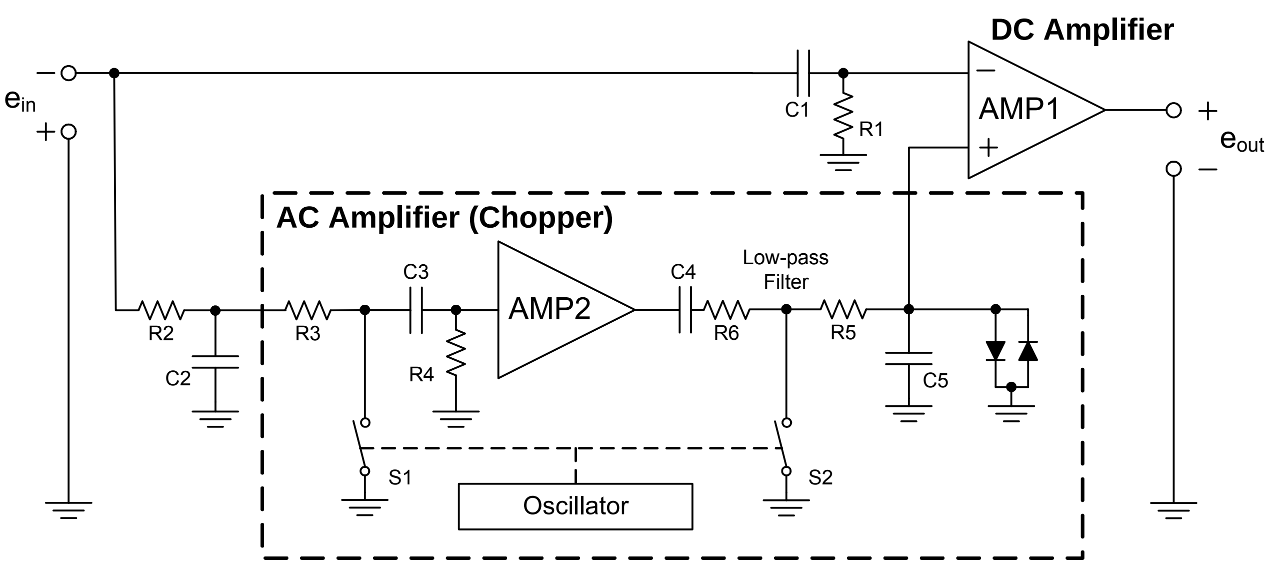


Figure 1. Basic Chopper-stabilized Amplifier Block Diagram

The Goldberg configuration was later used in a transistorized chopper-stabilized amplifier designed and sold by Zeltex Corporation in the 1970s for about $125 (US). The Zeltex chopper-stabilized amplifier follows the basic block diagram of Figure 1. The input signal (e_{in}) at the inverting input of the amplifier travels through two different signal paths. (The Goldberg configuration amplifier could only be used as an inverting amplifier.) The first path is into Amplifier #1 of Figure 1. Components R1-C1 act as a high-pass filter that prevents the DC portion of the signal from passing directly into Amplifier #1. The second path is through a low-pass filter composed of R2 and C2. The R2-C2 filter limits the bandwidth of the signal to be chopped by the chopper amplifier. Amplifier #2 is the chopper amplifier. The chopper amplifier is really a modulation system in which the DC and very low-frequency portion of the input signal is alternately turned on and off. This results in the signal being modulated at the carrier (chopping) frequency. An oscillator in the chopper amplifier toggles switches S1 and S2 on and off simultaneously. When switch S1 is conducting, the input to the chopper amplifier is ground. When switch S1 is off, the input signal is allowed to pass into Amplifier #2. The effect of chopping is to turn the DC input signal into a square wave (AC) signal whose amplitude changes between ground and the amplitude of the input signal. This signal is then amplified by the AC amplifier. Once the signal is amplified as an AC signal, it is restored to ground reference by the output chopping switch. This resulting signal, which is a ground-referenced square wave, is then filtered with a low-pass filter composed of resistors R5 and R6 in conjunction with capacitor C5. The corner frequency of this filter is very low – typically only fractions of a Hertz. The time constant must be very long to maintain the voltage on the filter capacitor over the half cycle when the chopped signal is not presented to the output filter.

Figure 2 illustrates the DC amplifier portion of the Zeltex device. This amplifier was constructed with a matched bipolar transistor pair as the front end. The open loop gain of the DC amplifier is about 94 dB.

Figure 3 illustrates the actual chopper amplifier portion of the Zeltex amplifier. The amplifier AC gain is about 3000, but because the signal is on only 50% of the time, the effective gain is only half as much. Therefore the AC amplifier gain is about 1500, or about 63 dB. The chopping oscillator operates at about 200 Hz. Note that the chopper output is filtered by a low-pass filter with an extremely low corner frequency.

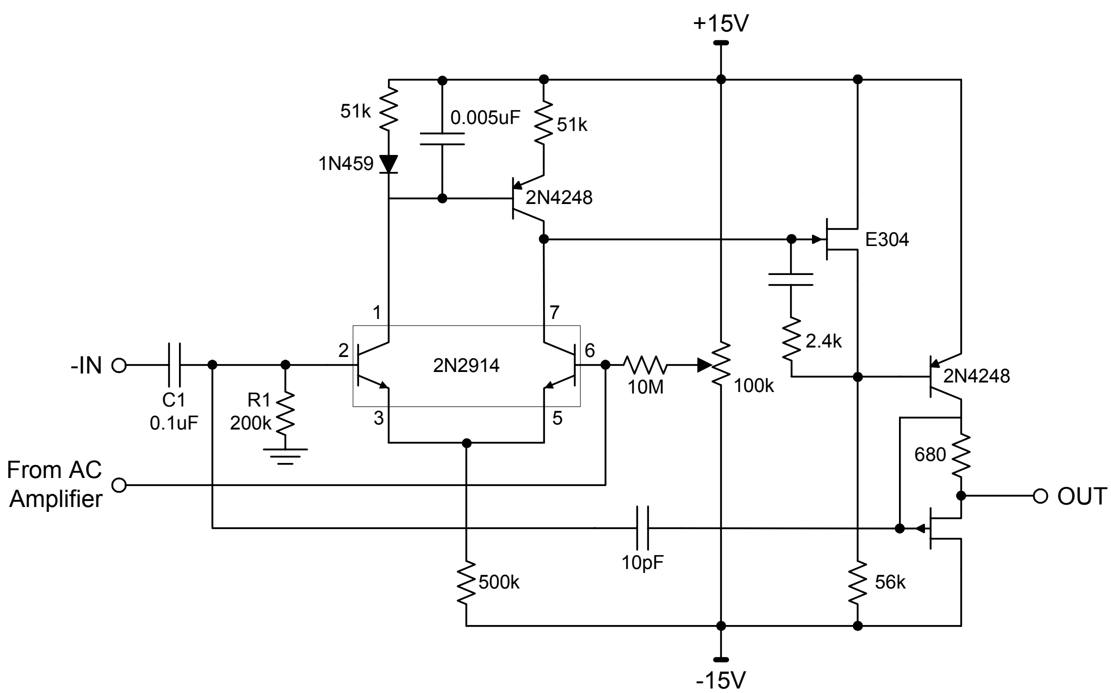


Figure 2. Amplifier 1: DC Amplifier Portion of the Zeltex Module

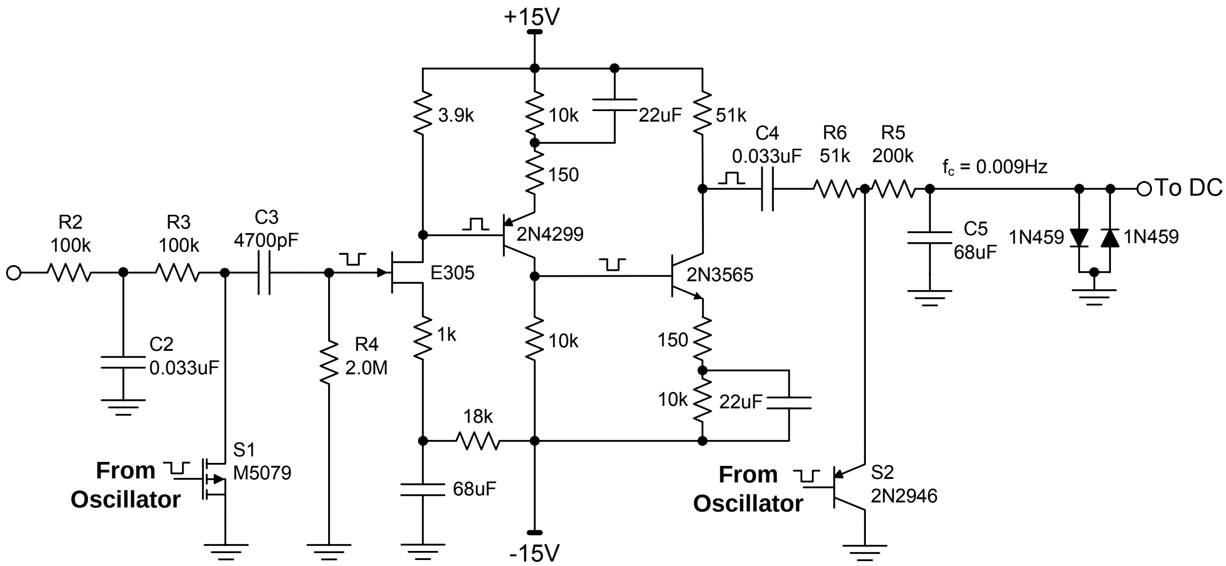
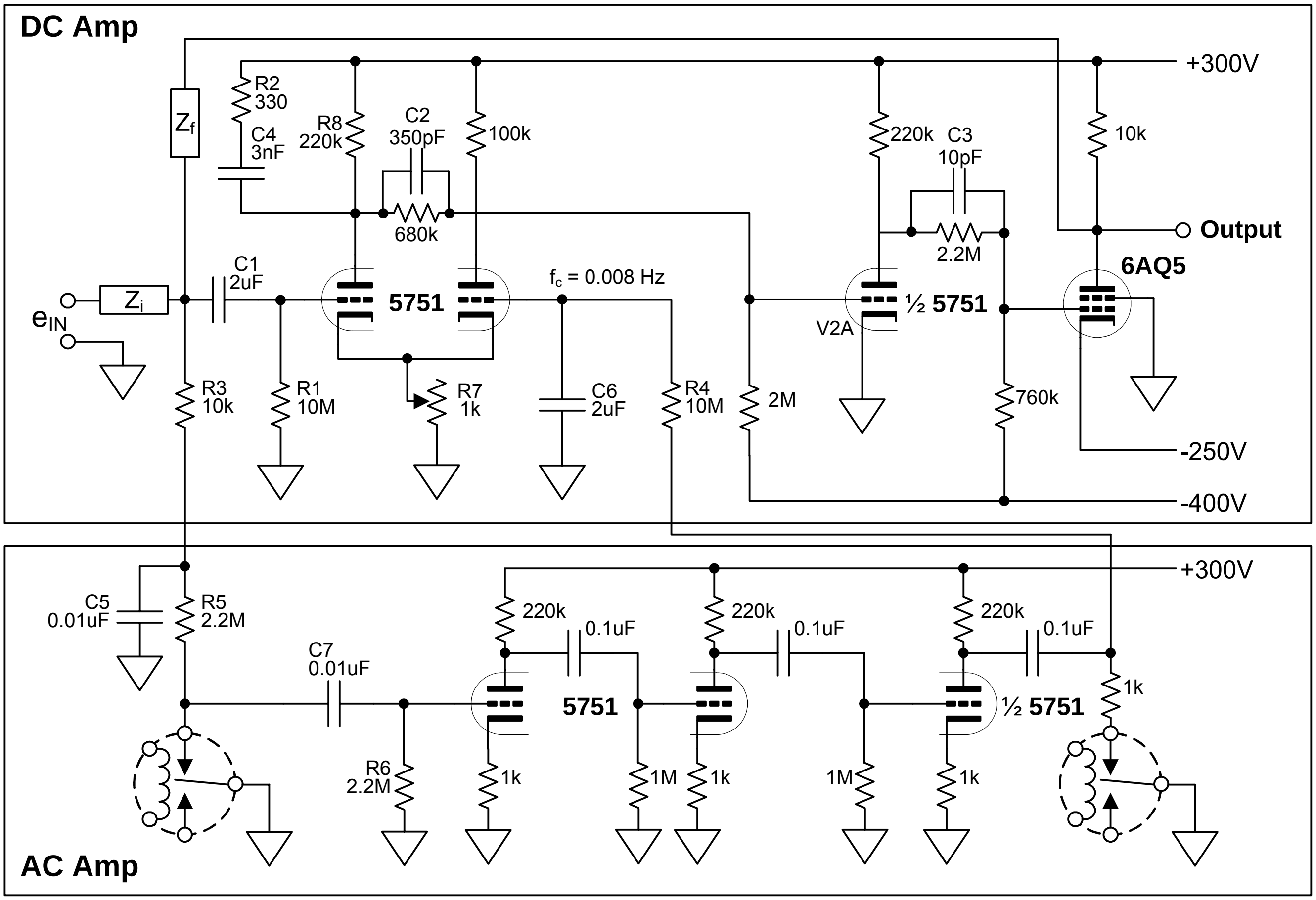


Figure 3. Amplifier 2: Chopper Amplifier Portion of the Zeltex Module

The gain transfer functions of the two amplifiers are multiplied together (or added when stated in dB). The combination of the two amplifiers produces an open loop gain of about 160 dB. One of the difficulties in the design of the chopper-stabilized amplifier combination is ensuring stability. The DC performance of the combined amplifiers is dictated by the performance of the chopping input. Input current of the Zeltex amplifier was dominated by charge injection in the chopping switch at the input of the chopper amplifier. Offset voltage and offset voltage drift of the amplifier combination was determined by how close the chopping switch at the input of the chopper amplifier approximated the ideal. The Zeltex amplifier achieved less than 100 pA of input bias current with an offset voltage drift less than 50 nV / °C.

Figure 4 illustrates a typical chopper-stabilized amplifier designed using electron tubes with the amplifiers connected in the Goldberg configuration. The circuit has the same layout as the block diagram of Figure 1. The chopping switches were mechanical vibrating switches (about 400 Hz) manufactured by Airpax Corporation. The output filter exhibits an extremely long time constant.

E.A. Goldberg filed a U.S. patent (#2,684,999; assigned to RCA) for a tube-based chopper-stabilized amplifier on April 28, 1948. But the invention of the chopper architecture itself predates this. J. W. Milnor filed for a U.S. patent on a chopper amplifier on January 17, 1918.



NOTE: 5751 = Ruggedized 12AX7.

Figure 4. Chopper-stabilized Amplifier Using Electron Tubes and Mechanical Vibrating Switches

3. MODERN CHOPPER-STABILIZED AMPLIFIERS

Monolithic chopper-stabilized amplifiers became available in the late 1970s. Different chopping architectures have been promoted by various vendors. The various architectures will not be examined in detail here. Before discussing the particulars of the Cirrus Logic chopper-stabilized amplifiers, it will be beneficial to understand some differences found in bipolar versus MOS transistors.

For many years bipolar transistors dominated monolithic amplifier designs. Bipolar transistors have some distinct advantages over CMOS transistors for some performance parameters. The bipolar transistor provides higher transconductance (I/V gain) for a specific value of operating current. The bipolar device, because of its construction, also provides lower noise than can easily be achieved in a MOS transistor, for devices of similar silicon area. The wide band spot noise level is lower in the bipolar transistor. And a much lower 1/f noise corner can be achieved in a bipolar transistor. Bipolar transistors can also be better matched when manufactured together on the same silicon die.

Most recently, the most prominent semiconductor processes being developed to shrink the geometry size of devices is being applied to CMOS technology. CMOS is favored because it can provide lower power consumption for massive digital chips with millions of transistors. Smaller transistors mean the availability of more transistors in a given area of silicon. This results in smaller device package sizes. In the last decade, more analog and mixed signal devices have been designed to take advantage of the smaller geometry CMOS processes. This includes monolithic amplifiers based upon CMOS processes.

As mentioned previously, bipolar transistors have long dominated the world of operational amplifiers. Let's look at some of the differences of parameters of bipolar transistors versus MOS transistors. Understanding the differences between these two technologies can help explain some of the constraints on the architectural choices used in the design of CMOS chopper-stabilized amplifiers.

The construction of bipolar transistors and MOS transistors are very different. The difference in construction results in large differences in some performance parameters. One area of significant difference is noise performance.

Figure 5 illustrates a noise plot for a bipolar transistor. This hypothetical but typical device exhibits a spot noise at 1 kHz of 4 nV/$\sqrt{Hz}$ with a 1/f corner at 2.5 Hz. Because of the difference in construction, a MOS transistor would have difficulty achieving this level of noise performance. Figure 6 illustrates a noise plot for a hypothetical but typical MOS transistor. This device exhibits a spot noise of 17 nV/$\sqrt{Hz}$ at 50 kHz with a 1/f corner at 2000 Hz.

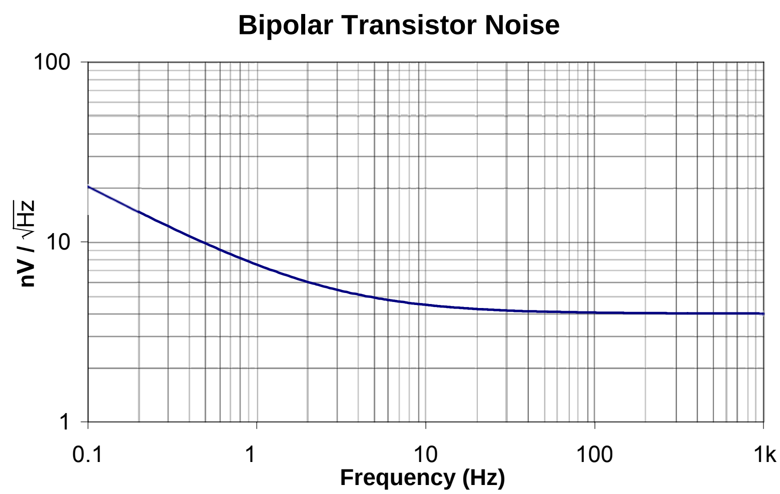


Figure 5. Noise Performance Plot for a Bipolar Transistor

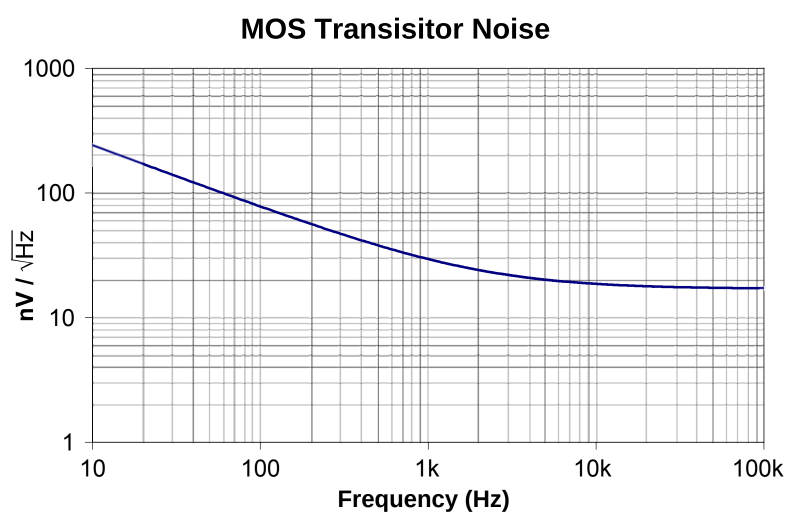


Figure 6. Noise Performance Plot for a MOS Transistor

Note from Figure 5 that the magnitude of the noise of the bipolar transistor at 0.1 Hz is about 20 nV/$\sqrt{Hz}$. The spot noise in the example MOS transistor does not match this 20 nV/$\sqrt{Hz}$ value until the frequency for the MOS transistor is at about 5 kHz. A MOS transistor can be designed to achieve a lower spot noise and a lower 1/f corner frequency than what is shown in Figure 6 by significantly increasing the size of the device and by increasing its operating current. But there is another approach to achieve low noise in a CMOS amplifier. That is to modulate (chop) the input signal and amplify the signal as an AC signal at a frequency that is significantly higher than the 1/f corner frequency. If the chopping is performed at a higher frequency where the spot noise is low, the noise floor will be dictated by the noise value at the chopping frequency. The chopper-stabilized amplifiers from Cirrus Logic use this approach. Most chopper amplifiers from other manufacturers chop at lower frequencies, where the spot noise is higher. Some choppers even chop in the region of the rising 1/f noise.

Cirrus Logic manufactures amplifiers having different chopper-stabilized architectures. The CS3003/4/13/14 amplifiers are similar to the architecture shown in Figure 1, but with the design optimized for silicon implementation. A block diagram of these devices is illustrated in Figure 7. The chopping frequency in the CS3003/4 devices is at about 150 kHz. The CS3013/14 chopping frequency is at about 125 kHz. The filter at the output of the chopping amplifier is on chip where capacitor sizes are limited. A higher chopping clock is more easily filtered when capacitor size of the filter must be a small value. These amplifiers combine chopper-stabilized input performance with rail-to-rail input and rail-to-rail output capability. Even though these amplifiers are chopped, they can be used for audio-bandwidth applications because no chopping clock residuals exist below 100 kHz.

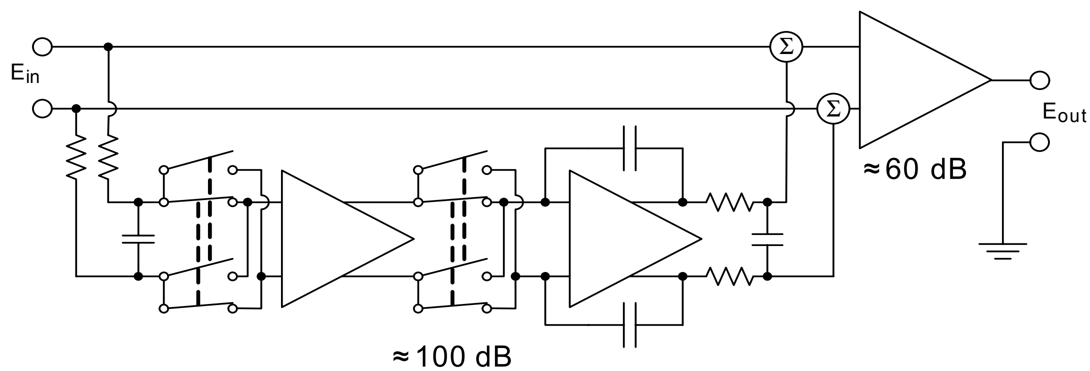


Figure 7. Block Diagram of Cirrus Logic's Chopper-stabilized Amplifier, CS3003/04/13/14

Figure 8 illustrates the open loop gain and phase of the CS3003/04 amplifiers. One can readily see from the plot that the transition point between the chopper amplifier signal path and the high frequency signal path cross over near 20 kHz.

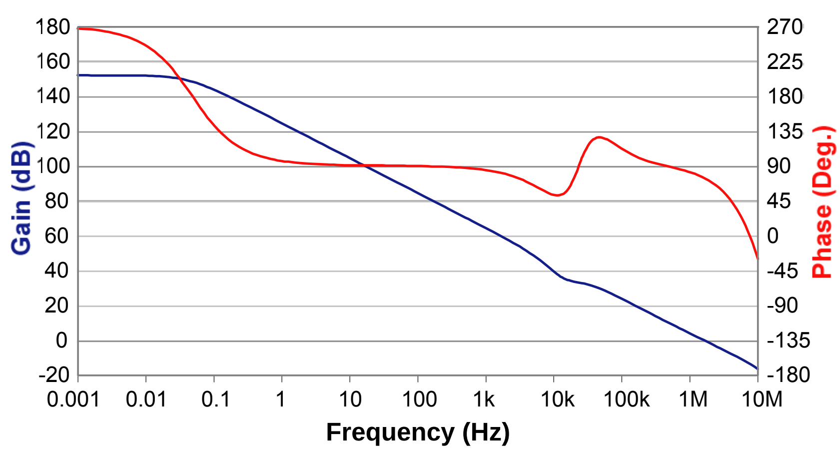


Figure 8. CS3003/04 Gain & Phase vs. Frequency

Recall that the gains of the amplifier stages add together (in dB). The combination requires careful design to maintain stability and to achieve the proper frequency crossover between the two signal paths. But the result is an amplifier with very high open loop gain.

The CS3001/2/11/12 amplifiers differ architecturally from the CS3003/04/13/14 devices. The CS3001/2/11/12 amplifiers have more signal paths than the typical chopper-stabilized amplifier. Figure 9 illustrates the signal paths inside the Cirrus Logic CS3001/2/11/12 amplifiers. Note that although not shown in the diagram, the signal is chopped as a differential signal.

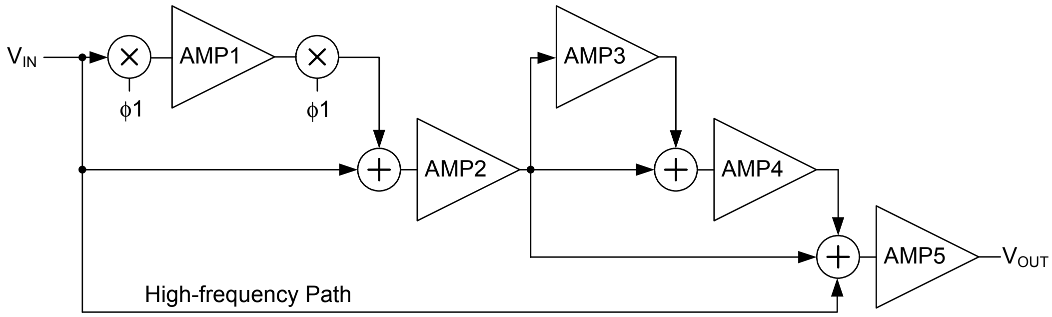


Figure 9. Block Diagram of Cirrus Logic's Multipath Chopper-stabilized Amplifier, CS3001/02/11/12

The "multi-path" approach to these amplifiers was used to achieve 300 dB of open loop gain. These amplifiers can be made stable for gains higher than 50X with a single feedback capacitor. They offer significant improvement over competing amplifiers when an amplifier with low noise, low offset drift and very high open loop gain is required for an application. Figure 10 illustrates the open loop gain and phase of the CS3001/2/11/12 amplifiers. Figure 11 illustrates an expanded view of the region of the open loop gain and phase above 10 kHz.

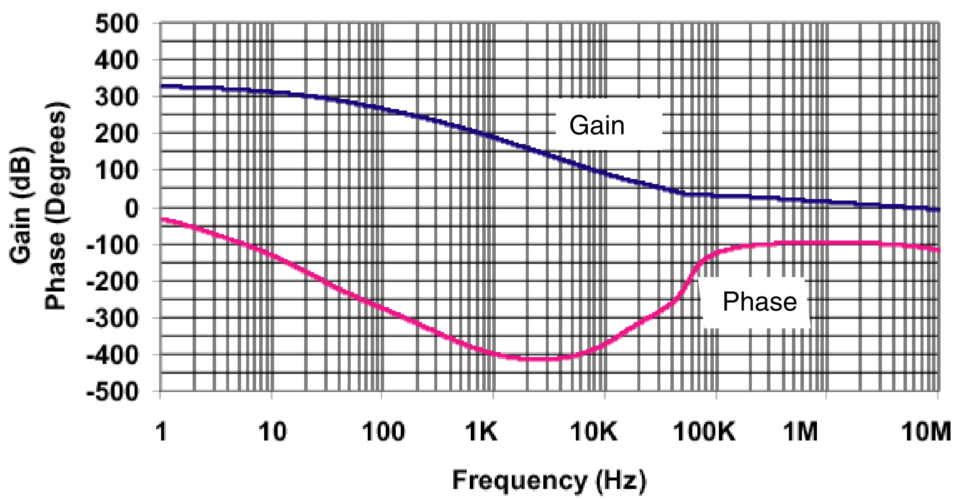


Figure 10. Open-loop Gain and Phase vs. Frequency, CS3001/02/11/12

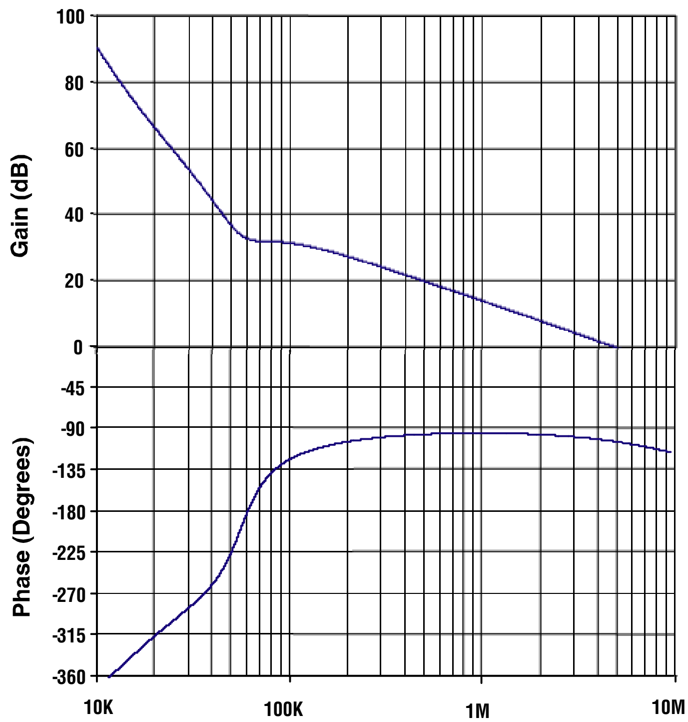


Figure 11. Open-loop Gain and Phase vs. Frequency, CS3001/02/11/12 (Expanded)

In applications that require a small signal (< 10 mV) to be amplified by a large gain (> 200X) the very high open loop gain of the CS3001/2/11/12 amplifiers ensures gain accuracy and excellent linearity. Figure 12 compares the open loop gain of the CS3001 to an operational amplifier with 120 dB of open loop gain where the amplifiers are configured for a gain of 400X (52 dB). If the CS3001 is configured for a gain of 400X (52 dB), the amplifier has 248 dB of loop gain (300 - 52 = 248) to ensure gain accuracy and to reduce linearity errors. 248 dB is a factor of 2500 billion. This appears to be excessive until one understands that the CS3001 was designed to achieve 20-bit linearity with a 1 kHz sine wave when set for a closed loop gain of 30X.

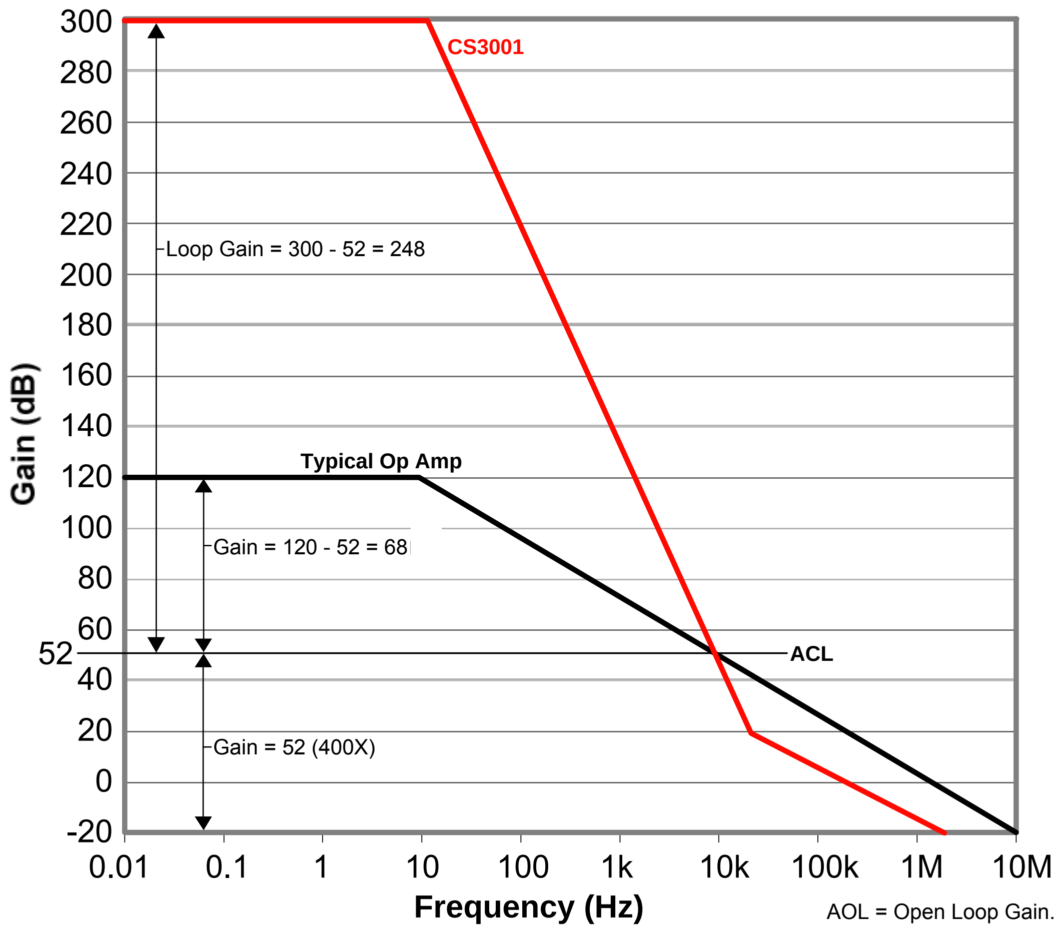


Figure 12. Open Loop Gain Comparison

If an operational amplifier with only 120 dB of open loop gain is configured for a forward gain of 400X (52 dB). This leaves only 68 dB of loop gain. A loop gain 68 dB is a factor of about 2500. Therefore, this amplifier set for a closed loop gain of 52 dB, would be able to reduce open loop linearity error by a factor of 2500. This factor is a billion times less (that is 1,000,000,000 times less) than what the CS3001 can achieve in the same configuration.

Figures 13 and 14 illustrate the noise performance of the CS3001/2 amplifiers. Figure 13 illustrates the extreme low-frequency noise performance of the CS3001/2. This plot is based upon a real measurement taken over an 18 hour period. Have you ever seen a data sheet for an operational amplifier from another vendor show a plot of noise below 0.1 Hz? Unlikely, because 0.1 Hz is arbitrarily considered the point of transition between examining the effects of 1/f noise versus the effects of offset drift due to temperature changes. This plot is possible for the CS3001/2/11/12 series amplifiers from Cirrus Logic only because of the very low drift due to chopping along with low-noise performance.

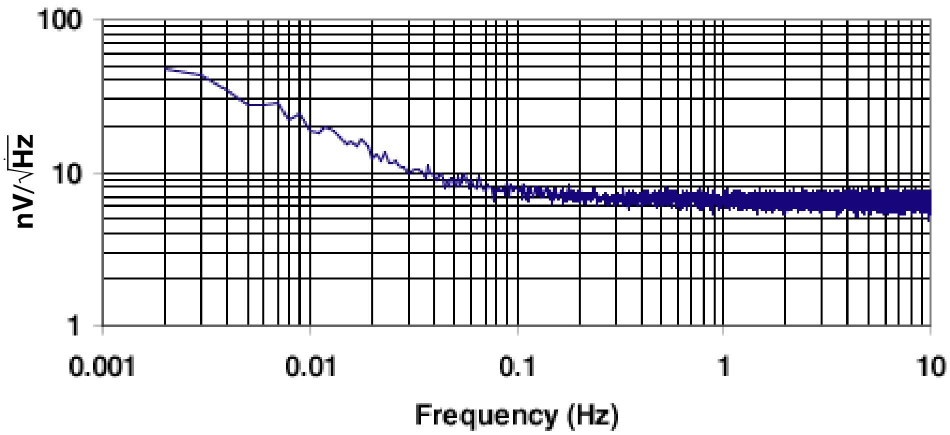


Figure 13. CS3001/02 Low-frequency Noise (Measured)

Figure 14 illustrates the noise behavior of the CS3001/2 as the frequency increases above 2 kHz. The CS3001/2 devices are designed to be used for low frequency (less than 2 kHz) applications. The CS3001/2 design achieves a significant reduction in power consumption by lowering the operating current of the last amplifier stage. This compromise causes the noise in the device to rise at frequencies above 2 kHz. This noise can be removed by filtering. Some delta-sigma A/D converters have digital filters that can remove the noise above 2 kHz.

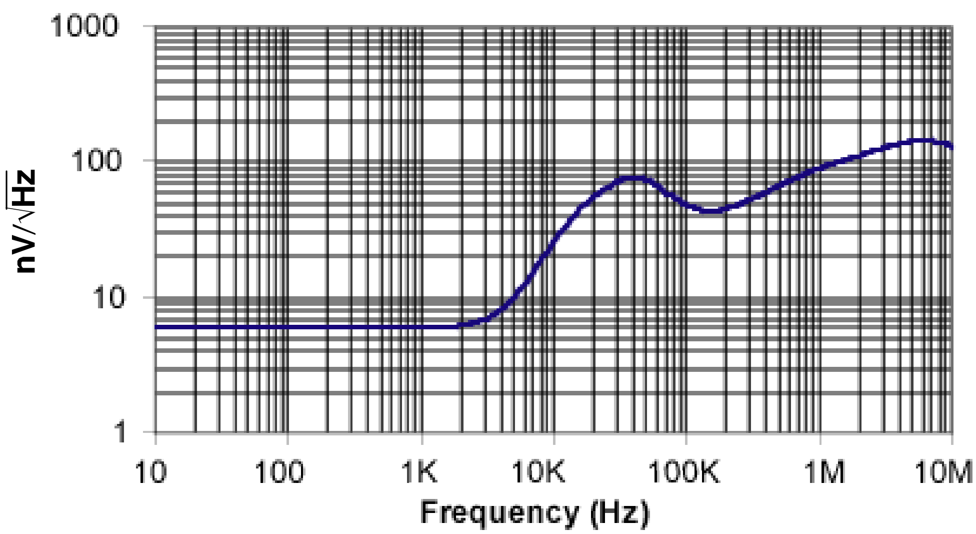


Figure 14. CS3001/02 Wideband Noise

Figure 15 illustrates the offset stability of the CS3001/2 over time. This plot was based upon band limiting the amplifier to 3.2 Hz and measuring the amplifier output for an hour. The fact that the plot of the statistical distribution of the noise out of the amplifier over an hour remains Gaussian validates that the offset of the amplifier is not moving over the time period.

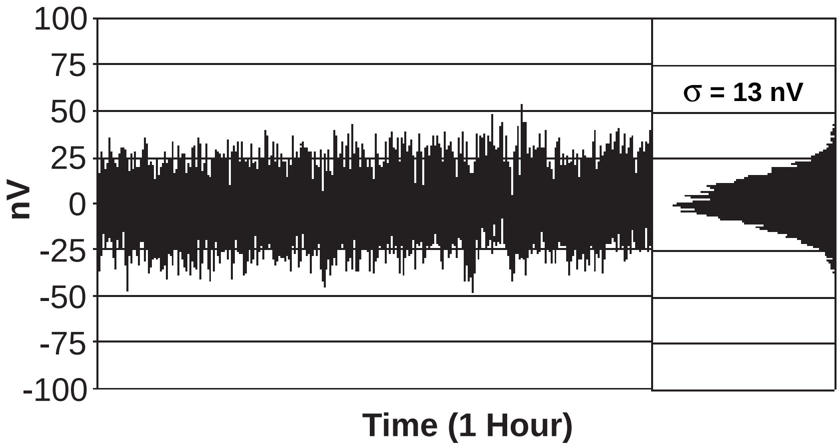


Figure 15. Offset Voltage Stability (DC to 3.2 Hz)

The CS3001/2/11/12 and CS3003/4/13/14 devices all use chopping clock frequencies greater than 100 kHz. This allows the clock to be more easily filtered on-chip.

Table 1 summarizes the typical amplifier specification parameters for the Cirrus Logic's chopper-stabilized amplifiers.

Table 1. Typical Specifications for Cirrus Logic Chopper-stabilized Amplifiers

Device	Amps	GBW	Slew Rate (V/ S)	AVOL (dB)	Voltage Noise	0.1 to 10 Hz Noise	I_{bias}	VOS (V)	Drift (V/°C)	Supply Range	I_q/Ch (mA)	R-to-R Input	R-to-R Output	Chop Freq.	Comments
3001	1	4 MHz	5	300	$6nV/\sqrt{Hz}$ @ 0.5 Hz	125nV p-p @ 10 Hz	100	10	0.01	2.7 to 6.7	2.100	N	Y	180 kHz	2 kHz Usable Bandwidth
3002	2	4 MHz	5	300	$6nV/\sqrt{Hz}$ @ 0.5 Hz	125nV p-p @ 10 Hz	100	10	0.01	2.7 to 6.7	1.800	N	Y	180 kHz	2 kHz Usable Bandwidth
3003	1	2 MHz	0.25	150	$17nV/\sqrt{Hz}$ @ 1 Hz	350nV p-p @ 10 Hz	170	10	0.01	2.7 to 5.5	1.000	Y	Y	150 kHz	
3004	2	2 MHz	0.25	150	$17nV/\sqrt{Hz}$ @ 0.5 Hz	350nV p-p @ 10 Hz	170	10	0.01	2.7 to 5.5	1.000	Y	Y	150 kHz	
3011	1	2 MHz	2	300	$12nV/\sqrt{Hz}$ @ 0.5 Hz	250nV p-p @ 10 Hz	50	10	0.01	2.7 to 6.7	0.900	N	Y	180 kHz	1 kHz Usable Bandwidth
3012	2	2 MHz	2	300	$12nV/\sqrt{Hz}$ @ 0.5 Hz	250nV p-p @ 10 Hz	50	10	0.01	2.7 to 6.7	0.850	N	Y	180 kHz	1 kHz Usable Bandwidth
3013	1	1 MHz	0.25	135	$22nV/\sqrt{Hz}$ @ 0.5 Hz	460nV p-p @ 10 Hz	170	10	0.05	2.7 to 5.5	0.500	Y	Y	125 kHz	
3014	2	1 MHz	0.25	135	$22nV/\sqrt{Hz}$ @ 0.5 Hz	460nV p-p @ 10 Hz	170	10	0.05	2.7 to 5.5	0.500	Y	Y	125 kHz	

4. APPLICATION CIRCUITS

4.1 Thermopile Amplifiers

Figures 16 illustrates a basic diagram of a thermopile. The thermopile is a collection of series-connected thermocouples designed to detect spectral radiation. The spectrum of light is first filtered by an optical filter to select the frequency of light that is to be measured. This light passes through the optical filter and strikes an energy absorbent coating that converts the light into heat. The thermal change due to the absorbed radiation then causes a change in the output voltage of the series-connected thermocouples. The resultant output voltage is usually very small and must be amplified. The magnitude of the output signal is affected by the sensor area, the sensor technology, the filter optics, and the last of all, the intensity of the radiation.

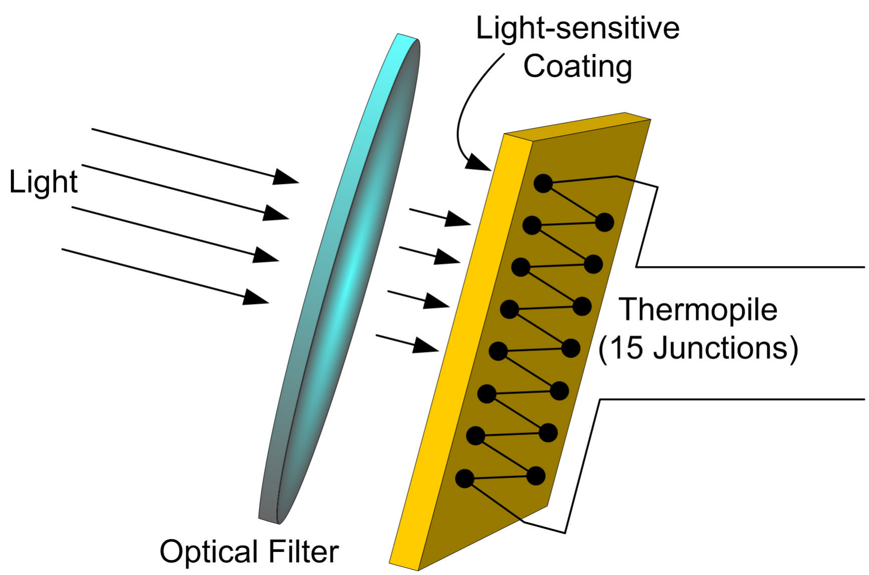
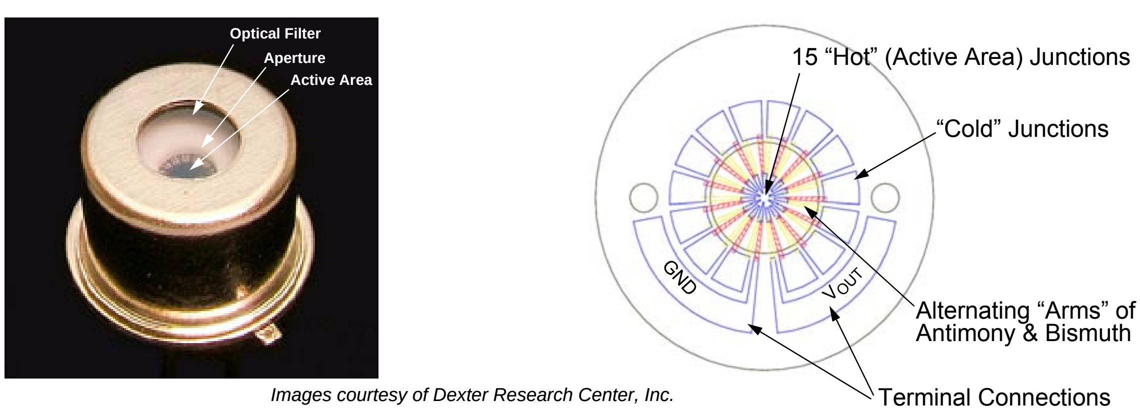


Figure 16. Typical Thermopile Block Diagram

A wide variety of thermopile devices are available. Various thermopile manufacturers offer thermopiles based upon thin film technology or upon silicon technology. Thin film devices tend to have lower noise and provide higher sensitivity. Silicon devices are less sensitive and have higher noise levels, but provide better temperature stability. Silicon devices are also less expensive.



Images courtesy of Dexter Research Center, Inc.

Figure 17. Typical Thermopile & Junction Layout

Figure 18 illustrates a thermopile amplifier set for a gain of 640 V/V. The Dexter Research 1M thermopile is a thin film device that exhibits a typical thermal noise of 7 nV/√Hz. In a typical infrared sensing application, the device may output only a few millivolts of signal. The CS3001 operational amplifier provides very high open loop gain and a low spot noise of 6 nV/√Hz. The circuit can readily amplify a 5 mV signal to several volts.

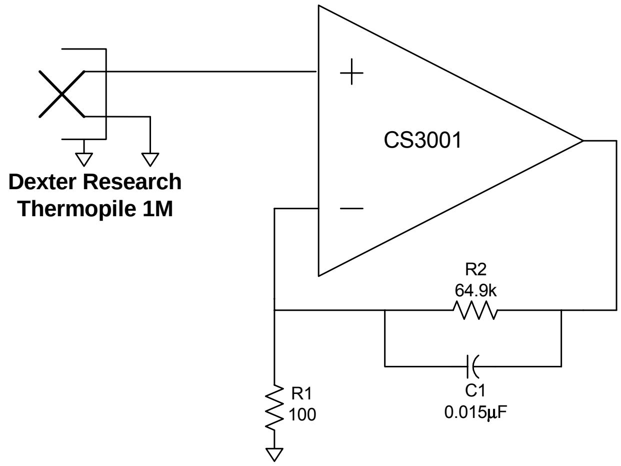


Figure 18. Thermopile Amplifier with Gain of 650 V / V

The thermopile, like the thermocouple, must be “cold junction” compensated. This would require a second sensor on the thermopile for this function. Manufacturers of thermopile sensors generally offer devices that include a sensor for cold junction sensing. This second sensor necessary for cold junction correction is not shown in Figure 18.

4.2 Load Cell Amplifiers

Load cells output small signals, typically less than 10 mV. To maintain high signal to noise, this small signal must be amplified with a low noise, low drift, high gain amplifier.

Cirrus Logic's chopper-stabilized amplifiers are very suitable for this type of application.

The combination of the CS3001 amplifier and the CS5512 A/D converter can provide a high resolution digitizer for a load cell as shown in Figure 19.

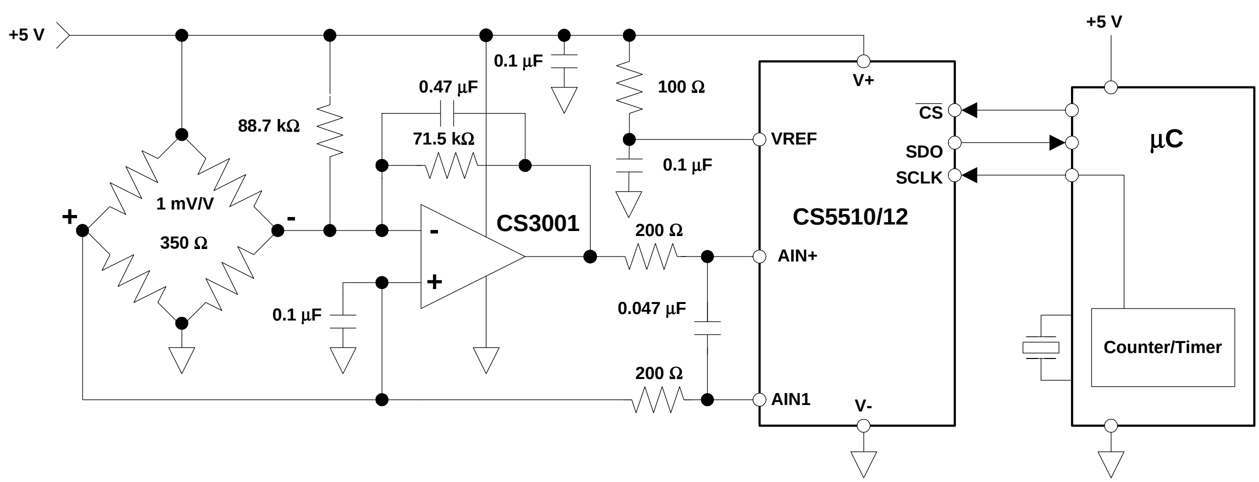


Figure 19. High-resolution Digitizer for a Load Cell

The CS3001 amplifier exhibits low noise, low drift, and incredibly high open loop gain.

The circuit illustrates the CS3001 with a gain of negative 408X. Note that the negative output from the bridge is connected to the inverting amplifier input. This results in a positive output from the amplifier into the A/D converter. The amplifier gain is set by the 71.5K and the parallel combination of the two 350 ohm resistors inside the bridge, or 175 ohm. The 88.7 K resistor offsets the bridge (offset is about +4.9 mV at the minus output side of the bridge) to allow the input of the A/D to be negative (about -2 V) with no weight on the load cell. The full input span of the A/D is nominally +/-4 V fully differential, as set by the 5 V on the VREF pin. Adding offset to the bridge output allows use of the negative range of the A/D and provides more codes out of the converter for the full output span of the bridge signal. When the full load is applied to the load cell, it will output approximately 5 mV.

The circuit shows the CS5510/12 devices, but the CS5511/13 devices can also be used.

The circuit in Figure 19 has the disadvantage that when full load is applied to the bridge, the inverting amplifier output current (2 V / 71.5 k, or about 28 microamperes) must flow through the 71.5 k resistor and into the inverting signal connection of the bridge. Therefore the inverting side of the bridge sees a different magnitude of current than the non-inverting side. This imbalance may introduce a signal dependent offset in the bridge due to different temperature effects on the bridge elements. This can limit the overall accuracy of the measurement.

Figure 20 illustrates a different load cell amplifier configuration than Figure 19. Using the CS3002, this amplifier configuration yields high impedance to both the plus and minus outputs of the load cell. The high impedance permits the use of the 1 kΩ & 300 pF components to prevent the effects of RFI (radio frequency interference).

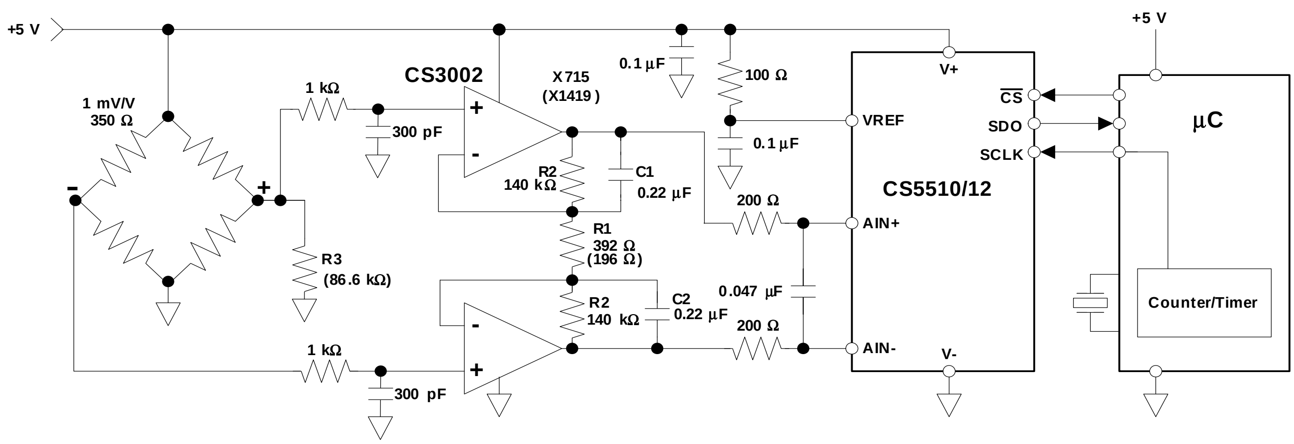


Figure 20. Digitizer for a Load Cell with High-impedance Inputs

In this schematic, the load cell has a sensitivity of 1 mV/V and outputs only about 5 mV under full load. The schematic illustrates two different gain configurations. If the bridge is used without being offset by resistor R3, the amplifier gain is set for 715X. The output of the amplifier (the input to the A/D) will change from about 0 volts (differential) to about 3.575 volts (differential) when the load on the load cell goes from zero to full load.

By adding resistor R3, the bridge is offset by about 5 mV. This causes the input to the A/D to be at -3.6 volts (differential) when no weight is on the scale. The amplifier gain is set for 1419X by changing the value of R1,and produces a change of about 7.1 volts, differential at the input of the A/D when the load on the load cell changes from zero to full load. The circuit will achieve about 27,000 noise-free counts on a 5 mV signal.

The noise in this circuit will be limited by the amplifier noise. Changing C1 & C2 to 0.47 µF can increase performance to about 38,000 noise-free counts. Again, averaging can greatly improve the number of useful counts from the circuit.

For more information about similar weigh-scale circuits, including some discussion about noise performance, please refer to Cirrus Logic Application Note AN330, *Load Cell Measurement using the CS3001/02/11/12 Amplifiers with the CS5510/11/12/13 A/D Converters*.

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