

CS5530/31/32/33/34: Rejection of 50 Hz & 60 Hz Line Interference

1. Introduction

The small signals from sensors in an industrial environment can often be affected by interference from the AC power mains. To improve measurement accuracy, it is desirable that this line interference be removed from the signal being measured. This can be accomplished by using an analog filter or an ADC that has an appropriate digital filter. This application note presents information about the digital filter in the CS5530/1/2/3/4 series of ADCs. It describes the filter attenuation characteristics of the filter at 60 Hz when the converter is set to output data at 50 Sps. And it illustrates how a 3.2768 MHz clock can be used to enable the converter to simultaneously reject both 50 Hz and 60 Hz line interference with a very high level of attenuation.

2. The Sinc Filter & Its Attenuation

Delta-sigma A/D converters consist of a modulator and a digital filter. The digital filter defines the characteristics of the gain and phase of the frequencies across the converter's passband.

One of the most common filters found in delta-sigma A/D converters that are used in low-frequency measurement is from a family of sinc filters. The basic sinc filter function can be implemented by averaging a group of samples. Figure 1 illustrates the attenuation of this type of filter.

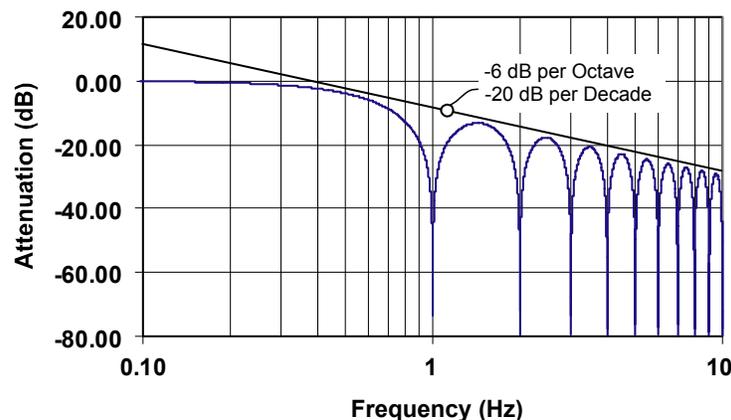


Figure 1. First-order Sinc (Sinc^1) Filter Response

In delta sigma converters it is common for the sinc filter to be convolved with itself multiple times. This results in a multi-order sinc such as Sinc^2 , Sinc^3 , Sinc^4 or Sinc^5 .

Figure 2 illustrates each Sinc filter function from Sinc¹ to Sinc⁵ with the frequency axis scaled logarithmically and the output word rate normalized to 1.

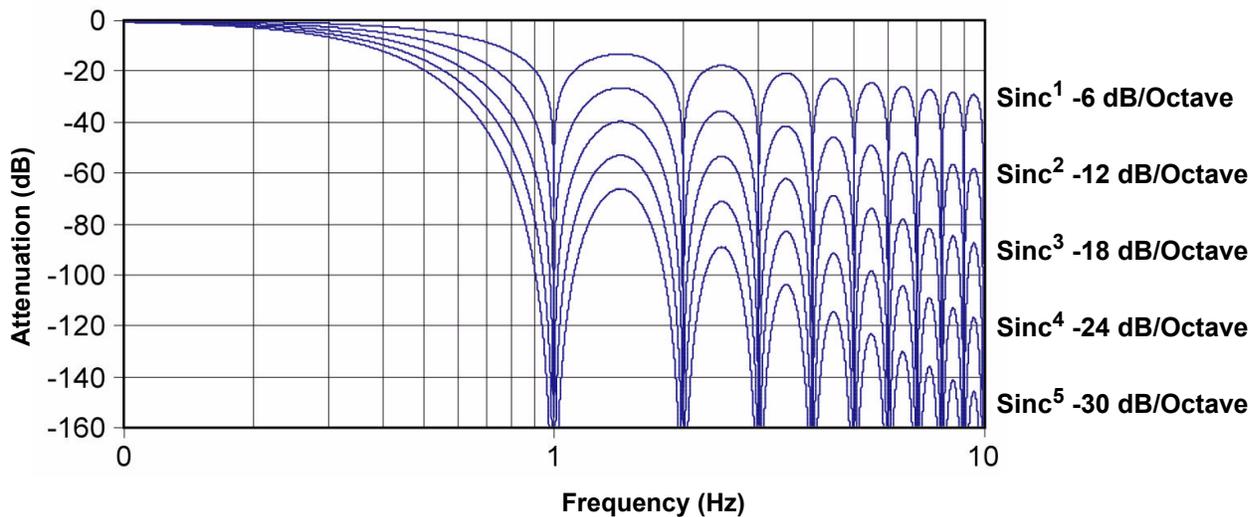


Figure 2. First-order Sinc Filter Response

While a Sinc¹ filter has a single zero at the output rate (normalized to 1 in Figure 1), a Sinc² filter would have two zeroes at the output word rate. A Sinc⁵ filter will have five zeroes at the output word rate. Notice in Figure 2 that each time the order of the Sinc filter increases, the magnitude response has 6 dB more of attenuation as the frequency doubles. Therefore a Sinc¹ filter has a slope of 6 dB per octave (20 dB per decade); a Sinc⁵ filter has a slope of 30 dB per octave (100 dB per decade).

3. The CS5530/31/32/33/34 Filter: Attenuating 60 Hz at 50 Sps Output Word Rate

The CS5530/31/32/33/34 series ADCs use Sinc filters. There are two stages of filtering. The first filter is a Sinc⁵ filter. This filter outputs words at the converter's highest rate. The second stage of the digital filter is a programmable Sinc³ filter. It accepts the output of the Sinc⁵ filter stage and provides the remainder of the available word rates.

The actual output rate depends upon the master clock (nominally 4.9152 MHz) and the setting of the FRS (Filter Rate Selection) bit in the CS5530/31/32/33/34 configuration register. Refer to Table 1.

Table 1. Crystal Frequency vs. Output Word Rate

Crystal Freq.	FRS	Available Word Rates
4.9152 MHz	0	3840, 1920, 960, 480, 240, 120, 60, 30, 15, 7.5
	1	3200, 1600, 800, 400, 200, 100, 50, 25, 12.5, 6.25

If the FRS bit is set to logic 0, the converter can provide output word rates of 3840, 1920, 960, 480, 240, 120, 60, 30, 15, and 7.5 samples per second (Sps). When set to output word rates of 60, 30, 15, or 7.5 Sps, the Sinc³ filter output will provide zeroes in the transfer function that will yield excellent rejection of 60 Hz line interference components.

If the FRS bit is set to logic 1, the converter can provide output word rates of 3200, 1600, 800, 400, 200, 100, 50, 25, 12.5, and 6.25 samples per second. When set to output word rates of 50, 25, 12.5, or 6.25 Sps, the filter will provide zeroes in the transfer function that will yield excellent rejection of 50 Hz line interference components.

Therefore, the CS5530/31/32/33/34 series of A/D converters provide the user the option of setting the FRS bit in the configuration register to modify the digital filter zero placement to be optimized for notching out either 50 Hz or 60 Hz.

4. The CS5530/31/32/33/34: A Method to Place Filter Zeroes at 50 Hz & 60 Hz Simultaneously

Some instrument manufacturers sell the same product design into multiple markets, some where 50 Hz line frequency is the standard and others where 60 Hz line frequency is standard. The CS5530/31/32/33/34 provide the operator with a software-selectable option for setting the FRS bit for 50 Hz or for 60 Hz. However, it may be desirable for the instrument to attenuate both 50 Hz and 60 Hz simultaneously.

There are several methods available to achieve both 50 Hz and 60 Hz attenuation. The method chosen depends upon the level of rejection that is needed in the application. There are two possible options which can provide line rejection of 50 Hz and 60 Hz that do not require the instrument user to make a software selection for line frequency.

The first solution is to operate the converter with the word rate set at 50 Sps and accept the amount of line rejection that this filter selection provides at 60 Hz.

Figure 3 illustrates an expanded view of the Sinc³ filter attenuation around the region of 0.5 to 1.5 times the output word rate when the word rate is scaled to 1 on the plot. With the converter set to output words at 50 Sps, the graph extends from 25 Hz to 75 Hz. Therefore, the graph actually illustrates the attenuation of the Sinc³ filter across 25 Hz to 75 Hz when the output word rate of the ADC is set for 50 Sps. One can read from the graph the amount of attenuation that would occur at any frequency from 25 Hz to 75 Hz when the word rate is set to 50 Sps.

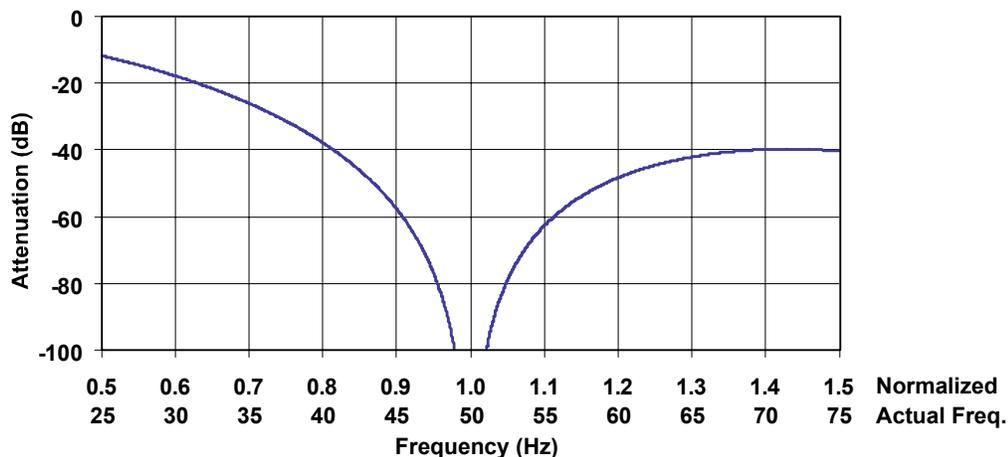


Figure 3. Third-order Sinc Filter Response (Sinc³), Normalized to 1

This graph can be used to determine the attenuation of the filter if the line frequency varies from 50 Hz. The filter notch frequency is determined by the clock source to the ADC and by the settings of the FRS bit and the word rate selection. In some electric utilities, the line frequency may vary widely. If the nominal line frequency of 50 Hz varies from 45 to 55 Hz the attenuation at these frequencies can be determined from the plot.

For example, for a line frequency of 45 Hz, one would examine the plot at 0.9 (45/50 = 0.9) and find that attenuation for 45 Hz would be about 58 dB.

With the ADC is configured to output words at 50 Sps, one can determine the attenuation of this filter at 60 Hz as shown in the plot in Figure 3. From the plot, one can see that the Sinc³ filter provides about -48 dB of attenuation at 60 Hz (an actual calculation yields 48.4 dB). 48 dB is equivalent to a factor of 251 to 1. If the range from 57 Hz to 63 Hz is examined (60 Hz, ±5%), the attenuation would vary from about -55 dB at 57 Hz to about -44 dB at 63 Hz. At 63 Hz the 44 dB of attenuation would translate to a factor of 158 to 1. Therefore, with the converter set to output words at 50 Sps, the filter attenuation at 63 Hz (60 Hz, +5%) would reduce any 63 Hz input component by the factor of 158.

Another design option that can achieve much higher rejection while attenuating 50 Hz and 60 Hz simultaneously is to operate the ADC from a 3.2786 MHz clock source.

Table 2 indicates the word rates available using either the 4.9152 MHz crystal or a 3.2768 MHz crystal. If the 3.768 MHz crystal is used, the FRS bit should be set to logic 0. Word rates of 5 and 10 Sps are then available.

Table 2. Crystal Frequency vs. Output Word Rate

Crystal Freq.	FRS	Available Word Rates
4.9152 MHz	0	3840, 1920, 960, 480, 240, 120, 60, 30, 15, 7.5
	1	3200, 1600, 800, 400, 200, 100, 50, 25, 12.5, 6.25
3.2768 MHz	0	2560, 1280, 640, 320, 160, 80, 40, 20, 10, 5
	1	2133.3, 1066.6, 533.3, 266.6, 133.3, 66.6, 33.3, 16.6, 8.3, 4.16

When the output of the converter is set for 5 or 10 Sps (FRS = 0), the Sinc³ filter provides simultaneous rejection of 50 Hz and 60 Hz line interference frequencies.

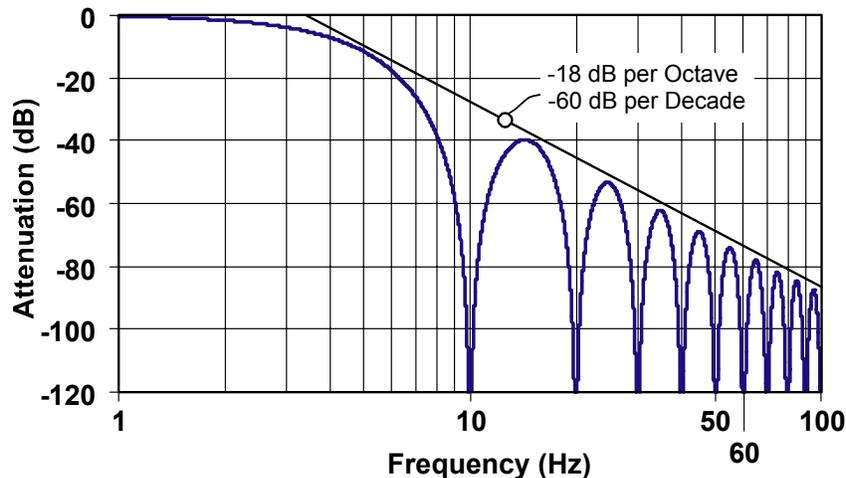
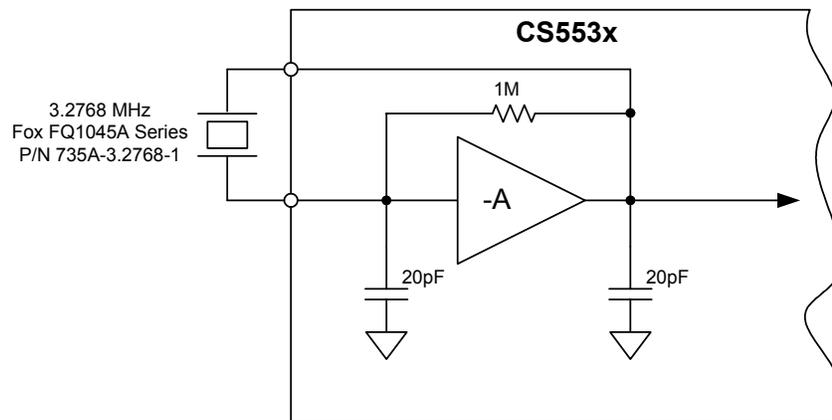


Figure 4. Third-order Sinc Filter Response (Sinc³)

With the output word rate at 5 or 10 Sps, the filter will produce three zeroes at each frequency that is an integer multiple of the word rate. For example, at 10 Sps the filter will produce a triple zero at 10, 20, 30, 40, 50, 60, etc. as shown in Figure 4.

Therefore, setting the converter to output either 5 or 10 Sps when operated from a 3.2768 MHz clock will provide filter notches at both 50 Hz and 60 Hz and their harmonics.

Figure 5 illustrates the crystal oscillator circuitry of the CS5530/31/32/33/34 series A/D converters. The figure includes the part number of a 3.2768 MHz surface mount crystal that is available from FOX as part number 735A-3.768-1.



The 20 pF capacitors are on-chip and should not be added externally.

Figure 5. CS5530/31/32/33/34 Crystal Oscillator Circuit

Revision History

Release	Date	Changes
REV1	JUN 2007	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

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