CS5480/84/90 Energy Measurement IC Calibration

1 Introduction

The Cirrus Logic CS5480/84/90 energy measurement IC is designed with industry-leading calibration algorithms that simplify measurement applications. The CS5480/84/90 calibration is engineered so power meter manufacturers can use low-cost components to achieve highly accurate power measurement. Calibration methods specified by IC manufacturers can vary substantially despite the power meter manufacturers' requirements to comply with tightly regulated standards. This application note will introduce the procedures available for calibrating the CS5480/84/90 devices, empowering power meter manufacturers to exceed industry standards.

2 Overview

This application note covers system scaling concepts, including hardware scaling, analog front end (AFE) scaling, and controller (MCU) scaling. The relationship between full-scale measurements and AFE measurements is discussed, and a corresponding application processor example is presented. The typical hardware configuration required to perform calibration and compensation is also presented. Then the types of calibrations in the CS5480/84/90 are detailed. The calibration and compensation procedure is provided in a step-by-step process that determines the AFE calibration and compensation constants.

Flow diagrams are provided for each calibration and compensation process. The customer demonstration board (CDB5484U) is used to illustrate the calibration process and provide examples of the serial port reads/writes transmitted at each calibration step.

Below are the calibration essentials discussed in this document:
- System Scaling
- Types of Calibration and Compensation
- Calibration and Compensation Procedure
  - Calibration and Compensation Example with Hardware Configuration

3 System Level Configurations

Upon power-up, the CS5480/84/90 requires an initial register configuration before executing power measurements. One of the key configurations is adjusting the system scaling for the power meter application. The key scaling constants are identified through calibration and compensations performed at the power meter manufacturer. After the configuration and calibration constants are established, the calibration constants are downloaded during a normal power-on reset. The application will start conversions and report power and input performance over time.

During power conversions and calculations, the analog inputs are sampled at 512 kHz, decimated down to 4 kHz high-rate conversion cycles. The high-rate samples are averaged to produce a 1 second low-rate power accumulation measurement, which is used to update registers and, when enabled, generate pulses that represent the power results (N = 4000, MCLK = 4.096 MHz). The CS5480/84/90 performs signal conditioning along the digital data path, which improves the accuracy of the power meter measurements. Signal conditioning is provided in the high-rate path (gain, phase, and DC offset) and in the lower rate path (no load current RMS offset, AC offset, active and reactive power offset).
3.1 System Scaling Overview

The maximum voltage, current, and power measurements are unique in each meter design and dependent on the sensors used in the measurement of these parameters. The CS5480/84/90 solves this problem using scaling. Instead of recording the actual voltage, current, or power sensed by the power meter, the IC records a ratio of each measurement that is proportional to the meter’s full-scale. Using this ratio, the actual voltage, current, and power can be calculated based on the values of the AFE registers.

There are two methods of obtaining the most recent power measurement readings:

- Voltage, current and power measurements are read directly from registers using the serial port.
- Power measurements are accumulated using the pulses on the DO pin(s).

Both methods are dependent on full-scale calibration to accurately scale the most recent power measurement. Traditional power meters typically use the pulse accumulation method. Since calibration constants are recorded in registers and power measurements are reported by register reads/writes, this document will focus on the register read/write method.

To use the built-in calibration functions, an understanding of the scaling factors due to the different system components within a typical meter is required. Below are three general scale factors in the signal path:

- **Hardware Scale**: The real voltage and currents are provided to the meter using sensors that must be attenuated on the meter board or by the sensor before applying the sensed signal to the input of the CS5480/84/90.

- **AFE Register Scale**: The device stores information for each voltage, current, and power parameter to internal registers. Each register value is scaled to a range of ±1 or 0 to 1 and stored in a 24-bit register. The values measured at the input (for example, 500 mVpp) are stored as a scaled version of input signal amplitudes. Refer to the CS5480/84/90 data sheet for register formats. The gain and offset registers are scaled to be within the range of 0 to 4 and ±1, respectively. Therefore, the MCU does not read the sensor output voltage and current; instead, it reads the scaled values recorded in the registers.

- **MCU Scale**: The MCU is typically used to rescale the real voltage, current, and power values for display.
3.2 System Scale Example

Figure 1 illustrates an example of the system scaling.

- **Hardware Scale**: The CS5480/84/90 inputs are scaled using attenuation circuits that apply a maximum input amplitude of 176mV_{RMS} or 35mV_{RMS}, which is dependent on an AFE gain setting of 10x gain or 50x gain, respectively.

- **AFE Scale**: The AFE registers record input levels that are displayed as a ratio of the most recent measurement to the maximum RMS voltage and RMS current. The maximum RMS register value is generated using a 0.6 ratio. The register value is read as a 24-bit hexadecimal number, which is proportioned to represent a 0.6V_{RMS} full scale. At maximum voltage (0.6) and maximum current (0.6) the maximum power is \( P_{\text{MAX}} = V_{\text{RMS,MAX}} \times I_{\text{RMS,MAX}} = 0.6 \times 0.6 = 0.36 \).

- **MCU Scale**: The MCU is required to read all registers and interpret the 24-bit hexadecimal numbers based on full-load conditions. Knowing the maximum hardware scaling and the most recent AFE register values in relation to the full-scale input, the MCU routines are able to calculate the actual power measurements.

*Figure 1. System Scaling*
3.3 AFE Scaling Range

The CS5484 full scale RMS register values are commonly reported as 0.6 when the inputs are at a maximum level. The ratio of the AFE inputs to full scale defines the reference point for all other input levels. The 24-bit $I_{1RMS}$ and $V_{1RMS}$ registers are defined in Figure 2. Note that the digital scaling for RMS current (positive only) does not match the scaling for power (signed). Section 6.2 Main Calibration Flow Diagram Using the CDB5484 on page 29 describes the scaling ratio of the AFE inputs when maximum input levels are applied.

Use Equation 1 to convert the hexadecimal value to a decimal value:

$$VALUE_{Decimal} = \frac{1}{2^{24} - 1} \times \text{hex2dec}(VALUE_{Hexadecimal})$$

[Eq: 1]

Using Equation 1, the following key values are identified:

<table>
<thead>
<tr>
<th>Key RMS Register Values Range (0 to 1)</th>
<th>Decimal Value</th>
<th>Register Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum RMS Register</td>
<td>1</td>
<td>0xFFFFFFF</td>
</tr>
<tr>
<td>Maximum RMS Input</td>
<td>0.6</td>
<td>0x999999</td>
</tr>
<tr>
<td>Half RMS Input</td>
<td>0.36</td>
<td>0x5C28F6</td>
</tr>
<tr>
<td>No Load Input</td>
<td>0</td>
<td>0x000000</td>
</tr>
</tbody>
</table>

If a sine wave is applied to the voltage channel input at full scale, then the peak voltage can be determined using Equation 2:

$$V_{PEAK} = V_{RMS} \times \sqrt{2} = 0.6 \times \sqrt{2} = 0.85$$

[Eq: 2]

The $V_{PEAK}$ register will have a maximum input margin of 15%, which prevents clipping.

The CS5480/84/90 provides a current channel scale register that allows a small load current during calibration. By default, the range is 0.6 (full-scale current load), but this value can be adjusted according to the load current available.
3.4 Application Processor Scaling Example

The scaling example below demonstrates how to convert from the current register value to the reported current using the full-scale value. The specified full-load (Current\textsubscript{FULLSCALE}) is 50A. If the AFE current register value (Current\textsubscript{REGISTER}) is 0.25 (0x40 0000), then the actual current value (ReportedCurrent\textsubscript{ACTUAL}) is calculated by the application processor using Equation 3.

Use Equation 3 to convert the current register value to the real current:

$$\text{ReportedCurrent}_{\text{ACTUAL}} = \frac{\text{Current}_{\text{REGISTER}} \times \text{Current}_{\text{FULLSCALE}}}{0.6} = \frac{0.25 \times 50A}{0.6} = 20.8A$$ \[Eq: 3\]

Scaling for power requires a change in the denominator to reflect a power scaling ratio of 0.36, which is equal to the voltage (0.6) multiplied by current (0.6). The input full load (\textit{Ich}_{\text{FULLSCALE}}) is 50A and the maximum voltage (\textit{Vch}_{\text{FULLSCALE}}) is 140V. If the present load is applied to the meter results in a power register (Power\textsubscript{REGISTER}) reading of 0.15 (0x13 3333), then the application processor needs to convert the power register value to the real current value. Use Equation 4 to convert the power register value to real reported power.

$$\text{ReportedPower}_{\text{ACTUAL}} = \frac{\text{Power}_{\text{REGISTER}} \times \text{Power}_{\text{FULLSCALE}}}{0.36} = \frac{\text{Power}_{\text{REGISTER}} \times (\text{Vch}_{\text{FULLSCALE}} \times \text{Ich}_{\text{FULLSCALE}})}{0.36} \[Eq: 4\]$$

$$\text{ReportedPower}_{\text{ACTUAL}} = \frac{0.15 \times (140 \times 50)}{0.36} = 2916.7W$$

Cirrus Logic power meters are bidirectional, which allows power to be measured in both directions (consumed or delivered). This reduces the digital scaling by one bit due to polarity, unlike the unsigned RMS current register. The 24-bit \textit{P1AVG} and \textit{P2AVG} registers are defined in Figure 3.

### Active Power 1 (P1\textsubscript{AVG}) – Page 16, Address 5

<table>
<thead>
<tr>
<th>MSB</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>\text{-}2^6</td>
<td>2^{-1}</td>
</tr>
</tbody>
</table>

Default = 0x00 0000

Instantaneous power is averaged over each low-rate interval (Sample\textit{Count} samples) and then added with power offset (\textit{POFF}) to compute active power (\textit{PAVG}).

This is a two's complement value in the range of \(-1.0 \leq \text{value} < 1.0\), with the binary point to the right of the MSB.

### Active Power 2 (P2\textsubscript{AVG}) – Page 16, Address 11

<table>
<thead>
<tr>
<th>MSB</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>\text{-}2^6</td>
<td>2^{-1}</td>
</tr>
</tbody>
</table>

Default = 0x00 0000

Instantaneous power is averaged over each low-rate interval (Sample\textit{Count} samples) to compute active power (\textit{P2AVG}).

This is a two's complement value in the range of \(-1.0 \leq \text{value} < 1.0\), with the binary point to the right of the MSB.

**Figure 3. Example of \textit{P1AVG} and \textit{P2AVG} Registers**
Use Equation 5 to convert the hexadecimal value to a decimal ratio value:

\[
\text{VALUE}_{\text{Decimal}} = -\text{MSB} \times \frac{1}{2^{23} - 1} \times \text{hex2dec(VALUE}_{\text{Hexadecimal}})
\]

[Eq: 5]

Using Equation 5, the following table identifies the key values.

<table>
<thead>
<tr>
<th>Key Power Register Values Range (-1 to 1)</th>
<th>Decimal Value</th>
<th>Register Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Power Register</td>
<td>1</td>
<td>0x7FFFFFFF</td>
</tr>
<tr>
<td>Maximum Power Input</td>
<td>0.36</td>
<td>0x2E147B</td>
</tr>
<tr>
<td>No Load Input</td>
<td>0</td>
<td>0x000000</td>
</tr>
</tbody>
</table>

4 Types of Calibration and Compensations

Calibration is self-contained within the CS5480/84/90, and all calculations are performed by the device and stored in internal registers. Compensations require that the MCU perform some of the calculations and then store the results back into the CS5480/84/90 registers. Since the CS5480/84/90 does not have non-volatile memory (NVM), permanent storage of calibration and compensation must be placed in the MCU NVM and re-loaded after any AFE reset condition.

In general, each calibration and compensation requires the following steps:

1. Configure the CS5480/84/90 initial conditions
2. Apply the analog input with stimulus from an accurate source
3. Enable the desired calibration
4. Execute calibration
5. Read the results
6. Calculate the new register values for compensations
7. Store the results in the AFE and NVM

It is common to perform calibration and compensation simultaneously. For example, since an AC gain calibration and a phase compensation require a similar input signal to be applied to the current and voltage channels, calibration and compensation are performed simultaneously.
Figure 4 illustrates a typical hardware configuration for calibration and compensation:

Automation can be established by a calibration controller that starts the calibration and/or the compensation, performs the required calculations, and finally initiates the storage of results. A calibration controller will control the AC source and load during calibration by adjusting the load for different AFE input conditions. The controller will also monitor the precision reference meter to confirm that load adjustments have been successfully executed, and the optical accumulation results are accurate from the Cirrus AFE. Communication from the controller to the Cirrus AFE is processed through the meter application processor to the calibration controller. Calculations and NVM results stored within the application processor are initiated by the controller when the calibration is completed.
4.1 AFE Calibrations

The CS5480/84/90 AFE incorporates three calibrations: gain, AC offset, and DC offset. Gain calibration is always required. AC offset calibration is only required when $I_{\text{RMS}}$ needs to be accurate at low input levels. DC offset calibration is made available but not recommended for AC power meters. Instead, high-pass filters are used to remove DC offset. The high-pass filter included in the CS5480/84/90 will remove any DC offset in real time, and it is the best choice for AC power meters.

Figure 5 shows a flow diagram of the calibration process included in the Cirrus AFE. Refer to the CS5480/84/90 data sheet for detailed information.

4.1.1 DC Offset Calibration

DC offset calibration is designed to remove the DC component from the ADC output. DC offset calibration is seldom used in AC power meters. The high-pass filter is the recommended choice and should be enabled at the modulator output, as illustrated in Figure 5.

4.1.2 Gain Calibration

Gain calibration will adjust the input for hardware and sensor variations and customer-specific inputs. It is recommended to use full-load conditions (full-scale voltage and current). (For non-full-load conditions, see section 4.1.2.1 on page 8). When the full current load is not available, the CS5480/84/90 allows the scale register to adjust for lower current loads to be provided. (See 3.3 on page 4 for adjusting the scale register.)

After gain calibration, full-scale input will yield:

- The Voltage RMS register, $V_{\text{RMS}}$, value: 0.6
- The Current RMS register, $I_{\text{RMS}}$, value: 0.6
- The Active Power register, $P_{\text{AVG}}$, value: $0.6 \times 0.6 = 0.36$ at $PF = 1$
- The Reactive Power register, $Q_{\text{AVG}}$, value: $0.6 \times 0.6 = 0.36$ at $PF = 0$
- The Apparent Power register, $S$, value: $0.6 \times 0.6 = 0.36$

4.1.2.1 When AC Source or AC Load Are Less Than Ideal

If the AC source or AC load are less than ideal, the meter can still be calibrated with an accurate reference meter using the Non-full-scale Gain Calibration procedure on page 9. It is common to see an AC load set to 15A actually measure in the range of 14.55A to 15.45A using a reference meter. When using the full-scale current, it may be necessary to use the Non-full-scale Gain Calibration procedure on page 9 to account for inaccurate resources.
4.1.2.2 Non-full-scale Gain Calibration

When resources are limited, it may be necessary to provide non-full-scale amplitudes and perform built-in calibration to provide the maximum voltage and current during calibration. To perform a non-full-scale calibration, the initial gain register conditions of the device must be identified before calibration. Usually, initial gain register conditions are set to a default value of one, but this is not required. Instead, the initial gain register conditions are set to accommodate the non-full-scale input calibration. Before calibration is executed, the gain register can be set using the following equations:

\[
V_{\text{GAIN(pre)}} = \frac{V_{\text{MAX}}}{V_{\text{REF}}} \times 2^{22} \quad \text{[Eq: 6]}
\]

\[
I_{\text{GAIN(pre)}} = \frac{I_{\text{MAX}}}{I_{\text{REF}}} \times 2^{22} \quad \text{[Eq: 7]}
\]

where:
- \(V_{\text{GAIN(pre)}}\) Value stored in voltage gain register (page 16, address 35) before calibration starts
- \(I_{\text{GAIN(pre)}}\) Value stored in current gain register (page 16, address 33) before calibration starts
- \(V_{\text{MAX}}\) Maximum voltage of the meter defined by customer
- \(I_{\text{MAX}}\) Maximum current of the meter defined by customer
- \(V_{\text{REF}}\) Voltage of the line just before calibration as measured with reference meter assumes stable input
- \(I_{\text{REF}}\) Load current just before calibration as measured with reference meter assumes stable input

Follow the steps below to perform a non-full-scale gain calibration:

1. Set the line voltage and load current \(V_{\text{REF}}\) and \(I_{\text{REF}}\), respectively.
2. Confirm that the reference meter shows \(V_{\text{REF}}\) and \(I_{\text{REF}}\) of the input.
3. Set \(V_{\text{GAIN(pre)}}\) per Equation 6 and \(I_{\text{GAIN(pre)}}\) per Equation 7.
4. Send the calibration command.
5. After calibration, the meter is adjusted for a full-scale voltage of \(V_{\text{MAX}}\) and \(I_{\text{MAX}}\) and will currently be measuring the \(V_{\text{REF}}\) and \(I_{\text{REF}}\) measurements.

Reference Limits

The calibration line voltage \((V_{\text{REF}})\) or load current \((I_{\text{REF}})\) must not be set too low. It is recommended to keep the register values at a minimum of \(\frac{1}{3}\) of the maximum levels. Since the gain register can be set to a maximum value of 4, the input could be set to \(\frac{1}{4}\) of the maximum levels. It is not recommended to set the input to \(\frac{1}{4}\) of the maximum levels due to variations in setup conditions. If the input is too low, the gain register will set the default value of one after calibration.
**Current Scale Register**

To perform calibration with less than full scale load *without using the above procedure*, it is possible to set the current channel's *Scale* register. The current channel calibration data path contains a *Scale* register (page 18, address 63) that can be adjusted before calibration to accommodate the non-full-scale load.

\[ I_{\text{SCALE}} = \frac{I_{\text{REF}}}{I_{\text{MAX}}} \times 0.6 \times 2^{23} \]  

[Eq: 8]

where:

- \( I_{\text{SCALE}} \): Value stored in the *Scale* register before calibration
- \( I_{\text{MAX}} \): Maximum current of the meter defined by the customer
- \( I_{\text{REF}} \): Load current before calibration, as measured with a reference meter, assuming stable input

Follow the steps below to set the current channel's *Scale* register.

1. Set the load current, \( I_{\text{REF}} \) (assuming \( V_{\text{REF}} \) is set to full scale).
2. Confirm that the reference meter shows \( V_{\text{REF}} \) and \( I_{\text{REF}} \) of the input.
3. Set the *Scale* register per Equation 8.
4. Send the calibration command.
5. After calibration, the meter is adjusted for a full-scale voltage of \( V_{\text{MAX}} \) and \( I_{\text{MAX}} \) and will currently be measuring the \( V_{\text{REF}} \) and \( I_{\text{REF}} \) measurements.
6. The *Scale* register is not in the normal data path but instead in the calibration path.

**4.1.3 AC Offset Calibration**

Following gain calibration, there may still be some AC offset remaining. AC offset calibration will allow for the removal of the remaining offset. The AC offset effects are only applicable to the \( I_{\text{RMS}} \) registers at small input. The AC offset calibration only needs to be performed when \( I_{\text{RMS}} \) readings are required to span a large dynamic range with high accuracy.

**4.2 Available Compensations**

Three compensations are available in the CS5480/84/90: phase, no-load active power, and no-load reactive power offset.

**4.2.1 Phase Compensation**

Phase compensation adjusts phase mismatches between the voltage and current channels. Setting the current to lag the voltage by 60º (the center of the COS range of 0º - 90º) allows the system to distinguish additional or less phase delay from the power factor (PF) directly. Follow the steps below to perform this compensation:

1. Apply source at full scale with a 60º phase shift (PF = 0.5 lagging)
2. Start continuous convert
3. Read the PF register and calculate:
   Phase error = ACOS(registry PF) - 60º
4. Calculate phase compensation (PC) register (MCLK=4.096MHz):
   50Hz PC register = phase error / 0.008789
   60Hz PC register = phase error / 0.010547

Phase error can be adjusted when it falls within ±8.99º at 50Hz or ±10.79º at 60Hz. Figure 6 shows the phase offset error range. When phase error is below -4.5º at 50Hz or -5.4º at 60Hz and above 0º, it is necessary to adjust both coarse compensation and fine compensation. The coarse and fine compensation settings for each region are shown in Figure 6.
4.2.2 No Load Power Compensation

There are two power compensations in the CS5480/84/90: active and reactive power offset. When no load is applied, the average active power register, $P_{AVG}$, and average reactive power register, $Q_{AVG}$, may have offsets. To remove any remaining active or reactive power, it is necessary to perform the following compensation:

- Apply full scale voltage source
- Apply no load to the current channel(s)
- Start continuous conversion
- Read $P_{AVG}$ and $Q_{AVG}$ register
- Write $-P_{AVG}$ and $-Q_{AVG}$ to $P_{OFF}$ and $Q_{OFF}$, respectively
5 Calibration and Compensation Procedures

A CS5480/84/90 power meter normally has two modes of operation: calibration, which is executed only once at the factory, and normal operation in the field.

Calibration will compensate for system-level errors and is only performed at the factory. Normal operation is a continuous running mode (continuous conversion mode) or user-initiated, single execution mode (single conversion mode). Most designs are continuously running and use the continuous conversion command. Normal operation is resetting the device, loading calibration and configuration information from non-volatile memory, and executing continuous conversion command. The MCU then needs to read various device registers to obtain the power, current, and voltage. As these registers are updated, the MCU will need to post the information to the user interface. This is accomplished by using DO pin interrupts or by periodically reading the status register. The default configuration of the part sets most of the registers to a common configuration. When continuous conversion is performed, the device will provide most register updates once per second (default at reset).

The normal field operation is simple and there is no need for extensive computation by the MCU. A simple, low cost MCU may be used to assist the normal operation.

5.1 Normal Operation Procedure (Performed at Every Reset in the Field)

The following procedure outlines the steps required to put the meter in normal operation mode. Figure 7 shows a simplified flow chart for the normal operation in the field.

1. Reset the CS5480/84/90.
2. Restore configuration and control registers.
3. Restore the $V_{GAIN}$ and $I_{GAIN}$ registers from the non-volatile memory (NVM).
4. If needed, restore the offset registers from NVM.
5. If needed, restore the phase compensation registers from the NVM.
6. If needed, restore the no load compensation to the $POFF$ and $QOFF$ registers from the NVM.
7. Send the single conversion command to the CS5480/84/90.
8. Confirm that the register checksum is valid, or return to step 1.
9. Send the continuous conversion command to the CS5480/84/90.
10. Enable and clear DRDY.
11. Poll DRDY.
12. If DRDY is set, clear DRDY.
13. Read $I_{RMS}$, $V_{RMS}$, and $P_{AVG}$. Scale the $I_{RMS}$, $V_{RMS}$, and $P_{AVG}$ back into true value by:
   \[
   \text{Amps} = \text{Full}_\text{Scale}_\text{Current} \times (I_{RMS}/0.6) \\
   \text{Volts} = \text{Full}_\text{Scale}_\text{Voltage} \times (V_{RMS}/0.6) \\
   \text{Watts} = \text{Full}_\text{Scale}_\text{Power} \times (P_{AVG}/0.36)
   \]
14. Loop back to “Poll DRDY” step.
AN366

Figure 7. Normal Field Flow

START CONVERSION 0xD5

POWER UP

RESET

RESTORE CONFIGURATION and CONTROL REGISTERS

From NVM RESTORE GAIN REGISTERS

From NVM RESTORE OFFSET REGISTERS

From NVM RESTORE POFF and QOFF REGISTERS

SINGLE CONVERSION

VALID REGISTER CHECKSUM ?

YES

NO

READ IRMS, VRMS, PAVG

CLEAR DRDY

DRDY SET ?

YES

NO

CALCULATE
VOLTS = FS_Voltage · (VRMS/0.6)
AMPS = FS_Current · (VRMS/0.6)
WATTS = FS_Scale_Power · (VRMS/0.36)

RESET VALID REGISTER
CHECKSUM ?

YES

NO

CLEAR DRDY
5.2 Full Calibration and Compensation Procedure (Performed Once at Factory)

The following procedure shows the steps required to perform calibration and compensation. A flow chart showing the full calibration procedure is shown in Figure 5.

1. Power up the CS5480/84/90 device.
2. Reset the CS5480/84/90 device.
3. Verify the register checksum to confirm the reset is successful.
4. Restore configuration and control registers.
5. Connect the reference line voltage and load current to the meter with a phase angle of 60° current lagging.
6. If the reference load current is not the full load, set the Scale register to a ratio of \( 0.6 \times 2^{23} \times \) reference load current \( \div \) full scale current. See Non-full-scale Gain Calibration on page 9 if the reference line voltage is lower than the maximum line voltage.
7. Perform continuous conversion (0xD5 command) for 2 seconds.
8. Stop the continuous conversion (0xD8 instruction).
9. Read \( I_{RMS}, V_{RMS}, P_{AVG}, \) and \( PF, \) and confirm the reference voltage and current signals are correctly attached by verifying if the \( I_{RMS}, V_{RMS}, P_{AVG}, \) and \( PF, \) are in a reasonable range.
11. Send AC gain calibration command (0xFE) to the CS5480/84/90.
12. Wait for DRDY to be set.
13. If needed, perform phase compensation, AC offset calibration, and power offset correction.
14. Send continuous conversion (0xD8 command).
15. Verify measurement accuracy. Check the setup or fail the meter if the accuracy is not within specifications.
16. Read \( V_{GAIN}, I_{GAIN}, I_{ACOFF}, P_{OFF}, Q_{OFF}, PC, \) and register checksum and save them into flash/eeprom.
17. Calibration completed.
Figure 8. Main Calibration Flow

Note 1: The default setting for all registers should be set before performing calibration. Resetting the device restores the default setting for all registers.

Note 2: Larger numbers in the Tsettle and SampleCount registers will increase calibration precision.

Note 3: Other configurations and controls might be necessary.

Note 4: For an expanded view showing more information about the main calibration flow, see Main Calibration Flow Diagram Using the CDB5484 on page 29.

Note 5: See Non-full-scale Gain Calibration on page 9.

Note 6: Scale register is only in calibration path and does not require resetting to 0.6 after the calibration.
Figure 9. Phase Compensation Flow

**Note 1:** Larger numbers in the \( T_{\text{settle}} \) and \( \text{SampleCount} \) registers will increase calibration precision.

**Note 2:** OWR=4000, MCLK=4.096 Mhz.

**Note 3:** For an expanded view showing more information about the phase compensation flow, see Phase Compensation Flow Diagram on page 40.

**Note 4:** Before calibration: Angle < 60; Phase offset < 0; I leads V; PF is leading--for more positive, delay I.

**Note 5:** Before calibration: Angle < 60; Phase offset < 0; I lags V; PF is lagging--only coarse adjustment can delay V, therefore delay V by 1 or 2 OWR and delay I by less than 1 or 2 OWR.
Figure 10. AC Offset Calibration Flow

Note: For an expanded view showing more information about the AC offset calibration flow, see AC Offset Calibration Flow Diagram on page 44.

Figure 11. DC Offset Calibration Flow

Note: For an expanded view showing more information about the DC offset calibration flow, see DC Offset Calibration Flow Diagram on page 46.

Figure 12. No Load Offsets Calibration Flow

Note: For more information, see No Load Offset Compensation Flow Diagram on page 47.
6 Full Calibration and Compensation Example Using the CDB5484 and MTE Meter Test Equipment

The calibration and compensation flows have been implemented using the CDB5484U and a PC as the controller. Using a MTE Meter Test Equipment AG PTS 400.3 Modular Portable Test System source and reference meter, the results of this calibration can be shown. More information can be found by visiting the MTE Meter Test Equipment website.

The CDB5484U connections are as follows:

1. The USB connects to the CDB5484U on the right. Using the standard CDB5484U GUI, commands and read results from the Cirrus AFE can be sent.
2. The DUT supplies are connected to terminals J36 and J37. It is not recommended to use the USB supply to power the Cirrus AFE during accuracy tests. Instead, use terminals J36 and J37.
3. Voltage is applied directly to the CDB5484U. Current inputs are looped through a terminal board and outputs are sent to the CDB5484U.
4. The PC was connected to the RS232 connection on the MTE Meter Test Equipment power source and power reference.
5. The pulse output is connected to an external counter or optically back to the MTE Meter Test Equipment power reference.
6. The controller in this example is the CDB5484U and PC. While the CDB5484U is good for presentation, it is not recommended to be used as a production solution.
Figure 13. MTE Meter Test Equipment Calibration Hardware Setup
6.1 Normal Operation Flow Diagram Using the CDB5484

The following flow diagram shows the implementation of normal flow executed in the field. The CDB5484U is used to load calibration constants obtained during the factory calibration. Obviously, the GUI is not used during actual execution, but it provides an excellent debugger for customer flow evaluation and modifications. The one-time factory calibration and compensation flows are discussed after the normal flow. The MTE Meter Test Equipment source is used to provide the source voltage and load current, but it is only required during this flow to simulate different loading conditions. Each step of the flow shows the CDB5484U GUI screen capture of execution and reading results. The register writes and reads are all identified for easy comparison to the GUI screen.

**POWER UP**

Power up CDB5484U per data sheet using terminals J36 and J37.

**RESET**

SDI = 0xC1    Reset CS5484 software Reset

**RESTORE FILTER CONFIGURATION**

(See Figure 14.)

**Config 2 Register**

SDI = 0x90 0x40 0x0602AA    Write Register Config2 to enable HPFs

SDO = 0xFF 0xFFFF 0xFFFF    (Page 16, Register 0)

SDI = 0x90 0x00 0xFFFFFF    Read Register Config2 to enable HPFs

SDO = 0xFF 0xFF 0x0602AA    (Page 16, Register 0)

---

**Figure 14. Setup Window**
RESTORE REGISTERS

Various configurations include writes to registers (see Figure 14):

**Config 0 Register**

<table>
<thead>
<tr>
<th>SDI</th>
<th>SDO</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x80</td>
<td>0x40</td>
<td>0x400000 Write Register Config0</td>
</tr>
<tr>
<td>0xFF</td>
<td>0xFFFF</td>
<td>(Page 0, Register 0)</td>
</tr>
<tr>
<td>0x80</td>
<td>0x00</td>
<td>0xFFFF Read Register Config0</td>
</tr>
<tr>
<td>0xFF</td>
<td>0x400000</td>
<td>(Page 0, Register 0)</td>
</tr>
</tbody>
</table>

**Config 1 Register**

<table>
<thead>
<tr>
<th>SDI</th>
<th>SDO</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x80</td>
<td>0x41</td>
<td>0x10FEE0 Write Register Config1</td>
</tr>
<tr>
<td>0xFF</td>
<td>0xFFFF</td>
<td>(Page 0, Register 1)</td>
</tr>
<tr>
<td>0x80</td>
<td>0x01</td>
<td>0xFFFF Read Register Config1</td>
</tr>
<tr>
<td>0xFF</td>
<td>0x10FEE0</td>
<td>(Page 0, Register 1)</td>
</tr>
</tbody>
</table>

**Pulse Control Register**

<table>
<thead>
<tr>
<th>SDI</th>
<th>SDO</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x80</td>
<td>0x49</td>
<td>0x000000 Write Register Pulse Control</td>
</tr>
<tr>
<td>0xFF</td>
<td>0xFFFF</td>
<td>(Page 0, Register 9)</td>
</tr>
<tr>
<td>0x80</td>
<td>0x09</td>
<td>0xFFFF Read Register Pulse Control</td>
</tr>
<tr>
<td>0xFF</td>
<td>0x000000</td>
<td>(Page 0, Register 9)</td>
</tr>
</tbody>
</table>

**Phase Comp Register**

<table>
<thead>
<tr>
<th>SDI</th>
<th>SDO</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x80</td>
<td>0x45</td>
<td>0x007C40 Write Register Phase Compensation</td>
</tr>
<tr>
<td>0xFF</td>
<td>0xFFFF</td>
<td>(Page 0, Register 5)</td>
</tr>
<tr>
<td>0x80</td>
<td>0x05</td>
<td>0xFFFF Read Register Phase Compensation</td>
</tr>
<tr>
<td>0xFF</td>
<td>0x007C40</td>
<td>(Page 0, Register 5)</td>
</tr>
</tbody>
</table>

**Pulse Width Register**

<table>
<thead>
<tr>
<th>SDI</th>
<th>SDO</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x80</td>
<td>0x48</td>
<td>0x0613F0 Write Register Pulse Width</td>
</tr>
<tr>
<td>0xFF</td>
<td>0xFFFF</td>
<td>(Page 0, Register 8)</td>
</tr>
<tr>
<td>0x80</td>
<td>0x08</td>
<td>0xFFFF Read Register Pulse Width</td>
</tr>
<tr>
<td>0xFF</td>
<td>0x0613F0</td>
<td>(Page 0, Register 8)</td>
</tr>
</tbody>
</table>

**Pulse Rate Register**

<table>
<thead>
<tr>
<th>SDI</th>
<th>SDO</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x92</td>
<td>0x5C</td>
<td>0x800000 Write Register Pulse Rate</td>
</tr>
<tr>
<td>0xFF</td>
<td>0xFFFF</td>
<td>(Page 18, Register 28)</td>
</tr>
<tr>
<td>0x92</td>
<td>0x1C</td>
<td>0xFFFF Read Register Pulse Rate</td>
</tr>
<tr>
<td>0xFF</td>
<td>0x800000</td>
<td>(Page 18, Register 28)</td>
</tr>
</tbody>
</table>

**Sample Count Register**

<table>
<thead>
<tr>
<th>SDI</th>
<th>SDO</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x90</td>
<td>0x73</td>
<td>0x000FA0 Write Register Sample Count</td>
</tr>
<tr>
<td>0xFF</td>
<td>0xFFFF</td>
<td>(Page 16, Register 51)</td>
</tr>
<tr>
<td>0x90</td>
<td>0x33</td>
<td>0xFFFF Read Register Sample Count</td>
</tr>
<tr>
<td>0xFF</td>
<td>0x000FA0</td>
<td>(Page 16, Register 51)</td>
</tr>
</tbody>
</table>

**Settle Time**

<table>
<thead>
<tr>
<th>SDI</th>
<th>SDO</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x90</td>
<td>0x79</td>
<td>0x800000 Write Register T Settle</td>
</tr>
<tr>
<td>0xFF</td>
<td>0xFFFF</td>
<td>(Page 16, Register 57)</td>
</tr>
<tr>
<td>0x90</td>
<td>0x39</td>
<td>0xFFFF Read Register T Settle</td>
</tr>
<tr>
<td>0xFF</td>
<td>0x800000</td>
<td>(Page 16, Register 57)</td>
</tr>
</tbody>
</table>
RESTORE GAIN CONFIGURATION
(See Figure 15.)

Gain Channel 1, Volt.
SDI = 0x90 0x63 0x401BE3 Write Register V1 Gain
SDO = 0xFF 0xFF 0xFFFFFFFF (Page 16, Register 35)
SDI = 0x90 0x23 0xFFFFFFFF Read Register V1 Gain
SDO = 0xFF 0xFF 0x401BE3 (Page 16, Register 35)

Gain Channel 1, Curr.
SDI = 0x90 0x61 0x3C4420 Write Register I1 Gain
SDO = 0xFF 0xFF 0xFFFFFFFF (Page 16, Register 33)
SDI = 0x90 0x21 0xFFFFFFFF Read Register I1 Gain
SDO = 0xFF 0xFF 0x3C4420 (Page 16, Register 33)

Gain Channel 2, Volt.
SDI = 0x90 0x6A 0x4037B6 Write Register V2 Gain
SDO = 0xFF 0xFF 0xFFFFFFFF (Page 16, Register 42)
SDI = 0x90 0x2A 0xFFFFFFFF Read Register V2 Gain
SDO = 0xFF 0xFF 0x4037B6 (Page 16, Register 42)

Gain Channel 2, Curr.
SDI = 0x90 0x68 0x3C465F Write Register I2 Gain
SDO = 0xFF 0xFF 0xFFFFFFFF (Page 16, Register 40)
SDI = 0x90 0x28 0xFFFFFFFF Read Register I2 Gain
SDO = 0xFF 0xFF 0x3C465F (Page 16, Register 40)

Figure 15. Calibration Window
RESTORE OFFSET CONFIGURATION
(See Figure 15.)

**DC Offset Channel 1, Volt.**
SDI = 0x90 0x62 0x000000 Write Register V1 DC Offset
SDO = 0xFF 0xFFFF 0xFFFF (Page 16, Register 34)
SDI = 0x90 0x22 0xFFFF Read Register V1 DC Offset
SDO = 0xFF 0xFF 0x000000 (Page 16, Register 34)

**DC Offset Channel 1, Curr.**
SDI = 0x90 0x22 0xFFFF Read Register I1 DC Offset
SDO = 0xFF 0xFF 0x000000 (Page 16, Register 32)

**DC Offset Channel 2, Volt.**
SDI = 0x90 0x69 0x000000 Write Register V2 DC Offset
SDO = 0xFF 0xFFFF 0xFFFF (Page 16, Register 41)
SDI = 0x90 0x29 0xFFFF Read Register V2 DC Offset
SDO = 0xFF 0xFF 0x000000 (Page 16, Register 41)

**DC Offset Channel 2, Curr.**
SDI = 0x90 0x67 0x000000 Write Register I2 DC Offset
SDO = 0xFF 0xFFFF 0xFFFF (Page 16, Register 39)
SDI = 0x90 0x27 0xFFFF Read Register I2 DC Offset
SDO = 0xFF 0xFF 0x000000 (Page 16, Register 39)

**AC Offset Channel 1, Curr.**
SDI = 0x90 0x65 0x050704 Write Register I1 AC Offset
SDO = 0xFF 0xFFFF 0xFFFF (Page 16, Register 37)
SDI = 0x90 0x25 0xFFFF Read Register I1 AC Offset
SDO = 0xFF 0xFF 0x050704 (Page 16, Register 37)

**AC Offset Channel 2, Curr.**
SDI = 0x90 0x6C 0x049959 Write Register I2 AC Offset
SDO = 0xFF 0xFFFF 0xFFFF (Page 16, Register 44)
SDI = 0x90 0x2C 0xFFFF Read Register I2 AC Offset
SDO = 0xFF 0xFF 0x049959 (Page 16, Register 44)
RESTORE NO LOAD CONFIGURATION
(See Figure 15.)

**P1 Offset**
- SDI = 0x90 0x64 0x0000003 Write Register P1 Active Power Offset
- SDO = 0xFF 0x00000000 (Page 16, Register 36)
- SDI = 0x90 0x24 0xFFFF Read Register P1 Active Power Offset
- SDO = 0xFF 0x00000000 (Page 16, Register 36)

**Q1 Offset**
- SDI = 0x90 0x66 0x0000002 Write Register Q1 Reactive Power Offset
- SDO = 0xFF 0x00000000 (Page 16, Register 38)
- SDI = 0x90 0x26 0xFFFF Read Register Q1 Reactive Power Offset
- SDO = 0xFF 0x00000000 (Page 16, Register 38)

**P2 Offset**
- SDI = 0x90 0x6B 0x0000001 Write Register P2 Active Power Offset
- SDO = 0xFF 0x00000000 (Page 16, Register 43)
- SDI = 0x90 0x2B 0xFFFF Read Register P2 Active Power Offset
- SDO = 0xFF 0x00000000 (Page 16, Register 43)

**Q2 Offset**
- SDI = 0x90 0x6D 0x0000002 Write Register Q2 Reactive Power Offset
- SDO = 0xFF 0x00000000 (Page 16, Register 45)
- SDI = 0x90 0x2D 0xFFFF Read Register Q2 Reactive Power Offset
- SDO = 0xFF 0x00000000 (Page 16, Register 45)

**SINGLE CONVERSION**
(See Figure 16.)

![Figure 16. Conversion Window](image-url)
VALID REGISTER CHECKSUM?

Read register checksum and compare to stored value in NVM (see Figure 17).

SDI = 0x90 0x01 0xFFFFFFF  Read Register Checksum
SDO = 0xFF 0xFF 0x5C0ED4  (Page 16, Register 1)

Figure 17. Setup Window
START CONTINUOUS CONVERSION
(See Figure 18.)

SDI = 0xD5 Send Continuous Conversion Command

START CONTINUOUS CONVERSION

SDI = 0x80 0x57 0x800000 Write DRDY Interrupt in Status 0
SDO = 0xFF 0xFFFF 0xFFFFFFFF (Page 0, Register 23)

CLEAR DRDY in INTERRUPT STATUS

SDI = 0x80 0x18 0xFFFF 0xFFFFFFFF Read Status 1 for DRDY Interrupt (Not Set).
SDO = 0xFF 0x400000 (Page 0, Register 24)

SDI = 0x80 0x18 0xFFFF 0xFFFFFFFF Read Status 1 for DRDY Interrupt (Set).
SDO = 0xFF 0x4C0000 (Page 0, Register 24)

WAIT FOR TSETTLE TIME
Wait for Tsettle time.

CLEAR DRDY

WAIT 2 SEC
Tsettle = 2000ms

Figure 18. Conversion Window
CLEAR DRDY in INTERRUPT STATUS
SDI = 0x80 0x57 0x800000  Write DRDY Interrupt in Status 0
SDO = 0xFF 0xFFFF 0xFFFFFFF (Page 0, Register 23)

READ IRMS, VRMS PAVG
(See Figure 19.)

Channel 1
SPI = 0x06 0xFFFFFFF Read I1RMS
SPO = 0xFF 0x999357 (Page 16 Register 6)
SPI = 0x07 0xFFFFFFF Read V1RMS
SPO = 0xFF 0x998956 (Page 16 Register 7)
SPI = 0x05 0xFFFFFFF Read P1AVG
SPO = 0xFF 0x2E0DC1 (Page 16 Register 5)
SPI = 0x14 0xFFFFFFF Read S1
SPO = 0xFF 0x2E0DB8 (Page 16 Register 20)
SPI = 0x0E 0xFFFFFFF Read Q1AVG
SPO = 0xFF 0x001226 (Page 16 Register 14)
SPI = 0x0D 0xFFFFFFF Read S1
SPO = 0xFF 0x6C9FCE (Page 16 Register 19)
SPI = 0x12 0xFFFFFFF Read I1PEAK
SPO = 0xFF 0x6CA12A (Page 16 Register 18)

Channel 2
SPI = 0x0C 0xFFFFFFF Read I2RMS
SPO = 0xFF 0x9993FE (Page 16 Register 12)
SPI = 0x0D 0xFFFFFFF Read V2RMS
SPO = 0xFF 0x9989D4 (Page 16 Register 13)
SPI = 0x0B 0xFFFFFFF Read P2AVG
SPO = 0xFF 0x2E0E17 (Page 16 Register 11)
SPI = 0x18 0xFFFFFFF Read S2
SPO = 0xFF 0x2E0E10 (Page 16 Register 24)
SPI = 0x10 0xFFFFFFF Read Q2AVG
SPO = 0xFF 0x00122C (Page 16 Register 16)
SPI = 0x19 0xFFFFFFF Read PF2
SPO = 0xFF 0x7FFFFF (Page 16 Register 25)
SPI = 0x17 0xFFFFFFF Read V2PEAK
SPO = 0xFF 0x935EC4 (Page 16 Register 23)
SPI = 0x16 0xFFFFFFF Read I2PEAK
SPO = 0xFF 0x6CA002 (Page 16 Register 22)

Total
SPI = 0x1D 0xFFFFFFF Read PSUM
SPO = 0xFF 0x5C1BD6 (Page 16 Register 29)
SPI = 0x1E 0xFFFFFFF Read SSUM
SPO = 0xFF 0x5C1BBE (Page 16 Register 30)
SPI = 0x1F 0xFFFFFFF Read QSUM
SPO = 0xFF 0x0024DE (Page 16 Register 31)
SPI = 0x1B 0xFFFFFFF Read T
SPO = 0xFF 0x000000 (Page 16 Register 27)
SPI = 0x31 0xFFFFFFF Read Epsilon
SPO = 0xFF 0x19943 (Page 16 Register 49)
CALCULATE VOLTS, AMPS, AND WATTS

Channel 1

AMPS1 = HEX2DEC(I1RMS) / 0xFFFF / 0.6 × FS_Current
VOLTS1 = HEX2DEC(V1RMS) / 0xFFFF / 0.6 × FS_Voltage
If (P1AVG ≤ 0xFFFF) Then

WATTS1 = HEX2DEC(P1AVG) / 0xFFFF / 0.36 × FS_Power
Else

WATTS1 = (HEX2DEC(P1AVG) - 0xFFFF) / 0xFFFF / 0.36 × FS_Power

Channel 2

AMPS2 = HEX2DEC(I2RMS) / 0xFFFF / 0.6 × FS_Current
VOLTS2 = HEX2DEC(V2RMS) / 0xFFFF / 0.6 × FS_Voltage
If (P2AVG ≤ 0xFFFF) Then

WATTS2 = HEX2DEC(P2AVG) / 0xFFFF / 0.36 × FS_Power
Else

WATTS2 = (HEX2DEC(P2AVG) - 0xFFFF) / 0xFFFF / 0.36 × FS_Power
6.2 Main Calibration Flow Diagram Using the CDB5484

The following flow diagram shows the implemented gain calibration using the CDB5484U and a PC as the controller. The MTE source is used to provide the source voltage and load current. Each step of the flow shows the CDB5484 GUI screen capture of execution and reading results. The register writes and reads are all identified for easy compares to the GUI screen. The GUI is not promoted for production level calibration but does provide an excellent debugger for customer flow evaluation.

**POWER UP**

Power up CDB5484U per data sheet using terminals J36 and J37.

**RESET**

(See Figure 20.)

SDI = 0xC1 Reset CS5484 software Reset.

Figure 20. Setup Window
SINGLE CONVERSION
The register checksum is computed each time a conversion is completed (Single or Continuous).
(See Figure 21.)
SDI = 0xD4  Send Single Conversion Command

VALID REGISTER CHECKSUM TEST
PC/Controller tests if valid checksum is received (see Figure 22).
SDI = 0x90 0x01 0xFFFFFF  Read Register Checksum
SDO = 0xFF 0xFF 0x46ECA1

Figure 21. Conversion Window

Figure 22. Setup Window
ENABLE HIGH PASS ON VOLTAGE AND CURRENT
(See Figure 23.)
SDI = 0x90 0x40 0x0602AA Write Register Config2 to enable HPFs
SDO = 0xFF 0xFFFF 0xFFFF
SDI = 0x90 0x00 0xFFFF Read Register Config2 to enable HPFs
SDO = 0xFF 0xFF 0x0602AA

Figure 23. Setup Window
APPLY FULL-SCALE VOLTAGE TO SOURCE
(See Figure 24.)

Figure 24. Meter Test Equipment

See Non-full-scale Gain Calibration on page 9.

FULL LOAD AVAILABLE
PC/Controller knows if full load or partial load is available (see Figure 25 for partial load).

SDI = 0x92 0x7F 0x200000 Write Scale 0.25
SDO = 0xFF 0xFF 0xFFFFFFFF

SDI = 0x92 0x3F 0xFFFFFFFF Read Scale 0.25
SDO = 0xFF 0xFF 0x200000

Figure 25. Calibration Window
SET TSETTLE
(See Figure 26.)
SDI = 0x90 0x79 0x001F40 Write TSETTLE = 2000ms
SDO =0xFF 0xFF 0xFFFFFFFF (Page 16, Register 57)
SDI = 0x90 0x39 0xFFFFFFFF Read TSETTLE = 2000ms
SDO =0xFF 0xFF 0x001F40 (Page 16, Register 57)

Figure 26. Setup Window

SET SAMPLE COUNT
(See Figure 27.)
SDI = 0x90 0x73 0x003E80 Write Sample Count = 16,000
SDO =0xFF 0xFF 0xFFFFFFFF (Page 16, Register 51)
SDI = 0x90 0x33 0xFFFFFFFF Read Sample Count = 16,000
SDO =0xFF 0xFF 0x003E80 (Page 16, Register 51)

Figure 27. Setup Window
START CONTINUOUS CONVERSION
(See Figure 28.)
SDI = 0xD5  Write Continuous Conversion
SDO = 0xFF

SDI = 0x90 0x06 0xFFFFFF Read I1RMS (page 16, register 6)
SDO = 0xFF 0xFF 0x9AC11C (0.604509151)

SDI = 0x90 0x0C 0xFFFFFF Read I2RMS (page 16, register 12)
SDO = 0xFF 0xFF 0x9ABB62 (0.604421771)

SDI = 0x90 0x07 0xFFFFFF Read V1RMS (page 16, register 7)
SDO = 0xFF 0xFF 0xA3A8BE (0.63929359)

SDI = 0x90 0x0D 0xFFFFFF Read V2RMS (page 16, register 13)
SDO = 0xFF 0xFF 0xA396E2 (0.639021077)

SDI = 0x90 0x05 0xFFFFFF Read P1AVG (page 16, register 5)
SDO = 0xFF 0xFF 0x3177E9 (0.386471914)

SDI = 0x90 0x0B 0xFFFFFF Read P2AVG (page 16, register 11)
SDO = 0xFF 0xFF 0x3170AF (0.3862514)

SDI = 0x90 0x0E 0xFFFFFF Read Q1AVG (page 16, register 14)
SDO = 0xFF 0xFF 0x000A92 (0.0003226)

SDI = 0x90 0x10 0xFFFFFF Read Q2AVG (page 16, register 16)
SDO = 0xFF 0xFF 0x000C84 (0.0003819)

SDI = 0x90 0x15 0xFFFFFF Read PF1 (page 16, register 21)
SDO = 0xFF 0xFF 0x7FFFFF (1)

SDI = 0x90 0x19 0xFFFFFF Read PF2 (page 16, register 25)
SDO = 0xFF 0xFF 0x7FFFFF (1)

Total
SDI = 0x90 0x1D 0xFFFFFF Read PSUM (page 16, register 29)
SDO = 0xFF 0xFF 0x000000 (0)

SDI = 0x90 0x1E 0xFFFFFF Read QSUM (page 16, register 30)
SDO = 0xFF 0xFF 0x000000 (0)

SDI = 0x90 0x1F 0xFFFFFF Read SSUM (page 16, register 31)
SDO = 0xFF 0xFF 0x000000 (0)
IS PF=1?
PC/Controller tests if PF returned is 1.

STOP CONVERSIONS
(See Figure 29.)
SDI = 0xD8  Write Halt Conversion
SDO = 0xFF

CLEAR DRDY in INTERRUPT STATUS
SDI = 0x80 0x57 0xFFFFFF  Write INT STATUS DRDY (page 0, register 23)
SDO = 0xFF 0xFF 0x800000  (Set DRDY INT)

SEND AC GAIN CALIBRATION
(See Figure 30.)
SDI = 0xFE  Write Gain Calibration – All Channels
SDO = 0xFF

STOP
CONVERSIONS
0xD8

Send AC GAIN CALIBRATION
0xFE

Figure 29. Conversion Window

Figure 30. Calibration Window
CHECK STATUS OF DRDY
SDI = 0x80 0x17 0xFFFFFFF Read INT STATUS DRDY (page 0, register 23) (DRDY not Set)
SDI = 0x80 0x17 0xFFFFFFF Read INT STATUS DRDY (page 0, register 23) (DRDY Set)

READ POWER REGISTERS
(See Figure 31.)
SDI = 0x90 0x06 0xFFFFFFF Read I1RMS (page 16, register 6) 0.2501238
SDI = 0x90 0x0C 0xFFFFFFF Read I2RMS (page 16, register 12) 0.2501286
SDI = 0x90 0x07 0xFFFFFFF Read V1RMS (page 16, register 7) 0.6002945
SDI = 0x90 0x0D 0xFFFFFFF Read V2RMS (page 16, register 13) 0.6003060
SDI = 0x90 0x05 0xFFFFFFF Read P1AVG (page 16, register 5) 0.1501835
SDI = 0x90 0x0B 0xFFFFFFF Read P2AVG (page 16, register 11) 0.1501892
SDI = 0x90 0x1D 0xFFFFFFF Read PSUM (page 16, register 29) 0.3002316
SDI = 0x90 0x1E 0xFFFFFFF Read QSUM (page 16, register 30) 0.0001857
SDI = 0x90 0x1F 0xFFFFFFF Read SSUM (page 16, register 31) 0.3002396

Figure 31. Conversion Window

PROPER CALIBRATION RESULTS?
PC/Controller should test for proper calibration results.

PERFORM NO LOAD COMPENSATION
No Load Offset Compensation Flow Diagram on page 47
PERFORM AC OFFSET AND READ IRMS

Note: AC offset is only required when IRMS measurements are needed with high dynamic range (only helpful at very low input levels). AC Offset Calibration Flow Diagram on page 44

SET SAMPLE COUNT
(See Figure 32.)

SDI = 0x90 0x73 0x000FA0 Write SampleCount (page 16, register 51)
SDO = 0xFF 0xFF 0xFFFFFF (4000)
SDI = 0x90 0x33 0xFFFFFF Read SampleCount (page 16, register 51)
SDO = 0xFF 0xFF 0x000FA0 (4000)

READ POWER REGISTERS
(See Figure 33.)

Gain Calibration, Channels 1 and 2, Voltage
SDI = 0x90 0x23 0xFFFFFF Read V1GAIN (page 16, register 35)
SDO = 0xFF 0x0FF 0x3C1078 (0.9385054)
SDI = 0x90 0x2A 0xFFFFFF Read V2GAIN (page 16, register 42)
SDO = 0xFF 0x0FF 0x3C1751 (0.9389233)

Gain Calibration, Channels 1 and 2, Current
SDI = 0x90 0x21 0xFFFFFF Read I1GAIN (page 16, register 33)
SDO = 0xFF 0x0FF 0x1A77A0 (0.4135514)
SDI = 0x90 0x28 0xFFFFFF Read I2GAIN (page 16, register 40)
SDO = 0xFF 0x0FF 0x1A78C4 (0.413621)

Offset Calibration, Channels 1 and 2, Current
SDI = 0x90 0x24 0xFFFFFF Read I1ACOFF (page 16, register 37)
SDO = 0xFF 0x0FF 0x000000 (0)
SDI = 0x90 0x2B 0xFFFFFF Read I2ACOFF (page 16, register 44)
SDO = 0xFF 0x0FF 0x000000 (0)

Offset Calibration, Channels 1 and 2, Active Power Offset
SDI = 0x90 0x24 0xFFFFFF Read P1OFF (page 16, register 36)
SDO = 0xFF 0x0FF 0x000000 (0)
SDI = 0x90 0x2B 0xFFFFFF Read P2OFF (page 16, register 43)
SDO = 0xFF 0x0FF 0x000000 (0)

Offset Calibration, Channels 1 and 2, Reactive Power Offset
SDI = 0x90 0x26 0xFFFFFF Read Q1OFF (page 16, register 38)
SDO = 0xFF 0x0FF 0x000000 (0)
SDI = 0x90 0x2D 0xFFFFFF Read Q2OFF (page 16, register 45)
SDO = 0xFF 0x0FF 0x000000 (0)
CHECK IF FULL LOAD IS AVAILABLE
PC/Controller knows if full load or partial load set. The following step is not required if full load is used.
(See Figure 34.)

SDI = 0x92 0x7F 0x4CCCCC Write Scale 0.6
SDO = 0xFF 0xFF 0xFFFFFF

SDI = 0x92 0x3F 0xFFFFFF Read Scale 0.6
SDO = 0xFF 0xFF 0x4CCCCC

Figure 33. Calibration Window

Figure 34. Calibration Window
COMPUTE CALIBRATED REGISTER CHECKSUM
The register checksum is computed each time a conversion is completed (Single or Continuous). If no register have changed the user needs only read the checksum register after prior conversion. But if a register has been updated (Scale for example) then the user must perform another conversion before the read (see Figure 35).

If register(s) changed since conversion (SCALE changed), then perform single conversion first, then read checksum:

$$\text{SDI} = 0xD4 \quad \text{Single Conversion Command (Optional)}$$
$$\text{SDO} = 0xFF$$
$$\text{SDI} = 0x90 \ 0x01 \ 0xFFFFFF \quad \text{Read Checksum (Page 16, Register 1)}$$
$$\text{SDO} = 0xFF \ 0xFF \ 0xF40578$$

![Figure 35. Setup Window and Conversion Window](image)

STORE CALIBRATION CONSTANTS & CHECKSUM
Write to MCU Flash all the calibration constants and checksum.
6.2.1 Phase Compensation Flow Diagram

The following flow diagram shows the implemented of phase compensation using the CDB5484U and a PC as the controller. The MTE Meter Test Equipment source is used to provide the source voltage and load current with a 60° phase shift (PF = 0.5). Each step of the flow shows the CDB5484 GUI screen capture of execution and reading results. The register writes and reads are all identified for easy compares to the GUI screen.

**Figure 36. Meter Test Equipment**
STOP CONVERSIONS
(See Figure 37.)

SDI = 0x90 0x15 0xFFFFFF Read PF1  (page 16, register 21)
SDO = 0xFF 0xFF 0x410F40  (0.508278)
SDI = 0x90 0x19 0xFFFFFF Read PF2  (page 16, register 25)
SDO = 0xFF 0xFF 0x4106A8  (0.5080157)

For 1 to Count {
  PF1SUM = PF1SUM + PF1
  PF2SUM = PF2SUM + PF2
}

PF1AVG = PF1SUM + Count
PF2AVG = PF2SUM + Count

PHASE1_OFFSET = ARCCOS(0.5083238) - 60º = -0.55224327
PHASE2_OFFSET = ARCCOS(0.5085984) - 60º = -0.57051489

Use this constant stored from PC/Controller memory in following calculations.
PHASE OFFSET
PC/Controller test for phase calibration range meet or fail meter. This example shows negative phase offset.

Figure 38. Negative Phase Offset

PHASE OFFSET
PC/Controller test for coarse phase calibration range.

When > 1 OWR, PC/Controller calculates Coarse Compensation
CPCC1 = 0
CPCC2 = 0

PC/Controller calculates Fine Compensation
FPCC1 = -(-0.55224327) / 0.008789 @ 50Hz = 62,
FPCC2 = -(-0.57051489) / 0.008789 @ 50Hz = 64,

CPCC1=0, FPCC1 = 62, CPCC2=0, FPCC2 = 64
SDI = 0x80 0x45 0x007C40 Write Phase Comp (page 0, register 69)
SDO = 0xFF 0xFF 0xFFFFFF

SDI = 0x80 0x05 0xFFFFFF Write Phase Comp (page 0, register 69)
SDO = 0xFF 0xFF 0x007C40

Example Location

0º

Before Calibration V is delayed from I
Delay added to I

8.99º @ 50Hz
10.79º @ 60Hz
4.5º @ 50Hz
5.4º @ 60Hz
-4.5º @ 50Hz
-5.4º @ 60Hz
-8.99º @ 50Hz
-10.79º @ 60Hz
ACCUMULATE MULTIPLE PF READING AND CONFIRM
(See Figure 39.)

SDI = 0x90 0x15 0xFFFFFF Read PF1 (page 16, register 21)
SDO = 0xFF 0x410F40 (0.508278)
SDI = 0x90 0x19 0xFFFFFF Read PF2 (page 16, register 25)
SDO = 0xFF 0x4106A8 (0.5080157)

For 1 to Count {
PF1SUM = PF1SUM + PF1
PF2SUM = PF2SUM + PF2
PF1AVG = PF1SUM ÷ Count
PF2AVG = PF1SUM + Count

Figure 39. Conversion Window
6.2.2 AC Offset Calibration Flow Diagram

The following flow diagram shows the implemented AC offset calibration using the CDB5484U and a PC as the controller. The MTE Meter Test Equipment source is used to provide the source voltage and no load current. Each step of the flow shows the CDB5484 GUI screen capture of execution and reading results. The register writes and reads are all identified for easy compares to the GUI screen.

REMOVE LOAD CURRENT
(See Figure 40.)

**Figure 40. Meter Test Equipment**

CLEAR DRDY in INTERRUPT STATUS
SDI = 0x80 0x57 0xFFFFFFFF Write INT STATUS DRDY
SDO = 0xFF 0xFF 0x800000 (Set DRDY INT) (page 0, register 23)
SEND AC OFFSET CALIBRATION
(See Figure 41.)

SDI = 0xF6  Write AC Offset Calibration – All Channels
SDO = 0xFF

Figure 41. Calibration Window

DRDY SET?
SDI = 0x80 0x17 0xFFFFFFFFRead INT STATUS DRDY (page 0, register 23)
SDO = 0xFF 0xFF 0x4XXXXX (DRDY not Set)

SDI = 0x80 0x17 0xFFFFFFFFRead INT STATUS DRDY (page 0, register 23)
SDO = 0xFF 0xFF 0xCXXXXX (DRDY Set)
6.2.3 DC Offset Calibration Flow Diagram

The implemented of DC offset calibration follows the same structure as AC offset except that the voltage and current source are both zero. The high pass filters must not be enabled and instead of sending AC Calibration command (F6), the DC Calibration command is sent (E6). Refer to the main flow for reading the DC offset registers.

Figure 42. Conversion Window
PC/Controller tests for change in IACOFF register to check for success.
6.2.4 No Load Offset Compensation Flow Diagram

The following flow diagram shows the implementation of no load power offset compensation using the CDB5484U and a PC as the controller. The MTE Meter Test Equipment source is used to provide the source voltage and no load current. Each step of the flow shows the CDB5484 GUI screen capture of execution and reading results. The register writes and reads are all identified for easy compare to the GUI screen.

**APPLY FULL SCALE VOLTAGE AND ZERO LOAD CURRENT**

(See Figure 43.)

**Figure 43. Meter Test Equipment**
ACCUMULATE MULTIPLE PAVG, QAVG READINGS
(See Figure 44.)

Channels 1 and 2, Active Power
SDI = 0x90 0x05 0xFFFFF Read P1AVG (page 16, register 5)
SDO = 0xFF 0xFF 0xFFFFFC (-0.00000048)
SDI = 0x90 0x0B 0xFFFFF Read P2AVG (page 16, register 11)
SDO = 0xFF 0xFF 0xFFFFFC (-0.00000012)

Channels 1 and 2, Reactive Power
SDI = 0x90 0x0E 0xFFFFF Read Q1AVG (page 16, register 14)
SDO = 0xFF 0xFF 0xFFFFFC (-0.00000024)
SDI = 0x90 0x10 0xFFFFF Read Q2AVG (page 16, register 16)
SDO = 0xFF 0xFF 0xFFFFFC (-0.00000048)
SET POFF AND QOFF

Negate PAVG and QAVG registers and store in POFF and QOFF respectively (see Figure 44).

SDI = 0x90 0x64 0xFFFF Write P1OFF (page 16, register 36)
SDO = 0xFF 0x000003 (3.57628E-07)
SDI = 0x90 0x24 0xFFFF Read P1OFF (page 16, register 36)
SDO = 0xFF 0x000003 (3.57628E-07)
SDI = 0x90 0x6B 0xFFFF Write P2OFF (page 16, register 43)
SDO = 0xFF 0x000001 (1.19209E-07)
SDI = 0x90 0x2B 0xFFFF Read P2OFF (page 16, register 43)
SDO = 0xFF 0x000001 (1.19209E-07)
SDI = 0x90 0x66 0xFFFF Write P1OFF (page 16, register 38)
SDO = 0xFF 0x000002 (2.38419E-07)
SDI = 0x90 0x26 0xFFFF Read P1OFF (page 16, register 38)
SDO = 0xFF 0x000002 (2.38419E-07)
SDI = 0x90 0x6D 0xFFFF Write P2OFF (page 16, register 45)
SDO = 0xFF 0x000002 (2.38419E-07)
SDI = 0x90 0x2D 0xFFFF Read P2OFF (page 16, register 45)
SDO = 0xFF 0x000002 (2.38419E-07)

Figure 45. Calibration Window
Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>REV1</td>
<td>APR 2012</td>
<td>Initial release.</td>
</tr>
<tr>
<td>REV 2</td>
<td>MAY 2012</td>
<td>Corrected typographical errors.</td>
</tr>
</tbody>
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Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to [http://www.cirrus.com](http://www.cirrus.com)

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