CIRRUS LOGIC®

AN397

Surface Mount Assembly Considerations for WLCSP Devices

1 Introduction

Wafer Level Chip Scale Packaging (WLCSP) is essentially the same as flip chip, but with solder bump sizes and pitches large enough to facilitate direct mounting of the device to a printed circuit board (PCB). As the name implies, all package processing is performed at the wafer level with finished devices singulated from the wafer and placed directly into shipping media.

The finished WLCSP devices are the same size as the integrated circuit die they are fabricated from, so this type of packaging allows the smallest possible board footprint. Also, the short electrical connections enabled by the solder bumps provide excellent electrical performance with parasitic resistance, capacitance, and inductance kept to a minimum.

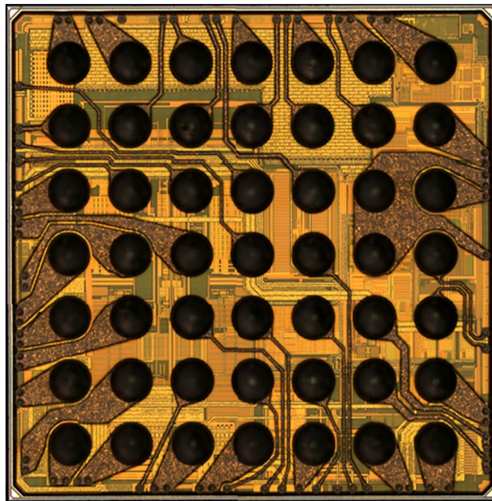

Figure 1: Typical WLCSP Device

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1.1 Structure

WLCSP’s can be fabricated in a variety of ways, but the most typical structure used by Cirrus Logic includes a copper redistribution layer (RDL) to route connections from the die to the solder bumps. The RDL is sandwiched between two polymer dielectric layers which provide mechanical and environmental protection to the die and redistribution layer. Copper metal pads are deposited on top of the dielectric layer stack and provide the electrical and mechanical connections for the solder bumps to attach to. Owing to their position under the solder bumps, these pads are known as the under bump metal or UBM pads.

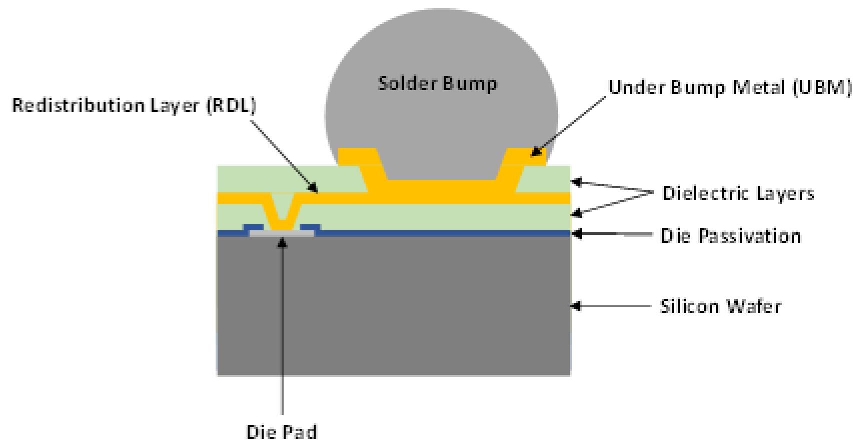

Figure 2: WLCSP Cross Section

2 Board Design Considerations

2.1 Board Material Selection

Standard glass reinforced epoxy laminate type printed circuit boards are acceptable for use with WLCSP devices. An FR4 material with high glass transition temperature (Tg > 170°C) should be used. The high-Tg materials are more stable during reflow and have lower coefficients of thermal expansion (CTE) than the standard FR4 material. A lower CTE will be better matched to the CTE of the WLCSP device and may result in improved solder joint life.

2.2 Land Pattern Design

The land pattern is the array of copper pads on the board that the WLCSP device will be soldered to. The design of these pads has a significant impact on manufacturing yield and solder joint reliability. Some suggestions for optimizing the land pattern design are provided below.

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2.2.1 Pad Types

There are two ways to define the size and shape of the land pads: Solder Mask Defined (SMD) and Non-Solder Mask Defined (NSMD). See the figure below for a comparison of these two pad types.

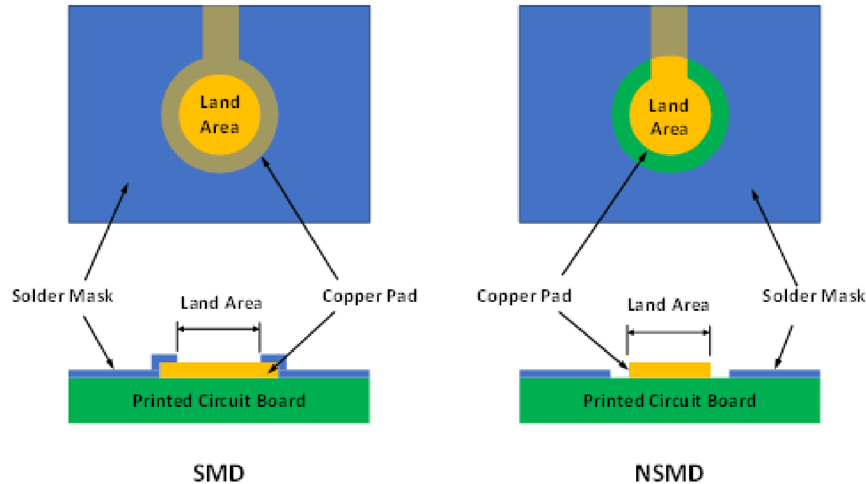

Figure 3: SMD Pad Compared to NSMD Pad

In the case of SMD pads, the copper pad is larger than the solder mask opening and the land area of the pad is defined by the solder mask opening. For NSMD pads, the copper pad defines the land area and the solder mask opening is larger than the copper pad.

Both types of pads can be used for WLCSP devices. Each type has its own specific advantages for different applications:

- SMD pads are typically selected to optimize drop test performance.
- NSMD pads are typically selected to optimize thermal cycling performance. Since the solder mask is pulled back from the copper pad, solder can wet the pad side walls and this results in a stronger solder joint. Also, the copper pad diameter is smaller for NSMD pads than for SMD pads, so there is more room between NSMD pads to route traces.

For most applications, designing with NSMD pads will yield the best results.

2.2.2 Pad Design

To achieve the best solder joint reliability, the land area of the pad (see Figure 3) should be circular in shape and the diameter of the land should match the diameter of the UBM pad on the WLCSP (see Figure 2). The diameter of the UBM pad varies with bump pitch and other design considerations. To determine the UBM pad diameter for the specific WLCSP device you are using, please contact your Cirrus Logic sales representative.

SMD Pads

The land area of the SMD pad is defined by the solder mask opening. The underlying copper pad should be 75–100 µm larger in diameter than the target solder mask opening. Solder mask registration needs to be controlled to assure that the solder mask opening does not overlap with the edge of underlying copper pad as this can result in a misshapen solder joint.

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NSMD Pads

The land area of the NSMD pad is defined by the copper pad. To assure proper clearance between the pad and the solder mask, the solder mask should be pulled back from the pad 60–75 µm. Solder mask registration needs to be controlled to assure that the solder mask does not overlap with the copper pad as this can result in a misshapen solder joint.

Traces connected to the NSMD pad will be exposed in the region between the pad and the solder mask (see figure below). Solder can wick down this segment of the trace, depleting solder from the primary solder joint. To minimize this solder depletion, the width of the trace in the exposed region should be no more than 60% the diameter of the copper pad. The width of the trace can be increased once the trace is fully covered by solder mask.

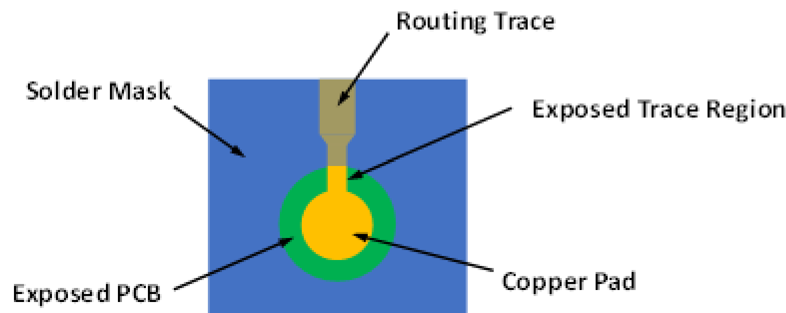

Figure 4: NSMD Pad Structure Top View

Via-in-Pad

If Via-in-Pad is used, the via hole should be filled and plated over, leaving a level surface with the rest of the pad. Unfilled vias will allow solder to wick down the hole, depleting solder from the primary solder joint. Depressions in the pad surface can trap air or other contaminants which can outgas during reflow and create voids in the solder joint.

2.3 Surface Finish

OSP (Organic Surface Preservative) provides excellent flatness and solderability and is recommended for WLCSP applications.

ENIG (Electroless Ni/Au) also provides excellent flatness and solderability but may not perform as well in drop test as OSP finishes. Also, ENIG is susceptible to “black pad” failures if the plating bath is not well controlled. Controlling the gold thickness may help to mitigate the risk of black pad formation as excessive nickel corrosion can take place in an aggressive gold plating bath. IPC-4552 recommends that the gold thickness be maintained in a range from 0.04–0.10 µm (1.58–3.97 µin).

HASL (Hot Air Solder Leveling) is not recommended as the flatness of the finished surface is not as well controlled as for OSP or ENIG, which can result in inconsistent solder joint quality.

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3 Stencil Design

3.1 Stencil Type

The small land pad sizes used for WLCSP devices drive correspondingly small aperture sizes in the solder paste stencil. As the aperture size decreases, solder paste release from the aperture becomes more difficult. When designing a stencil for WLCSP applications, consideration must be given to the paste transfer efficiency.

For most WLCSP applications, a laser-cut and electro-polished stainless-steel stencil will perform well. The aperture walls should be cut to be trapezoidal, with the bottom of the aperture larger than the top, to facilitate paste release.

If sufficient paste release is not achieved with a laser-cut stencil, an electroformed (E-Fab) nickel stencil may be considered. Electroforming produces very smooth, trapezoidal aperture walls which are ideal for paste release, however, at a higher cost than laser cutting.

3.2 Aperture Design

Studies have shown that square apertures perform better than round apertures for the small land pads used with WLCSP devices. Paste transfer efficiency is better and the extended corners of the square aperture provide roughly 25% more paste volume to the solder print. The length of the sides of the square should match the land pad diameter. Rounding the corners will also help to improve the paste release (see figure below).

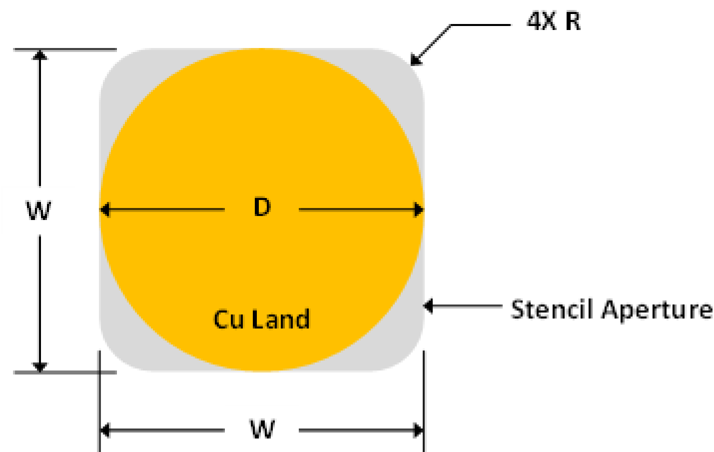

Figure 5: Aperture Design

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3.3 Stencil Thickness

The stencil thickness affects how well the solder paste will release from the stencil. More specifically, the release performance has been correlated to the ratio between the aperture opening area and the aperture wall area. Considering the square apertures used for WLCSP devices (shown in figure 5), the ratio of these two areas is defined as:

$$Area\ Ratio = \frac{Area\ of\ Aperture\ Opening}{Area\ of\ Aperture\ Walls} = \frac{W^2}{4Wt} = \frac{W}{4t}$$

Where W = width of the square aperture and t = stencil thickness.

The area of the aperture opening affects the adhesion of paste to the board while the area of the aperture walls affects adhesion of paste to the stencil. The stencil must be designed to achieve the appropriate balance between these competing forces. IPC-7525 defines the optimum area ratio as >0.66. However, with the use of electroformed stencils or special coatings on the stencil, effective paste release can be achieved with area ratios down to 0.50. Area ratios for some common aperture sizes versus stencil thickness have been calculated and are shown in the table below.

Table 1: Area Ratios for Common Aperture Sizes and Stencil Thicknesses

	Stencil Thickness			
Aperture Width (W)	50 µm	75 µm	100 µm	125 µm
170 µm	0.85	0.57	0.43	0.34
200 µm	1.00	0.67	0.50	0.40
240 µm	1.20	0.80	0.60	0.48

Color	Meaning
Green	Good
Yellow	OK
Red	Not Recommended

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4 Solder Paste

4.1 Solder Paste Composition

4.1.1 Solder Alloy

All Cirrus Logic WLCSP's are lead-free and should only be assembled to the board using a lead-free solder paste. Solder pastes using a SAC (Tin-Silver-Copper) alloy for the solder component are common and should perform well for WLCSP assembly.

4.1.2 Flux

Cleaning flux from under the WLCSP device is difficult due to the very small stand-off height. Best results will be achieved using a no-clean type flux.

4.2 Solder Paste Types

Just as the aperture dimensions affect the selection of the stencil thickness, they also affect the selection of the appropriate solder paste type. Solder pastes are characterized by the size of the particles in the solder powder used to make the paste. Some common solder paste types and their associated particle size distributions are shown in the following table.

Table 2: Solder Paste Types

IPC Type	Particle Size Range (Central 80% of the Distribution)
3	25–45 µm
4	20–38 µm
5	15–25 µm
6	5–15 µm

A rule-of-thumb, known as the *Five Ball Rule*, states that to achieve good paste transfer, a minimum of five of the largest solder balls in the paste should fit within the minimum width of aperture (see figure below).

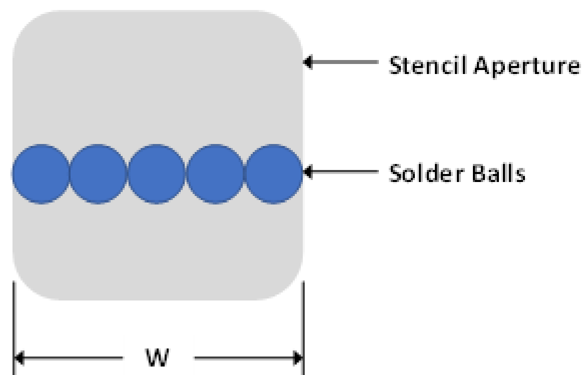

Figure 6: Five Ball Rule

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Applying the five-ball rule to the maximum particle sizes given in table 2, the theoretical minimum aperture widths for each paste type can be calculated and are shown in the following table.

Table 3: Minimum Aperture Width by Solder Paste Type

IPC Type	Maximum Particle Size (Central 80% of the Distribution)	Minimum Aperture Width (W)
3	45 µm	225 µm
4	38 µm	190 µm
5	25 µm	125 µm
6	15 µm	75 µm

5 Reflow Profile

All the Cirrus Logic WLCSP devices are qualified to withstand the reflow conditions defined in the JEDEC J-STD-020 specification for Pb-free, small body components. However, the reflow profile specified in that document represents the worst case conditions the device can be expected to see. The appropriate reflow profile for any given board will depend on the board size, layer count, metal loading, component count, solder paste, and reflow furnace used. The customer must determine the appropriate profile by taking measurements on an actual board and using the same equipment type that will be used for mass production.

Most of the lead-free solder pastes have melting points around 217°C. To achieve proper flux activation and solder wetting, reflow should take place at least 20°C above the melting point. If you experience poor solder wetting, it is often due to the peak temperature being too low or the dwell time at peak being too short. Adjusting these parameters can often resolve the issue.

6 Reference Documents

The documents listed in the following table provide useful information regarding the different design considerations discussed in this application note. The document revision letters have been left off the document numbers as the revisions change frequently. Please reference the most recent revision.

Table 4: List of Reference Documents

Document Number	Title
IPC-7094	Design and Assembly Process Implementation for Flip Chip and Die Size Components
IPC-4101	Specification for Base Materials for Rigid and Multilayer Boards
IPC-4552	Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards
IPC-7351	General Requirements for Surface Mount Design and Land Pattern Reference
IPC-7525	Stencil Design Guidelines
J-STD-005	Requirements for Soldering Pastes
IPC-7527	Requirements for Solder Paste Printing
J-STD-020	Moisture/Reflow Sensitivity Classification for Non-Hermetic Surface Mount Devices

7 Revision History

Revision	Changes
R1 Nov 2020	• Initial release

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