INTRODUCTION

This document describes the layout Guidelines for the CS47L15-M-1 customer board.

GENERAL BOARD CONSIDERATIONS

1. Avoid routing digital signals between power planes on an adjacent layer.
2. Avoid routing analogue and Digital signals next to each other

LAYOUT GUIDELINES

Note 1: Analogue Inputs
Route analogue inputs differentially
- Match impedance of input pairs and track together. [Medium Priority]
- Keep inputs away from High Speed signals. [High Priority]
- Mixed analogue/digital inputs are IN1AL.
- Analogue only inputs are IN1AR, IN1BL, IN1BR & IN2.

Note 2: HPOUT
- Route HPOUTL & HPOUTR as a pair. [Medium Priority]
- Single Ended: Route MICDET1/HPOUTFB1 & MICDET2/HPOUTFB2 between HPOUTL and HPOUTR. [High Priority]
- The HPOUT signal tracks should have low DC resistance tracks. Recommended DC resistance is 1% of Min load. (0.06 Ohms for 6 ohm load) [Medium Priority]

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Resistance</td>
<td>&lt; 0.06</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

Note 3: EPOUT
- Route EPOUTP & EPOUTN as a pair. [Medium Priority]
- The EPOUT signal tracks should have low DC resistance tracks. Recommended DC resistance is 1% of Min load. (0.06 Ohms for 6 ohm load) [Medium Priority]

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Resistance</td>
<td>&lt; 0.06</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>
**Note 4:**  **SPKOUT**
- Route SPKOUTP & SPKOUTN as a pair. [Medium Priority]
- The SPKOUT signal tracks should have low DC resistance tracks. Recommended DC resistance is 1% of Min load. (0.06 Ohms for 6 ohm load) [Medium Priority]

<table>
<thead>
<tr>
<th>DC Resistance</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>&lt; 0.04</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

**Note 5:**  **Device Decoupling** [Medium/High Priority]
Place de-coupling capacitors close to device.

**Note 6:**  **Charge Pump** [High Priority]
A local ground plane should be used for CPGND and the charge pump de-coupling. The local ground plane should be connected to the common ground plane close to the CPVDD de-coupling cap.
- VIAs to all GND planes should also be placed under the local ground plane. (4 - 8 VIA's)
- Traces on inside layers should use multiple Via’s to the capacitors.
- Order of priority in relation to charge pump.

<table>
<thead>
<tr>
<th>Priority</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CPC2n CPGND</td>
</tr>
<tr>
<td>2</td>
<td>CPVOUT2n CPVDD</td>
</tr>
<tr>
<td>3</td>
<td>CPC1n</td>
</tr>
<tr>
<td>4</td>
<td>CPVOUT1n</td>
</tr>
</tbody>
</table>
Note 7: **VREFC GND Return [High Priority]**
The VREFC cap current return path should be routed to AGND (Pin D3). AGND should be connected to the GND plane at the pin.

![VREFC trace to decoupling capacitor](image)

![VREFC GND return](image)

Note 8: **Digital Signals**
- Use controlled 50Ω characteristic impedance for digital signals.  
  [Low Priority]
- Place series termination resistors close to DUT.  
  [Medium Priority]
Note 9: PDM Outputs [Low Priority]
Route each set of speaker PDM outputs as a pair.

Note 10: Speaker Protection Current Sense Resistors. [High Priority]
- Place R78 close to SPKGNDP (H1)
- Place R80 close to SPKGNDN (K1)

Note 11: TVS Diode placement [Medium/High Priority]
- Use 4 vias or more in GND
- Tracks with TVS diodes should be thicker
- Place a close as possible to the headphone jack

Note 12: Headset [Medium/High Priority]
- Star connect IN1BRP, MICDET2/HPOUTFB2, SP1 & U4:P6 & P8 at J2:P1.
- Star connect IN1BLN, MICDET1/HPOUTFB1, SP2 & U4:P3 & P7 at J2:P2.
- Use a low impedance connection between SP1, SP2 & and GND.
- Use a low impedance connection between J4:P1 & U4:P6 & P8
- Use a low impedance connection between J4:P2 & U4:P3 & P7
KEY TO LAYOUT ITEM PRIORITY

<table>
<thead>
<tr>
<th>Priority</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>High</td>
<td>Items of high priority must be followed by the customer. If not, this will affect the correct operation of the Cirrus device.</td>
</tr>
<tr>
<td>Medium</td>
<td>Items of Medium priority, if not followed may potentially affect the performance of the Cirrus device.</td>
</tr>
<tr>
<td>Low</td>
<td>Items of Low priority are listed as a ‘good practice’ measure.</td>
</tr>
</tbody>
</table>

SYSTEM ESD GUIDELINES FOR HEADSET

ESD PROTECTION DIODES

The customer should make sure the response time of any ESD protection Diodes used can protect the system for a broad spectrum of ESD transient pulses, from very fast, to extremely slow for large and small ESD voltages.

When testing ESD performance of a system, testing with different contact discharge waveforms from 500V to 8kV in incremental steps, helps verify the selected ESD protection devices can sufficiently protect the system.

BOARD SCHEMATIC OPTIMIZATION

Component placement and board layout are as important as selecting the most suitable ESD protection components. Figure 1 shows a typical combined ESD and EMI circuit protection for a headphone output.

![Figure 1 combined ESD and EMI protection](image_url)
POSITION OF ESD PROTECTION COMPONENTS

PCB layout is critical when using ESD protection components. The ESD protection device should protect the whole PCB, not just the Cirrus Logic device, by diverting the discharge to ground and not letting it pass through the ICs. The following guidelines, as well as any stated on the ESD protection devices manufacturer’s datasheet for ESD protection should be followed:

1. The ESD protection device should be placed as close to the connector as possible.
2. The ESD protection device should be placed on the line to be protected, not joined by a track stub, which adds inductance.
3. The ESD protection device must have a short return path to ground to reduce inductance. A good way to achieve this is to place a pair of GND vias as close as possible to the GND pin of the ESD protection device and the GND pin of the connector, as shown in Figure 2. The double via technique reduces inductance. The best way to achieve it is a GND plane added to the top side of the PCB, to link the ESD diode and connector, as shown in Figure 3. This top side plane must have several vias to the main PCB GND plane in case the discharge path from the connector goes to another part of the end-product.
4. Don’t share the GND return path between more than one ESD protection devices, unless it is via a low inductance GND plane.
5. Wide signal tracks from the connector to the protection device reduce the inductance for the ESD charge.
6. Figure 2 and Figure 3 below summaries the above suggestions.

Please consult the datasheet of the ESD protection diode for further advice.
If you require more information or require technical support, please contact one of the Cirrus Logic regional offices. To find one nearest you, go to www.cirrus.com.
## REVISION HISTORY

<table>
<thead>
<tr>
<th>DATE</th>
<th>REV</th>
<th>DESCRIPTION OF CHANGES</th>
<th>PAGE</th>
<th>CHANGED BY</th>
</tr>
</thead>
<tbody>
<tr>
<td>06/05/2016</td>
<td>1.0</td>
<td>Original document created</td>
<td></td>
<td>Craig McAdam</td>
</tr>
</tbody>
</table>
**Contacting Cirrus Logic Support**

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find one nearest you, go to [www.cirrus.com](http://www.cirrus.com).

The products and services of Cirrus Logic International (UK) Limited; Cirrus Logic, Inc.; and other companies in the Cirrus Logic group (“Cirrus”) are sold subject to Cirrus’s terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, indemnification, and limitation of liability. Software is provided pursuant to applicable license terms. Cirrus reserves the right to make changes to its products and specifications or to discontinue any product or service without notice. Customers should therefore obtain the latest version of relevant information from Cirrus to verify that the information is current and complete. Testing and other quality control techniques are utilized to the extent Cirrus deems necessary. Specific testing of all parameters of each device is not necessarily performed. In order to minimize risks associated with customer applications, the customer must use adequate design and operating safeguards to minimize inherent or procedural hazards. Cirrus is not liable for applications assistance or customer product design. The customer is solely responsible for its selection and use of Cirrus products.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE (“CRITICAL APPLICATIONS”). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, NUCLEAR SYSTEMS, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER’S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER’S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS’ FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied, under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Any provision or publication of any third party’s products or services does not constitute Cirrus’s approval, license, warranty or endorsement thereof. Cirrus gives consent for copies to be made of the information contained herein only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus, and only if the reproduction is without alteration and is accompanied by all associated copyright, proprietary and other notices and conditions (including this notice). This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale. This document and its information is provided “AS IS” without warranty of any kind (express or implied). All statutory warranties and conditions are excluded to the fullest extent possible. No responsibility is assumed by Cirrus for the use of information herein, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. Cirrus Logic, Cirrus, the Cirrus Logic logo design and SoundClear are among the trademarks of Cirrus. Other brand and product names may be trademarks or service marks of their respective owners.

Copyright © 2016 Cirrus Logic, Inc. All rights reserved.