AN0679

CS430xx Output Buffer/Filter Circuits

Introduction

The CS430xx family of high-performance DAC devices provide a current-mode output and require an external current-to-voltage (I to V) buffer/filter circuit. This document describes the recommended external buffer/filter circuits.

Different buffer/filter solutions are described and compared in this document.

Table of Contents

1 Output Buffer Circuits – CS4304P, CS4308P

This section describes differential and single-ended output-buffer/filter circuits for the CS4304P and CS4308P high-performance DAC devices. Four options are described, as summarized in Table 1.

Table 1 Output Buffer/Filter Circuits Summary

Description	Op-Amps	Advantages	Disadvantages
Differential Output in Inverting Configuration	2 per output	Maximum dynamic range. Common mode rejection.	—
Single-Ended Non-Inverting Output with Line Driver	3 per output	Drives headphone/line loads.	3 op-amps required per output.
Single-Ended Non-Inverting Output Configuration	2 per output	Large dynamic range. 2 op-amps required per output.	Increased noise below 200 Hz.
Single-Ended Inverting Output with Reduced BOM	1 per output, plus 1 shared between outputs	Reduced bill of materials (BOM).	Reduced dynamic range. Increased noise below 200 Hz

1.1 Differential Output in Inverting Configuration

Figure 1 shows a differential output buffer using dual op-amps in inverting configuration.

This circuit provides a full-scale output of 2 V_{RMS}. The full-scale output level is configurable using the op-amp feedback resistors (see Section 5 of the device datasheet for further information).

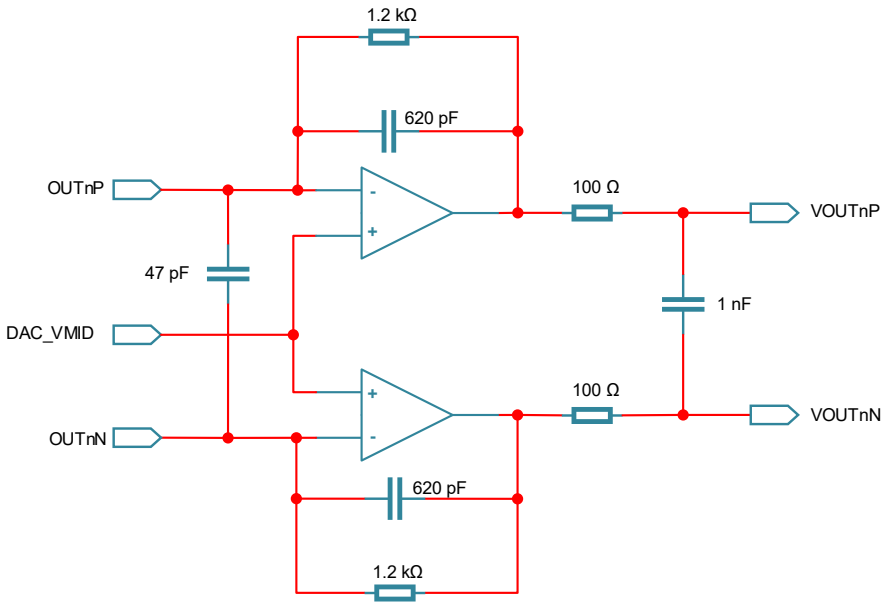

Figure 1 Differential Output in Inverting Configuration

1.2 Single-Ended Non-Inverting Output with Line Driver

Figure 2 shows a single-ended output buffer, comprising a differential inverting I-to-V stage and an inverting line driver.

This circuit provides a full-scale output 2 V_{RMS}. The full-scale output level is configurable using the op-amp feedback resistors in the I-to-V stage (see Section 5 of the device datasheet for further information).

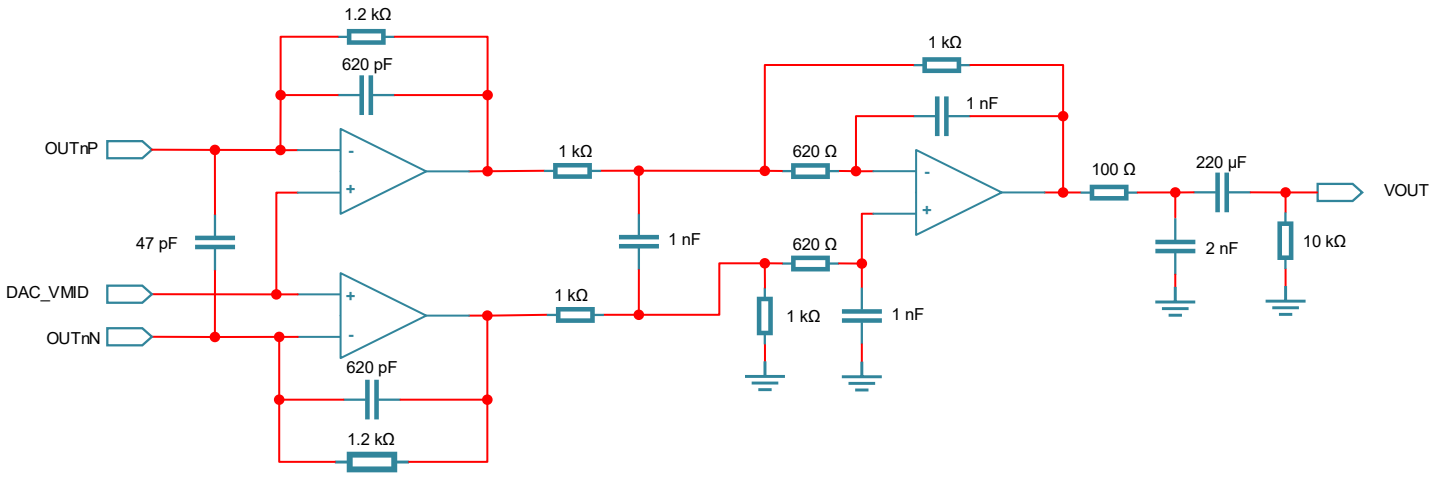

Figure 2 Single-Ended Non-Inverting Output with Line Driver

1.3 Single-Ended Non-Inverting Output Configuration

Figure 3 shows a single-ended output buffer using two op-amps in series.

This circuit provides a full-scale output of 2 V_{RMS}. The full-scale output level is configurable using the op-amp feedback resistors (see Section 5 of the device datasheet for further information).

The THD+N performance is degraded using the configuration shown. The loss of performance can be minimized by adding two 10 µF capacitors between the DAC_VMID path and GND. Note that adding these capacitors also increases the start-up time for the output paths.

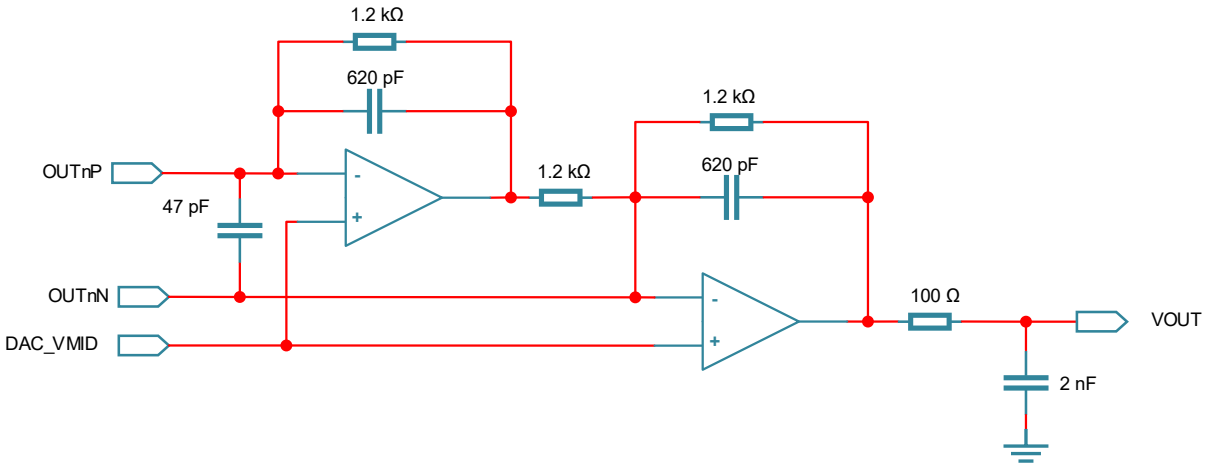

Figure 3 Single-Ended Non-Inverting Output Configuration

1.4 Single-Ended Inverting Output with Reduced BOM

Figure 4 shows a single-ended output buffer with a reduced bill of materials (BOM). One op-amp is required for each OUTnP channel; the additional op-amp driving OUTnN can be shared across multiple channels.

This circuit provides a full-scale output of 2 V_{RMS}. The full-scale output level is configurable using the op-amp feedback resistor (see Section 5 of the device datasheet for further information).

The THD+N performance is degraded using the configuration shown. The loss of performance can be minimized by adding two 10 µF capacitors between the DAC_VMID path and GND. Note that adding these capacitors also increases the start-up time for the output paths.

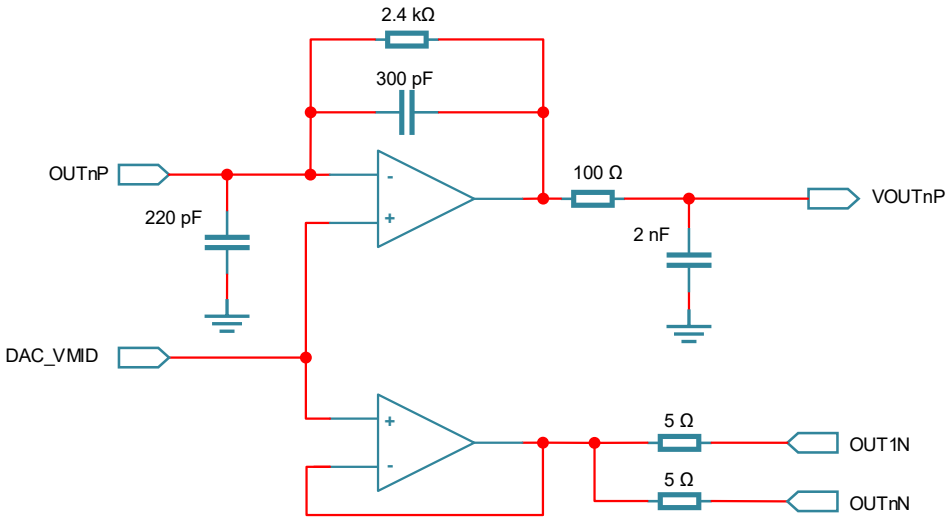

Figure 4 Single-Ended Inverting Output with Reduced BOM

2 Output Buffer Circuits – CS4304S, CS4308S

This section describes differential and single-ended output-buffer/filter circuits for the CS4304S and CS4308S high-performance DAC devices. Four options are described, as summarized in Table 2.

Table 2 Output Buffer/Filter Circuits Summary

Description	Op-Amps	Advantages	Disadvantages
Differential Output in Inverting Configuration	2 per output	Maximum dynamic range. Common mode rejection.	—
Single-Ended Non-Inverting Output with Line Driver	3 per output	Drives headphone/line loads.	3 op-amps required per output.
Single-Ended Non-Inverting Output Configuration	2 per output	Large dynamic range. 2 op-amps required per output.	Increased noise below 200 Hz.
Single-Ended Inverting Output with Reduced BOM	1 per output, plus 1 shared between outputs	Reduced bill of materials (BOM).	Reduced dynamic range. Increased noise below 200 Hz

2.1 Differential Output in Inverting Configuration

Figure 5 shows a differential output buffer using dual op-amps in inverting configuration.

This circuit provides a full scale output of 2 V_{RMS}. The full-scale output level is configurable using the op-amp feedback resistors (see Section 5 of the device datasheet for further information).

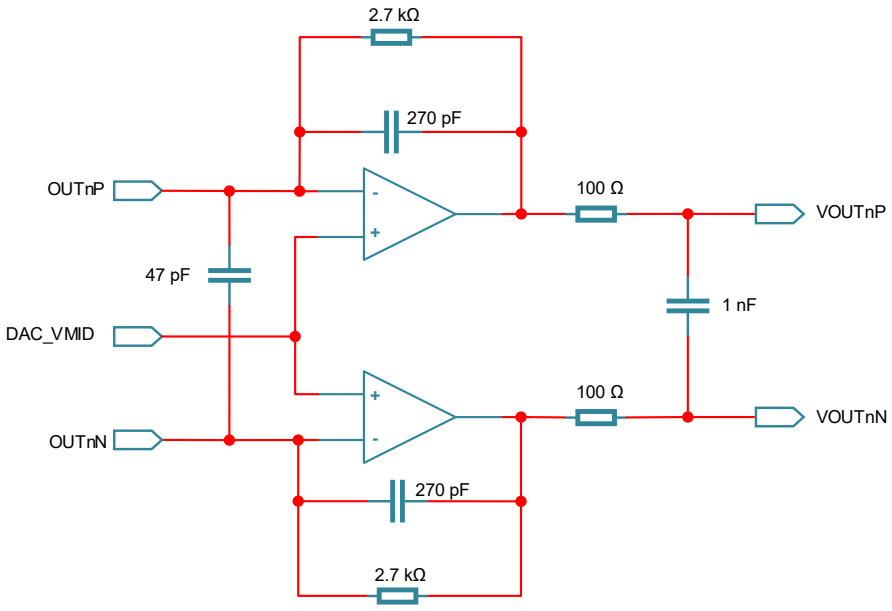

Figure 5 Differential Output in Inverting Configuration

2.2 Single-Ended Non-Inverting Output with Line Driver

Figure 6 shows a single-ended output buffer, comprising a differential inverting I-to-V stage and an inverting line driver.

This circuit provides a full-scale output 2 V_{RMS}. The full-scale output level is configurable using the op-amp feedback resistors in the I-to-V stage (see Section 5 of the device datasheet for further information).

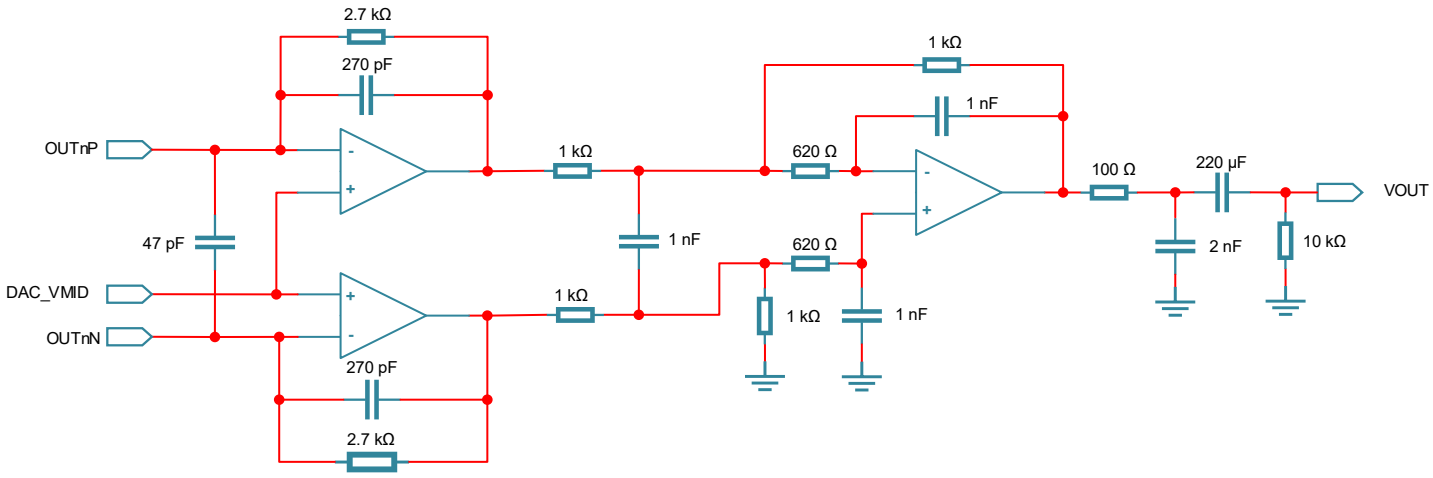

Figure 6 Single-Ended Non-Inverting Output with Line Driver

2.3 Single-Ended Non-Inverting Output Configuration

Figure 7 shows a single-ended output buffer using two op-amps in series.

This circuit provides a full scale output of 2 V_{RMS}. The full-scale output level is configurable using the op-amp feedback resistors (see Section 5 of the device datasheet for further information).

The THD+N performance is degraded using the configuration shown. The loss of performance can be minimized by adding two 10 µF capacitors between the DAC_VMID path and GND. Note that adding these capacitors also increases the start-up time for the output paths.

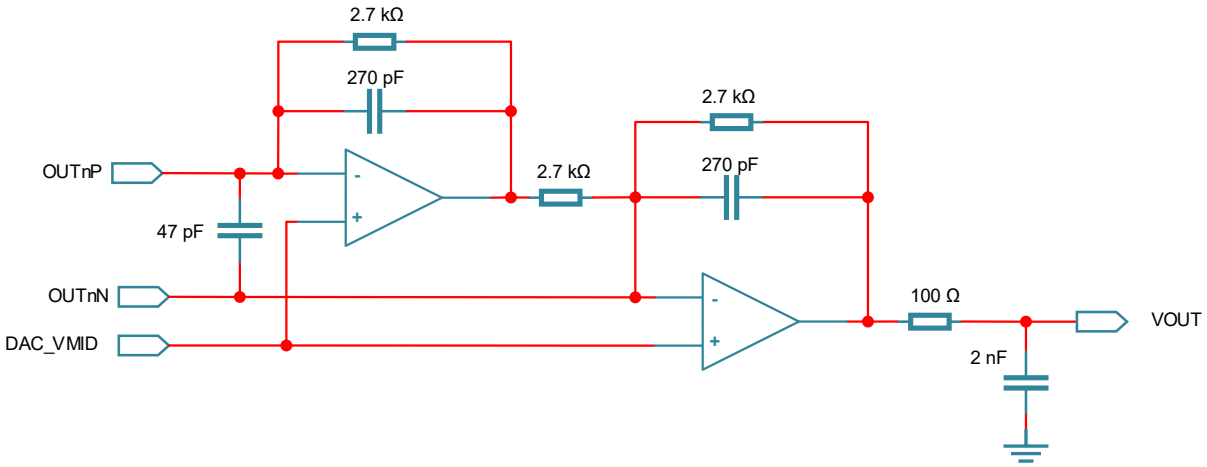

Figure 7 Single-Ended Non-Inverting Output Configuration

2.4 Single-Ended Inverting Output with Reduced BOM

Figure 8 shows a single-ended output buffer with a reduced bill of materials (BOM). One op-amp is required for each OUTnP channel; the additional op-amp driving OUTnN can be shared across multiple channels.

This circuit provides a full-scale output of 2 V_{RMS}. The full-scale output level is configurable using the op-amp feedback resistor (see Section 5 of the device datasheet for further information).

The THD+N performance is degraded using the configuration shown. The loss of performance can be minimized by adding two 10 µF capacitors between the DAC_VMID path and GND. Note that adding these capacitors also increases the start-up time for the output paths.

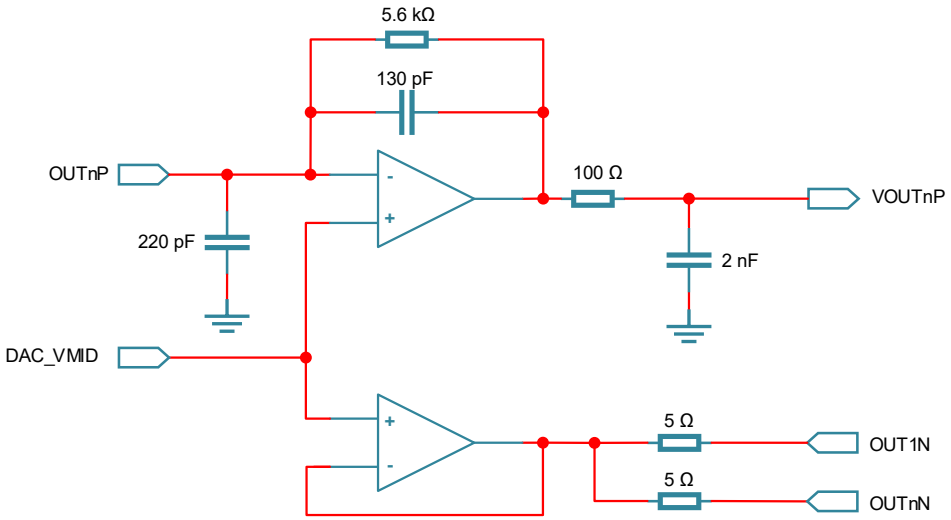

Figure 8 Single-Ended Inverting Output with Reduced BOM

3 Output Buffer Circuits – CS4302P

This section describes differential and single-ended output-buffer/filter circuits for the CS4302P high-performance DAC. Four options are described, as summarized in Table 3.

Table 3 Output Buffer/Filter Circuits Summary

Description	Op-Amps	Advantages	Disadvantages
Differential Output in Inverting Configuration	2 per output	Maximum dynamic range. Common mode rejection.	—
Single-Ended Non-Inverting Output with Line Driver	3 per output	Drives headphone/line loads.	3 op-amps required per output.
Single-Ended Non-Inverting Output Configuration	2 per output	Large dynamic range. 2 op-amps required per output.	Increased noise below 200 Hz.
Single-Ended Inverting Output with Reduced BOM	1 per output, plus 1 shared between outputs	Reduced bill of materials (BOM).	Reduced dynamic range. Increased noise below 200 Hz

3.1 Differential Output in Inverting Configuration

Figure 9 shows a differential output buffer using dual op-amps in inverting configuration.

This circuit provides a full-scale output of 2 V_{RMS}. The full-scale output level is configurable using the op-amp feedback resistors (see Section 5 of the device datasheet for further information).

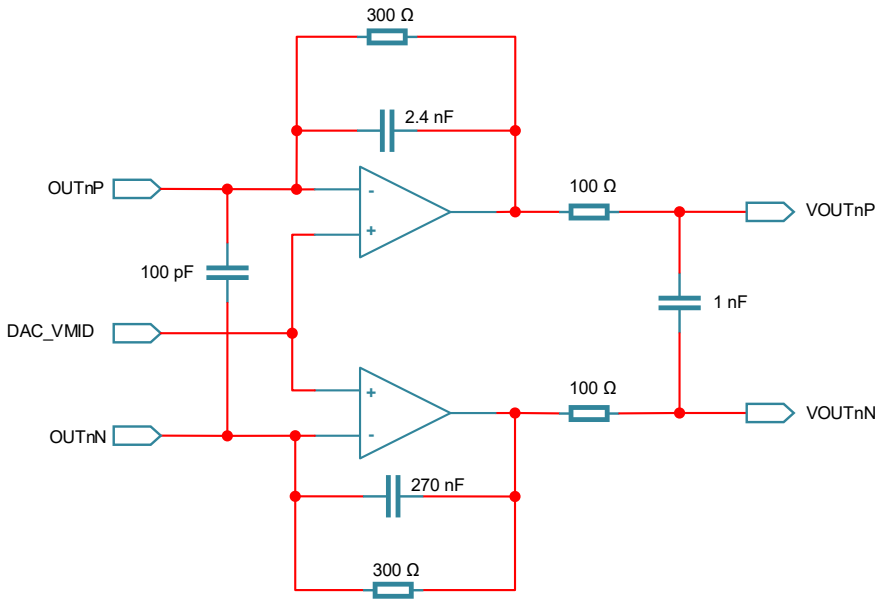

Figure 9 Differential Output in Inverting Configuration

3.2 Single-Ended Non-Inverting Output with Line Driver

Figure 10 shows a single-ended output buffer, comprising a differential inverting I-to-V stage and an inverting line driver.

This circuit provides a full-scale output 2 V_{RMS}. The full-scale output level is configurable using the op-amp feedback resistors in the I-to-V stage (see Section 5 of the device datasheet for further information).

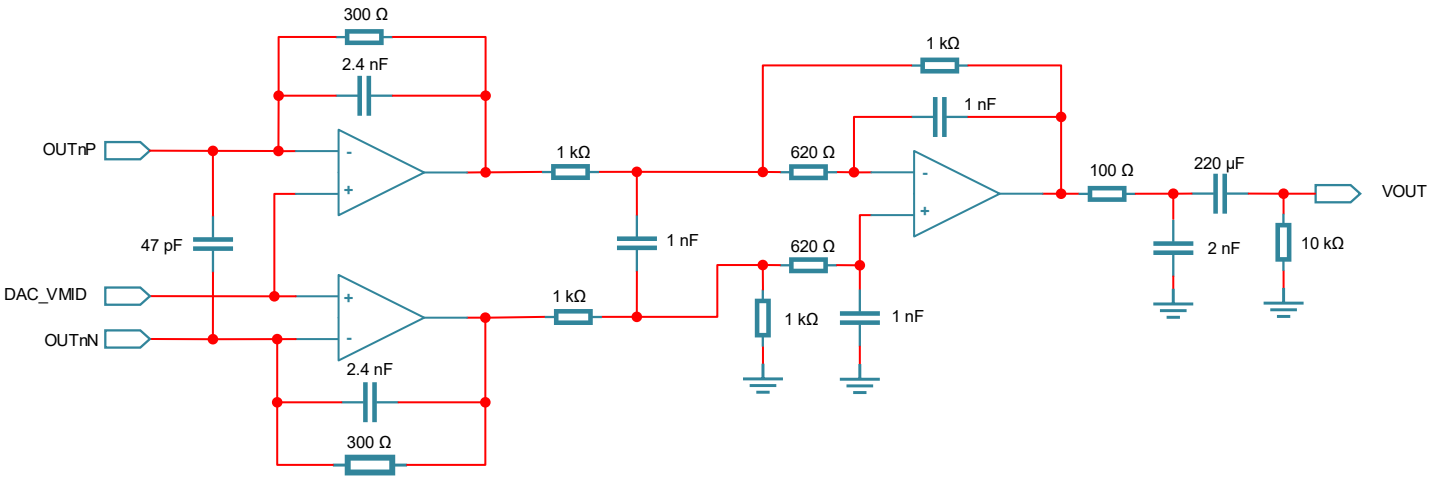

Figure 10 Single-Ended Non-Inverting Output with Line Driver

3.3 Single-Ended Non-Inverting Output Configuration

Figure 11 shows a single-ended output buffer using two op-amps in series.

This circuit provides a full-scale output of 2 V_{RMS}. The full-scale output level is configurable using the op-amp feedback resistors (see Section 5 of the device datasheet for further information).

The THD+N performance is degraded using the configuration shown. The loss of performance can be minimized by adding two 10 µF capacitors between the DAC_VMID path and GND. Note that adding these capacitors also increases the start-up time for the output paths.

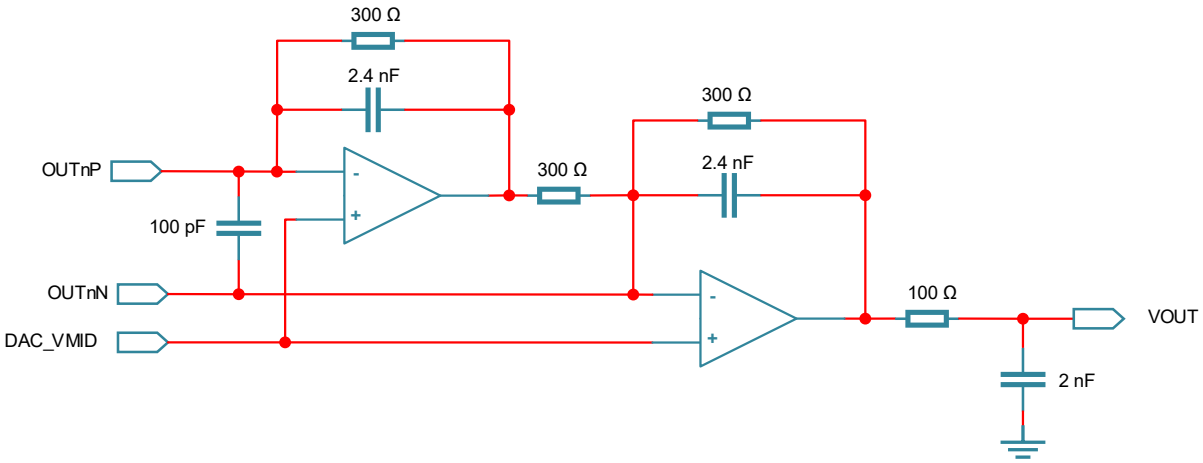

Figure 11 Single-Ended Non-Inverting Output Configuration

3.4 Single-Ended Inverting Output with Reduced BOM

Figure 12 shows a single-ended output buffer with a reduced bill of materials (BOM). One op-amp is required for each OUTnP channel; the additional op-amp driving OUTnN can be shared across multiple channels.

This circuit provides a full-scale output of 2 V_{RMS}. The full-scale output level is configurable using the op-amp feedback resistor (see Section 5 of the device datasheet for further information).

The THD+N performance is degraded using the configuration shown. The loss of performance can be minimized by adding two 10 µF capacitors between the DAC_VMID path and GND. Note that adding these capacitors also increases the start-up time for the output paths.

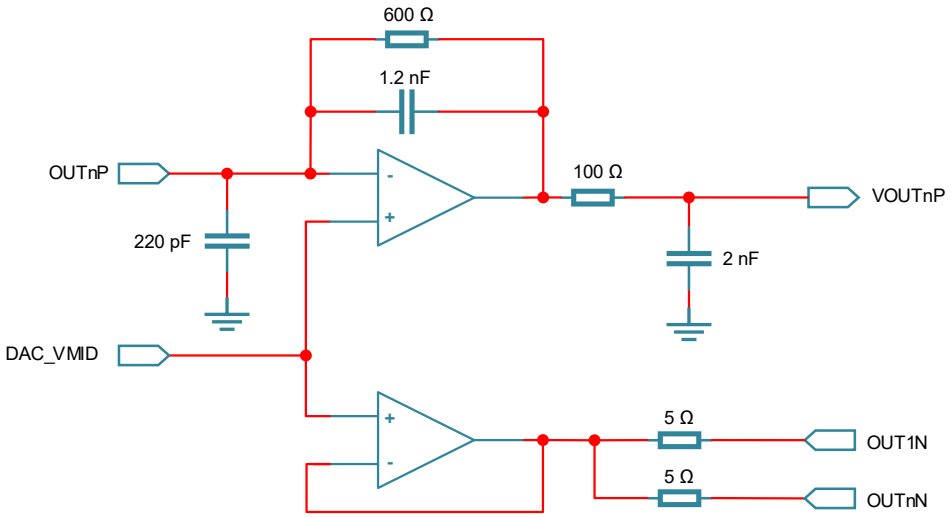

Figure 12 Single-Ended Inverting Output with Reduced BOM

4 Additional Information

4.1 Recommended Components

To achieve the specified performance characteristics, the choice of external components should observe the following recommendations:

- Capacitors should be stable dielectric types, such as C0G (NP0) or electrolytic.
- Resistors should be low value where possible, to minimize thermal noise.
- Low-noise op-amps should be used, such as Texas Instruments OPA1612 or OPA1656. The op-amps should meet the minimum performance requirements noted in Table 4.

Table 4 Op-Amp Specification

Parameter	Specification
Input noise	5 nV/√Hz
Unity gain bandwidth	15 MHz
Slew rate	5 V/µs
Total harmonic distortion + noise (THD+N)	–128 dB

4.2 Switching Frequency

The CS430xx family of high-performance DAC devices operate at a switching frequency of 49.152 MHz.

5 Revision History

Revision History

Revision	Changes
R1 AUG 2025	• Initial version

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.