AN0635

CS5304P/8P DNR Improvements and ADC Input Channel Summing

Introduction

The CS5304P/8P high-performance ADC devices support an input channel summing mode. In this mode, the ADC signal paths are combined into groups of two, four, or eight channels. (Eight channels only supported on CS5308P.) This can be used to achieve enhanced dynamic-range performance on the respective paths.

This document describes the register settings and the recommended external components to achieve improved performance when combining the input channels, while using a single input buffer/filter circuit to drive each combined input signal path.

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1 Input Buffer/Filter Noise

The dynamic range (DNR) specification in the CS5304P/8P datasheet is measured without an input buffer/filter. The recommended input buffer/filter circuit is designed to provide the best combination of THD+N and DNR performance. The DNR of the input buffer/filter circuit is limited by the op-amp noise and the thermal noise of the resistors R1 and R2, shown in Figure 1. Reducing the value of R1 and R2 will reduce their thermal noise contribution and improve the overall DNR performance. However, this is at the expense of increased THD+N.

1.1 Op-amp Buffer/Filter Input

The DC5304P/8P customer boards use the recommended input buffer/filter shown in the datasheet, with a OPA1656 op-amp as shown in Figure 1.

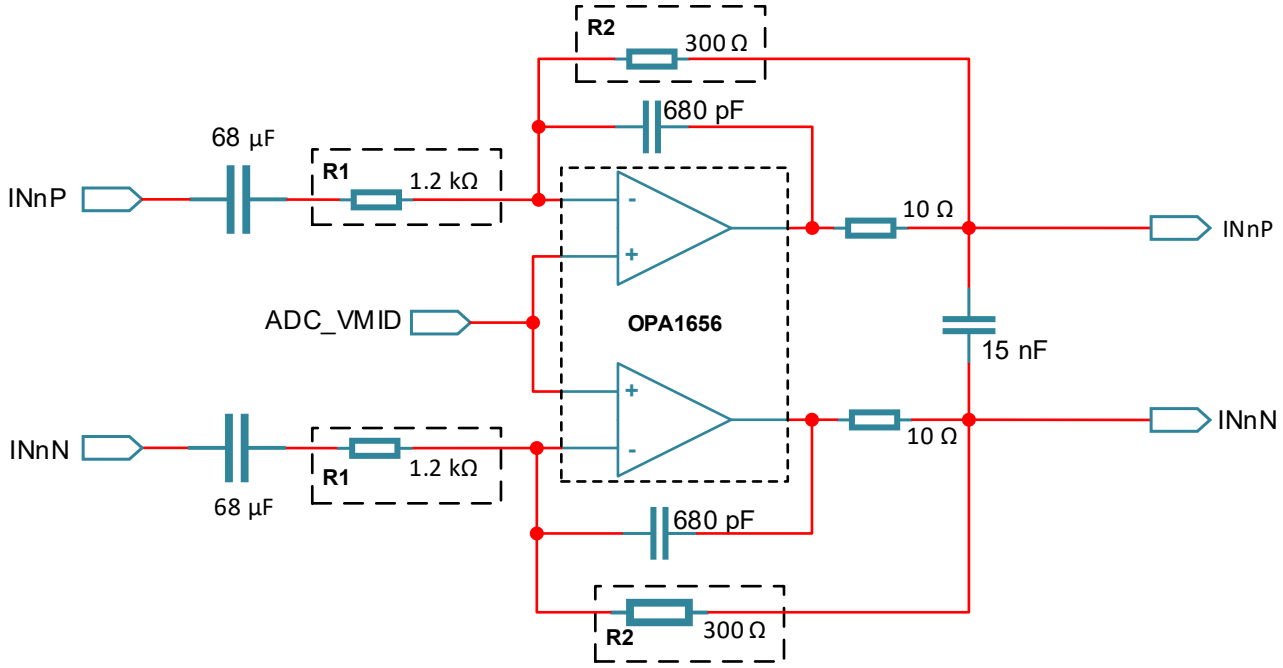

Figure 1: Customer Board Input Buffer/Filter Circuit

1.2 Improved DNR Op-amp Buffer/Filter Input

The DNR performance of the DC5304P/8P customer board can be improved by using a lower noise OPA1612 op-amp and reducing the R1/R2 resistor values, as shown in Figure 2.

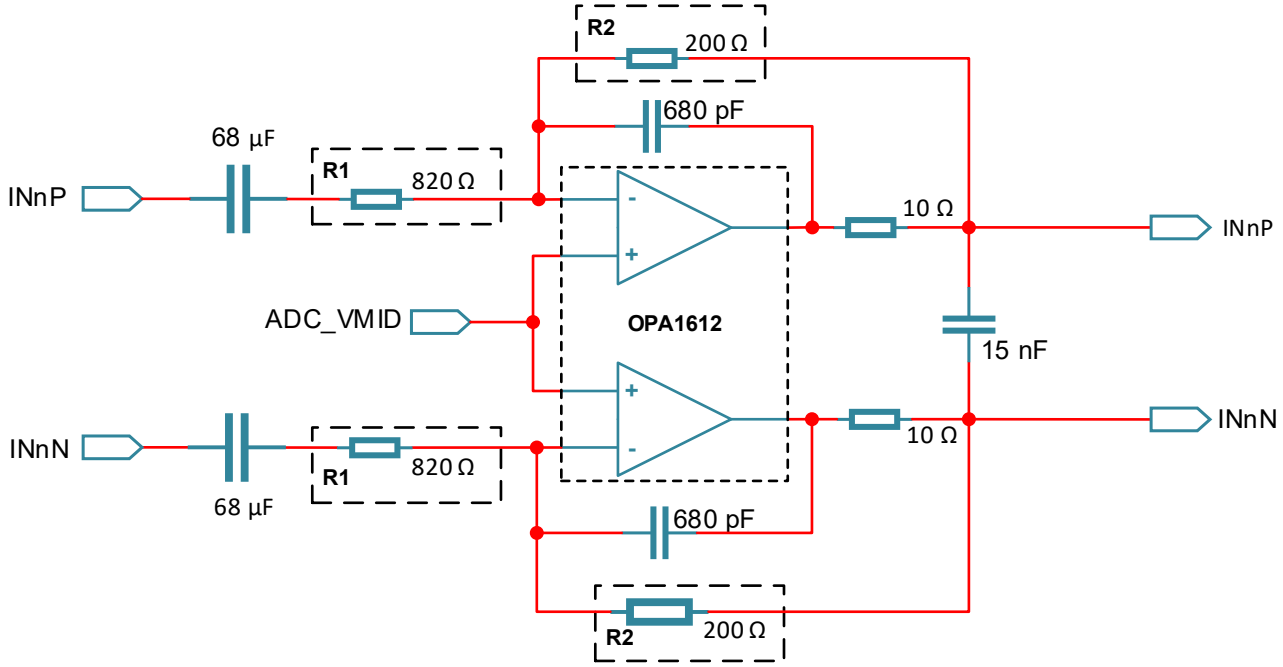

Figure 2: Improved DNR Input Buffer/Filter Circuit

1.3 Electrical Performance

Key noise specifications for op-amps OPA1656 and OPA1612 are shown in Table 1.

Table 1. Comparison of Op-Amp Noise Specifications

OP-AMP	Input Voltage Noise density f = 1kHz	Gain-bandwidth product G = 100
OPA1656	4.3 nV/√Hz	53 MHz
OPA1612	1.1 nV/√Hz	80 MHz

Key performance measurements for the DC5304P/8P with the recommended and improved DNR input buffer/filter circuit are shown in Table 2.

Table 2. Op-amp Buffer/Filter Input Performance Measurements

Measurement	DC5304P/8P Default Input Buffer/Filter Circuit	Improved DNR Input Buffer/Filter Circuit
Signal to Noise Ratio	118 dB	120 dB
THD +N Ratio at –1dBFS	–113 dB	–112 dB
Dynamic Range A-weighted	121 dB	123 dB

2 ADC Input Channel Summing

The CS5304P/8P supports the option to combine the ADC signal paths in groups of two, four or eight (CS5308P only) channels; this can be used to achieve enhanced dynamic-range performance on the respective paths. The respective analog input connections must be linked together externally to provide the same input to each of the respective ADC channels corresponding to the setting of the IN_SUM_MODE field. The typical input connections for two, four, and eight ADC input summing mode are shown in the following sections.

The ADC input summing is configured using IN_SUM_MODE register field. The input impedance will decrease with each additional input that is summed. A summary of the supported options, along with the corresponding Mid-Z and Hi-Z impedance and IN_SUM_MODE register value, is shown in Table 3.

Note: The IN_SUM_MODE field should not be changed while GLOBAL_EN is set. The GLOBAL_EN bit should always be cleared before writing to IN_SUM_MODE.

Table 3. Summing Mode Summary

Configuration	Description	Input Summing Configuration	Mid Z Impedance	Hi Z Impedance	IN_SUM_MODE setting
Default	8-channel output	ADC1-ADC8 as individual ADCs	3 kΩ	100 kΩ	0x0
ADCs combined in groups of two	4-channel output	ADC1+ADC2 ADC3+ADC4 ADC5+ADC6 ADC7+ADC8	1.5 kΩ	50 kΩ	0x1
ADCs combined in groups of four	2-channel output	ADC1+ADC2+ADC3+ADC4 ADC5+ADC6+ADC7+ADC8	750 Ω	25 kΩ	0x2
ADCs combined in groups of eight	1-channel output	ADC1+ADC2+ADC3+ADC4+ADC5+ADC6+ADC7+ADC8	375 Ω	12.5 kΩ	0x3

The combined ADC paths are configured using the control registers associated with the lowest-numbered ADC in the group. For example, the ADC3+ADC4 group is configured using the IN3/ADC3 control registers.

The channel summing mode performance specifications quoted in this document are measured using the improved buffer/filter circuit shown in Figure 2.

2.1 ADCs Combined in Groups of 2

For ADCs combined in groups of 2, (IN_SUM_MODE = 0x1) the ADCs inputs must be combined into groups of 2.

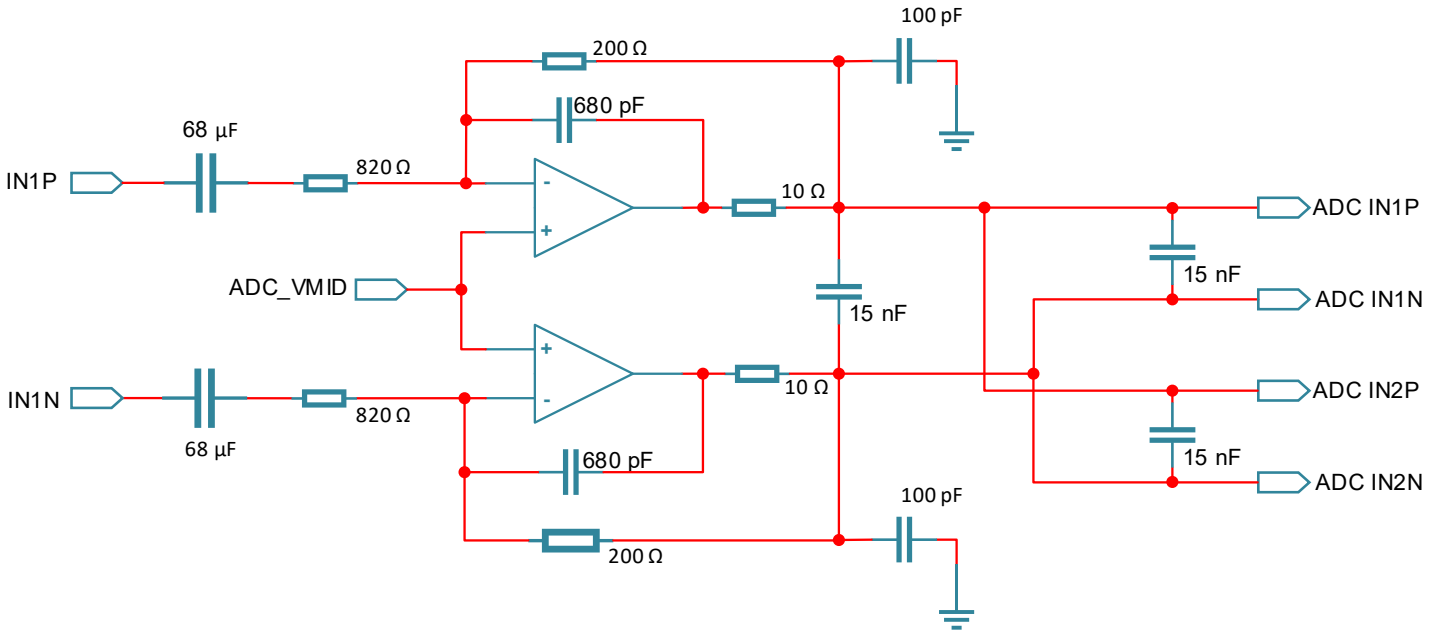

Figure 3: ADCs Combined in Groups of 2 Input Buffer/Filter Circuit

Key performance measurements for this configuration are shown in Table 4.

Table 4: ADCs Combined in Groups of 2 Performance Measurements

Measurement	No Summing	ADCs Combined in Groups of 2
Signal to Noise Ratio	120 dB	122 dB
THD +N Ratio at –1dBFS	–112 dB	–112 dB
Dynamic Range A-weighted	123 dB	125 dB

2.2 ADCs Combined in Groups of 4

For ADCs combined in groups of 4, (IN_SUM_MODE = 0x2) the ADCs inputs must be combined into groups of 4.

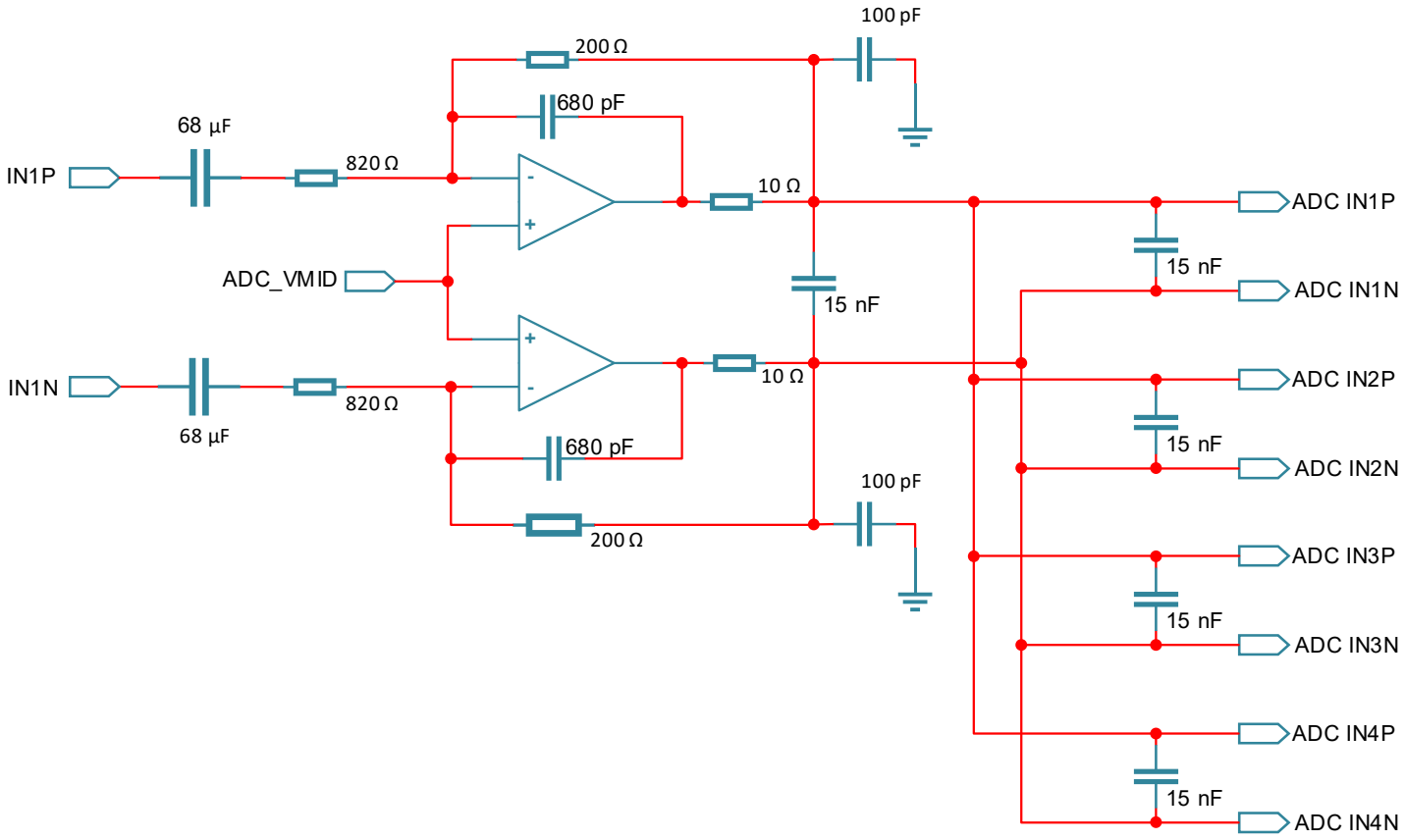

Figure 4: ADCs Combined in Groups of 4 Input Buffer/Filter Circuit

Key performance measurements for this configuration are shown in Table 5

Table 5: ADCs Combined in Groups of 4 Performance Measurements

Measurement	No Summing	ADCs Combined in Groups of 4
Signal to Noise Ratio	120 dB	125 dB
THD +N Ratio at –1dBFS	–112 dB	–112 dB
Dynamic Range A-weighted	123 dB	128 dB

2.3 ADCs Combined in a Group of 8

For ADCs combined in groups of 8, (IN_SUM_MODE = 0x3) the ADCs inputs must be combined into a group of 8. This ADC input channel summing mode is only available on the CS5308P.

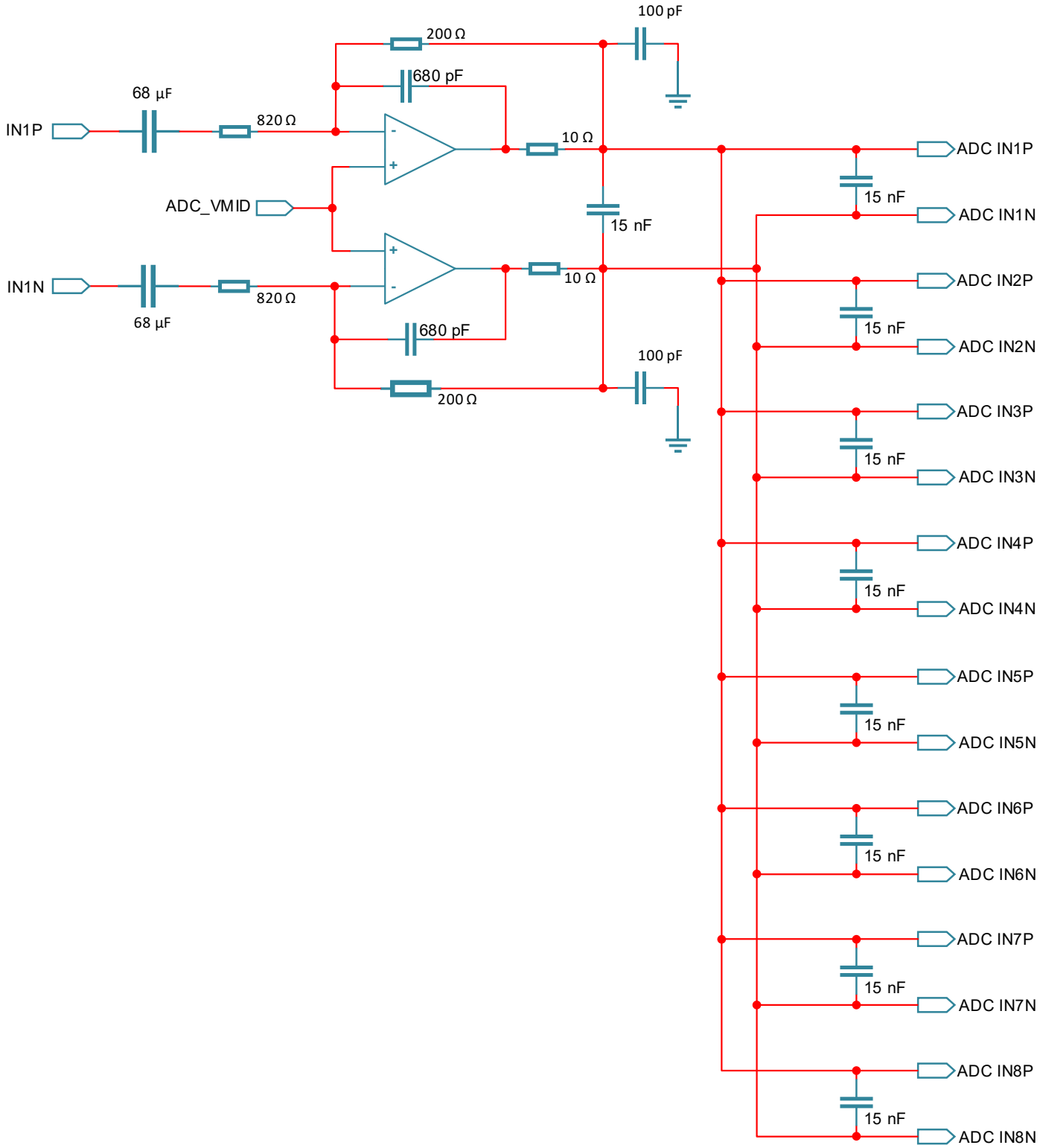

Figure 5: ADCs Combined in a Group of 8 Input Buffer/Filter Circuit

Key performance measurements for this configuration are shown in Table 6.

Table 6: ADCs Combined in a Group of 8 Performance Measurements

Measurement	No Summing	ADCs Combined in a Group of 8
Signal to Noise Ratio	120 dB	127 dB
THD +N Ratio at –1dBFS	–112 dB	–112 dB
Dynamic Range A-weighted	123 dB	130 dB

3 Revision History

Revision History

Revision	Changes
R1 MAY 2024	• Initial Release
R2 JAN 2025	• Updated typical connection diagrams and performance tables.
R3 JUL 2025	• Updated Table 3 with Mid-Z and Hi-Z impedance levels for each channel summing mode. • Fixed incorrect resistor value in Figure 2, 3, 4, and 5. • Amended input capacitor value in Figure 1, 2, 3, 4, and 5.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
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