CS530x Input Buffer/Filter Circuits

Introduction

The CS530xx family of high-performance ADC devices require external input buffer/filter circuits to bias the input signal to the ADC. This document describes the recommended external buffer/filter circuits.

Designing and implementing an external buffer circuit should take account of the following considerations: noise contribution from resistors, input biasing, isolation from switched-capacitor currents, maintaining a low impedance so as not to cause distortion, and providing anti-alias filtering.

Different buffer/filter solutions are described and compared in this document.

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1 Input Buffer Circuits – CS5304P/4S/8P/8S and CS53A04P/8P

This section describes differential and single-ended input-buffer/filter circuits for the CS5304P/4S/8P/8S and CS53A04P/8P high-performance ADC devices. Six options are described, as summarized in Table 1.

Table 1 Input Buffer/Filter Circuits Summary

Description	Op-Amps	Advantages	Disadvantages
Differential Input in Inverting Configuration	2 per input	Maximum dynamic range. Common mode rejection. Supports input higher than 2 V_{RMS}	Inverting input stage.
Differential Input in Non-Inverting Configuration	2 per input	Maximum dynamic range. Common mode rejection.	2 V_{RMS} maximum input. Higher noise. Requires buffered ADC_VMID.
Single-Ended to Differential Input with Parallel Op-Amps	2 per input	Maximum dynamic range.	1 V_{RMS} maximum input. Requires buffered ADC_VMID.
Single-Ended to Differential Input with Inverter and Parallel Op-Amps	3 per input	Maximum dynamic range. Supports input higher than 1 $V_{RMS.}$	3 op-amps required per input. Signal-alignment mismatch INnP/N. Noise mismatch between INnP/N.
Single-Ended Input with Single Op-Amp	1 per input	1 op-amp per input. Maximum dynamic range. Supports input higher than 1 $V_{RMS.}$	Requires external VMID. Signal-alignment mismatch INnP/N. Noise mismatch between INnP/N.
Single-Ended to Pseudo-Differential Input	2 per input	Reduced noise. Supports input higher than 1 $V_{RMS.}$	Reduced dynamic range.

1.1 Differential Input in Inverting Configuration

Figure 1 shows a differential input-buffer configuration using dual op-amps in inverting configuration. This circuit supports maximum input of 8 V_{RMS}; the signal gain of –12 dB results in a maximum input voltage of 2 V_{RMS} at the ADC inputs. The attenuation of –12 dB reduces the noise floor at the output of the buffer/filter circuit.

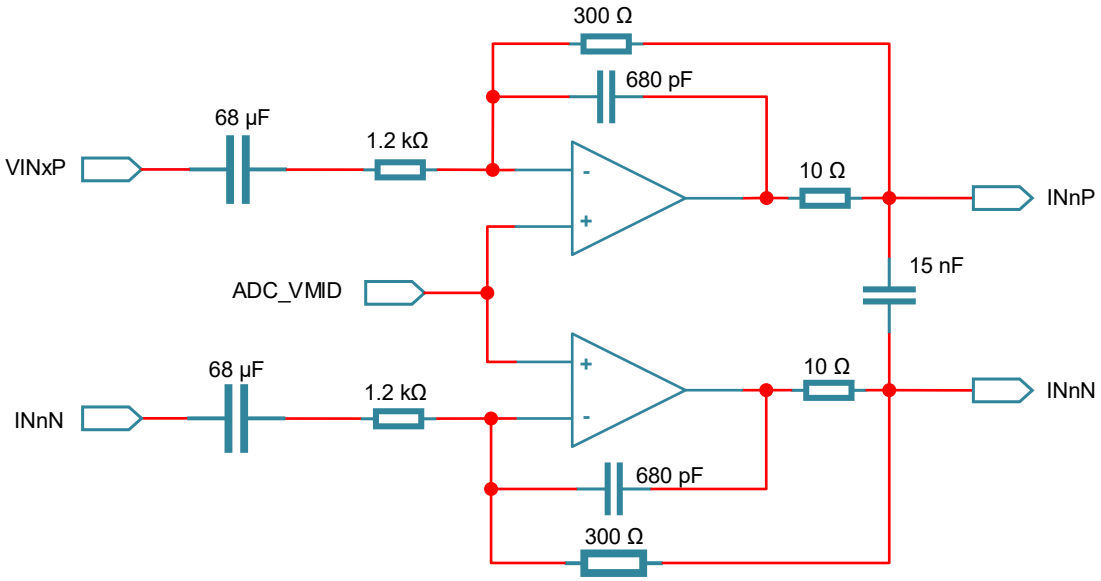

Figure 1 Differential Input in Inverting Configuration

The input components (68 µF capacitor and 1.2 kΩ resistor) provide a first-order high-pass filter (HPF); the op-amp and associated components provide a second-order low-pass filter (LPF). The respective filter characteristics are shown in Table 2. For further information on these filters, see Section 5 of the device datasheet.

Table 2 Input Buffer Filter Characteristics

Parameter	Components	Frequency
HPF –3 dB cut-off frequency	R = 1.2 kΩ, C = 68 µF	1.95 Hz
LPF cut-off frequency	R = 300 Ω, 10 Ω, C = 680 pF, 15 nF	640 kHz

The maximum input level is configurable using the ratio of the input resistor and feedback resistor connected to the op-amp. In Figure 1, the ratio of four (1.2 kΩ / 300 Ω) supports a full-scale input of 8 V_{RMS}, i.e., four times the maximum ADC input level.

1.2 Differential Input in Non-Inverting Configuration

Figure 2 shows a differential input-buffer configuration using dual op-amps in a non-inverting configuration. This circuit supports a maximum input of 2 V_{RMS} with a unity signal gain.

Note that a buffered ADC_VMID reference is required in this circuit.

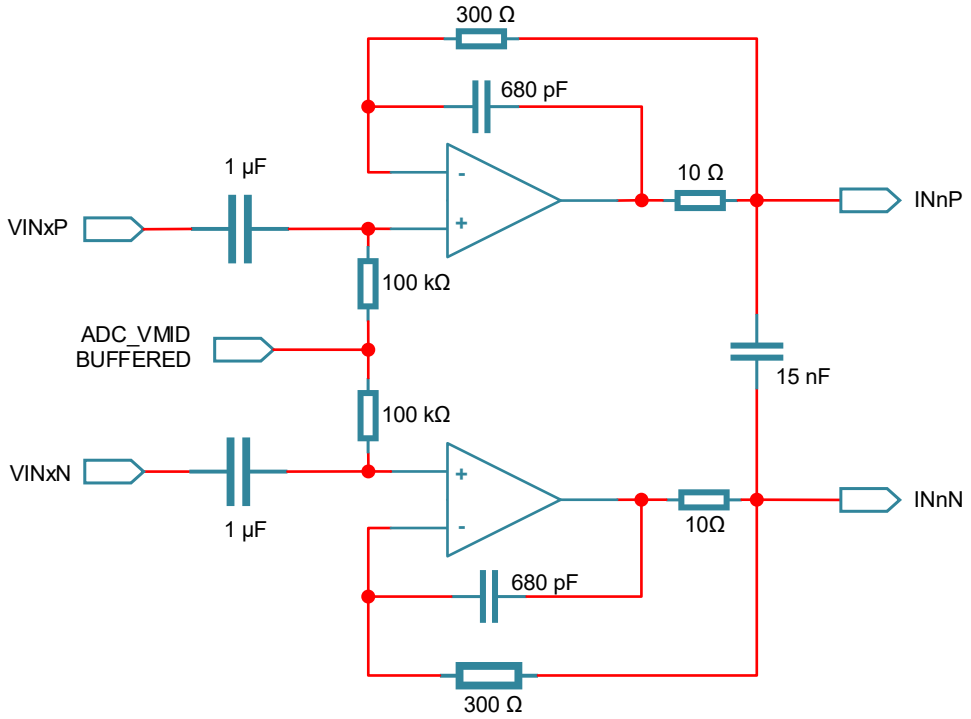

Figure 2 Differential Input in Non-Inverting Configuration

The input components (1 µF capacitor and 100 kΩ resistor) provide a first-order high-pass filter (HPF); the op-amp and associated components provide a second-order low-pass filter (LPF). The respective filter characteristics are shown in Table 3. For further information on these filters, see Section 5 of the device datasheet.

Table 3 Input Buffer Filter Characteristics

Parameter	Components	Frequency
HPF –3 dB cut-off frequency	R = 100 kΩ, C = 1 µF	1.59 Hz
LPF cut-off frequency	R = 300 Ω, 10 Ω, C = 680 pF, 15 nF	640 kHz

1.3 Single-Ended to Differential Input with Parallel Op-Amps

Figure 3 shows a single-ended to differential input-buffer configuration using dual op-amps in parallel. This circuit supports a maximum input of 1 V_{RMS}; the signal gain of 6 dB results in a maximum input voltage of 2 V_{RMS} at the ADC inputs.

Note that a buffered ADC_VMID reference is required in this circuit.

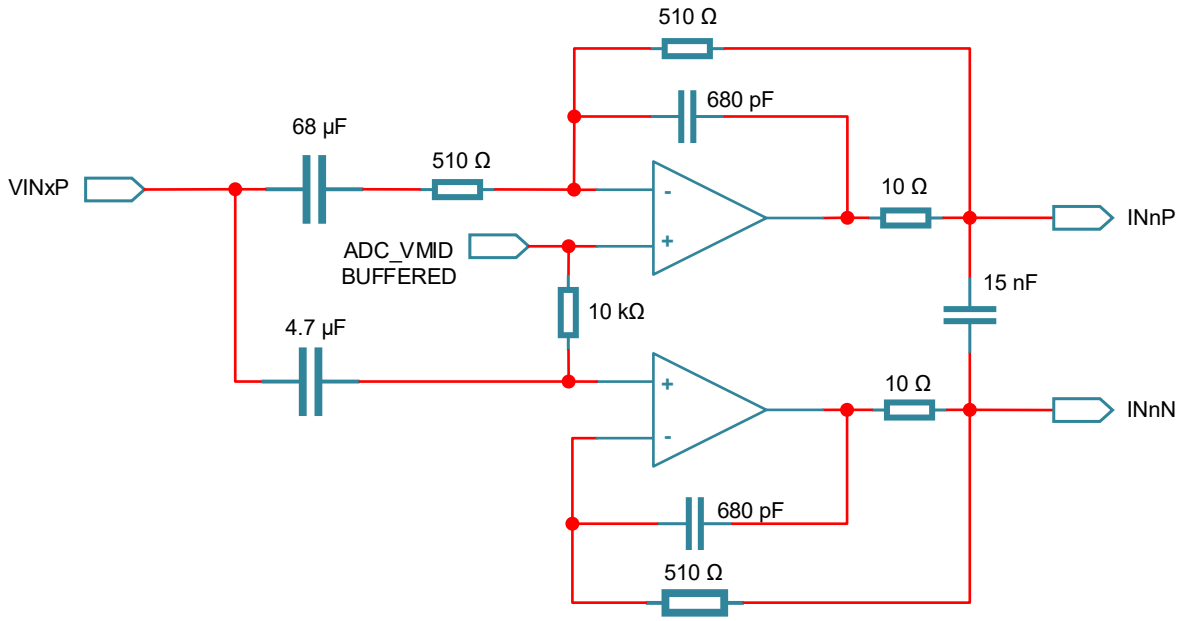

Figure 3 Single-Ended to Differential Input with Parallel Op-Amps

The input components (e.g., 68 µF capacitor and 510 Ω resistor) provide a first-order high-pass filter (HPF); the op-amp and associated components provide a second-order low-pass filter (LPF). The respective filter characteristics are shown in Table 4. For further information on these filters, see Section 5 of the device datasheet.

Table 4 Input Buffer Filter Characteristics

Parameter	Components	Frequency
HPF –3 dB cut-off frequency (INnP)	R = 510 Ω, C = 68 µF	4.59 Hz
HPF –3 dB cut-off frequency (INnN)	R = 10 kΩ, C = 4.7 µF	3.39 Hz
LPF cut-off frequency	R = 510 Ω, 10 Ω, C = 680 pF, 15 nF	490 kHz

1.4 Single-Ended to Differential Input with Inverter and Parallel Op-Amps

Figure 4 shows a single-ended to differential input-buffer configuration using an inverting op-amp to produce the inverted input signal. This circuit supports maximum input of 4 V_{RMS}; the signal gain of –12 dB results in a maximum input voltage of 2 V_{RMS} at the ADC inputs.

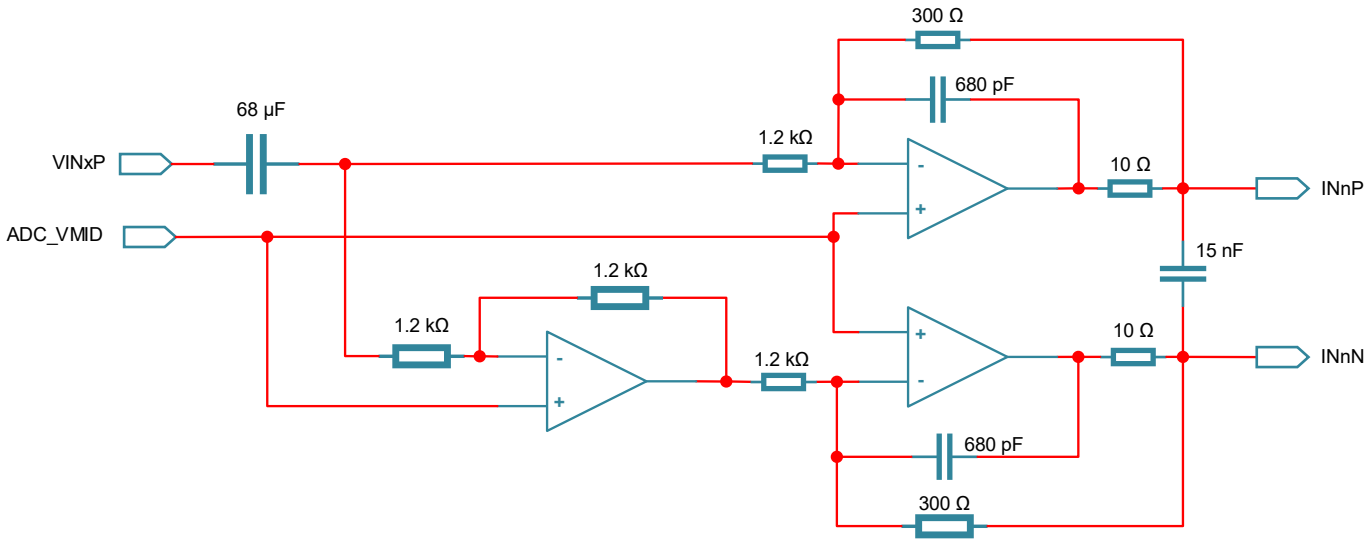

Figure 4 Single-Ended to Differential Input with Inverter and Parallel Op-Amps

The input components (68 µF capacitor and 1.2 kΩ resistor) provide a first-order high-pass filter (HPF); the op-amp and associated components provide a second-order low-pass filter (LPF). The respective filter characteristics are shown in Table 5. For further information on these filters, see Section 5 of the device datasheet.

Table 5 Input Buffer Filter Characteristics

Parameter	Components	Frequency
HPF –3 dB cut-off frequency	R = 1.2 kΩ, C = 68 µF	1.95 Hz
LPF cut-off frequency	R = 300 Ω, 10 Ω, C = 680 pF, 15 nF	640 kHz

The maximum input level is configurable using the ratio of the input resistor and feedback resistor connected to the op-amp. In Figure 4, the inverting op-amp creates an 8 V_{RMS} differential signal from the 4 V_{RMS} input. The resistor ratio of four (1.2 kΩ / 300 Ω) supports a full-scale 8 V_{RMS} differential signal, i.e., four times the maximum ADC input level.

1.5 Single-Ended Input with Single Op-Amp

Figure 5 shows a single-ended input-buffer configuration using a single op-amp. This circuit supports a maximum input of 4 V_{RMS}; the signal gain of –12 dB results in a maximum input voltage of 1 V_{RMS} at the INnP input.

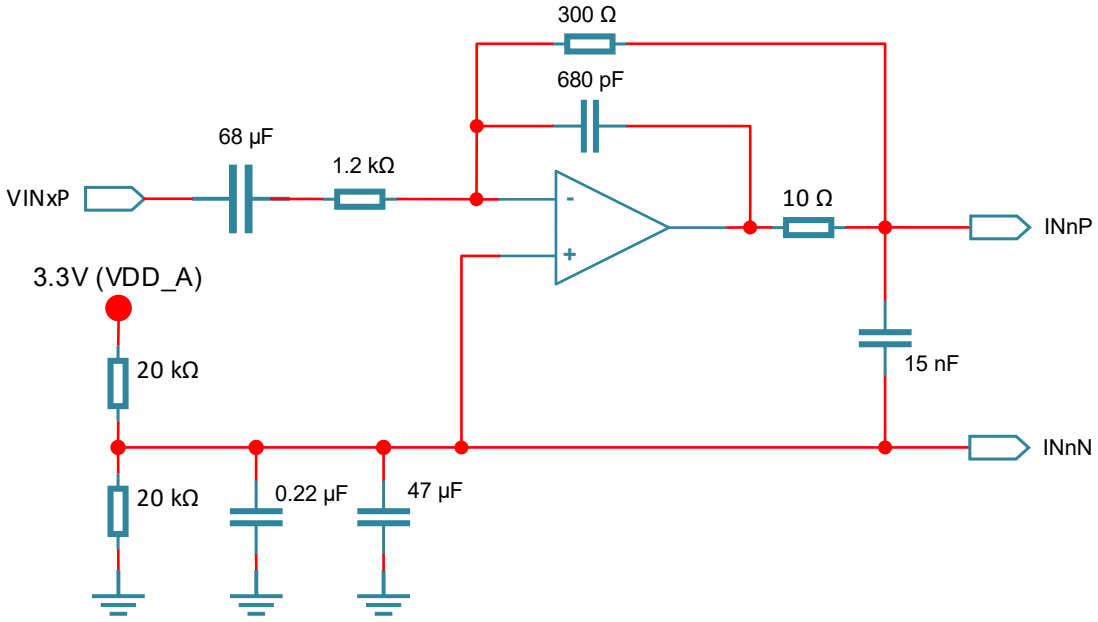

Figure 5 Single-Ended Input with Single Op-Amp

The input components (68 µF capacitor and 1.2 kΩ resistor) provide a first-order high-pass filter (HPF); the op-amp and associated components provide a second-order low-pass filter (LPF). The respective filter characteristics are shown in Table 6. For further information on these filters, see Section 5 of the device datasheet.

Table 6 Input Buffer Filter Characteristics

Parameter	Components	Frequency
HPF –3 dB cut-off frequency	R = 1.2 kΩ, C = 68 µF	1.95 Hz
LPF cut-off frequency	R = 300 Ω, 10 Ω, C = 680 pF, 15 nF	640 kHz

The maximum input level is configurable using the ratio of the input resistor and feedback resistor connected to the op-amp. In Figure 5, the ratio of four (1.2 kΩ / 300 Ω) supports a full-scale input of 4 V_{RMS}, i.e., four times the maximum level at the INnP input.

1.6 Single-Ended to Pseudo-Differential Input

Figure 6 shows a single-ended to pseudo-differential input buffer configuration using dual op-amps in parallel. This circuit supports a maximum input of 4 V_{RMS}; the signal gain of –12 dB results in a maximum input voltage of 1 V_{RMS} at the INnP input. The pseudo-differential configuration reduces noise at the ADC input connection.

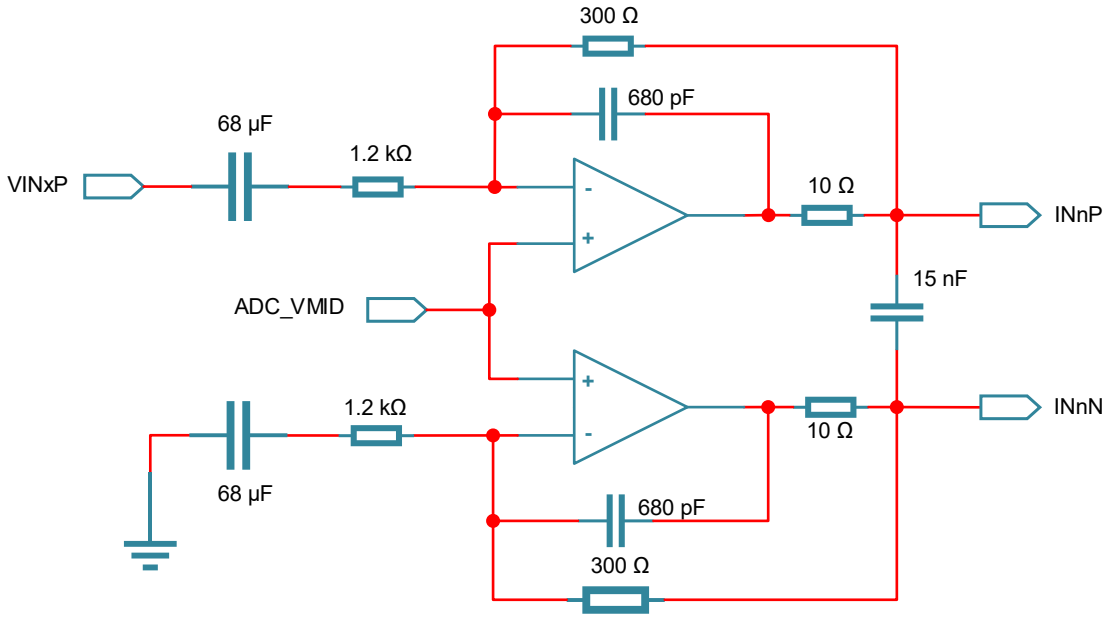

Figure 6 Single-Ended to Pseudo-Differential Input

The input components (68 µF capacitor and 1.2 kΩ resistor) provide a first-order high-pass filter (HPF); the op-amp and associated components provide a second-order low-pass filter (LPF). The respective filter characteristics are shown in Table 7. For further information on these filters, see Section 5 of the device datasheet.

Table 7 Input Buffer Filter Characteristics

Parameter	Components	Frequency
HPF –3 dB cut-off frequency	R = 1.2 kΩ, C = 68 µF	1.95 Hz
LPF cut-off frequency	R = 300 Ω, 10 Ω, C = 680 pF, 15 nF	640 kHz

The maximum input level is configurable using the ratio of the input resistor and feedback resistor connected to the op-amp. In Figure 6, the ratio of four (1.2 kΩ / 300 Ω) supports a full-scale input of 4 V_{RMS}, i.e., four times the maximum level at the INnP input.

2 Input Buffer Circuits – CS5302P

This section describes the differential and single-ended input-buffer/filter circuits for the CS5302P high-performance ADC device. Six options are described, as summarized in Table 8.

Table 8 Input Buffer/Filter Circuits Summary

Description	Op-Amps	Advantages	Disadvantages
Differential Input in Inverting Configuration	2 per input	Maximum dynamic range. Common mode rejection. Supports input higher than 2 V_{RMS}	Inverting input stage.
Differential Input in Non-Inverting Configuration	2 per input	Maximum dynamic range. Common mode rejection.	2 V_{RMS} maximum input. Higher noise. Requires buffered ADC_VMID.
Single-Ended to Differential Input with Parallel Op-Amps	2 per input	Maximum dynamic range.	1 V_{RMS} maximum input. Requires buffered ADC_VMID.
Single-Ended to Differential Input with Inverter and Parallel Op-Amps	3 per input	Maximum dynamic range. Supports input higher than 1 $V_{RMS.}$	3 op-amps required per input. Signal-alignment mismatch INnP/N. Noise mismatch between INnP/N.
Single-Ended Input with Single Op-Amp	1 per input	1 op-amp per input. Maximum dynamic range. Supports input higher than 1 $V_{RMS.}$	Requires external VMID. Signal-alignment mismatch INnP/N. Noise mismatch between INnP/N.
Single-Ended to Psuedo-Differential Input	2 per input	Reduced noise. Supports input higher than 1 $V_{RMS.}$	Reduced dynamic range.

2.1 Differential Input in Inverting Configuration

Figure 7 shows a differential input-buffer configuration using dual op-amps in inverting configuration. This circuit supports maximum input of 8 V_{RMS}; the signal gain of –12 dB results in a maximum input voltage of 2 V_{RMS} at the ADC inputs. The attenuation of –12 dB reduces the noise floor at the output of the buffer/filter circuit.

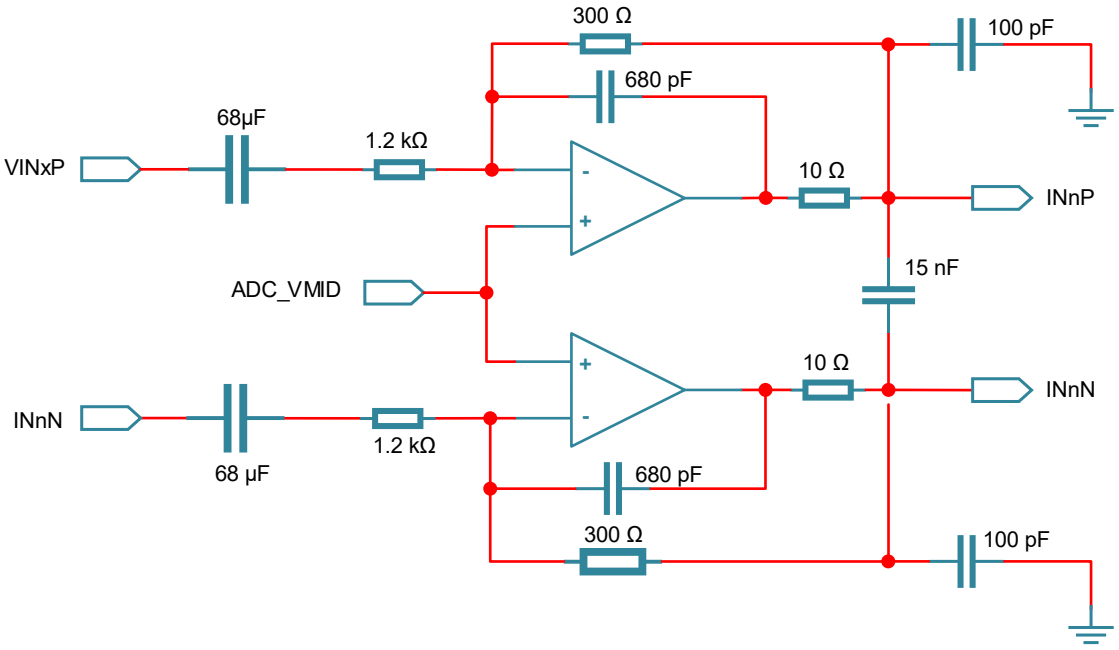

Figure 7 Differential Input in Inverting Configuration

The input components (68 µF capacitor and 1.2 kΩ resistor) provide a first-order high-pass filter (HPF); the op-amp and associated components provide a second-order low-pass filter (LPF). The respective filter characteristics are shown in Table 9. For further information on these filters, see Section 5 of the device datasheet.

Table 9 Input Buffer Filter Characteristics

Parameter	Components	Frequency
HPF –3 dB cut-off frequency	R = 1.2 kΩ, C = 68 µF	1.95 Hz
LPF cut-off frequency	R = 300 Ω, 10 Ω, C = 680 pF, 15 nF	640 kHz

The maximum input level is configurable using the ratio of the input resistor and feedback resistor connected to the op-amp. In Figure 7, the ratio of four (1.2 kΩ / 300 Ω) supports a full-scale input of 8 V_{RMS}, i.e., four times the maximum ADC input level.

2.2 Differential Input in Non-Inverting Configuration

Figure 8 shows a differential input-buffer configuration using dual op-amps in a non-inverting configuration. This circuit supports a maximum input of 2 V_{RMS} with a unity signal gain.

Note that a buffered ADC_VMID reference is required in this circuit.

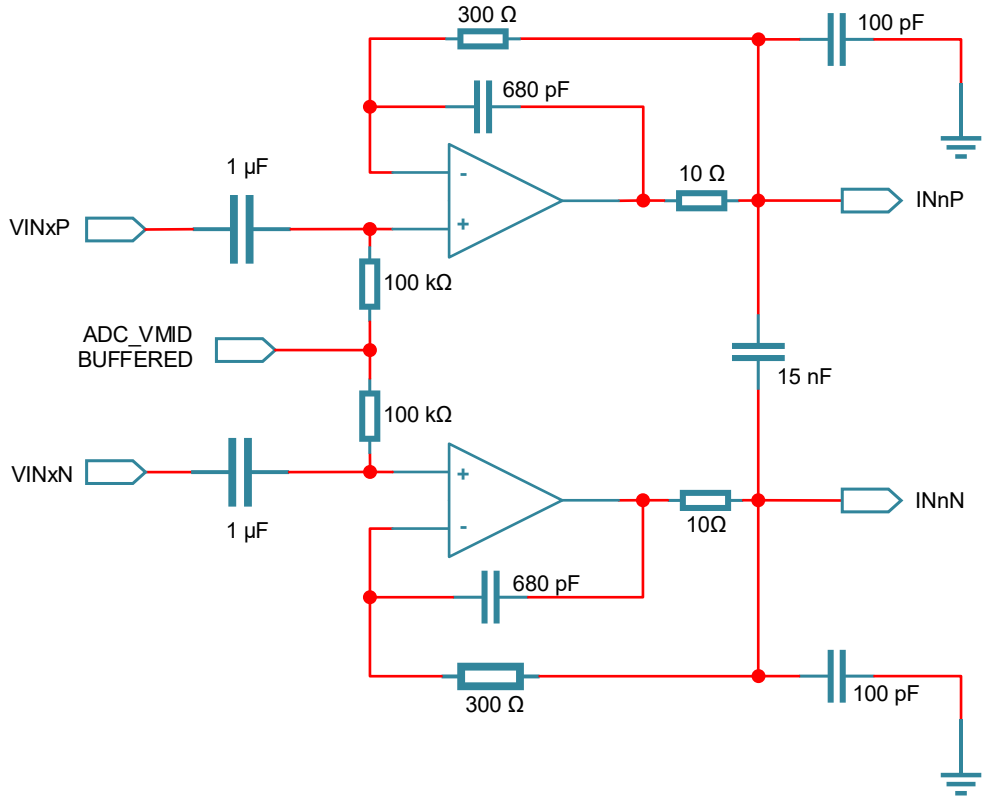

Figure 8 Differential Input in Non-Inverting Configuration

The input components (1 µF capacitor and 100 kΩ resistor) provide a first-order high-pass filter (HPF); the op-amp and associated components provide a second-order low-pass filter (LPF). The respective filter characteristics are shown in Table 10. For further information on these filters, see Section 5 of the device datasheet.

Table 10 Input Buffer Filter Characteristics

Parameter	Components	Frequency
HPF –3 dB cut-off frequency	R = 100 kΩ, C = 1 µF	1.59 Hz
LPF cut-off frequency	R = 300 Ω, 10 Ω, C = 680 pF, 15 nF	640 kHz

2.3 Single-Ended to Differential Input with Parallel Op-Amps

Figure 9 shows a single-ended to differential input-buffer configuration using dual op-amps in parallel. This circuit supports a maximum input of 1 V_{RMS}; the signal gain of 6 dB results in a maximum input voltage of 2 V_{RMS} at the ADC inputs.

Note that a buffered ADC_VMID reference is required in this circuit.

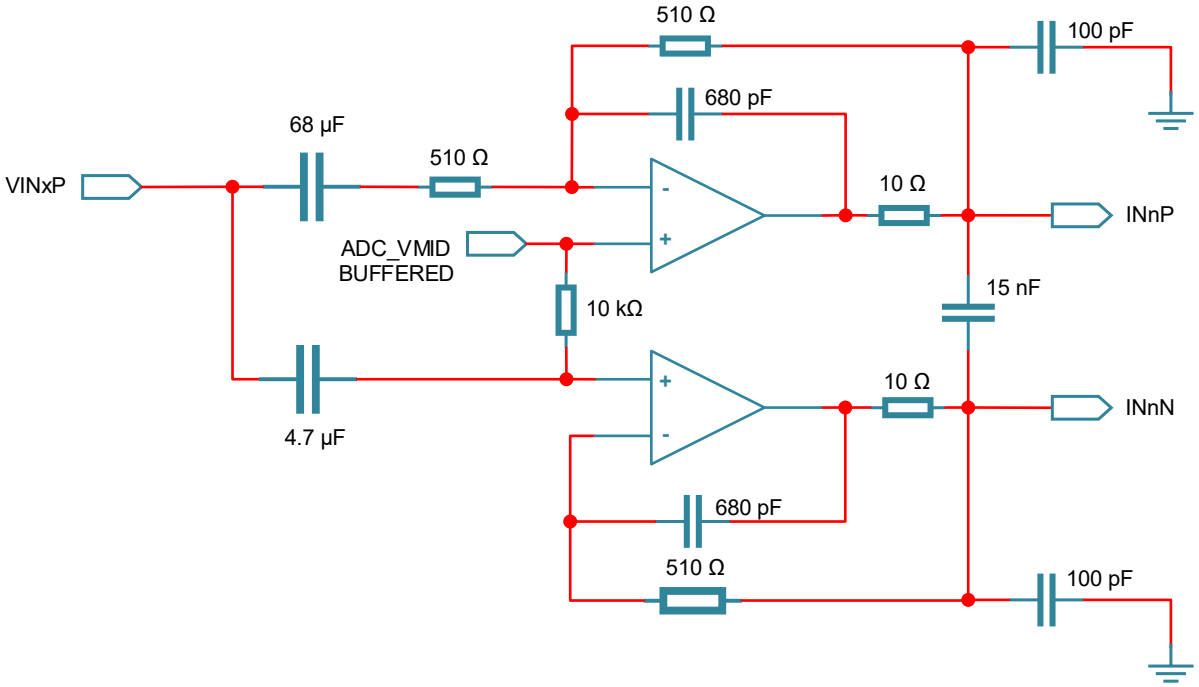

Figure 9 Single-Ended to Differential Input with Parallel Op-Amps

The input components (e.g., 68 µF capacitor and 510 Ω resistor) provide a first-order high-pass filter (HPF); the op-amp and associated components provide a second-order low-pass filter (LPF). The respective filter characteristics are shown in Table 11. For further information on these filters, see Section 5 of the device datasheet.

Table 11 Input Buffer Filter Characteristics

Parameter	Components	Frequency
HPF –3 dB cut-off frequency (INnP)	R = 510 Ω, C = 68 µF	4.59 Hz
HPF –3 dB cut-off frequency (INnN)	R = 10 kΩ, C = 4.7 µF	3.39 Hz
LPF cut-off frequency	R = 510 Ω, 10 Ω, C = 680 pF, 15 nF	490 kHz

2.4 Single-Ended to Differential Input with Inverter and Parallel Op-Amps

Figure 10 shows a single-ended to differential input-buffer configuration using an inverting op-amp to produce the inverted input signal. This circuit supports maximum input of 4 V_{RMS}; the signal gain of –6 dB results in a maximum input voltage of 2 V_{RMS} at the ADC inputs.

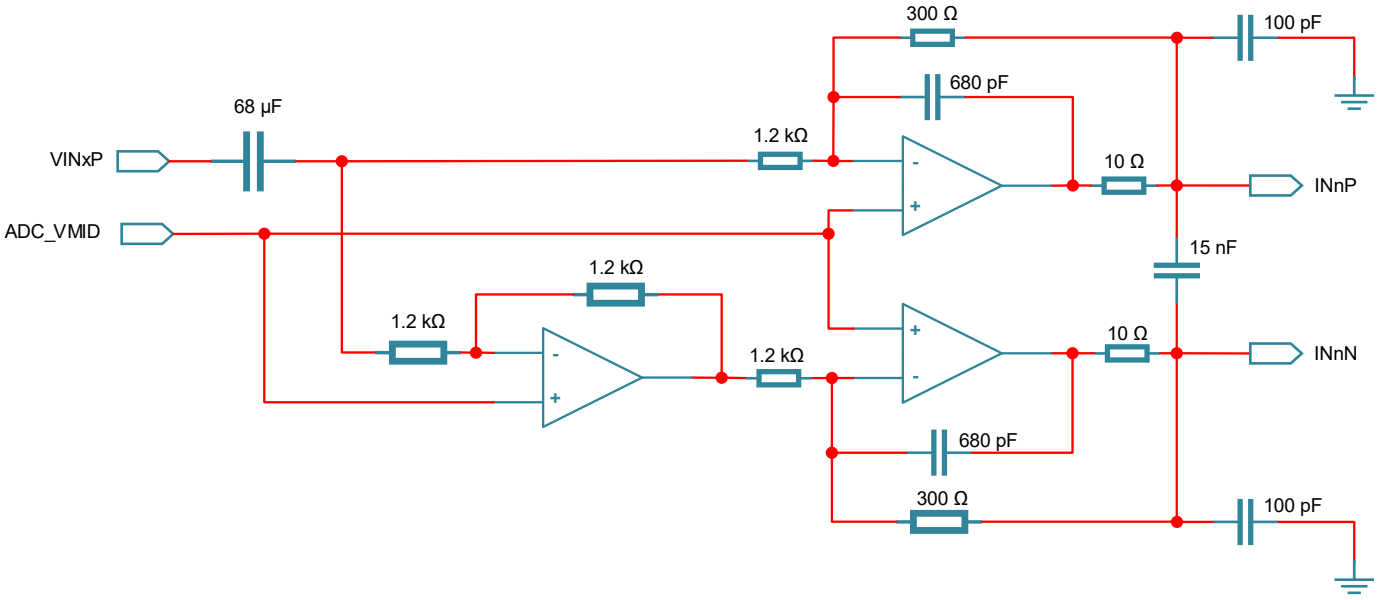

Figure 10 Single Ended to Differential Input with Inverter and Parallel Op-Amps

The input components (68 µF capacitor and 1.2 kΩ resistor) provide a first-order high-pass filter (HPF); the op-amp and associated components provide a second-order low-pass filter (LPF). The respective filter characteristics are shown in Table 12. For further information on these filters, see Section 5 of the device datasheet.

Table 12 Input Buffer Filter Characteristics

Parameter	Components	Frequency
HPF –3 dB cut-off frequency	R = 1.2 kΩ, C = 68 µF	1.95 Hz
LPF cut-off frequency	R = 300 Ω, 10 Ω, C = 680 pF, 15 nF	640 kHz

The maximum input level is configurable using the ratio of the input resistor and feedback resistor connected to the op-amp. In Figure 10, the inverting op-amp creates an 8 V_{RMS} differential signal from the 4 V_{RMS} input. The resistor ratio of four (1.2 kΩ / 300 Ω) supports a full-scale 8 V_{RMS} differential signal, i.e., four times the maximum ADC input level.

2.5 Single-Ended Input with a Single Op-Amp

Figure 11 shows a single-ended input-buffer configuration using a single op-amp. This circuit supports a maximum input of 4 V_{RMS}; the signal gain of –12 dB results in a maximum input voltage of 1 V_{RMS} at the INnP input.

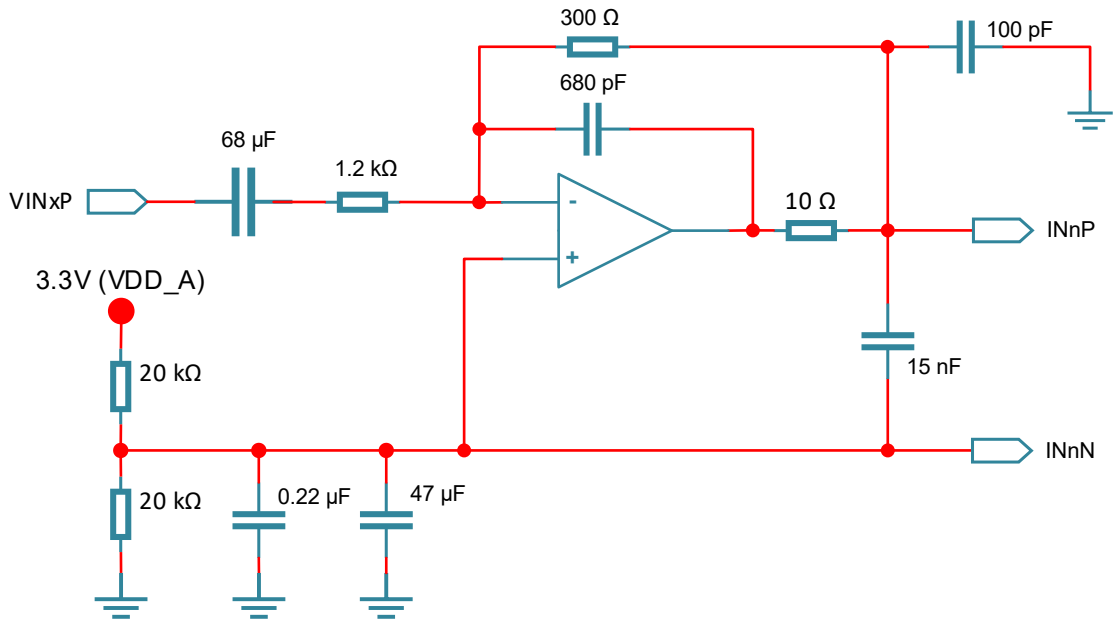

Figure 11 Single-Ended Input with Single Op-Amp

The input components (68 µF capacitor and 1.2 kΩ resistor) provide a first-order high-pass filter (HPF); the op-amp and associated components provide a second-order low-pass filter (LPF). The respective filter characteristics are shown in Table 13. For further information on these filters, see Section 5 of the device datasheet.

Table 13 Input Buffer Filter Characteristics

Parameter	Components	Frequency
HPF –3 dB cut-off frequency	R = 1.2 kΩ, C = 68 µF	1.95 Hz
LPF cut-off frequency	R = 300 Ω, 10 Ω, C = 680 pF, 15 nF	640 kHz

The maximum input level is configurable using the ratio of the input resistor and feedback resistor connected to the op-amp. In Figure 11, the ratio of four (1.2 kΩ / 300 Ω) supports a full-scale input of 4 V_{RMS}, i.e., four times the maximum level at the INnP input.

2.6 Single-Ended to Pseudo-Differential Input

Figure 12 shows a single-ended to pseudo-differential input buffer configuration using dual op-amps in parallel. This circuit supports a maximum input of 4 V_{RMS}; the signal gain of –12 dB results in a maximum input voltage of 1 V_{RMS} at the INnP input. The pseudo-differential configuration reduces noise at the ADC input connection.

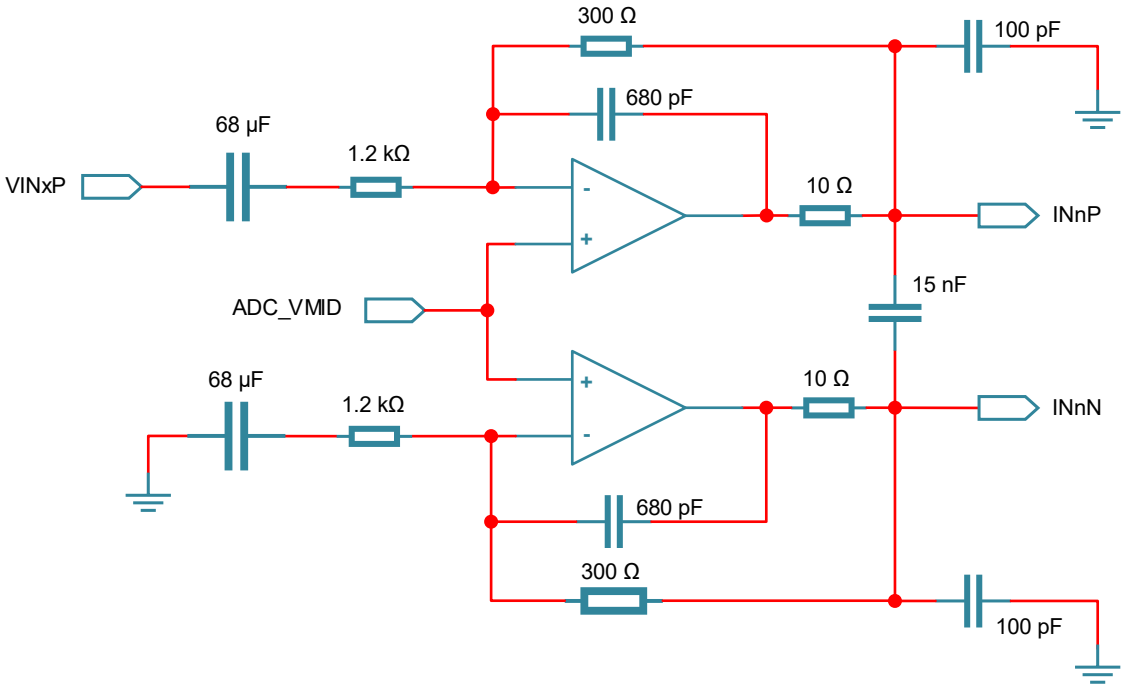

Figure 12 Single Ended to Psuedo-Differential Input

The input components (68 µF capacitor and 1.2 kΩ resistor) provide a first-order high-pass filter (HPF); the op-amp and associated components provide a second-order low-pass filter (LPF). The respective filter characteristics are shown in Table 14. For further information on these filters, see Section 5 of the device datasheet.

Table 14 Input Buffer Filter Characteristics

Parameter	Components	Frequency
HPF –3 dB cut-off frequency	R = 1.2 kΩ, C = 68 µF	1.95 Hz
LPF cut-off frequency	R = 300 Ω, 10 Ω, C = 680 pF, 15 nF	640 kHz

The maximum input level is configurable using the ratio of the input resistor and feedback resistor connected to the op-amp. In Figure 12, the ratio of four (1.2 kΩ / 300 Ω) supports a full-scale input of 4 V_{RMS}, i.e., four times the maximum level at the INnP input.

3 Passive Input Buffer Circuit

This section describes the passive differential input-buffer/filter circuit for the CS530x high-performance ADC devices. The characteristics are summarized in Table 15.

Table 15 Passive Input Buffer Summary

Description	Op-Amps	Advantages	Disadvantages
Passive Input Buffer	—	Reduced component cost. Simple circuit.	THD+N degraded. Requires buffered ADC_VMID.

An active buffer/filter, such as described in Section 1 and Section 2, is recommended for typical applications. The active circuits provide enhanced filter characteristics and noise reduction through signal gain. If maximum ADC performance is not required, a passive buffer/filter can be used to reduce component costs.

Note that the THD+N performance is degraded by approximately 10 dB when using the passive buffer/filter.

3.1 Passive Input Buffer Configuration

Figure 13 shows a passive input buffer configuration. This circuit supports a maximum input of 2 VRMS with a unity signal gain.

Note that a buffered ADC_VMID reference is required in this circuit. (Alternatively, the 1.65 V reference can be provided using a 2 x 20 kΩ resistor string connected to the 3.3 V supply.)

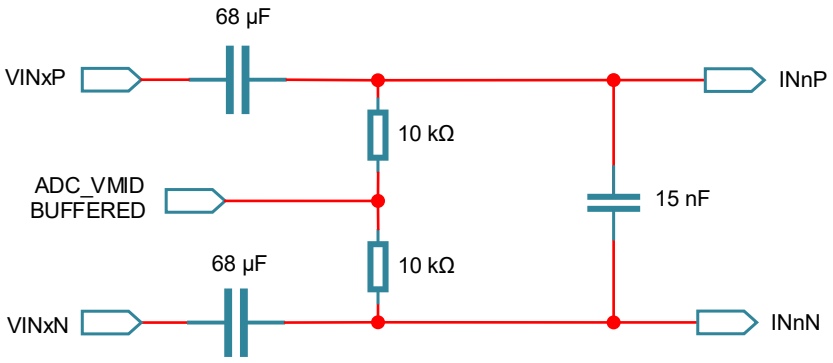

Figure 13 Passive Input Buffer Configuration

The input components (68 µF capacitor and 10 kΩ resistor) provide a first-order high-pass filter (HPF); the respective cut-off frequency is shown in Table 16. For further information on this filter, see Section 5 of the device datasheet.

Table 16 Input Buffer Filter Characteristics

Parameter	Components	Frequency
HPF –3 dB cut-off frequency	R = 10 kΩ, C = 68 µF	0.23 Hz

4 Additional Information

4.1 Recommended Components

To achieve the specified performance characteristics, the choice of external components should observe the following recommendations:

- Capacitors should be stable dielectric types, such as C0G (NP0) or electrolytic.
- Resistors should be low value where possible, to minimize thermal noise.
- Low-noise op-amps should be used, such as Texas Instruments OPA1612 or OPA1656. The op-amps should meet the minimum performance requirements noted in Table 17.

Table 17 Op-Amp Specification

Parameter	Specification
Input noise	5 nV/√Hz
Unity gain bandwidth	15 MHz
Slew rate	5 V/µs
Total harmonic distortion + noise (THD+N)	–128 dB

4.2 Buffered VMID Circuit

In most cases, the VMID reference for the input buffer can be provided from the ADC_VMID output on the CS530x. If the ADC_VMID current for all the buffer circuits exceeds 10 µA, an external VMID buffer should be used.

For the use cases shown in Section 1.2, Section 1.3, Section 2.2, Section 2.3, and Section 3.1, a buffered ADC_VMID must be provided.

The buffered VMID can be provided using the circuit shown in Figure 14.

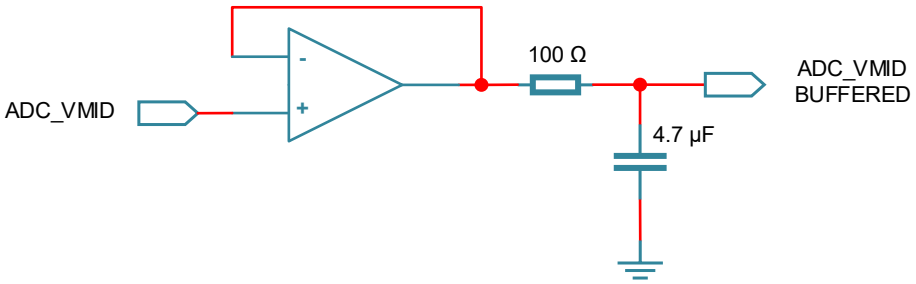

Figure 14 Buffered ADC_VMID Circuit

4.3 Unused Inputs

The recommended input buffer circuits provide a differential connection to the input pins INxP and INxN. If a single-ended input configuration is used, the unused input pin must be connected to a VMID reference – either a buffered VMID as shown in Figure 14, or else a resistor string as shown in Section 1.5 and Section 2.5.

If one or more input channel is not used (disabled), the respective input pins INxP and INxN should be floating.

5 Revision History

Revision History

Revision	Changes
R1 JUL 2025	• Initial Release

Contacting Cirrus Logic Support
For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.