MODE8X AND DUAL DIFFERENTIAL MODES ON THE WM8716/40 HIGH PERFORMANCE STEREO DACs

INTRODUCTION

The MODE8X (8 x fs) function on the WM8716/40, allows the digital filtering stage prior to the sigma-delta modulators in the devices to be bypassed, allowing an alternative 'high performance' digital filter to be used. Due to the higher speed of the digital interface in this mode, the audio data is input on two pins. One pin is used for left channel data with the other used for right.

The Dual Differential Mode allows two DACs to be used in parallel with the aim of improving performance (i.e. approximately 3dB improvement in SNR is expected). The DACs will output differential left or right channel data, depending on their configuration.

MODE8X is also supported for differential inputs but with limitations as explained in the last section of this note.

MODE8X CONTROL

When using the MODE8X function, data may be input at 8x the normal rate. Due to the higher speed of the interface, separate left and right channels must be supplied to the WM8716/40 device (unless DIFFHW mode is also selected). The left channel is input on the DIN pin (pin 2) and the right channel on the MODE pin (pin 24).

The MODE8X pin provides a multiplexer control signal (active high) that selects these two pins as inputs to the internal sigma-delta modulators and so invalidates inputs to the Serial Interface. The MODE8X pin has an internal pull-down to deselect this function when the pin is not connected.

Software control is suspended when MODE8X is active, therefore word length and justification of data are selected through hardware means, using the CSBIWO (pin 23) and the ML/I2S (pin 28) pins as detailed in Table 1. The MSB is always clocked in first for both modes.

ML/I2S	CSBIWO	WORD LENGTH (BITS) & DATA JUSTIFICATION
Low	Low	20-bit, Right Justified
Low	High	24-bit, Right Justified
High	Low	20-bit, Left Justified
High	High	24-bit, Left Justified

Table 1   Selection of Word Length and Data Justification in MODE8X

MODE8X CLOCKING SCHEME

For data sent in left justified mode, the start of the word is marked by the falling edge of LRCIN. The data is then clocked in on the next 20/24 BCKIN rising edges as shown in Figure 1.
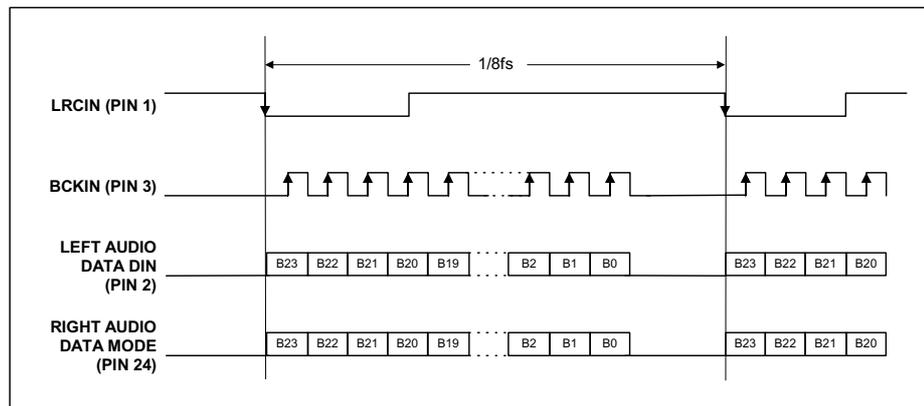
Figure 1   MODE8X Left Justified Data Format

For data sent in right justified mode, the word is justified to the rising edge of LRCIN and the data is clocked in on the preceding 20/24 BCKIN rising edges before the LRCIN rising edge. This is shown in Figure 2.
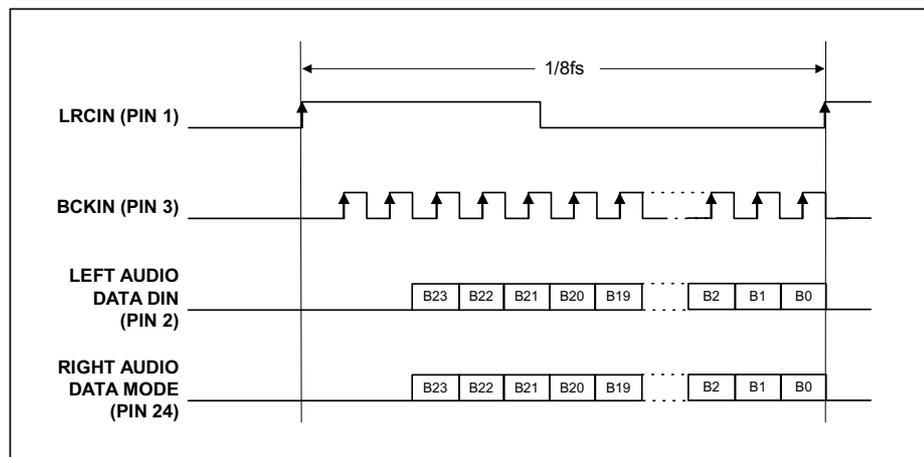

Figure 2   MODE8X Right Justified Data Format

In both modes, the polarity of LRCIN can be switched using MD/DM0.

DUAL DIFFERENTIAL MODE CONTROL

Dual differential mode is available in both software and hardware modes.

The WM8716/40 is put into dual differential mode in hardware mode by pulling the DIFFHW pin (pin 17) high. In this mode the MODE pin (pin 24) is used to define which data channel the DAC is to process, left or right. This is defined in Table 2.

DIFFHW	Output Mode	MODE	Channel Processed when DIFFHW is High
Low	Normal Stereo	Low	Left
High	Mono Dual Differential	High	Right

Table 2 Selection of Output Mode and Channel in Dual Differential Mode

The WM8716/40 is put into dual differential mode in software mode by writing 0x05e0 to register M2. This allows register M4 to then be written to. It is important to note that if this value is not written to the WM8740, any subsequent writes made to register M4 will be ignored. The DIFF[1:0] bits of register M4 should then be written to set the required mode active (see table 3).

The advantage offered by using the WM8740 in software dual differential mode is that all other software features such as attenuation controls are still available.

Two WM8716/40 devices can be used in parallel to support stereo dual differential outputs. The diagram shown in Figure 3, is an example of a stereo dual differential design using the more complex and higher performance WM8740. The audio interface is set up as 24-bit, I^2S data format. The top device (U1) has the MODE pin (pin 24) pulled high to process the right channel data and the lower device (U2) has the MODE pin (pin 24) pulled low to process the left channel information.

Table 3 lists the WM8740 output arrangement when the Dual Differential mode is set active.

Right Channel DAC (U1)				Left Channel DAC (U2)		
Software setting DIFF [1:0] = 11 [0x0c30]				Software setting DIFF [1:0] = 01 [0x0c10]		
Output	Pin No.	Function		Output	Pin No.	Function
OUTLP	17	Right Chnl Inverted		OUTLP	17	Left Chnl
OUTLN	16	Right Chnl		OUTLN	16	Left Chnl Inverted
OUTRP	12	Right Chnl		OUTRP	12	Left Chnl Inverted
OUTRN	13	Right Chnl Inverted		OUTRN	13	Left Chnl

Table 3 WM8740 Outputs in Dual Differential Mono Mode

As can be seen from the example circuit in Figure 3, a standard 2nd order low pass filter has been used. These filter characteristics may be tailored to a specific design as required. The dual positive and negative outputs of the WM8740 are summed separately by a resistor network before inputting into the non-inverting and inverting inputs of the op-amps.

This circuit will be simplified for the WM8716 device, as there are only single positive and negative outputs.
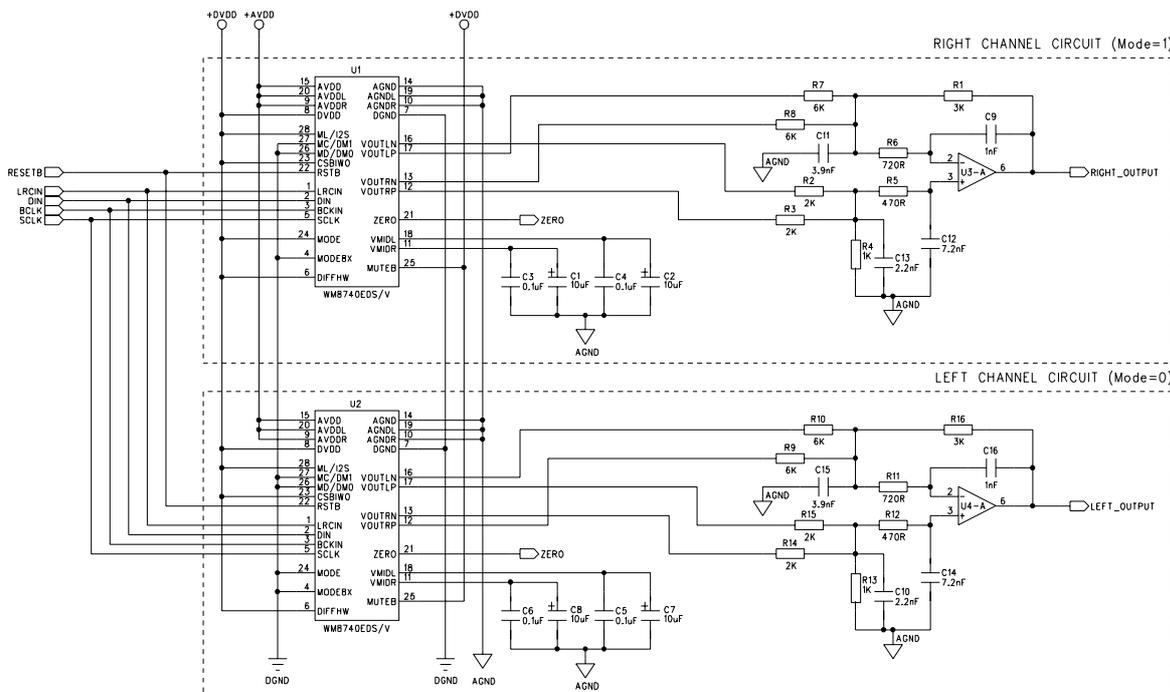

Figure 3 Dual Differential Mode Example Configuration

DUAL DIFFERENTIAL AND MODE8X MODES USED IN CONJUNCTION

Both Dual Differential Mode and MODE8X modes can be used in conjunction but with some limitations.

As previously mentioned, when the MODE8X function is active, software control of the WM8716/40 is disabled. Also, two pins; DIN (pin 2) and MODE (pin 24) are used for left and right channel data to bypass the pre sigma-delta modulator digital filters.

If Dual Differential Mode is also set active, only one pin is available for data input per device; DIN (pin 2). The single channel input will be fed to both left and right DAC's and will produce differential outputs.

In this joint configuration, the MODE pin (pin 24) must be tied low, setting the device into hardware mode. Setting the MODE pin low will also select the left channel as the input data to be processed. To allow the right channel data to be processed, the MD/DMO pin (pin 26) must be tied low, so inverting the LRCIN clock. This inversion will cause an offset of one sample when compared to the left channel data, but at this sampling rate, any effect should be unnoticeable at the output.

Note: As previously mentioned in the MODE8X control and clocking sections, only Left or Right justified data formats are supported when used in this configuration.

MODE8X	DIFFHW	Output Mode	MODE	MD/DMO	Channel Processed (input on DIN)
High	High	Mono Dual Differential and MODE8X	Low	High	Left
High	High	Mono Dual Differential and MODE8X	Low	Low	Right

Table 4 Settings for Combined MODE8X and Dual Differential Modes

Using two WM8716/40 devices in this manner will provide both flexibility in digital filtering and superb SNR performance.

APPLICATION SUPPORT

If you require further information or require technical support, please contact Wolfson Microelectronics Applications group through the following channels:

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