WAN_0135

WM9712 GPIO IRQ Control and Sequencing

INTRODUCTION

This application note describes the setup of GPIO's when used to input logic levels and generate interrupts. The sequencing of setup is important in order for the generated interrupts to be detected correctly.

GPIO SETUP

The WM9712L has five GPIO pins that operate as defined in the AC'97 Revision 2.2 specification. Each GPIO pin can be set up as an input or as an output, and has corresponding bits in register 54h and in slot 12. The state of a GPIO output can only be changed by sending data through slot 12 of outgoing frames (SDATAOUT). Data can be returned from a GPIO input by reading the register bit, or examining slot 12 of incoming frames (SDATAIN). GPIO inputs can be made sticky, and can be programmed to generate an interrupt, transmitted either through the AC-Link or a dedicated interrupt pin (pin 45).

GPIO pins 2 to 5 are multi-purpose pins that can also be used for other (non-GPIO) purposes, e.g. as a SPDIF output or to signal pen-down. This is controlled by register 56h.

Independently of the GPIO pins, the WM9712L also has five virtual GPIOs. These are signals from inside the WM9712L, which are treated as if they were GPIO input signals. From a software perspective, virtual GPIOs are the same as GPIO pins, but they cannot be set up as outputs, and are not tied to an actual pin. This allows for simple, uniform processing of different types of signals that may generate interrupts (e.g. pen down, battery warnings, jack insertion, high-temperature warning, or GPIO signals).

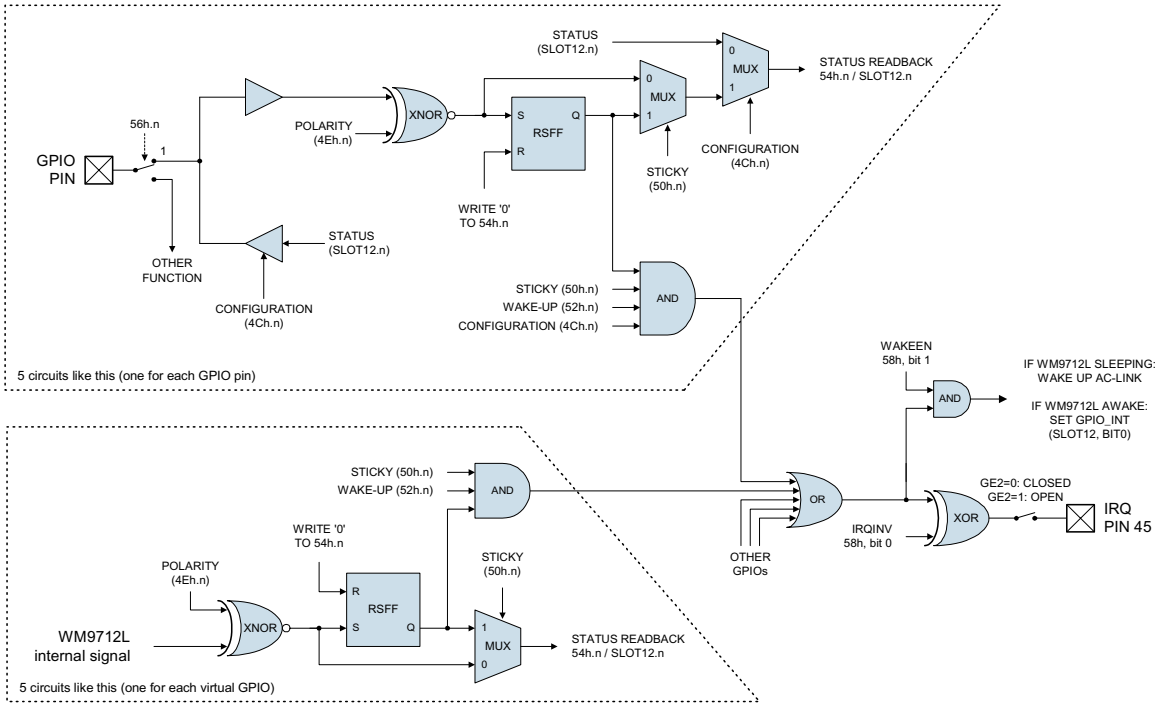

Figure 1 GPIO Logic

IRQ SETUP AND SEQUENCING

There is a set sequence for setting up the GPIO input for IRQ operation which is listed below. This example shows how a Logic input created from Comparator 2 can be used to generate an interrupt. This process is virtually identical for all other GPIO inputs. Please note it is perfectly acceptable to use either comparator inputs as standard GPIO inputs if not being used for battery monitoring.

1. Set Comparator 2 signal source (reg 5Ch bit 10:9). Selects which signal source is connected to Comparator 2
2. Set Comparator 2 as input and IRQ as output (reg 4Ch bit 14 and bit 2). Setting bit 2 of 4Ch to "0" makes GPIO2 an output (This will be later set to output IRQ). Setting bit 14 to "1" makes the Comparator logic level an input.
3. Set Comparator 2 active level (reg 4Eh bit 14). Set the relevant polarity of the logic level from Comparator 2. This will be application specific.
4. Set Comparator 2 "Sticky" bit (reg 50h bit 14). Writing "1" to bit 14 of register 50h makes the signal Stick at a specific level so that even a short pulse received on the Input will be detected (Minimum pulse width approximately MCLK Period divided by 2).
5. Write "0" to 54h for Comparator 2 (reg 54h bit 14). This write clears the status of the sticky bit so that the next transition monitored on the input of Comparator 2 will cause the level to be stuck HIGH.
6. Set Comparator 2 GPIO "Wake-up" (reg 52h bit 14). This register bit must be set to "1" if interrupts are to be generated from the relevant GPIO.
7. Set relevant GPIO for IRQ (reg 56h bit 2). Sets pin 45 to be IRQ rather than GPIO2.

Writing "0" to 54h causes the GPIO status signal to be cleared. It should be made clear that unless the source of the interrupt is first removed the status bit will be set again immediately. Once an interrupt is generated, Slot 12 or 54h should be interrogated to obtain details of which GPIO caused the interrupt. The interrupt can then be cleared again by writing to reg 50h and clearing the "sticky" bits.

SUMMARY

This document provides an example of how to use the GPIO inputs to the WM9712 to generate interrupts via the IRQ pin. The setup of registers is fairly complex and must be completed in a set sequence to ensure the IRQ interrupt is generated correctly.

APPLICATION SUPPORT

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