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WM9711/12 Power Management Using Pin 47

INTRODUCTION

One of the main advantages of the WM9711 and WM9712 (now referred to as device) from the standard AC97 specification is the externally selectable power management configuration of the powerdown register following the completion of a standard cold reset. This application note is intended to explain how the power arrangement can be externally configured, the configuration of the device in each mode and the advantages of using the modes available.

PIN 47 OPERATION (GPIO4/ADA/MASK)

The state of pin 47 (GPIO4/ADA/MASK) is sampled during the AC97 standard cold reset. A cold reset is performed by a high-low-high transition on the RESETB (pin11) input; please refer to the AC97 specification and device datasheet for more information. Once the RESETB line is released (low-high transition), pin 47 will by default become a GPIO input. The status of pin 47 is sampled on the transition from low-high of the RESETB input. The status of pin 47 during the RESETB low period and transition will determine the default configuration of the standard power management register, 26h.

POWER MANAGEMENT REGISTER

There are two possible configurations for the power management register after a cold reset has been completed:

1. All PR bits (PR6 – PR0) **Enabled**.

2. All PR bits (PR6 – PR0) **Disabled**.

The status of the power management register in relation to pin 47 is detailed in Table 1.

REGISTER ADDRESS	BIT	LABEL	REGISTER STATUS AFTER COLD RESET		DESCRIPTION
			PIN 47 'LOW' DURING RESET	PIN 47 'HIGH' DURING RESET	
26h Powerdown/ Status Register	14	PR6	0 (ON)	1 (OFF)	Disables HPOUTL, HPOUTR and OUT3 Buffer
	13	PR5	0 (ON)	1 (OFF)	Disables internal clock
	12	PR4	0 (ON)	1 (OFF)	Disables AC-link interface (external clock off)
	11	PR3	0 (ON)	1 (OFF)	Disables VREF, analogue mixers and outputs
	10	PR2	0 (ON)	1 (OFF)	Disables analogue mixers, LOUT2, ROUT2 (but not VREF)
	9	PR1	0 (ON)	1 (OFF)	Disables stereo DAC
	8	PR0	0 (ON)	1 (OFF)	Disables audio ADCs and input MUX
	3	REF	1	0	Read-only bit, indicates VREF is ready (inverse of PR2)
	2	ANL	1	0	Read-only bit, indicates analogue mixers are ready (inverse of PR3)
	1	DAC	1	0	Read-only bit, indicates audio DACs are ready (inverse of PR1)
	0	ADC	1	0	Read-only bit, indicates audio ADCs are ready (inverse of PR0)

Table 1 Register 26h Default Configuration

The value of R26h can be configured to allow the device to be in a fully operational mode (all PR bits enabled) or in a low power mode (all PR bits disabled) after the cold reset.

There are two possible recommended hardware configurations for configuring the default enable condition and one for configuring the default disable condition.

PIN 47 LOW CONFIGURATION

By configuring the value of pin 47 low during a cold rest, the device will be enabled in a fully operational mode. Pin 47 is a bi-directional pin and has three possible functions for use:

1. GPIO4 (**Input** or **Output** signal).

2. ADA (**Output** signal).

3. MASK (**Input** signal)

By default, pin 47 will be configured as a GPIO input after a cold reset has been completed. Since the pin is configured as an input, the connection to GND has two possible configurations:

1. Direct connection to ground. This option should only be used if none of the three possible functions for pin 47 are required at reset or are enabled during device operation.

2. Connection to GND using 100kΩ pull down resistor. This option should be used if any of the three functions available to pin 47 are intended to be used or enabled.

These two possible external pin configurations are detailed within the external component diagram of the relevant device datasheet. For AC97 default compatibility, it is recommended that option 2 (100kΩ to GND) is used.

The advantage of configuring the power management register as default enable after a cold reset is that the device is ready to operate and therefore saves time and software writes for device configuration after reset.

PIN 47 HIGH CONFIGURATION

Pin 47 should be configured high using a 100kΩ pull up resistor connected to DBVDD. A pull up resistor should be used to ensure minimal power consumption is maintained.

Pin 47 high external configuration is detailed within the external component diagram of the relevant device datasheet.

The main advantage of using this mode is that the device can be configured in a low power mode after the supplies have been applied and a cold reset command sent. This configuration has the advantage of preserving the battery life if the operation of the device is required after an unknown or long delay after the power has been initially provided to the device.

ENABLE THE AC LINK FROM LOW POWER MODE

If pin 47 is configured with a pull up resistor to DBVDD, the power management register will be disabled by default (all PR bits set to 1) after a cold reset command is completed. The only way to enable the AC link is to perform a standard AC97 warm reset; this is completed using the SYNC line. Full details are available in the datasheet and the AC97 specification. When a warm reset is commanded from this disabled condition, the only PR bit which will be enabled (set to '0') is PR4 [R26h Bit 12], a read of R26h will return the value 0xEF00h. The warm reset enables only the AC link and allows full access to all device registers.

SOFTWARE RESET

The device supports standard AC97 register reset by writing to R00h. Writing to this register does not sample the status of pin 47 and therefore the power management register will be enabled as default, R26h = 000F.

A software reset to R00h does not internally enable the device after power has been supplied to the device. Only a standard cold reset using the RESETB input pin can be used to initialise the device after power is applied.

CONCLUSION

The WM9711 and WM9712 have added functionality from the AC97 specification which allows the device to be configured in a low power mode which is more applicable to portable applications where power consumption is important to preserve battery life. This added functionality is made possible using external configuration of pin 47 using one of the three possible external solutions.

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