WAN_0196

Jack / Headphone Detect Operation and Example Applications

INTRODUCTION

Jack / Headphone detect is used to trigger an action in the CODEC device in response to an accessory (eg. microphone or headphone) being connected or disconnected. The CODEC action may be to switch between headphone and speaker outputs, or to select different signal path routing configurations. In some cases, the action may be implemented autonomously within the CODEC; in other cases, an Interrupt signal may be generated by the CODEC in order to trigger a response via a host processor.

There are differences in the headphone/jack detect features provided on different Wolfson CODECs. Different implementations are applicable according to the number and type of output drivers, and according to the intended application(s) of the devices.

This application note summarises the headphone/jack detect features provided on a selection of Wolfson devices, and provides details of how to use these features in typical applications.

SUMMARY

The devices specifically covered by this application note are listed in Table 1.

As a summary of the headphone/jack detect capability of each device, Table 1 indicates how many input pins are capable of supporting a headphone/jack detect function, and what type of response can be triggered by the jack detect signal.

In some devices, the jack detect signal can be configured to autonomously enable or disable selected signal paths. In some devices, a jack detect (or GPIO input) signal can be used to generate a processor Interrupt signal in hardware or software, in order that a host processor can be commanded to implement the required sequence of register re-configurations.

Many devices have the capability to detect the current drawn from the microphone bias circuit; this feature can also be used to detect the presence of an accessory inserted in a jack socket. In this case, the current detection is indicated via an Interrupt signal in hardware or software or through a GPIO hardware output.

DEVICE	INPUT PINS	JACK DETECT SIGNAL PATH CONTROL	JACK DETECT / GPIO INTERRUPT	MICBIAS CURRENT DETECT
WM8750	1 analogue input	Yes	-	-
WM8753	1 GPIO pin	Yes	Yes	Yes
WM8900	2 analogue inputs + 3 GPIO pins	Yes	-	-
WM8903	5 GPIO pins	-	Yes	Yes
WM8350	2 analogue inputs + 13 GPIO pins	-	Yes	Yes
WM8400	2 analogue inputs + 6 GPIO pins	-	Yes	Yes
WM8990	2 analogue inputs + 4 GPIO pins	-	Yes	Yes

Table 1 Summary of Headphone / Jack Detect Capabilities on Selected CODECs

SWITCHED JACK SOCKET CONFIGURATION

The most common configuration of a switched headphone socket has one or more jack detect pins which are disconnected by jack insertion. A typical circuit incorporating this type of jack socket is shown in Figure 1. The circuit shows a recommended method for connecting a switched headphone socket to a pin configured as the jack detect input sensing pin. The pin names are applicable to the WM8750, but the circuit configuration is generic and applicable to other devices.

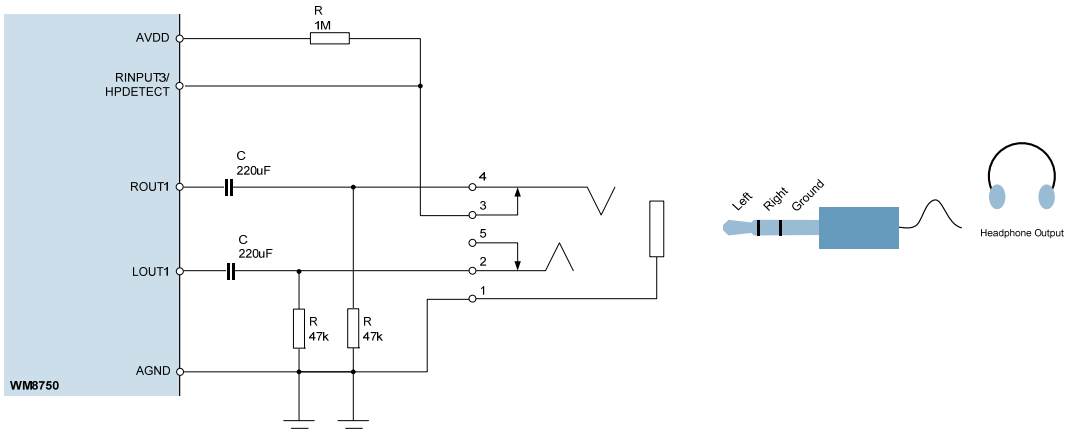

Figure 1 Switched Socket Connection

The headphone outputs on many CODECs are DC biased, requiring external blocking capacitors to remove the DC bias. This capacitance (typically 220µF), together with the load resistance, forms a high pass filter and blocks the DC bias. This type of output is found on the WM8350, WM8400, WM8990, WM8753, WM8750 and many other devices.

The 47kΩ resistors shown in Figure 1 are advisable in order to prevent the headphone circuit from driving an open circuit; this ensures amplifier stability and stable power consumption whenever the headphone is disconnected. These resistors also serve as part of a potential divider with the 1MΩ resistor illustrated.

When a stereo jack is inserted, the external accessory (headphone) connects to pins 1, 2 and 4 of the socket; pins 3 and 5 are isolated. In this case, the GPIO pin is at the logic 1 level as a result of the 1MΩ pull-up resistor to AVDD.

When the jack is removed, a circuit is made between Pin 3 and Pin 4 and also (separately) between Pin 5 and Pin 2. In this case, the GPIO pin is at the logic 0 level as a result of the potential divider formed by the 47kΩ and 1MΩ resistors.

MICBIAS CURRENT DETECT CIRCUIT CONFIGURATION

An electret condenser microphone requires a bias current in order to operate correctly. A suitable high quality voltage reference is incorporated on Wolfson CODECs, and output on the MICBIAS pin. Internal circuits on many CODECs allow the MICBIAS current to be monitored and to be compared with programmable thresholds. This current detect feature can be used to trigger an Interrupt signal to a host processor, which can then implement the required CODEC configuration according to the connection or disconnection of the external accessory.

The pin names illustrated in Figure 2 are applicable to the WM8400, but the circuit configuration is generic and applicable to other devices.

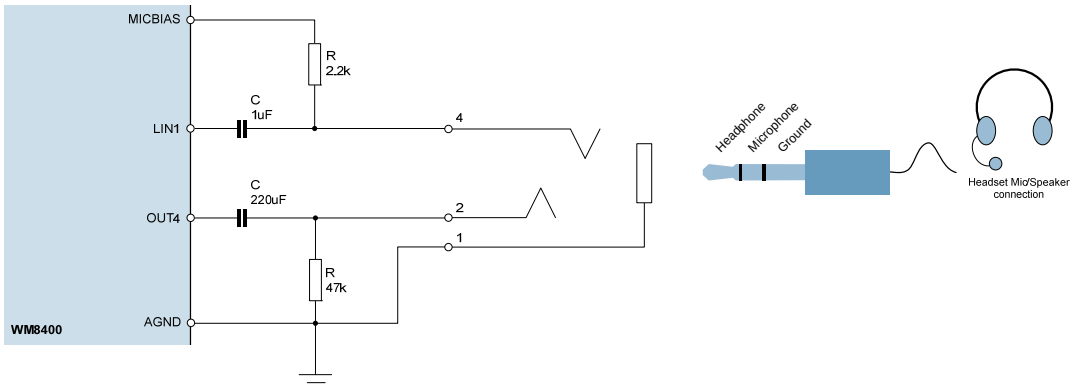

Figure 2 MicBias Current Detect Connection

The circuit shows the microphone input on the LIN1 pin, via a 1µF DC blocking capacitor. The microphone bias is provided from MICBIAS, via a 2.2kΩ current limiting resistor. The mono headset output is provided on the OUT4 pin, via a 220µF DC blocking capacitor. The 47kΩ output resistance is also to ensure amplifier stability and stable power consumption whenever the headphone is disconnected

When a compatible accessory is inserted in the jack, a current will be drawn from the MICBIAS pin. Provided that the current threshold is set correctly, this event will set an internal register bit and, optionally, assert an external GPIO pin configured as an Interrupt Event output.

EXAMPLE APPLICATIONS

The following sections outline the options and register settings for a variety of headphone/jack detect scenarios in selected Wolfson devices. It is not practical to illustrate every available configuration, but the aim is to provide sufficient guidance to show how variations on these examples could be derived.

EXAMPLE 1 - JACK DETECT SIGNAL PATH CONTROL (WM8750)

The WM8750 supports headphone output on LOUT1 / ROUT2 and loudspeaker output on LOUT2 / ROUT2. When the RINPUT3/HPDETECT pin is connected and configured as the jack detect input (as illustrated in Figure 1), it is possible to disable the speaker driver and enable the headphone driver when the headphone jack is inserted. The applicable register settings for this application are given in Table 2.

REGISTER ADDRESS	BIT	LABEL	VALUE	DESCRIPTION
R26 (1Ah) Power Management (2)	6	LOUT1	1	Enables LOUT1
	5	ROUT1	1	Enables ROUT1
	4	LOUT2	1	Enables LOUT2
	3	ROUT2	1	Enables ROUT2
R24 (18h) Additional Control (2)	6	HPSWEN	1	Enables Headphone Switch
	5	HPSWPOL	0	Logic 1 on HPDETECT selects Headphone output

Table 2 WM8750 - Jack Insertion Disables Speaker Output and Enables Headphone

Note that the headphone and speaker output drivers must all be enabled in Register R26; the headphone detect function disables selected outputs as required. A possible variation on this example could be to change the polarity set by HPSWPOL, for example, if the HPDETECT pin relates to the connection of a loudspeaker, not the connection of a headphone.

If cap-less output configuration is used, with OUT3 providing the virtual ground, then care must be taken to ensure that the voltage levels at the HPDETECT input pin are compatible with the HPDETECT logic threshold. This can be adjusted by using a pull-down resistor instead of the pull-up resistor at this point.

EXAMPLE 2 - JACK DETECT SIGNAL PATH CONTROL (WM8753)

The WM8753 supports headphone output on LOUT1 / ROUT2 and loudspeaker output on LOUT2 / ROUT2. When the GPIO4 pin is connected and configured as the jack detect input, it is possible to disable the speaker driver and enable the headphone driver when the headphone jack is inserted. The applicable register settings for this application are given in Table 3.

REGISTER ADDRESS	BIT	LABEL	VALUE	DESCRIPTION
R21 (15h) Pwr Mgmt (3)	8	LOUT1	1	Enables LOUT1
	7	ROUT1	1	Enables ROUT1
	6	LOUT2	1	Enables LOUT2
	5	ROUT2	1	Enables ROUT2
R27 (1Bh) GPIO Control (1)	2:0	GPIO4M [2:0]	000	GPIO4 is an input
R45 (2Dh) Output Control	6	HPSWEN	1	Enables Headphone Switch
	5	HPSWPOL	0	Logic 1 on GPIO4 selects Headphone output
R52 (34h) Clock Control	5	SLWCLK	0	Selects MCLK to drive the debounce timeout

Table 3 WM8753 - Jack Insertion Disables Speaker Output and Enables Headphone

Note that the headphone and speaker output drivers must all be enabled in Register R21; the headphone detect function disables selected outputs as required. A possible variation on this example could be to change the polarity set by HPSWPOL, for example, if the GPIO4 pin relates to the connection of a loudspeaker, not the connection of a headphone. The WM8753 supports two separate clock inputs, allowing flexibility for one or other clock to be disabled when not required. For reliable Jack Detect operation, it is important that the SLWCLK bit in Register R52 selects a timeout clock source that is active. If the MCLK input is disabled, and the PCMCLK is used, then SLWCLK should be set to logic 1.

If cap-less output configuration is used, with OUT3 or OUT4 providing the virtual ground, then care must be taken to ensure that the voltage levels at the GPIO4 input pin are compatible with the GPIO4 logic threshold. This can be adjusted by using a pull-down resistor instead of the pull-up resistor at this point.

Different settings of GPIO4M can be used to connect internal pull-up or pull-down resistors, removing the need for an external component; this may be useful in both cap-less and dc-biased headphone output configurations.

It is possible for the WM8753 to generate an Interrupt in response to the headphone detect input. The polarity is selectable, allowing either 'Interrupt on Insert' or 'Interrupt on Removal' functionality as required. The Interrupt status may be output on any available GPIO pin.

EXAMPLE 3 - MICBIAS CURRENT DETECT IRQ OUTPUT (WM8753)

The WM8753 supports current detection on the MICBIAS pin. In applications which require to detect the connection of a microphone accessory, this feature can provide an equivalent function to the headphone jack detect.

On the WM8753, this feature can be used to generate an Interrupt signal on a GPIO pin when the current exceeds a threshold. This allows a host processor to initiate the required reconfiguration of the device via the Control interface. Example register settings for this application are given in Table 4; the output pin is GPIO5 in this example.

REGISTER ADDRESS	BIT	LABEL	VALUE	DESCRIPTION
R20 (14h) Power Management (1)	5	MICB	1	Microphone Bias is Enabled
R51 (33h) Mic bias comp control	8	MBVSEL	0	Microphone Bias is AVDD x 0.9
	3:1	MBTHRESH [2:0]	001	Microphone current threshold set to 410μA
	0	MBCEN	1	Microphone bias current comparator is Enabled
R25 (19h) Interrupt Polarity	1	MICDETPOL	0	Interrupt when above the threshold
R26 (1Ah) Interrupt Mask	1	MICDETEN	1	Mic Current Detect Interrupt is Enabled
R27 (1Bh) GPIO Control (1)	8:7	INTCON [1:0]	10	Interrupt signal is Active High
	4:3	GPIO5M [1:0]	01	GPIO5 is an interrupt output

Table 4 WM8753 - Mic Current Detect Generates Interrupt Output on GPIO5

Note that the Interrupt signal is latched once set. The latch is reset by disabling the source that triggered the Interrupt - setting MICDETEN = 0 in this example. However, if the source is disabled, then the device can no longer indicate the insertion or removal of the jack. The recommended implementation is to reset the interrupt (MICDETEN = 0), then invert the polarity (using MICDETPOL), and then re-enable the Mic Detect Interrupt (MICDETEN = 1). In this manner, a new Interrupt will be generated for each insertion/removal of the external jack.

Depending on other circuit components, a different current threshold may be applicable. The internal interrupt logic and the electrical characteristics of the interrupt output can be changed using the register fields above. The Interrupt status could be also output on other GPIO pins.

In a similar manner, the Interrupt event could be programmed to indicate the status of the Headphone/Jack detect function using the HPSWIEN and HPSWIPOL bits in Registers R26 and R27. (See the WM8753 datasheet for definitions of these bits.) This would be desirable if a host processor was used to reconfigure the device between headphone and speaker modes. In this case, the Headphone Detect Switch function would be disabled (HPSWEN = 0), and the necessary Register writes could be tailored to the particular application.

EXAMPLE 4 - JACK DETECT SIGNAL PATH CONTROL (WM8900)

The WM8900 supports two pairs of Line Outputs and one pair of Headphone Outputs. The jack detect function can be enabled on 5 possible input pins, and can be set to enable or disable specific outputs in either state. The Charge Pump that drives the headphone output can also be controlled by the jack detect function.

A possible application would be for the LINPUT3/JD pin to be used as the jack detect input, where jack insertion disables LINEOUT1 (left and right), enables LINEOUT2 (left and right), enables the Headphone driver and enables the Charge Pump. The applicable register settings for this application are given in Table 5.

REGISTER ADDRESS	BIT	LABEL	VALUE	DESCRIPTION
R2 (02h) Power Management (2)	8	OUT1L_ENA	1	Enables LINEOUT1 (Left)
	7	OUT1R_ENA	1	Enables LINEOUT1 (Right)
R3 (03h) Power Management (3)	7	CP_ENA	1	Enables Charge Pump
	6	OUT2L_ENA	1	Enables LINEOUT2 (Left)
	5	OUT2R_ENA	1	Enables LINEOUT2 (Right)
R7 (07h) Clocking 2	0	TOCLK_ENA	1	Jack detect de-bounce clock is enabled (providing SYSCLK is also present).
R58 (3Ah) Headphone Control 1	7	HP_IPSTAGE_ ENA	1	Headphone input stage is Enabled
	6	HP_OPSTAGE _ENA	1	Headphone output stage is Enabled
R18 (12h) GPIO Control	9	JD_ENA	1	Jack detect function is Enabled
	8	JD_MODE	0	Jack detect function is Active High
	3:1	JD_SRC [2:0]	010	Jack detect input is LINPUT3/JD
R17 (11h) Jack Detect Control	13	JD_EN1[5]	1	Charge Pump is enabled when Jack Detect input is high
	12	JD_EN1[4]	1	Headphone outputs are enabled when Jack Detect input is high
	11	JD_EN1[3]	1	LINEOUT2R and LINEOUT2L are enabled when Jack Detect input is high
	10	JD_EN1[2]	1	
	9	JD_EN1[1]	0	LINEOUT1R and LINEOUT1L are disabled when Jack Detect input is high
	8	JD_EN1[0]	0	
	5	JD_EN0[5]	0	Charge Pump is disabled when Jack Detect input is high
	4	JD_EN0[4]	0	Headphone outputs are disabled when Jack Detect input is high
	3	JD_EN0[3]	0	LINEOUT2R and LINEOUT2L are disabled when Jack Detect input is high
	2	JD_EN0[2]	0	
	1	JD_EN0[1]	1	LINEOUT1R and LINEOUT1L are enabled when Jack Detect input is high
	0	JD_EN0[0]	1	

Table 5 WM8900 - Jack Insertion Disables Lineout1 and Enables Headphone

Note that the output drivers and charge pump must all be enabled in Registers R2, R3 and R58 - the Jack Detect function disables selected outputs as required. Bits [13:8] in Register R17 determine the status of the output drivers and charge pump when the Jack Detect input is high (assuming the JD_MODE polarity is Active High). Bits [5:0] in Register R17 determine the status of the output drivers and charge pump when the Jack Detect input is low.

The required functionality can be easily modified by adjusting the bits in Register R17. One possible variation would be to leave LINEOUT1 enabled regardless of the Jack Detect input. To achieve this, the bits associated with LINEOUT1 should all be set to 1 - R17, bits [9, 8, 1, 0]. If it is desired that the Charge Pump is not controlled by the Jack Detect input, then set R17, bits [13, 5] to 1. Note that any circuit that is not controlled by the Jack Detect input can still be enabled or disabled by writing to the Power Management bits associate with that circuit block.

EXAMPLE 5 - MICBIAS CURRENT DETECT GPIO OUTPUT (WM8903)

The WM8903 supports current detection on the MICBIAS pin. In applications which require to detect the connection of a microphone accessory, this feature can provide an equivalent function to the headphone jack detect.

On the WM8903, the status of the MICBIAS current can be output directly on a GPIO pin, which can be used by a host processor to initiate the required reconfiguration of the device via the Control Interface. Example register settings for this application are given in Table 6; the output pin is GPIO3 in this example.

REGISTER ADDRESS	BIT	LABEL	VALUE	DESCRIPTION
R6 (06h) Mic Bias Control	6:4	MICDET_THR [2:0]	001	Microphone current threshold set to 400μA
	1	MICDET_ENA	1	Microphone current detection is Enabled
	0	MICBIAS_ENA	1	Microphone Bias is Enabled
R118 (76h) GPIO Control 3	12:8	GP3_FN [4:0]	00100	GPIO3 outputs Mic Detect status
	7	GP3_DIR	0	GPIO3 is output
	6	GP3_OP_CFG	0	GPIO3 is CMOS output
	3	GP3_PD	0	GPIO3 pull-down resistor is disabled
	2	GP3_PU	0	GPIO3 pull-up resistor is disabled

Table 6 WM8903 - Mic Current Detect Generates a Status Output on GPIO3

If required, the MICBIAS Current Detect can also be used to trigger an Interrupt event, which can be indicated in hardware on either of two output pins. By this method, multiple events can share a single Interrupt connection with the host processor. When the Interrupt is asserted, the host processor can determine which of the possible sources caused the Interrupt by reading the WM8903 registers.

EXAMPLE 6 - MICBIAS CURRENT DETECT IRQ EVENT (WM8350)

The WM8350 supports headphone jack detection on the IN2L or IN2R input pins. When jack detection is enabled on these pins, they act is inputs to the Interrupt controller. The register bits associated with jack detection on IN2L are described in Table 7.

REGISTER ADDRESS	BIT	LABEL	VALUE	DESCRIPTION
R11 (0Bh) Power Mgmt 1	8	TOCLK_ENA	1	Jack detect de-bounce clock is enabled (providing MCLK is also present).
R77 (4Dh) Jack Detect	15	JDL_ENA	1	Jack detect is enabled on IN2L pin
R3 (03h) System Control (2)	0	IRQ_POL	0	IRQ pin is Active Low
R24 (18h) System Interrupts	7	CODEC_INT	(see text below)	This bit indicates the status of the CODEC interrupt. (This is an 'OR' function of all unmasked Jack Detect and Mic Current Detect events.)
R32 (20h) System Interrupt Mask	7	IM_CODEC_INT	(see text below)	CODEC Interrupts Mask bit
R31 (1Fh) Comparator Interrupt Status	11	CODEC_JACK_DET_L_EINT	(see text below)	This bit indicates the status of the Left Channel Jack Detect Interrupt.
R39 (27h) Comparator Interrupt Status Mask	11	IM_CODEC_JACK_DET_L_EINT	(see text below)	Left Channel Jack Detect Mask bit

Table 7 WM8350 - Jack Detect on IN2L Generates Interrupt Event

When the Mask bits IM_CODEC_INT and IM_CODEC_JACK_DET_L_EINT are set to 0 (unmasked), then a logic 1 on the IN2L input pin will cause the Interrupt event to be triggered. As determined by the selected polarity (IRQ_POL), the IRQ pin will go to logic 0 to indicate the Interrupt event has occurred. A separate host processor is required to determine which event caused the Interrupt event, and to initiate the appropriate response.

The Interrupt bit CODEC_JACK_DET_L_EINT is triggered on a rising or a falling edge and is latched once set. It is cleared by reading the bit. Therefore, a new Interrupt event will occur on every jack insertion or jack removal, providing that the host processor reads the applicable Interrupt Status register (R31 in this case) in order to clear the IRQ following each event.

The WM8350 also supports current detection on the MICBIAS pin. In applications which require to detect the connection of a microphone accessory, this feature can be used to generate an Interrupt event or can be indicated on a GPIO pin configured as a MICDET output. The current detection status can also be read from the Register Map at any time, without using the Interrupt or GPIO output circuits.

EXAMPLE 7 - MICBIAS CURRENT DETECT GPIO OUTPUT (WM8400)

The WM8400 supports current detection on the MICBIAS pin. In applications which require to detect the connection of a microphone accessory, this feature can provide an equivalent function to the headphone jack detect.

On the WM8400, the status of the MICBIAS current can be output directly on a GPIO pin, which can be used by a host processor to initiate the required reconfiguration of the device via the Control Interface. Example register settings for this application are given in Table 8; the output pin is GPIO2 in this example.

REGISTER ADDRESS	BIT	LABEL	VALUE	DESCRIPTION
R2 (02h)	4	MIC1BIAS_ENA	1	Microphone Bias is Enabled
R58 (3Ah)	7:6	MCDTHR [1:0]	00	Microphone current threshold set to 410μA
	2	MCD		Microphone current detection is Enabled
	0	MBSEL	0	Microphone Bias is AVDD x 0.9
R8 (08h)	15	MCLK_SRC	0	GPIO2 pin is configured as GPIO
R10 (0Ah)	13	AIF_TRIS	0	Audio Interface and GPIO pins are not tri-stated
R19 (13h)	13	GPIO2_PU	0	GPIO2 pull-up resistor is disabled
	12	GPIO2_PD	0	GPIO2 pull-down resistor is disabled
	11:8	GPIO2_SEL [3:0]	1000	GPIO2 outputs Mic Detect status

Table 8 WM8400 - Mic Current Detect Generates a Status Output on GPIO2

The WM8400 also supports logic inputs on 8 input pins, which can be used as jack detect inputs. The status of these inputs can be read via the GPIO registers and can be used to trigger latching Interrupt events. The MICBIAS current detect function feeds into this GPIO/Interrupt block in the same way. The Interrupt status can be read from the Register Map and can also be output on a GPIO pin. See the following WM8990 Example Application for notes on how to handle the Interrupt events to generate separate Interrupt events for accessory connection and disconnection.

EXAMPLE 8 - JACK DETECT IRQ OUTPUT (WM8990)

The WM8990 supports GPIO inputs on 4 digital pins (GPIO1, GPIO3, GPIO4 and GPIO6) and on 2 analogue input pins (GPI7 and GPI8). Any of these inputs can be used as jack detect inputs and reported to a host processor via a GPIO pin configured as an Interrupt Output.

Example register settings for this application are given in Table 8; In this case, the input (Jack Detect) pin is GPIO1 and the output (Interrupt/IRQ) pin is GPIO5. It is important to note that GPIO1 - GPIO6 are referenced to the DBVDD power domain, whilst GPI7 and GPI8 are referenced to the AVDD power domain. Care must be taken to ensure that the Jack Detect input signal is compatible with the digital logic thresholds of the chosen pin of the WM8990.

REGISTER ADDRESS	BIT	LABEL	VALUE	DESCRIPTION
R6 (06h)	14	TOCLK_ENA	1	De-bounce clock is enabled (providing SYSCLK is also present).
R8 (08h)	13	AIF_SEL	0	Audio Interface 1 is selected
R9 (09h)	15	ALRCGPIO1	1	GPIO1 pin is configured as GPIO
	13	AIF_TRIS	0	Audio Interface and GPIO pins are not tri-stated
R18 (12h)	12	IRQ	(see text below)	This bit indicates the status of the internal Interrupt flag. The polarity of this bit is controlled by IRQ_INV
	0	GPIO_STATUS [0]	(see text below)	This bit indicates the status of the GPIO1 Interrupt. This bit latches on when set. It is reset by writing a logic 1 to this bit.
R19 (13h)	7	GPIO1_DEB_ENA	0	Input de-bounce circuit is enabled on GPIO1
	6	GPIO1_IRQ_ENA	1	IRQ trigger is enabled on GPIO1 input
	5	GPIO1_PU	0	GPIO1 pull-up resistor is disabled
	4	GPIO1_PD	0	GPIO1 pull-down resistor is disabled
	3:0	GPIO1_SEL [3:0]	0000	GPIO1 is configured as an input
R21 (13h)	6	GPIO5_IRQ_ENA	0	IRQ trigger is disabled on GPIO5
	5	GPIO5_PU	0	GPIO5 pull-up resistor is disabled
	4	GPIO5_PD	0	GPIO5 pull-down resistor is disabled
	3:0	GPIO5_SEL [3:0]	0111	GPIO5 outputs the Interrupt status
R23 (17h)	12	IRQ_INV	0	IRQ polarity is Active High
	0	GPIO_POL [0]	(see text below)	This bit controls the polarity of the GPIO1 input to the Interrupt function.

Table 9 WM8990 - Jack Detect Input on GPIO1 Generates an IRQ Output on GPIO5

In this configuration, a logic level at the GPIO1 input will cause the Interrupt bit to be set, and this will cause the GPIO5 output to be asserted. The polarity of the GPIO5 output can be reversed, if required, by setting IRQ_INV = 1. A separate host processor is required to determine which event caused the Interrupt event, and to initiate the appropriate response. The host processor can detect an Interrupt event by reading the IRQ bit. In this example, however, the IRQ status is also output directly on GPIO5.

On the WM8990, an Interrupt bit can be reset by writing a 1 to the applicable bit in Register R18. However, if the jack detect input is still asserted, then the Interrupt event will continue to be flagged, even though no new event has occurred. In order to overcome this, and also to enable a separate Interrupt to be generated at the next transition of the jack detect input, the polarity of the GPIO1 should be reversed after a jack detect event has been indicated. The polarity is reversed by inverting the GPIO_POL[0] bit. Following this polarity change, the Interrupt can be cleared by writing to the GPIO1 status bit GPIO_STATUS[0]. After these actions, the device is primed to generate a subsequent Interrupt event on the next transition of the GPIO1 input.

APPLICATION SUPPORT

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