WAN_0202

Guidelines on How to Use W-CSP Packages and Create Associated PCB Footprints

INTRODUCTION

The Wolfson Wafer level ChipScale Package (W-CSP) is a die-sized package, which obtains electrical contact via solder bumps on the bottom surface of the device to a Printed Circuit Board (PCB). But it differs from Ball Grid Array (BGA) package by using Redistribution Layer (RDL) instead of bonding wire to connect the die pads.

This Application note sets out to explain some of the issues related to the design of a PCB footprint for the W-CSP package and then goes on to describe practical considerations when soldering the device to a PCB.

PACKAGE DIMENSIONS

The first thing to consider when creating a W-CSP footprint is the package drawing for the device. Wolfson uses a number of different W-CSP packages based on JEDEC specifications as follows in Table 1. Current W-CSP package I/O designs include from sixteen up to 42 solderable terminals but the max terminal count is possibly increasing to 105. See Figures 1 – 4. Package dimensions are shown in Figures 5 – 8. The dimensions of the packages are, at time of document release, as follows. Please refer to the individual datasheets for the most current issue of the package dimensions.

SIZE	PIN	BALL PITCH
1.640mm×1.640mmX0.7mm	16	0.4mm
2.552mmX2.602MMX0.7mm	25	0.5mm
2.590mm×2.500mmX0.7mm	28	0.4mm
3.226mm×3.440mmX0.7mm	42	0.5mm

Table 1 WLCSP Package Range

Figure 1 16 PIN WLCSP Package

Figure 2 25 PIN W-CSP Package

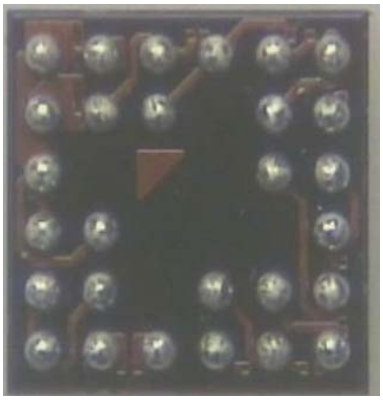
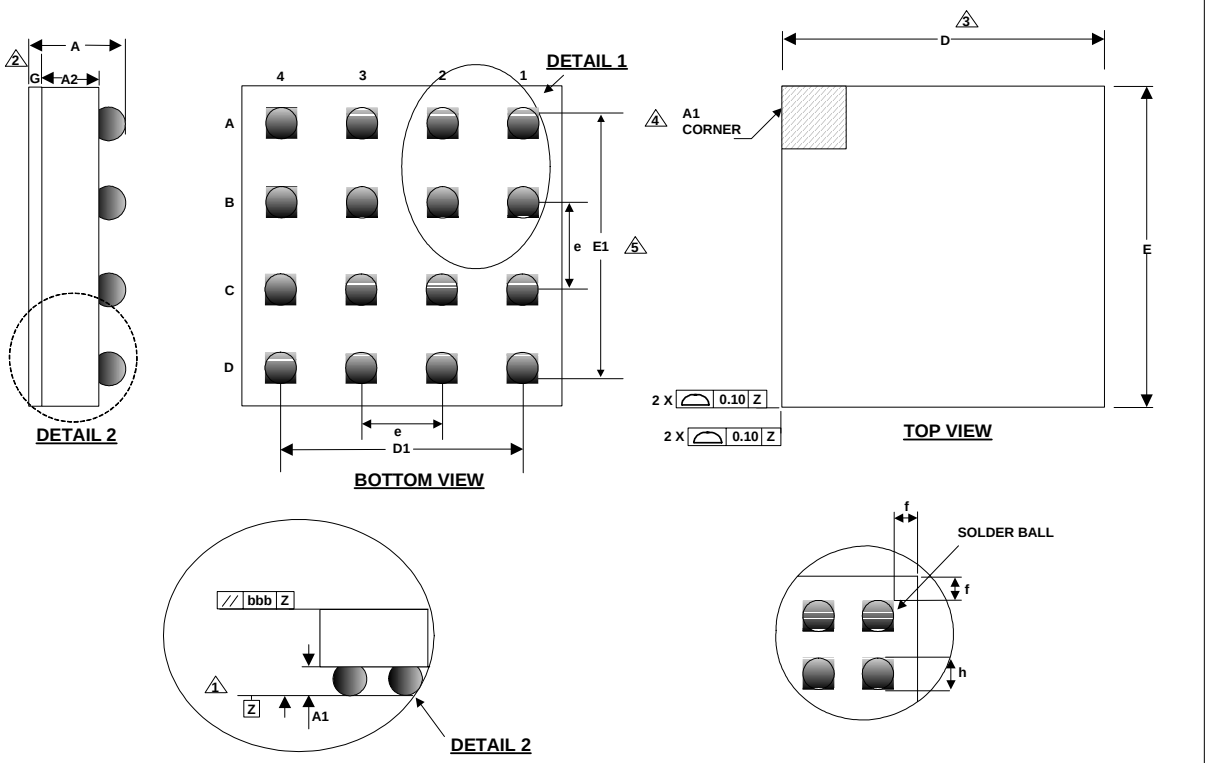


Figure 3 28 PIN W-CSP Package

Figure 4 42 PIN W-CSP Package

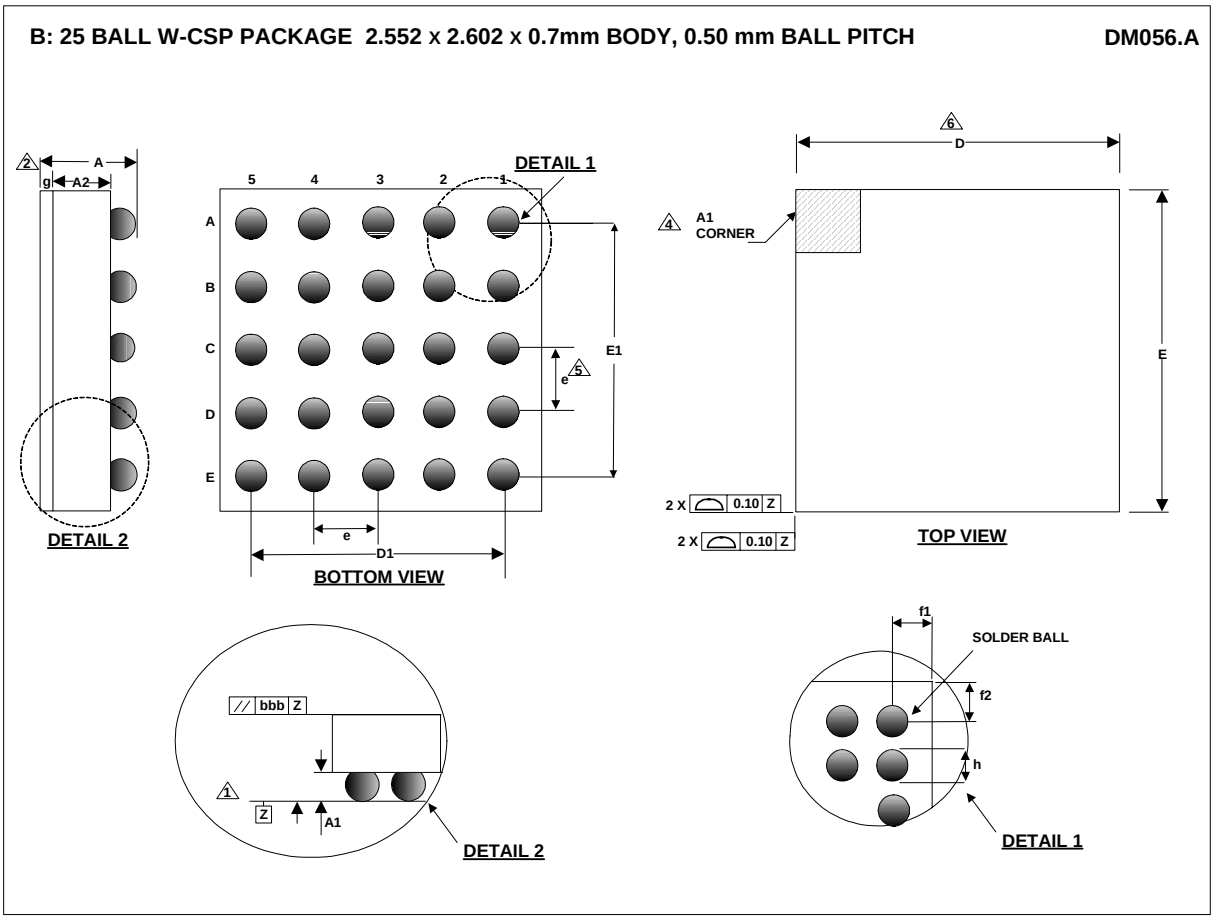
B: 16 BALL W-CSP PACKAGE 1.640 x 1.640 x 0.7mm BODY, 0.40 mm BALL PITCH **DM052.A**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.615	0.7	0.785	
A1	0.195	0.220	0.245	
A2	0.385	0.410	0.435	
D		1.640 BSC		
D1		1.200 BSC		
E		1.640 BSC		
E1		1.200 BSC		
e		0.400 BSC		5
f	0.091			
g	0.035	0.070	0.105	
h		0.260 BSC		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1' AND BACKSIDE COATING.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

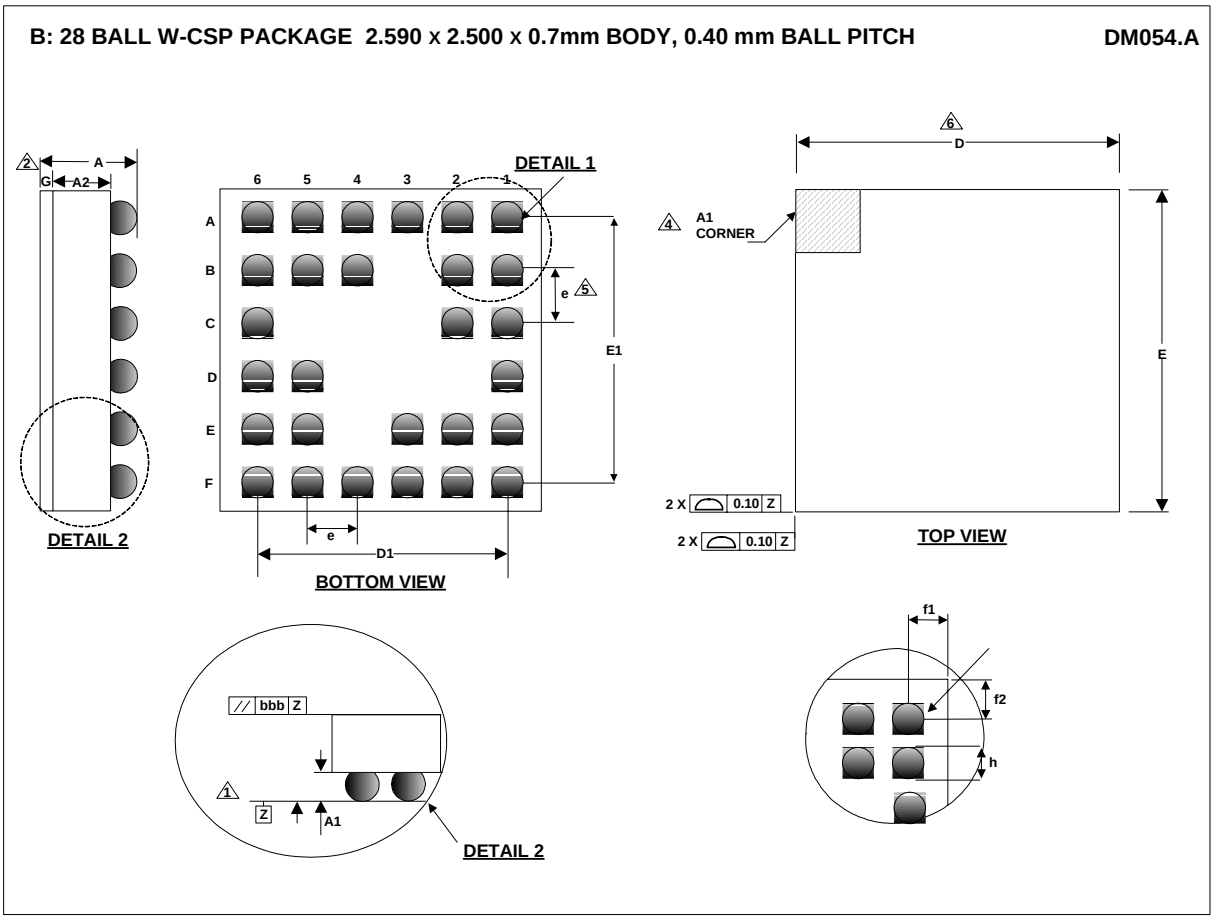
Figure 5 16 pin W-CSP Package



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.615	0.7	0.785	
A1	0.225	0.250	0.275	
A2	0.355	0.380	0.405	
D		2.552 BSC		
D1		2.00 BSC		
E		2.602 BSC		
E1		2.00 BSC		
e		0.50 BSC		5
f1	0.266 BSC			
f2	0.291 BSC			
g	0.035	0.070	0.105	
h		0.314 BSC		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1' AND BACKSIDE COATING.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

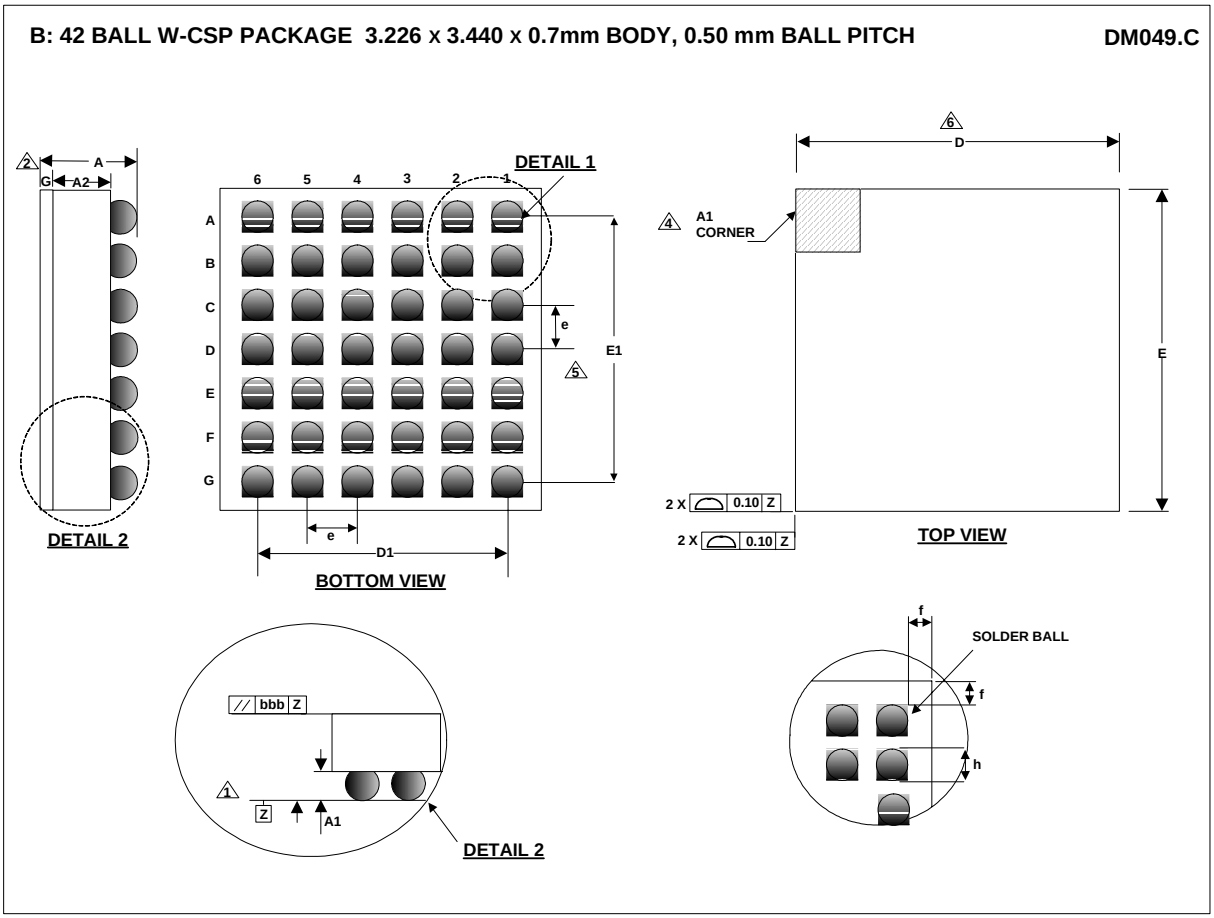
Figure 6 25 pin W-CSP Package



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.615	0.7	0.785	
A1	0.195	0.220	0.245	
A2	0.385	0.410	0.435	
D		2.590 BSC		
D1		2.000 BSC		
E		2.500 BSC		
E1		2.000 BSC		
e		0.400 BSC		5
f1	0.275			
f2	0.230			
g	0.035	0.070	0.105	
h		0.260 BSC		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1' AND BACKSIDE COATING.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

Figure 7 28 pin W-CSP Package



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.615	0.7	0.785	
A1	0.225	0.250	0.275	
A2	0.355	0.380	0.405	
D		3.226 BSC		
D1		2.500 BSC		
E		3.440 BSC		
E1		3.00 BSC		
e		0.50 BSC		5
f	0.060 BSC			
g	0.035	0.070	0.105	
h		0.315 BSC		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1' AND BACKSIDE COATING.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
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Figure 8 42 pin W-CSP Package

PACKAGE CONSTRUCTION

A cross-section of a typical RDL W-CSP is given in Figure 9.

RDL W-CSP construction consists of:

- Die with bond pad and original passivation
- Passivation 1
- Metallization etch (RDL metal) to move solder bumps from peripheral bond pads to any bump array pattern
- Passivation 2
- Under Bump Metal (UBM) contact
- Ball drop 250/300µm solder sphere (solder composition: SnAg(3%)Cu(0.5%))

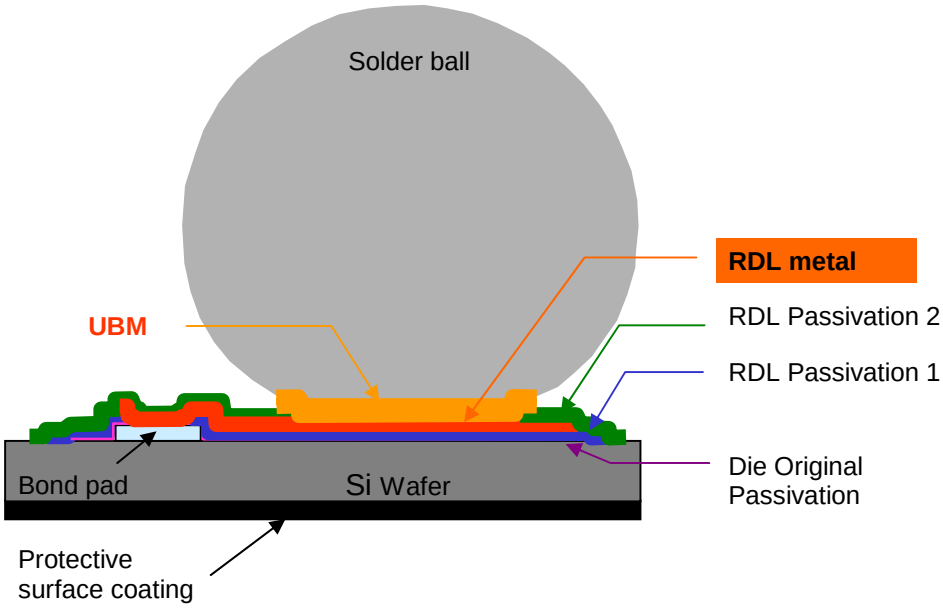

Figure 9 RDL W-CSP Cross-Section

PCB DESIGN CONSIDERATIONS

The PCB design rules when using the CSP packages are fundamentally no different to those for BGA devices of the same pitch. The most important considerations are those effects that occur during the PCB assembly process, which do affect the PCB land layout.

It is recommended that the CSP device is not mounted in an area of the board that is subject to high degrees of mechanical stress.

ROUTING OF TRACES

Routing strategy for CSP devices will depend upon the PCB technology being used and the volume in which they are being manufactured. Best practice for high assembly yield and minimum component footprint is a “via in pad” approach with a flat, filled microvia to an inner layer where the traces can be fanned out. Where the device pitch and available technology permit a “dog-bone” approach may also be used where the signal is tracked out to an adjacent via down to an inner layer (or opposite side of PCB).

The trace-width for connecting to CSP pads (either for dog-bone or tracking directly out on top layer) should be a maximum of half the pad diameter wherever possible. Exceptions may need to be made for power and ground or other signals that are high current or are sensitive to voltage drop.

UNDERFILL

Underfill can affect the mechanical reliability of the die and substrate assembly, for example, board level mechanical performance during bending, vibration, drop testing and thermal cycling. Underfill material can affect the solder joints thermal cycle life. Wolfson performs die and board level CSP qualification without the use of underfill.

CSP FOOTPRINTS DIMENSIONS

The actual PCB footprint used for a CSP device will depend on the intended assembly process. It is recommended that footprint design be carried out with reference to IPC-7351 (latest revision) and the assembler’s recommendations.

SOLDER MASK AND STENCIL DESIGN CONSIDERATIONS

Non-Solder Mask Defined (NSMD) pads are recommended for “via in pad” routing on CSP devices. Solder Mask Defined (SMD) pads may be used as an alternative. The CSP footprint should exclusively use either NSMD or SMD pads, the two types should never be mixed on the same package.

For effective solder paste release it is recommended that the stencil aperture be square with rounded corners (25µm radius) and trapezoidal sidewalls (larger opening to bottom side).

CSP DEVICE HANDLING

Due to CSP devices are silicon level packages rather than plastic encapsulated IC packages, CSP devices are more easily damaged than other IC packages. It is recommended that a vacuum nozzle be used to pick the device up in both manual and automated assembly. If tweezers need to be used to lift or position a device they should always be plastic rather than metal.

SOLDER PASTE RECOMMENDATIONS AND REFLOW PROFILE

Due to the size, pitch and depth of the stencil apertures for the W-CSP package it is recommended that type 4 no-clean solder pastes be used for printing. For reflow it is recommended an IR or Forced Convection system be used or a combination system of IR and Forced Convection. For further information on soldering, please refer to WAN_0158.

INSPECTION OF SOLDER JOINTS AFTER REFLOW

Due to the pad layout of the W-CSP the solder joints are formed underneath the package and are not visible. It is recommended that to ensure the joints are soldered sufficiently X-ray inspection be utilized whenever possible. Visual inspection may be used for a cursory inspection to ensure that there is no obvious solder bridging.

Shown below in Figure 10 is a typical x-ray inspection of the Wolfson 42-pin W-CSP Daisychain part on test board.

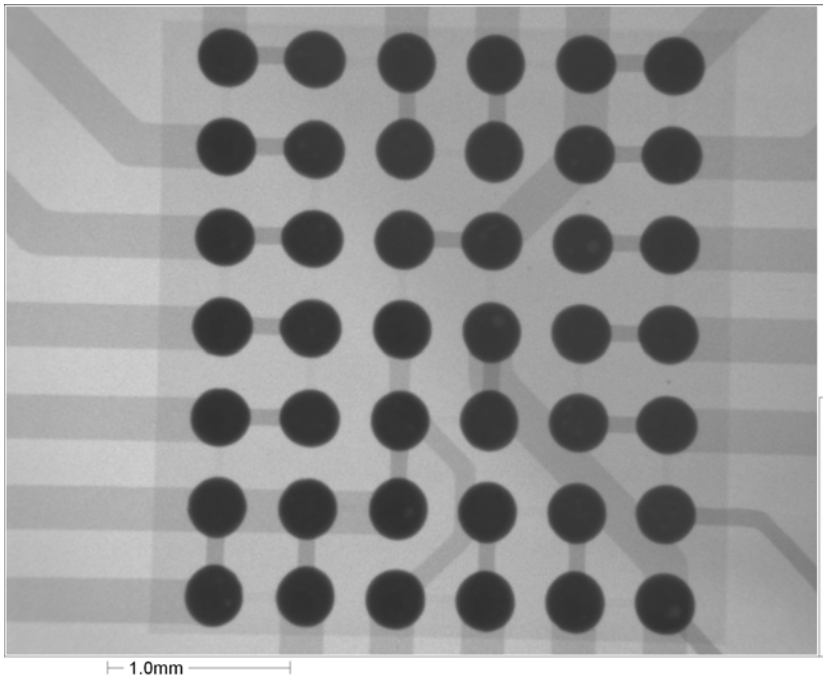

Figure 10 X-Ray Inspection of 42 pin W-CSP Daisychain Part on Test Board

As can be seen the solder has reflowed to form acceptable joints and there is minimal voiding in the solder joints, also there is no bridging visible between the joints. X-Ray inspection can also be useful in highlighting possible process problems such as solder balling and voiding which are often indications of poorly optimized reflow profiles.

W-CSP REWORK

Wolfson does not recommend any rework on W-CSP part itself.

APPLICATION SUPPORT

If you require further information or require technical support, please contact Wolfson Microelectronics Applications group through the following channels:

Email: apps@wolfsonmicro.com
Telephone: (+44) 131 272 7070
Fax: (+44) 131 272 7001
Mail: Applications at the address on the last page.

or contact your local Wolfson representative.

Additional information may be made available from time to time on our web site at:
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