

WM8224 Supply Current Ramp When Clocks Stopped

INTRODUCTION

This document details a condition where the analogue supply current (I_{AVDD}) ramps up when the MCLK or the VSMP clocks are stopped on the WM8224.

THE ISSUE

When the WM8224 is powered up and the MCLK or the VSMP clocks are not applied to the device, the analogue supply current (I_{AVDD}) slowly ramps up from around 69mA to around 93mA. The VRLC, VRX, VRT and VRB output voltages also increase very slightly, by around 0.2-0.4%.

When the MCLK and the VSMP clocks are applied to the WM8224, the analogue supply current (I_{AVDD}) increases to the active current of around 115mA and the device functions normally.

This effect can also be seen if the MCLK or the VSMP clocks are stopped for an extended period of time after/during operation. Refer to graph in Figure 1 showing the analogue supply current (I_{AVDD}) versus time.

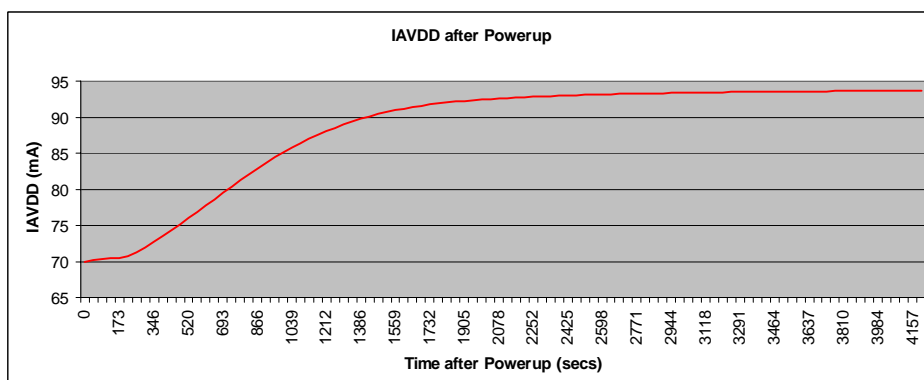


Figure 1 Analogue Supply Current (I_{AVDD}) vs Time

This time period is relatively long and varies between devices. In the example of Figure 1, the time is about 2400s (40mins) to reach within a few percent of the maximum level.

CONCLUSION

The cause of this is the switched capacitor nature of the device. It is recommended that the device is powered down, or the PGAs disabled, if the device is not clocked for significant periods of time to prevent this condition from occurring.

This condition does not damage the device and the device will recover and operate normally when the clocks are reapplied.

APPLICATION SUPPORT

If you require more information or require technical support, please contact the Wolfson Microelectronics Applications group through the following channels:

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