WAN-0236

Recommendations on Soldering a Dual Row QFN Package to a PCB

INTRODUCTION

The Quad Fine Pitch No Leads (QFN) package is a leadless plastic package, which obtains electrical contact via lands on the bottom surface of the device. Its compact nature and low profile makes the QFN package ideal for designs where space considerations are at a premium. This small size is one of the main reasons why the QFN package is chosen for Wolfson Microelectronics devices for portable applications.

In addition to the bottom surface mounted pins, the other distinguishing feature of this package type is the exposed die paddle on the bottom side of the device. This paddle is used to add extra strength in PCB mounting and to conduct heat more efficiently away from the die. The paddle is also bonded as an analogue ground so it should be connected to the analogue ground of the PCB it is mounted onto.

This Application note sets out to explain some of the practical considerations when soldering the QFN device to a PCB.

SOLDER MASK AND STENCIL DESIGN CONSIDERATIONS

The complexity of the QFN footprint due to the inclusion of the die paddle means that the solder mask used during assembly will be of equal complexity. To prevent the solder of the die paddle transgressing onto the land pads during reflow, the solder mask should overlap the die paddle outer edges by at least 100um. This overlap will prevent transgression to the land pads even in the worst case scenario.

As per Figure 1, the vias should be left bare or untented. This minimizes the presence of voids and prevents outgassing during reflow. Additionally, if the application permits the use of plated through hole vias, then the bottom side soldermask should have a clearance around the vias equal in size to the one on the top side.

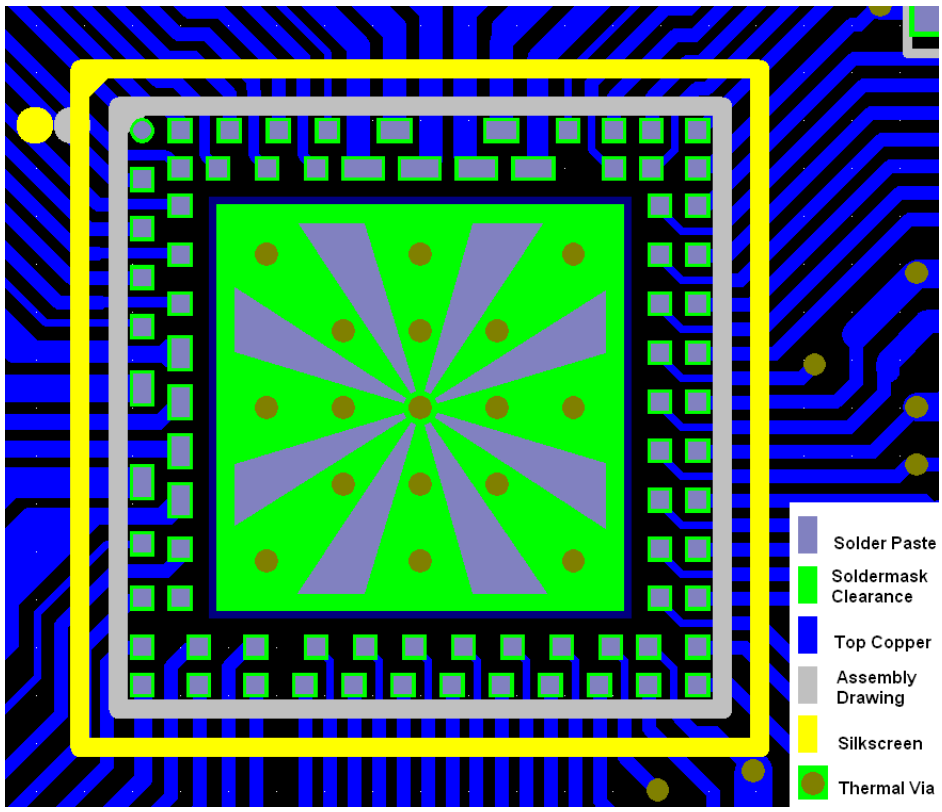

Figure 1 81 Pin 8x8 Dual-Row QFN Design Guide

STENCIL DESIGN FOR PERIMETER PADS

The stencil should be 1:1 or 90% of the PCB pad size and should be laser cut for accuracy and electro-polished which helps in smoothing the stencil sidewalls. The recommended stencil thickness used is 0.075mm to 0.127mm (0.003in to 0.005in) and the sidewalls of the stencil openings should be tapered approximately 5 degrees to facilitate better paste release.

DISSECTION OF THE DIE PADDLE SOLDER PASTE STENCIL

If the solder paste coverage of the die paddle is too big, out-gassing occurs during the reflow process which may cause defects (splatter, solder balling). As per Figure 1, dividing the die paddle into smaller screen openings reduces the risk of solder voiding and allows the solder joints for the smaller terminal pads to be at the same height as the larger ones. Figure 1 also shows how the solder paste stencil pattern can minimize the risk of the solder paste wicking down untented vias.

SOLDER PASTE RECOMMENDATIONS AND REFLOW PROFILE

Due to the size, pitch and depth of the stencil apertures for the QFN package it is recommended that type 3 no-clean solder pastes be used for printing. For reflow it is recommended an IR or Forced Convection system be used or a combination system of IR and Forced Convection. For further information on soldering, please refer to WAN_0158.

INSPECTION OF SOLDER JOINTS AFTER REFLOW

Due to the pad layout of the QFN the solder joints are formed underneath the package and are not visible. It is recommended that to ensure the joints are soldered sufficiently x-ray inspection be utilized whenever possible. Visual inspection may be used for a cursory inspection to ensure that there is no obvious solder bridging.

Shown below in Figure 2 is a typical x-ray inspection of the Wolfson 32-pin QFN.

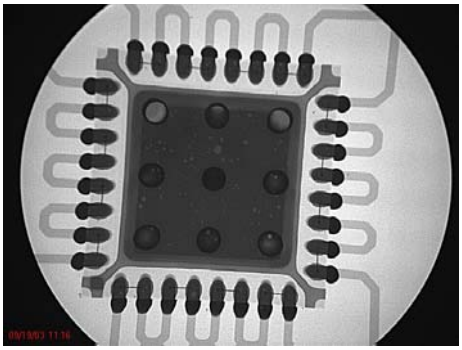

Figure 2 X-Ray Inspection of 5mm×5mm 32-pin QFN

As can be seen, the solder has reflowed to form acceptable joints and there is minimal voiding in the thermal die paddle and pad solder joints, also there is no bridging visible between the joints. X-Ray inspection can also be useful in highlighting possible process problems such as solder balling and voiding that are often an indication of poorly optimized reflow profiles.

APPLICATION SUPPORT

If you require further information or require technical support, please contact Wolfson Microelectronics Applications group through the following channels:

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