Interfacing WM72xx Digital Microphones

INTRODUCTION

Cirrus Logic's WM72xx DMIC (Digital Microphone) offers best in class, low noise performance with PDM (Pulse Density Modulation) output. As the digital interface provides direct connection to the CODECs digital domain, the DMIC requires less external components and PCB area. This provides a simplified interface connection and gives a higher robustness to system noise interference compared to an analogue microphone interface.

Cirrus Logic provides a wide range of audio CODECs with single or multiple DMIC input interfaces. Connectivity is achieved using a simple 2 wire CLK and DATA interface. As each DMIC interface supports up to 2 microphones, the DMIC interface is more flexible and makes it easier to implement additional microphones to support stereo recording, ambient noise cancellation, microphone array or beam forming features into single DMIC voice recording applications. Further information on system solutions with Cirrus's CODECs and Microphones is available in WAN_0225.

ADVANTAGE	DIGITAL MICROPHONE	ANALOGUE MICROPHONE
Noise performance	Digital Interface signals are more robust to system noise coupling.	Careful design consideration required for the sensitive analogue interface signals.
External components	Direct interface to CODECs with digital microphone interface, significant saving on PCB area with more microphones in system	Each input supports only one microphone with DC isolation capacitor required.
Application	Suitable for one or more microphones in the system. Flexibility to add additional microphones into the application.	More suitable for single microphone applications.

Table 1 Digital vs Analogue Microphone

This application note details the interface of the DMIC to CODEC to achieve optimum microphone performance in the system.

PDM SIGNAL

The DMIC incorporates a sigma-delta architecture and hence outputs a 1-bit PDM signal to represent the acoustic input signal. A typical PDM representation of an analogue sine wave is shown in Figure 1. High occurrences of '1' represents the positive cycle and vice versa for the negative cycle with higher density of '0's. In other words, the amplitude of the analogue signal is encoded by the density of bits. The DMIC interface supports single or dual WM72xx DMICs with separate PDM streams multiplexed together on different clock edges.

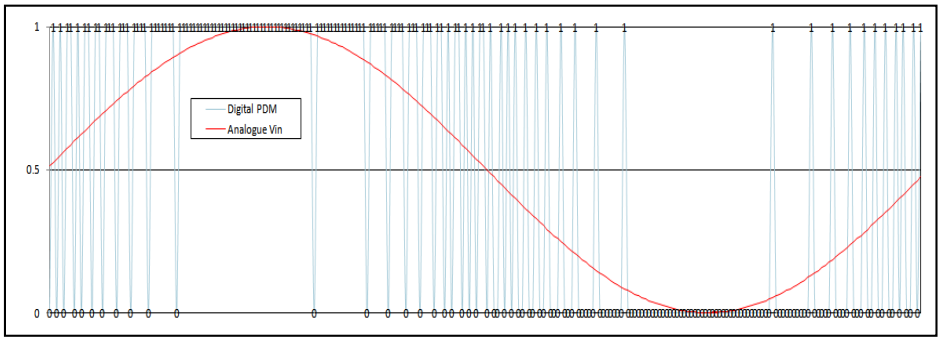

Figure 1 PDM Representation of Analogue Input Sine Wave

The DMIC interface with PDM output is much more robust and insensitive to noise on the PCB as the critical analogue domain is shielded inside the DMIC. The analogue signal from the MEMS transducer in the DMIC is sampled at high speed into 1 bit ADC and PDM output at the applied DMIC CLK rate. The estimated signal bandwidth (BW) available from the DMIC, PDM output is:

BW = Fclk / 100

Where:

BW = signal bandwidth available from PDM

Fclk = DMIC input CLK frequency

Given the microphone internal oversampling rate is 50FS

The DMIC interfaces directly to the CODECs digital domain without any analogue pre amplifier or gain stage required. The PDM signal is down sampled by the decimation filters in the CODEC into PCM (Pulse Code Modulation) at much lower sampling frequency with n bits (n > 1 bit) in audio samples to represent the signal amplitude.

The DMIC CLK frequency is in the range 1 to 3.25MHz and will depend on CODEC internal clocking scheme. However, CODECs support a standard sampling clock frequency for PCM output. Therefore, the DMIC CLK frequency must be chosen to support the targeted signal bandwidth in PCM.

For example, A CODEC ADC sampling at 48kHz, the PCM signal bandwidth is BW = 48kHz / 2 = 24kHz. Therefore, the minimum DMIC CLK frequency required Fclk(min) = 2.4MHz. If the DMIC is given 1.536MHz DMIC CLK, the available PDM bandwidth is limited to 15.36kHz; the limited bandwidth in PDM will be translated into higher noise floor observed in the PCM signal from 15.36 to 24kHz.

CONNECTION TO CODECS

Figure 2 shows the mono DMIC interface connection to the CODEC. The DAT (Data) pin outputs data on the rising or falling edges of the incoming CLK (Clock) signal (depending on the LRSEL pin). The DAT output is high impedance when not outputting logic data at the other CLK edges. Note that, due to high output impedance and the line capacitance, the DAT line typically shows the same logic status as when it is enabled on the previous clock cycle. In other words, same logic status on DAT appears for both rising and falling CLK edges with mono DMIC.

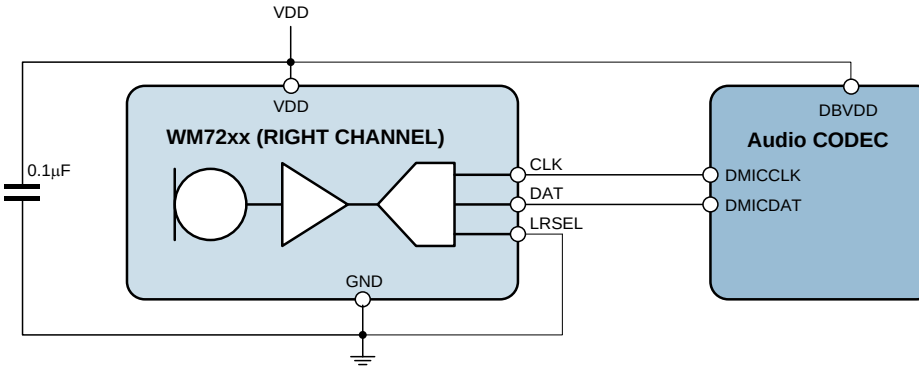

Figure 2 Mono Digital Microphone Interface

There are two ADCs in the CODEC, sharing the same input DAT line. If both ADCs are enabled, then both ADCs will register the same logic status from the mono digital microphone as detailed earlier. It is therefore recommended to enable only one ADC (consistent with the LRSEL channel selection), in order to avoid stereo recording of two ADCs from the mono digital microphone.

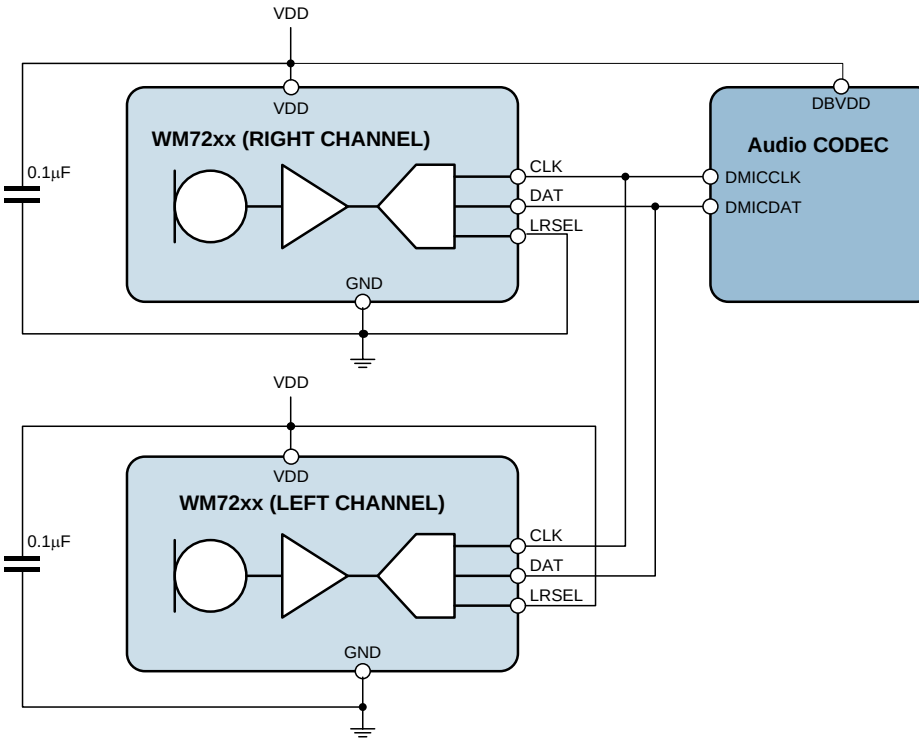

Figure 3 Stereo Digital Microphone Interface

The output characteristic of the DMIC enables the output of two microphones to be connected together in a stereo configuration as in Figure 3. The data from one microphone is interleaved with the data from the others. The Left channel is transmitted following the rising CLK edge when LRSEL = 1. Therefore the Left channel should be sampled by the CODEC on the falling edge. Similarly when LRSEL = 0, the DMIC is set as right channel. In this case, the right channel DMIC is sampled by the CODEC on the rising CLK edge. The output data on the stereo DMIC configuration is summarised in Figure 4.

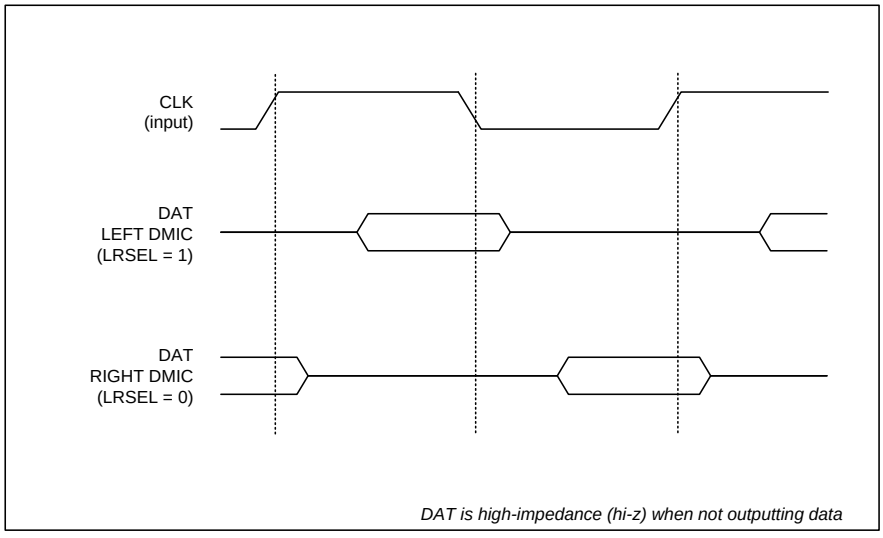

Figure 4 Output Data on Stereo DMIC Configuration

The design ensures DMIC data output is always delayed compared to the output disable into high impedance mode, care must be taken to ensure the CLK and DAT tracks to the two microphones are equal length to get the same delays, to secure a safe timing margin when two microphone are used in the stereo recording.

SUPPLY DECOUPLING

The DMIC VDD pin should be powered at the same supply voltage level as the CODEC DBVDD (Digital Buffer Voltage) to ensure both the CLK and DAT signals are operating within the digital voltage limits. As common practice in digital design, decoupling capacitors are required for each component on the same power supply voltage as DMIC VDD to ensure effective noise filtering.

For an effective decoupling scheme, the DMIC GND pin should be connected to a solid ground plane and share the same ground plane as the CODEC. As a general guideline a 0.1µF decoupling capacitor is recommended for DMIC VDD pin. The decoupling capacitor provides low impedance between the power and solid ground plane. Therefore, this should be positioned close to the VDD pin of each DMIC in a stereo microphone application. A ceramic 0.1µF capacitor with X7R dielectric or better is recommended.

SIGNAL ROUTING

The DMIC can be directly surface mounted to the same board as the CODEC, mounted separately on flexible PCB or small peripheral board for strategic acoustic considerations. In any case, the track or transmission line for the CLK and DAT will have several sections, each with different characteristic impedance (Z_0). Since any changes in impedance along the track will cause reflection, the circuit will often generate multiple reflections with fast CLK edges from the CODEC, which can result in the incorrect decoding of PDM signal or overall performance degradation in the signal chain. Therefore careful consideration of CLK and DAT routing are recommended to avoid ringing in the DMIC interface.

As a general rule for digital audio interfaces, transmission line effects will be evident on PCB tracks whose length is greater than 50mm. The characteristic impedance of such a track, based on signal rise/fall times of 2ns-6ns, will be in the range 33Ω to 150Ω.

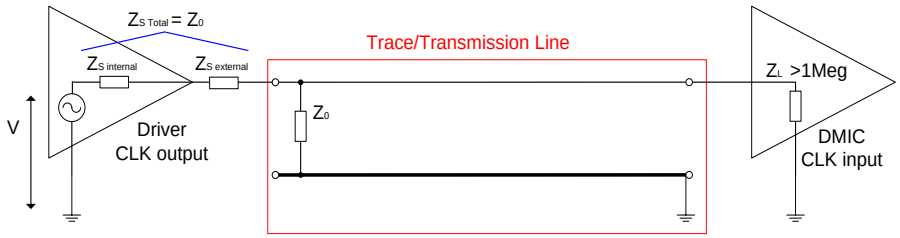

Figure 5 Source Termination of Single DMIC Circuit

For a single DMIC application with irregular CLK edges observed on oscilloscope, a series resistor on the CLK line needs to be added close to the CODEC in order to match the source impedance ($Z_{s\ Total}$) to the track impedance. The value of the external resistor is chosen according to the output impedance of the CLK source (Z_s) and the characteristic impedance (Z_0) of the transmission line as follows:

$$Z_{s\ Total} = Z_{s\ Internal} + Z_{s\ External} = Z_0$$

In other words,

$$Z_{s\ External} = Z_0 - Z_{s\ Internal}$$

For application design incorporating ribbon cable or flexible PCB interconnection for the DMIC interface, the GND track should be routed next to the CLK track in order to secure uniform characteristic impedance (Z_0) along the track. Source termination is recommended to minimize the reflection and potential EMI from high frequency components due to fast clock edges.

As each DMIC interface supports up to two microphones, Figure 6 shows the source termination scheme for stereo microphone configuration. Two equal and smaller value external resistors are required as follows:

$$Z_{s\ Total} = 2 \times Z_{s\ Internal} + Z_{s\ External} = Z_0$$

In other words,

$$Z_{s\ External} = Z_0 - 2 \times Z_{s\ Internal}$$

The stereo source termination scheme works when the two CLK tracks are of equal length with the same characteristic impedance. Serpentine track line is recommended for the DMIC populated closer to the source to ensure equal delays applied to two DMICs.

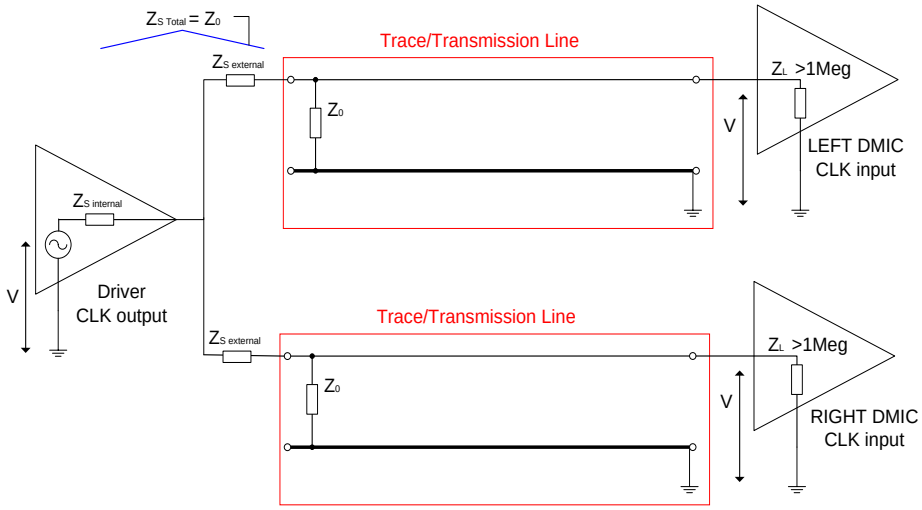

Figure 6 Source Termination for Stereo Microphone Interface

SUMMARY

The DMIC interface offers seamless integration with Cirrus CODECs. With the design consideration as discussed in this application note, the system designer can take full advantage of the Cirrus DMIC to meet the most demanding acoustic design challenges in the system application.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.