

## Guidelines on How to Use QFN Packages and Create Associated PCB Footprints

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### INTRODUCTION

The Quad Fine Pitch No Leads (QFN) package is a leadless plastic package, which obtains electrical contact via lands on the bottom surface of the device. Its compact nature and low profile makes the QFN package ideal for designs where space considerations are at a premium. This small size is one of the main reasons why the QFN package is chosen for Wolfson Microelectronics devices for portable applications.

In addition to the bottom surface mounted pins, the other distinguishing feature of this package type is the exposed die paddle on the bottom side of the device. This paddle can be used to add extra strength in PCB mounting and to conduct heat more efficiently away from the die. The paddle may in future be bonded as a further analogue ground and so it is recommended that it be connected to the analogue ground of the PCB it is mounted to. The Chip On Lead Quad Fine Pitch No Leads (COL QFN) package has no paddle.

This Application note sets out to explain some of the issues related to the design of a PCB footprint for the QFN package and then goes on to describe practical considerations when soldering the device to a PCB.

### PACKAGE DIMENSIONS

The first thing to consider when creating a QFN footprint is the package drawing for the device. Wolfson uses a number of different QFN packages based on JEDEC specifications as follows:

| SIZE    | PIN | WOLFSON TYPE |
|---------|-----|--------------|
| 4MMx4MM | 24  | C            |
| 4MMx4MM | 28  | A AND C      |
| 5MMx5MM | 28  | A            |
| 5MMx5MM | 32  | A AND C      |
| 6MMx6MM | 40  | C            |
| 7MMx7MM | 48  | C            |
| 7MMx7MM | 56  | C            |
| 9MMx9MM | 64  | C            |

Figure 1 QFN Package Range

The Wolfson QFN package currently has two types of lead termination features, these are as follows.

### WOLFSON TYPE A

The Wolfson Type A package is based on the JEDEC MO-220 specification with a slight modification on the pad design. In the Type A package there is mould compound round the bottom corner of the package (see arrow). After reflow a solder fillet between the PCB and the side of the package is not required; the side of the package is not required to be solderable. This is as defined in international standard IPC-A-610D. Refer to extract in the Appendix.

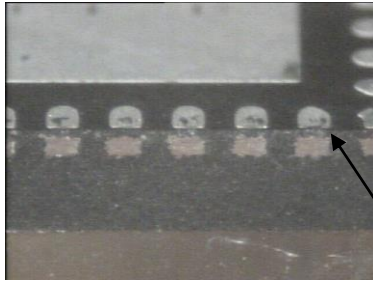


Figure 2 Type A QFN Package

### WOLFSON TYPE C

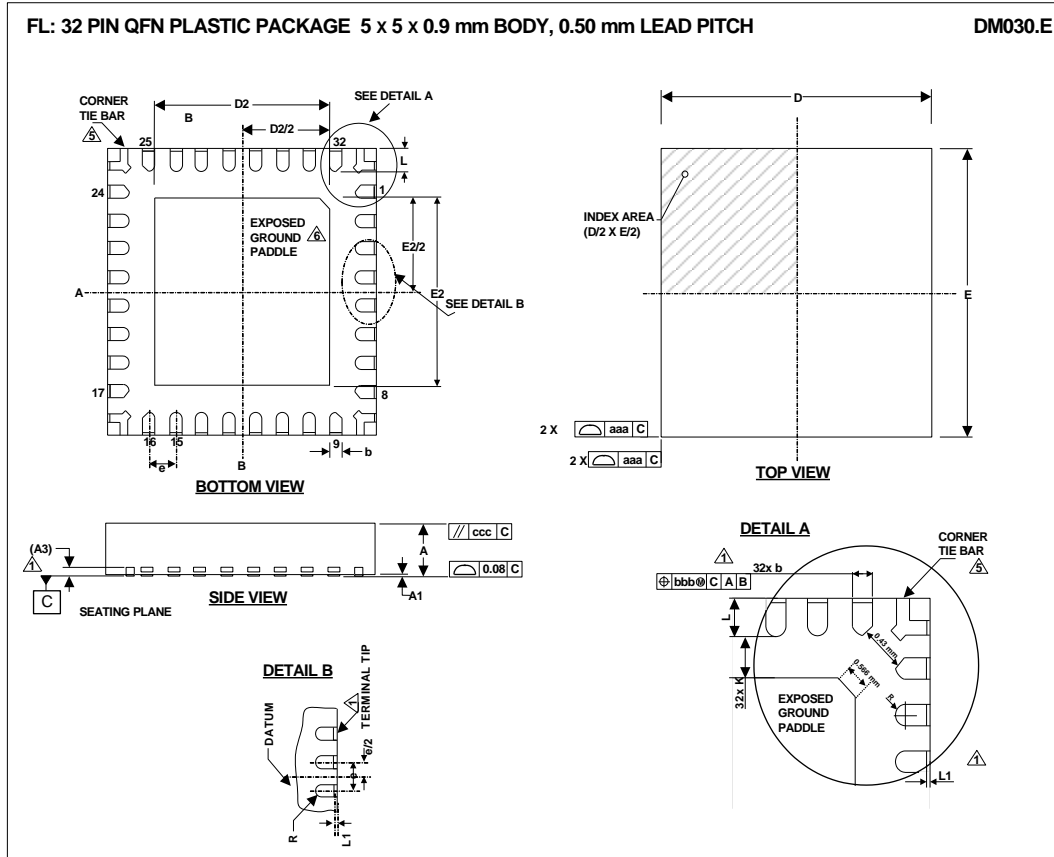
The Type C package is based on the JEDEC MO-220 specification with pads that are extended up the side of the package. After reflow a solder fillet between the PCB and the side of the package is not required; the side of the package is not required to be solderable. This is as defined in international standard IPC-A-610D. Refer to extract in the Appendix.



Figure 3 Type C QFN Package

The package type is dependant on the types of the part supplied and product family and can be found in the product data sheet. Figure 4 below shows an example of a package drawing for a 32pin 5mm x 5mm Type A package for illustration purposes only.

For the current package drawing for any Wolfson Microelectronics device please check the latest revision of the datasheet for the device in question. The current revision of the datasheet can be found at - [http://www.wolfsonmicro.com/resource\\_centre/products/](http://www.wolfsonmicro.com/resource_centre/products/)



| Symbols                                | Dimensions (mm)                 |         |      | NOTE |
|--|---------------------------------|---------|------|------|
|  | MIN                             | NOM     | MAX  |      |
| A                                      | 0.85                            | 0.90    | 1.00 |      |
| A1                                     | 0                               | 0.02    | 0.05 |      |
| A3                                     |                                 | 0.2 REF |      |      |
| b                                      | 0.18                            | 0.23    | 0.30 | 1    |
| D                                      | 4.90                            | 5.00    | 5.10 |      |
| D2                                     | 3.2                             | 3.3     | 3.4  | 2    |
| E                                      | 4.90                            | 5.00    | 5.10 |      |
| E2                                     | 3.2                             | 3.3     | 3.4  | 2    |
| e                                      |                                 | 0.5 BSC |      |      |
| L                                      | 0.35                            | 0.4     | 0.45 |      |
| L1                                     |                                 |         | 0.1  | 1    |
| R                                      | b(min)/2                        |         |      |      |
| K                                      | 0.20                            |         |      |      |
| <b>Tolerances of Form and Position</b> |                                 |         |      |      |
| aaa                                    |                                 | 0.15    |      |      |
| bbb                                    |                                 | 0.10    |      |      |
| ccc                                    |                                 | 0.10    |      |      |
| REF:                                   | JEDEC, MO-220, VARIATION VHHD-2 |         |      |      |

- NOTES:
- DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL PULL BACK FROM PACKAGE SIDE WALL. MAXIMUM OF 0.1mm IS ACCEPTABLE. WHERE TERMINAL PULL BACK EXISTS, ONLY UPPER HALF OF LEAD IS VISIBLE ON PACKAGE SIDE WALL DUE TO HALF ETCHING OF LEADFRAME.
  - FALLS WITHIN JEDEC, MO-220 WITH THE EXCEPTION OF D2, E2:
  - D2, E2: LARGER PAD SIZE CHOSEN WHICH IS JUST OUTSIDE JEDEC SPECIFICATION
  - ALL DIMENSIONS ARE IN MILLIMETRES
  - THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
  - SHAPE AND SIZE OF CORNER TIE BAR MAY VARY WITH PACKAGE TERMINAL COUNT. CORNER TIE BAR IS CONNECTED TO EXPOSED PAD INTERNALLY.
  - REFER TO APPLICATION NOTE WAN\_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.

**Figure 4 32 pin 5x5 QFN Package Wolfson Type A**

## PCB DESIGN CONSIDERATIONS

The PCB design rules when using the QFN packages are fundamentally no different to those for other more well known packages. The most important considerations are those effects that occur during the PCB assembly process, which do affect the PCB land layout.

The most obvious difference is the presence of a large thermal die paddle on the bottom side of the device. Concern is also often shown to the pull-off strength of the QFN device when simply using the pads to fix the package. For added strength and improved thermal dissipation characteristics, the die paddle should ideally be soldered to the PCB in addition to the pins.

## ROUTING OF TRACES

Traces should be routed straight out from the peripheral pads to a minimum of 500um beyond the device extremities. Traces should not be routed inwards to a via at the expense of all or part of the thermal die paddle as there would be a strong possibility of the via shorting to the die paddle. For QFN Type A packages traces from the corner pads should not be routed perpendicularly as there would be a strong possibility of the trace shorting to the corner tie bars. This corner area should also be free of other signal traces or copper plane areas that are connected to different ground planes than that of the die paddle. Figure 13 below, shows a good example layout where all of the above and below recommendations have been considered and adhered to.

## THERMAL DISSIPATION

To allow the heat generated through this large pad to dissipate, the area under the device may require the inclusion of a thermal landing on the component side of the PCB equal in size to the maximum size of the device thermal die paddle (it is also recommended to place a thermal landing on the opposite side of the PCB) connected to analogue ground using a number of thermal vias, approximately 0.33mm (0.013 inches) diameter. These thermal vias should be completely connected (flooded over) to the thermal landing(s) (as well as internal ground planes if using a multilayer PCB) and should not be confused with "thermal relief" or "web-constructed" vias which are designed with "spokes" to decrease thermal transfer through the PCB. The number of vias will depend upon device package size, but as a guide the pitch between the vias should be between 0.74mm and 1.27mm. In Figures 5 – 12 below, 3x3 vias are used for the packages. In Figure 13, the 9X9 package's size allows an additional 8 vias. Figures 5 - 13 are not to scale for the purpose of clarity.

QFN FOOTPRINTS DIMENSIONS

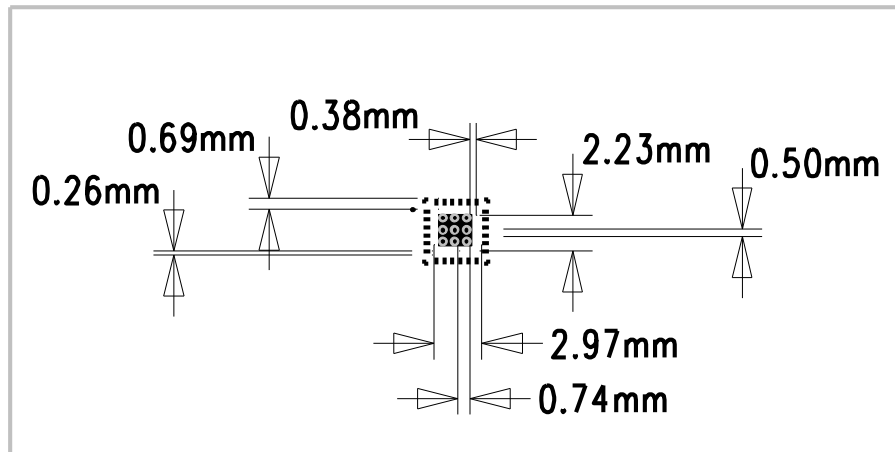


Figure 5 24 Pin 4x4 QFN Footprint

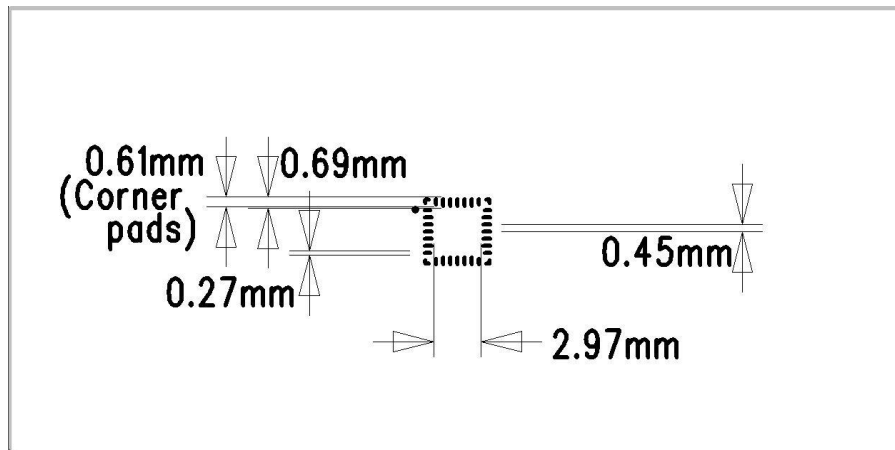


Figure 6 28 Pin 4x4 COL QFN Footprint

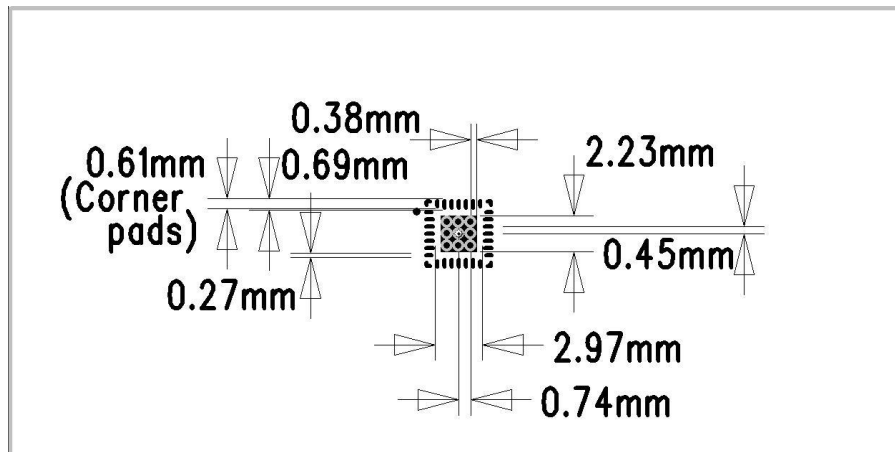


Figure 7 28 Pin 4x4 QFN Footprint

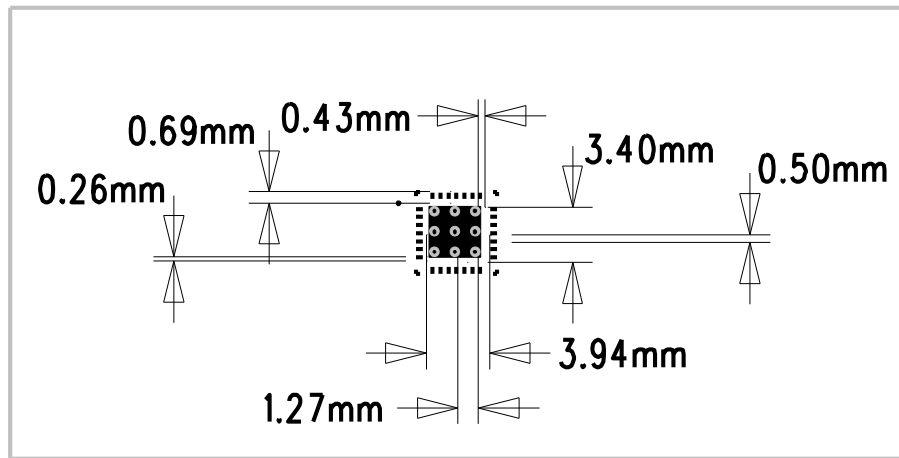


Figure 8 28 Pin 5x5 QFN Footprint

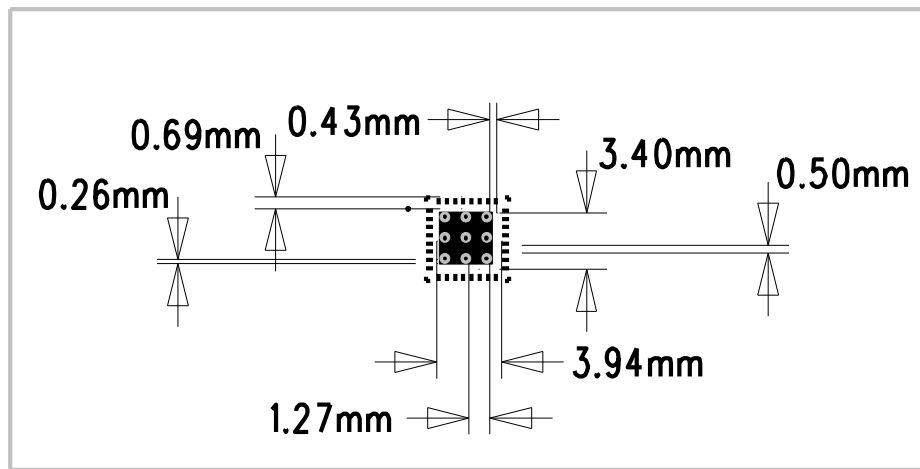


Figure 9 32 Pin 5x5 QFN Footprint

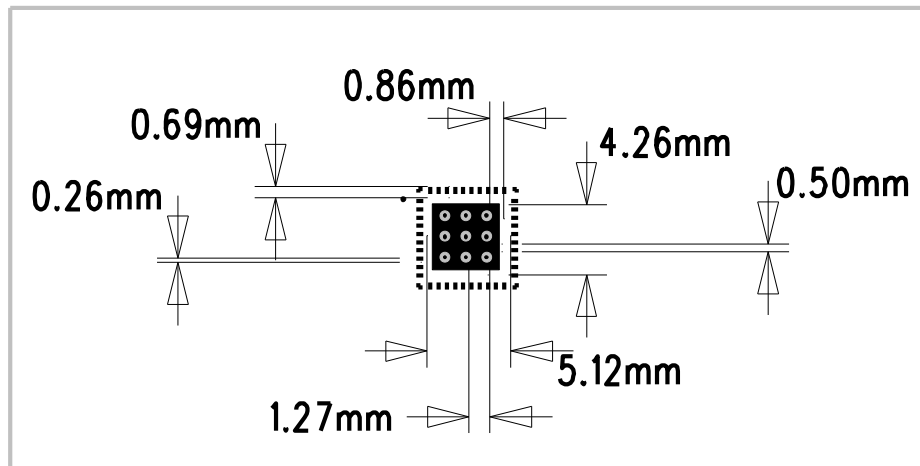


Figure 10 40 Pin 6x6 QFN Footprint

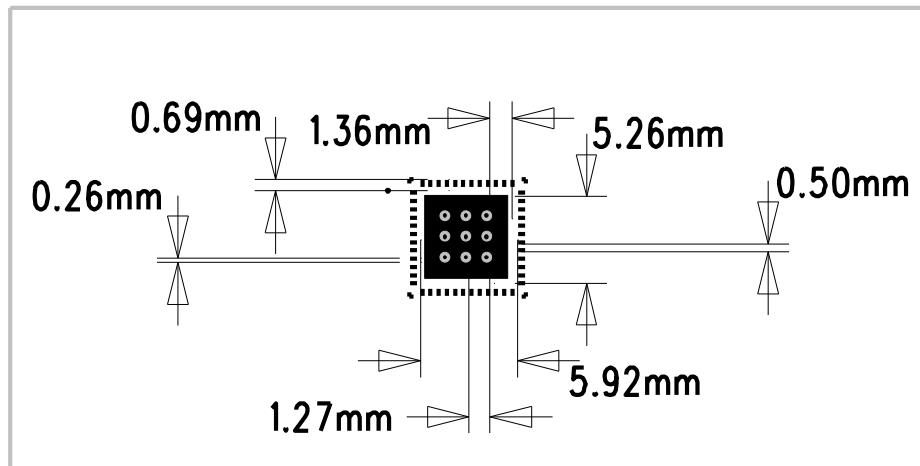


Figure 11 48 Pin 7x7 QFN Footprint

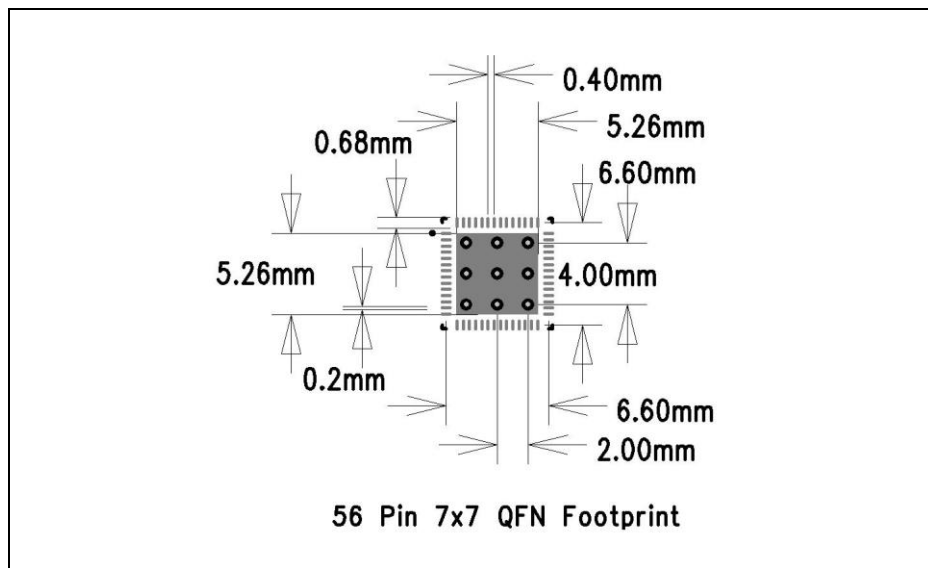


Figure 12 56 Pin 7x7 QFN Footprint

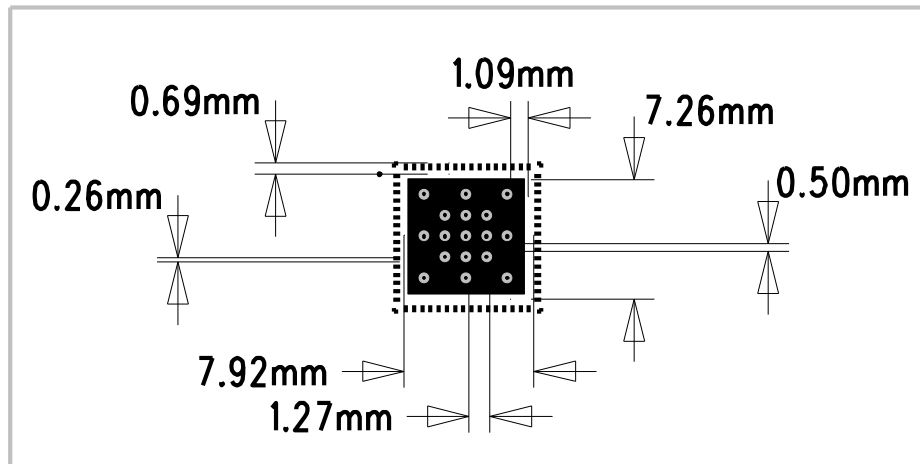


Figure 13 64 Pin 9x9 QFN Footprint

## SOLDER MASK AND STENCIL DESIGN CONSIDERATIONS

The greater complexity of the QFN footprint due to the inclusion of the die paddle also means that the solder mask used during assembly will be of equal complexity. To prevent the solder of the die paddle transgressing onto the land pads during reflow, the solder mask should overlap the thermal pad outer edges by at least 100µm. This overlap will prevent transgression to the land pads even in the worst case scenario.

As per Figure 14, the vias should be left bare or untented. This minimizes the presence of voids and prevents outgassing during reflow. Additionally, if the application permits the use of plated through hole vias, then the bottom side soldermask should have a clearance around the vias equal in size to the one on the top side.

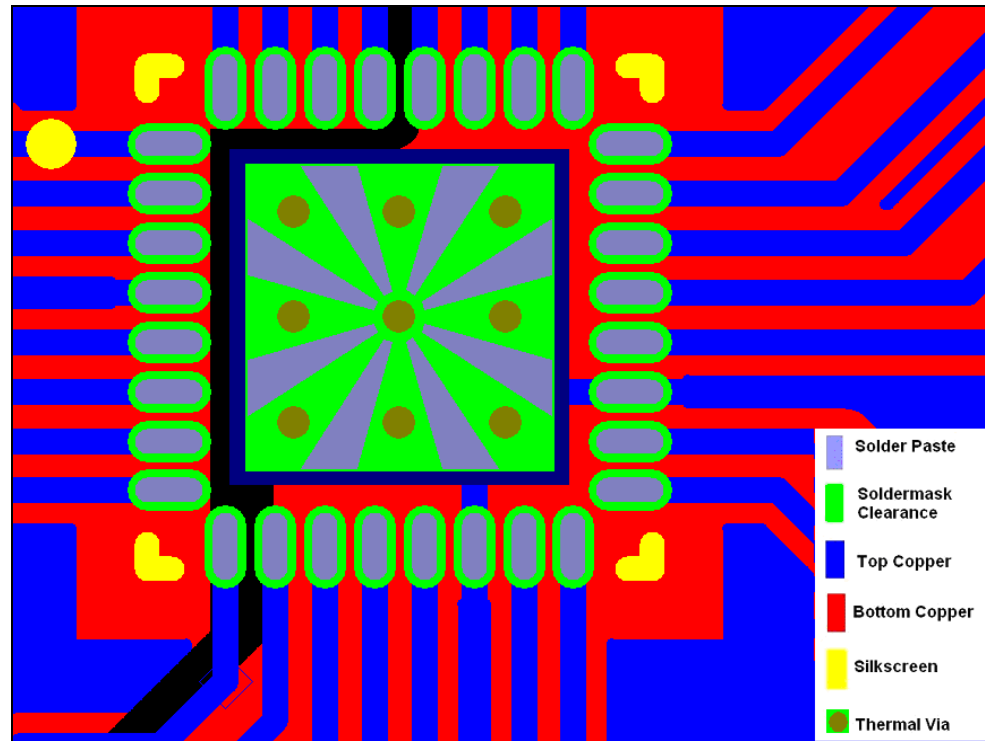


Figure 14 32 Pin 5x5 QFN Design Guide

### STENCIL DESIGN FOR PERIMETER PADS

The stencil should be 1:1 or 90% of the PCB pad size and should be laser cut for accuracy and electro-polished which helps in smoothing the stencil sidewalls. The recommended stencil thickness used is 0.075mm to 0.127mm (0.003in to 0.005in) and the sidewalls of the stencil openings should be tapered approximately 5 degrees to facilitate better paste release.

### DISSECTION OF THE DIE PADDLE SOLDER PASTE STENCIL

If the solder paste coverage of the thermal landing is too big, out-gassing occurs during the reflow process which may cause defects (splatter, solder balling). As per Figure 14, dividing the thermal landing into smaller screen openings reduces the risk of solder voiding and allows the solder joints for the smaller terminal pads to be at the same height as the larger ones. Figure 14 also shows how the solder paste stencil pattern can minimize the risk of the solder paste wicking down untented vias.

The COL QFN package has no Die Paddle.



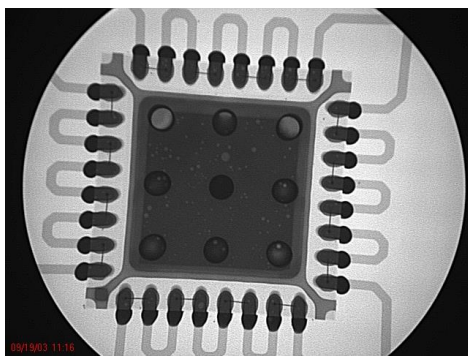
## SOLDER PASTE RECOMMENDATIONS AND REFLOW PROFILE

Due to the size, pitch and depth of the stencil apertures for the QFN package it is recommended that type 3 no-clean solder pastes be used for printing. For reflow it is recommended an IR or Forced Convection system be used or a combination system of IR and Forced Convection. For further information on soldering, please refer to Wan\_0158.

## INSPECTION OF SOLDER JOINTS AFTER REFLOW

Due to the pad layout of the QFN the solder joints are formed underneath the package and are not visible. It is recommended that to ensure the joints are soldered sufficiently x-ray inspection be utilized whenever possible. Visual inspection may be used for a cursory inspection to ensure that there is no obvious solder bridging.

Shown below in Figure 15 is a typical x-ray inspection of the Wolfson 32pin QFN.



**Figure 15 X-Ray Inspection of 5mmx5mm 32 pin QFN**

As can be seen the solder has reflowed to form acceptable joints and there is minimal voiding in the thermal die paddle and pad solder joints, also there is no bridging visible between the joints. X-Ray inspection can also be useful in highlighting possible process problems such as solder balling and voiding which are often an indication of poorly optimized reflow profiles.

For a cursory visual inspection it should be noted that Wolfson currently provides its packages with two different QFN package types as mentioned. However it should be noted that solder fillets up the side of the QFN package are not required for acceptability of soldering; as specified in international standard IPC-A-610D; whether fillets are formed or not does not affect the mechanical strength and reliability of the solder joints. There is no difference in the mechanical strength and reliability between the two packages; the differences are only cosmetic.

**APPENDIX:**

Extract from IPC-A-610D (Copyright IPC, Bannockburn, IL. Used by permission)

**8 Surface Mount Assemblies**

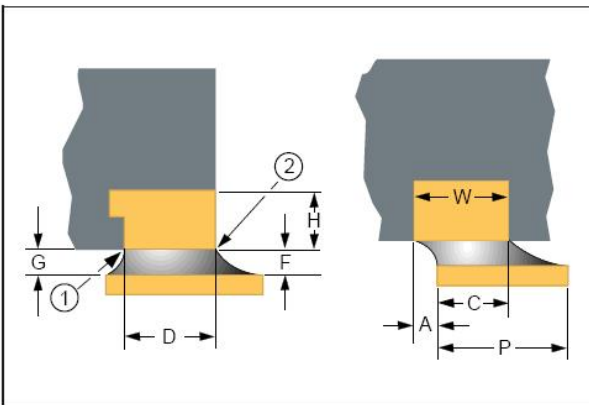
**8.2.13 Plastic Quad Flat Pack – No Leads (PQFN)**

Some other names for these devices are Microlead Packages, Leadless Plastic Chip Carriers (LPCC), and Quad Flat Pack No-Lead Exposed Pad (QFN-EP). Nonconformance to the requirements of Table 8-13 is a defect.

**Table 8-13 Dimensional Criteria - PQFN**

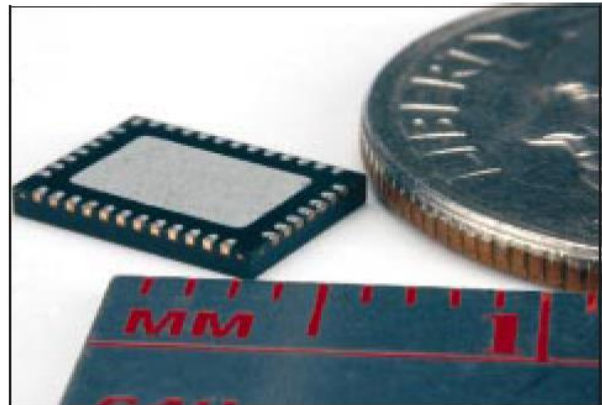
| Feature  | Dim. | Class 1       | Class 2       | Class 3 |
|--|------|---------------|---------------|---------|
| Maximum Side Overhang                                | A    | 50% W, Note 1 | 25% W, Note 1 |         |
| Toe Overhang (outside edge of component termination) | B    | Not permitted |               |         |
| Minimum End Joint Width                              | C    | 50% W         | 75% W         |         |
| Minimum Side Joint Length                            | D    | Note 4        |               |         |
| Solder Fillet Thickness                              | G    | Note 3        |               |         |
| Minimum Toe (End) Fillet Height                      | F    | Notes 2, 5    |               |         |
| Termination Height                                   | H    | Note 5        |               |         |
| Solder Coverage of Thermal Pad                       |      | Note 4        |               |         |
| Land Width   | P    | Note 2        |               |         |
| Termination Width                                    | W    | Note 2        |               |         |

- Note 1.** Does not violate minimum electrical clearance.
- Note 2.** Unspecified parameter or variable in size as determined by design.
- Note 3.** Wetting is evident.
- Note 4.** Not a visually inspectable attribute.
- Note 5.** Toe (end) surfaces are not required to be solderable. Toe fillets are not required.



**Figure 8-147**

- 1. Heel
- 2. Toe



**Figure 8-148**

## 8 Surface Mount Assemblies

## 8.2.13 Plastic Quad Flat Pack – No Leads (PQFN) (cont.)

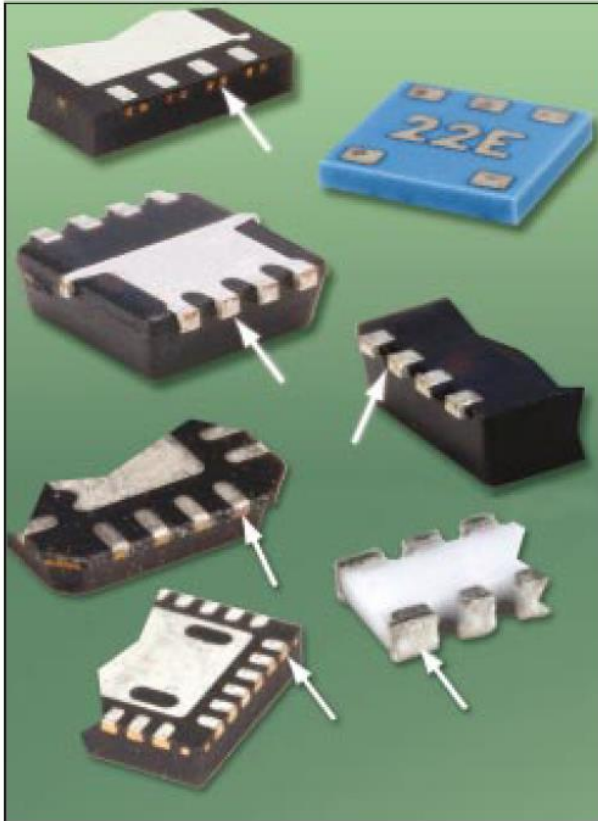


Figure 8-149

There are some package configurations that have no toe exposed or do not have a continuous solderable surface on the exposed toe on the exterior of the package (Figure 8-149 arrows) and a toe fillet will not form, see Figures 8-150 and 8-151.

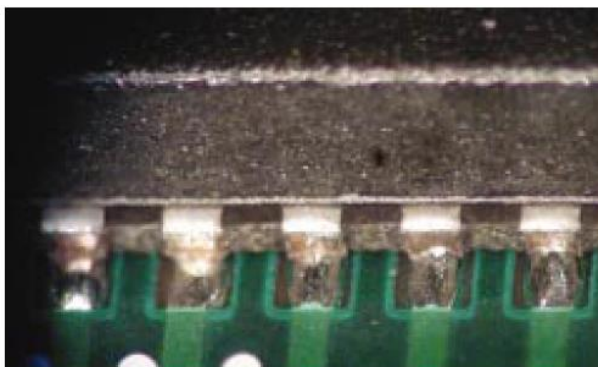


Figure 8-150

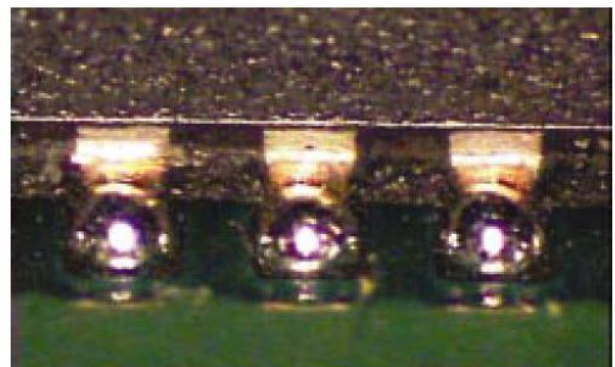


Figure 8-151

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