

CS5361/CS5381 Compatibility

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1. Analog Input Buffer Design

1.1 Introduction

There are many considerations that must be taken into account when designing and implementing an analog input buffer. These include negligible noise contribution, input biasing, isolation from switched capacitor currents, maintaining a low output impedance so as not to cause distortion, and providing anti-alias filtering appropriate for the modulator sample rate.

1.2 Recommended Differential Input Buffer

Figure 1 shows the recommended fully differential input buffer for the CS5361 and CS5381. This input buffer will work well with both devices. However, if full performance is to be realized, then care must be taken when selecting the op amps to ensure that the noise level of the input buffer is insignificant relative to the converter. The CDB5361 and CDB5381 implement the NE5532 op amp, which provides an adequate noise floor to see full performance from these two converters.

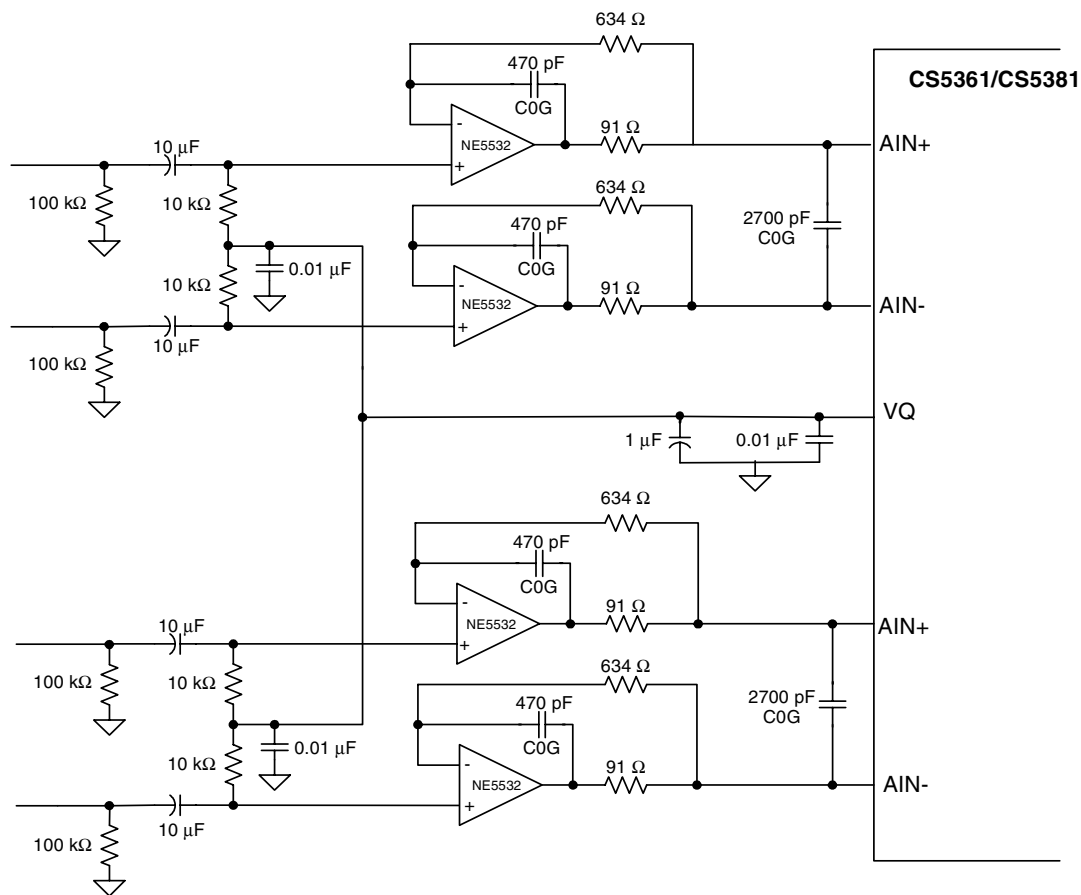


Figure 1. Recommended Differential Input Buffer for the CS5361 and CS5381

2. Capacitor Requirements for FILT+ (pin 24)

2.1 Introduction

The CS5361 and CS5381 utilize a positive reference voltage for the internal sampling circuits. This reference pin, called FILT+ (pin 24), requires external capacitors for decoupling purposes. The size of the decoupling capacitor will affect the low frequency (<200 Hz) distortion performance of the converter. The larger the capacitor, the better the low frequency distortion performance.

2.2 Recommended Capacitor Values

The recommended capacitors for the CS5361 are a 0.1 μ F in parallel with a 47 μ F. Using these values, the CS5361 can achieve -105 dB of distortion performance at 1 kHz and approximately -103 dB at 20 Hz. Increasing the size of the 47 μ F capacitor will increase the low frequency distortion performance of the converter until the -105 dB level is attained across the entire bandwidth down to 20 Hz.

The recommended capacitors for the CS5381 are a 0.1 μ F in parallel with a 220 μ F. Using these values, the CS5381 can achieve -110 dB of distortion performance at 1 kHz and approximately -106 dB at 20 Hz. Increasing the size of the 220 μ F capacitor will increase the low frequency distortion performance of the converter until the -110 dB level is attained across the entire bandwidth down to 20 Hz. On the other hand, lowering the value of the capacitor on FILT+ will decrease the low frequency distortion performance. Using a 47 μ F capacitor on the FILT+ pin of the CS5381 will provide approximately -95 dB of distortion at 20 Hz.

Therefore, it is possible to use the same capacitor values on the FILT+ pins of the CS5361 and CS5381, but the above performance characteristics must be taken into consideration.

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