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## ***Errata: CS4350 Rev. C2 Silicon***

***(Reference CS4350 DS691F5 Datasheet)***

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### **1 Errata**

The following errata describes revision C2 silicon variances from specifications published in the CS4350 DS691F5 datasheet.

1.  **$\overline{\text{RST}}$  Rising Edge to  $\overline{\text{CS}}$  Falling ( $t_{\text{SRs}}$ ) minimum requirement.** (See Table 8. Switching Characteristics – Control Port – SPI Format in the datasheet.)

Revision C2 silicon requires a minimum duration between  $\overline{\text{RST}}$  rising edge and  $\overline{\text{CS}}$  falling edge ( $t_{\text{SRs}}$ ) of at least 25  $\mu\text{s}$ , contrary to Table 8 on page 15 of the CS4350 DS691F5 datasheet which states a minimum of only 500 ns. Accommodating this longer minimum duration ensures the success of an initial SPI operation after coming out of reset.

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## 2 Revision History

Revision	Changes
R1 JUL 2023	• Initial release

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**Contacting Cirrus Logic Support**

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

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