1 Errata

The following errata describes revision C2 silicon variances from specifications published in the CS4350 DS691F5 datasheet.

1. **RST Rising Edge to CS Falling (t_{SRS}) minimum requirement.** (See Table 8. Switching Characteristics – Control Port – SPI Format in the datasheet.)

   Revision C2 silicon requires a minimum duration between RST rising edge and CS falling edge (t_{SRS}) of at least 25 µs, contrary to Table 8 on page 15 of the CS4350 DS691F5 datasheet which states a minimum of only 500 ns. Accommodating this longer minimum duration ensures the success of an initial SPI operation after coming out of reset.
## 2 Revision History

<table>
<thead>
<tr>
<th>Revision</th>
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</tr>
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<tbody>
<tr>
<td>R1</td>
<td>Initial release</td>
</tr>
<tr>
<td>JUL 2023</td>
<td></td>
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