

## **Errata: CS4299 Rev. D**

(Reference CS4299\_DS319PP6 Data Sheet dated March '06)

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1. The CS4299 requires a minimum SYNC pulse width of 1.13  $\mu$ s in the absence of BIT\_CLK for a warm reset to occur. AC '97 version 2.1 requires SYNC to be asserted for a minimum of only 1.0  $\mu$ s.

**Note:** This requirement refers to the behavior of SYNC during warm reset only. During normal operation, SYNC is asserted for the entire period of slot 0 (the tag phase), which is 16 cycles of BIT\_CLK.

2. SDATA\_IN does not meet the AC '97 specification of driving a 47.5 pF capacitive load within the rise time constraints of  $2 \text{ ns} \leq T_{\text{rise}} \leq 6 \text{ ns}$ . However, even at maximum capacitive loading, the codec provides sufficient SDATA\_IN data setup margin to prevent any functional issues.

**Workaround Solution** - Minimize SDATA\_IN trace length during board layout, and keep the total capacitive loading to 22 pF or less.

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### **Contacting Cirrus Logic Support**

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

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