Errata: CS4265 Rev. C0 Silicon

Reference CS4265_DS657F1 Data Sheet

- The quiescent voltage present on VQ is typically (0.45 x VA) V_{DC}.
- The $\overline{\text{MUTEC}}$ output pin drives high when the device is in reset. When the device is released from reset, the $\overline{\text{MUTEC}}$ pin will remain high until the device is taken out of power-down mode and a mute condition is met.

Contacting Cirrus Logic Support
For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to http://www.cirrus.com