Errata: CS4270 Rev C0 Silicon
Reference CS4270 Data Sheet DS686PP1

♦ Measured DAC THD+N (0 dB) with VA = 5 V or 3.3 V (nominal voltage) could be -81 dB and does not meet the -83 dB maximum specification in the Data Sheet. Measured DAC THD+N (0 dB) with VA = 3.0 V (3.3 V min.) is -79 dB and does not meet the -83 dB maximum specification in the Data Sheet.

♦ The digital portions of the part (both ADC and DAC) will not function when MCLK divide by 1.5 is selected and VD = 3.3 V. The following start-up sequences will correct the problem.

In Control Port Mode:
– Power-up the part
– Hold MCLK Static
– Hard reset the part
– Set PDN
– Set the Ratio Select bits in Reg. 03h
– Release PDN

In Stand-Alone Mode:
– Power-up the part
– Hold the part in reset
– Set the MDIV1,2 pin logic levels
– Release reset