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**Errata: CS4270 Rev. C0 Silicon**

(Reference CS4270 DS686F2 Data Sheet)

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- Measured DAC THD+N (0 dB) with VA = 5 V (nominal voltage) could be -81 dB and does not meet the -83 dB maximum specification in the Data Sheet.
- The digital portions of the part (both ADC and DAC) will not function when MCLK divide by 1.5 is selected and VD = 3.3 V. The following start-up sequences will correct the problem.

In Control Port Mode:

- Power-up the part
- Hold MCLK static
- Hard reset the part
- Set PDF
- Set the Ratio Select bits in Reg. 03h
- Release PDN

In Stand-Alone Mode:

- Power-up the part
- Hold the part in reset
- Set the MDIV1,2 pin logic levels
- Release reset

# 1 Revision History

**Table 1-1. Revision History**

Revision	Change
ER686B2 AUG 2006	Initial revision
ER686C0R2 APR 2021	No changes to stated errata items from previous revision; Updates due to: <ul style="list-style-type: none"> <li>• Reference to DS686F2 data sheet</li> <li>• Removal of functionality at VA = 3.3 V</li> </ul>

**Important:** Please check [www.Cirrus.com](http://www.Cirrus.com) to confirm that you are using the latest revision of this document.

## Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.  
To find the one nearest to you, go to [www.cirrus.com](http://www.cirrus.com).

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