DC4282P-CODEC User Guide

Introduction

The DC4282P-CODEC is a daughter card for the Cirrus Logic Dunglass (CDB-PROAUDIO) system for high performance ADC, DAC and codec devices. This user guide details how to connect the DC4282P-CODEC to a Dunglass (CDB-PROAUDIO) system platform and how to get started.

The default jumper link configuration for DC4282P-CODEC is shown in Figure 1.

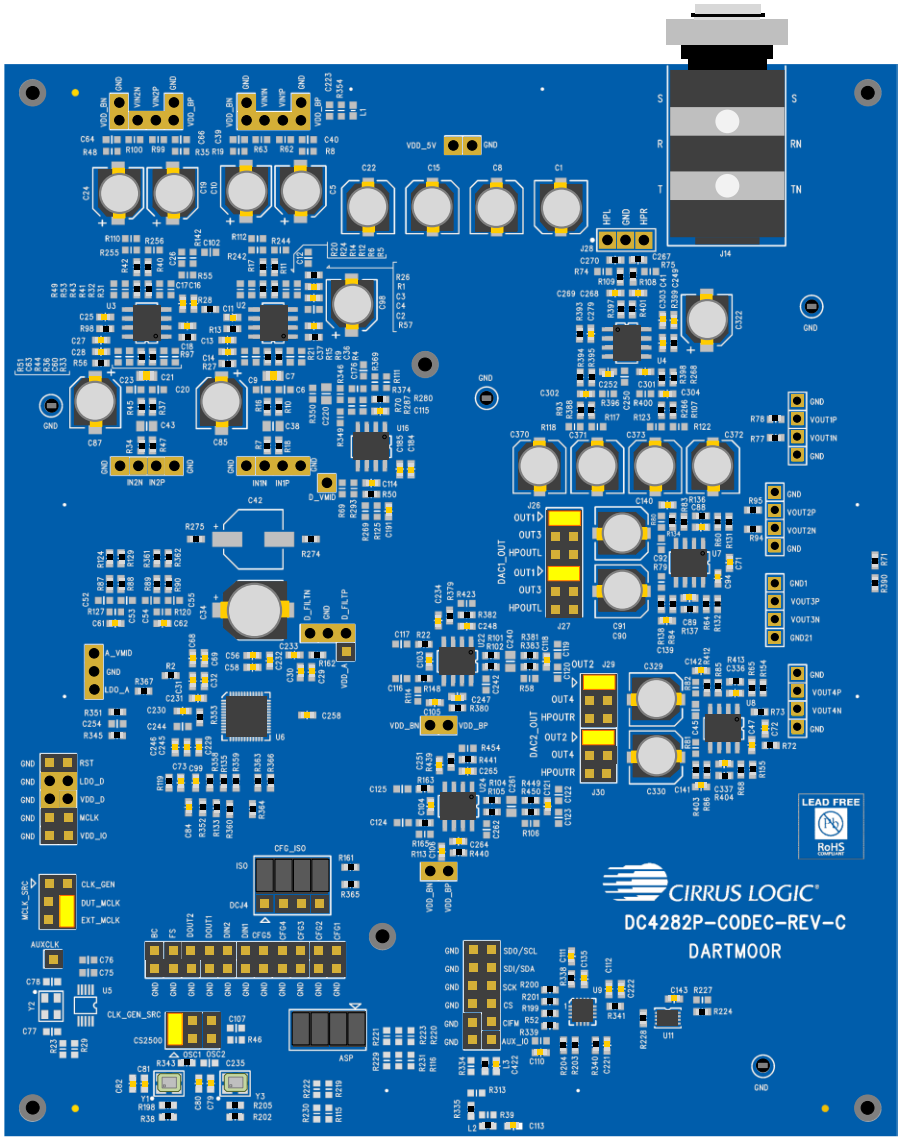

Figure 1: DC4282P-CODEC Daughter Card

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1 Hardware Connections

The Dunglass system supports interchangeable daughter cards for a variety of ADC, DAC and CODEC devices.

Caution:

Daughter cards should not be inserted or removed while the Dunglass system is powered. Fully disconnect or power down external power supply before changing daughter cards.

For more information on the Dunglass (CDB-PROAUDIO) platform, refer to the CDB-PROAUDIO User Guide.

1.1 How to Connect DC4282P-CODEC onto the Dunglass System

The DC4282P-CODEC is a 4-header daughter card and should be plugged onto DCJ1, DCJ2, DCJ3 & DCJ4. The daughter card connectors are keyed and will only plug in one way. There is also an alignment dot on each board to help with placement.

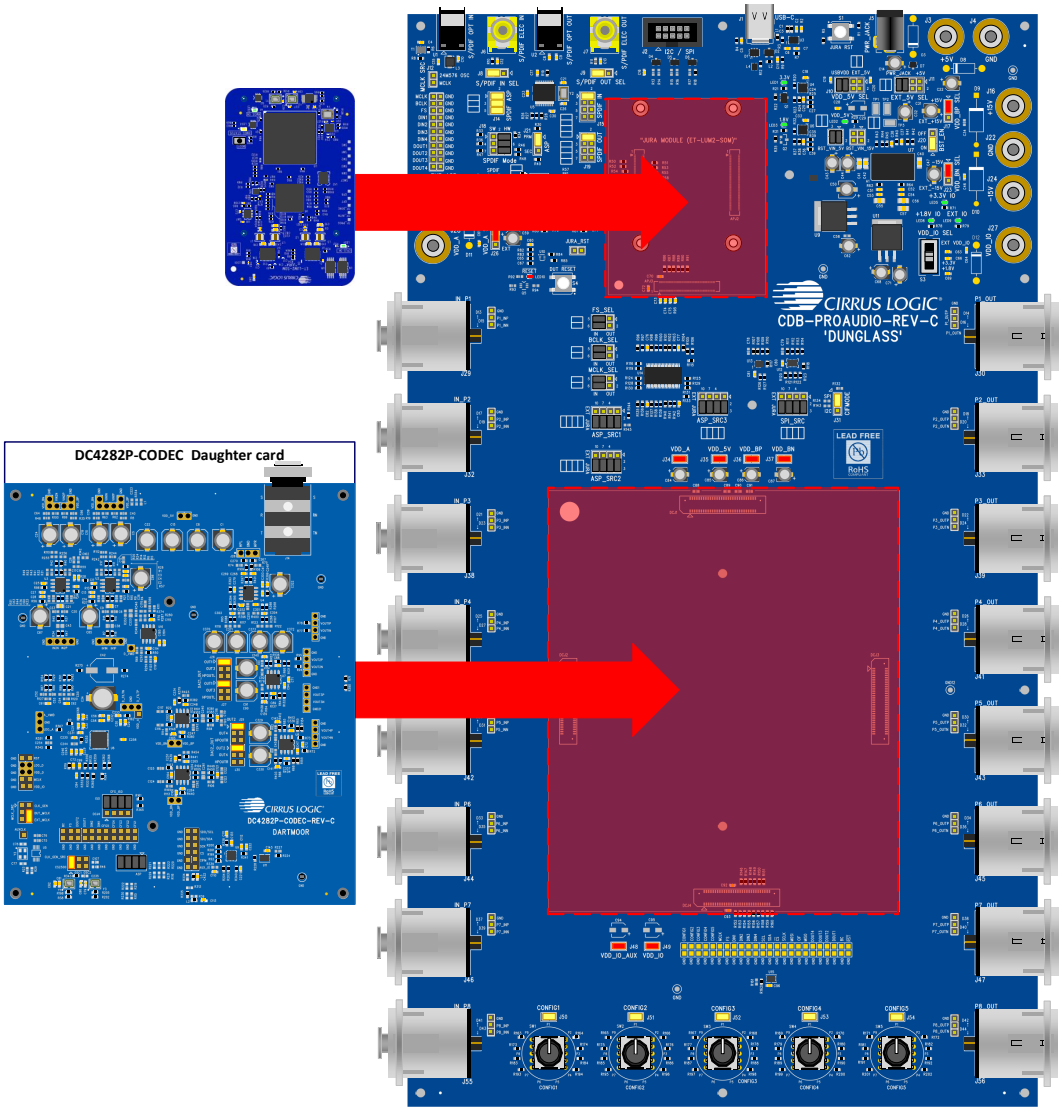


Figure 2: How to Connect DC4282P-CODEC onto the Dunglass System

1.2 USB & Power Connection

Dunglass is powered using a 5V external power supply and is controlled via a single USB connection. The Jura module supports the following functions via the USB connection:

- I2C/SPI communications to control device and board.
- Multichannel USB streaming audio (USB class 2).

The Dunglass board is provided with a USB-A to USB-C cable and a 5V wall supply.

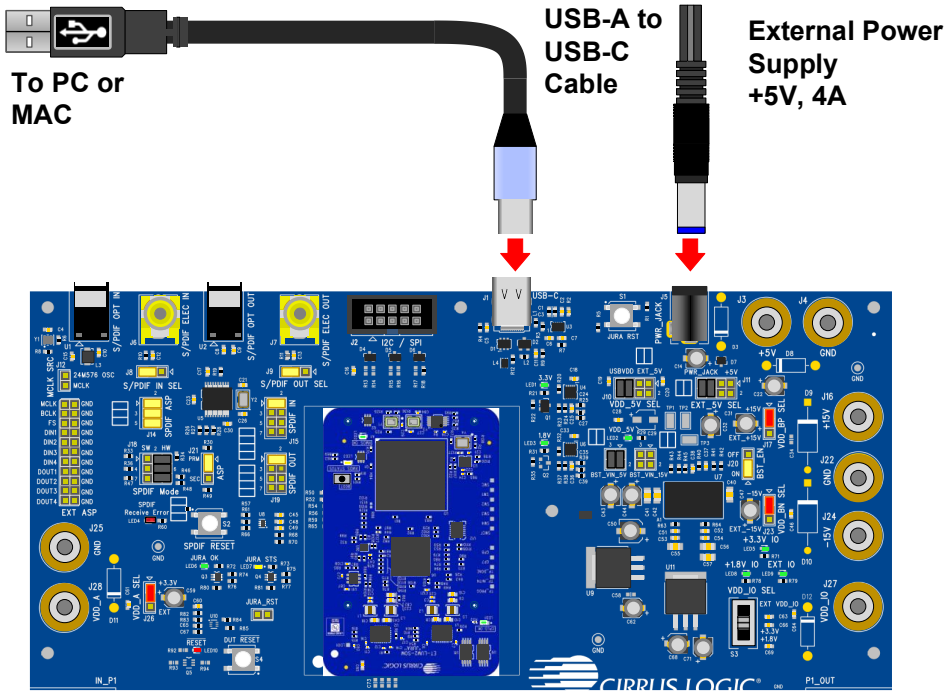


Figure 3: Dunglass (CDB-PROAUDIO) USB & Power Connection

A Total Phase Aardvark connector can be used for I2C/SPI communication. Refer to the CDB-PROAUDIO User Guide for more details.

1.2.1 JURA Module

The Jura module supports I2C/SPI communication to control the Dunglass system and daughter card; it also enables multichannel USB streaming audio (USB audio Class 2).

The Jura module is connected to the Dunglass board as shown below:

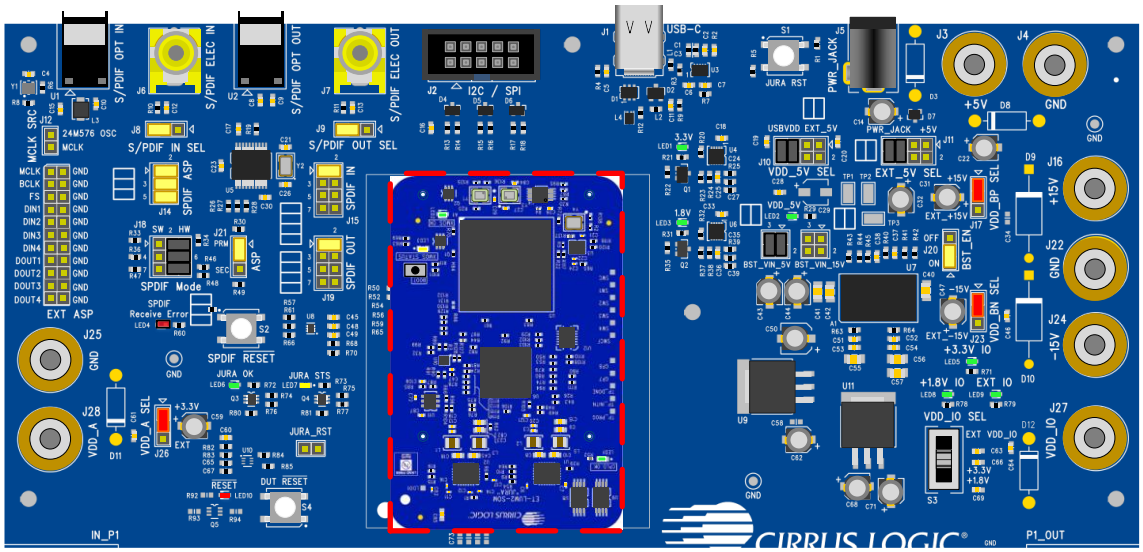


Figure 4: How to Connect JURA Module to Dunglass System

1.2.2 Dunglass Boot Procedure with Jura Module

The USB-C cable must be connected between the Dunglass system and the PC/Mac prior to powering up the board.

The boot time of the Dunglass system varies depending on the version of firmware on the Jura module but is typically in the range of 2 to 5 seconds after applying power to the board.

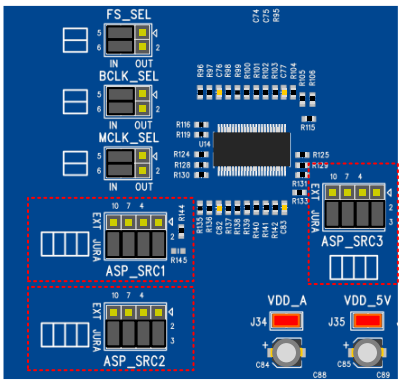
1.3 Routing the Digital Audio PCM Signals

The digital audio PCM paths to the daughter card can be routed from the Jura module, or else from the EXT ASP header and S/PDIF transceiver. The routing is configured using the ASP_SRC1, ASP_SRC2 & ASP_SRC3 headers.

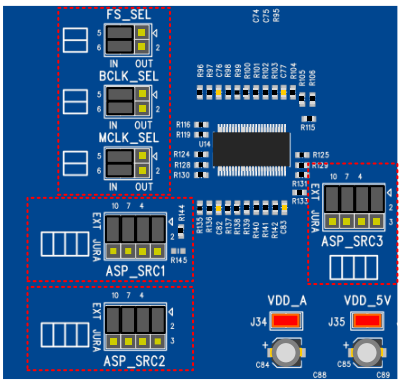
- JURA = Digital audio signals routed from Jura module.
- EXT = Digital audio signals routed from EXT ASP header/SPDIF.

The ASP_SRC1, ASP_SRC2 & ASP_SRC3 headers are configured as shown in Table 1.

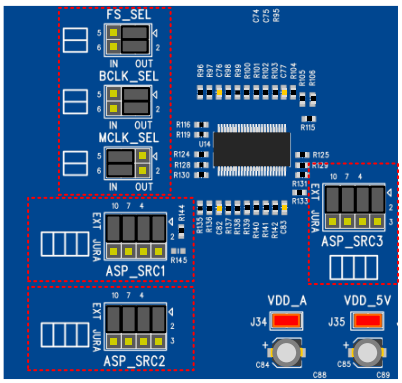
Table 1 Digital Signal Routing



Jura Module Primary Mode



EXT ASP / SPDIF Primary Mode



EXT ASP / SPDIF Secondary Mode

The Jura module always operates in Primary Mode – the MCLK, BCLK and FSYNC are generated by the Jura module, as inputs to the daughter card.

If the digital audio is routed from the EXT ASP header or S/PDIF transceiver, the direction of the MCLK, BCLK, and FSYNC signals are configured using the MCLK_SEL, BCLK_SEL & FS_SEL headers. Each signal is configured independently using the respective header.

- IN = EXT_ASP header or S/PDIF transceiver supports the signal as input to the daughter card
- OUT = EXT_ASP header or S/PDIF transceiver supports the signal as output from the daughter card

Note that the EXT ASP header and S/PDIF transceiver use 3.3 V logic levels; a level shifter is incorporated to interface with the VDD_IO domain on the DC4282P-CODEC daughter card.

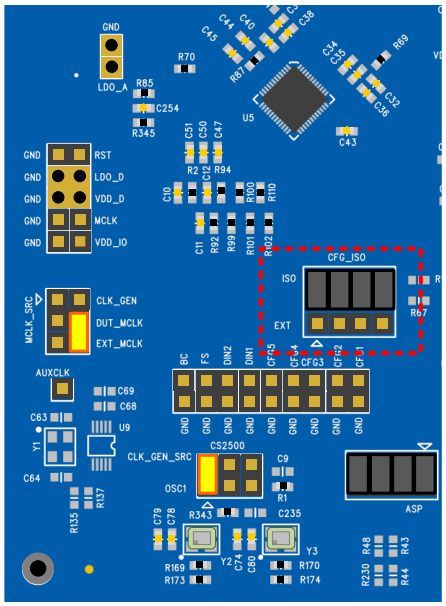
1.4 Selection of Hardware/Software Control Mode

The CS4282P supports Hardware and Software modes. The hardware and software modes are set via the CFG_ISO header on the DC4282P-CODEC and the rotary switches on the Dunglass system. The jumper link must be configured as in Table 2.

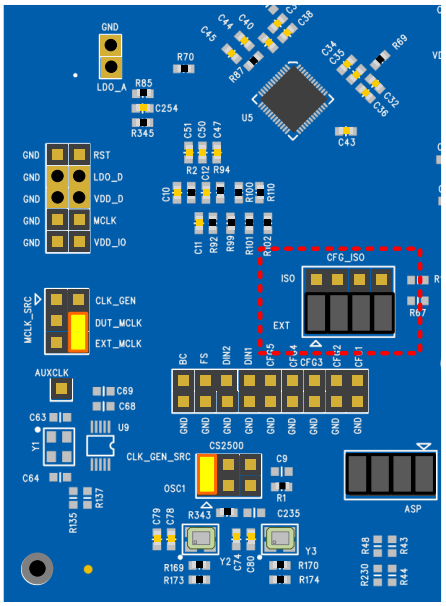
- ISO = Software mode.
- EXT = Hardware mode.

In Hardware mode, rotary switches are used to select the desired configuration. See Section 4 for information on hardware mode.

Table 2 Software/Hardware mode Jumper Link Configuration for DC4282P-CODEC



Software Mode Jumper Link Configuration



Hardware Mode Access Jumper Link Configuration

Note that Hardware mode is only supported for VDD_IO = 3.3V on the DC4282P-CODEC due to the rotary switch pull-up supply = 3.3V on the Dunglass system.

1.5 DC4282P-CODEC MCLK Source Selection

The DC4282P-CODEC board provides two on-board oscillators that can be used as an MCLK source for the CS4282P. The oscillators are configured for different frequencies; the oscillators are enabled by removing the applicable resistor on the DC4282P-CODEC board.

- OSC1 (22.5792 MHz). Enabled by removing R173.
- OSC2 (24.576 MHz). Enabled by removing R174.

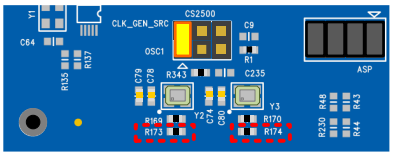
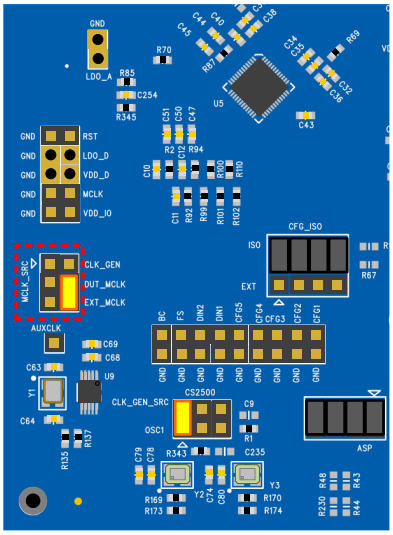


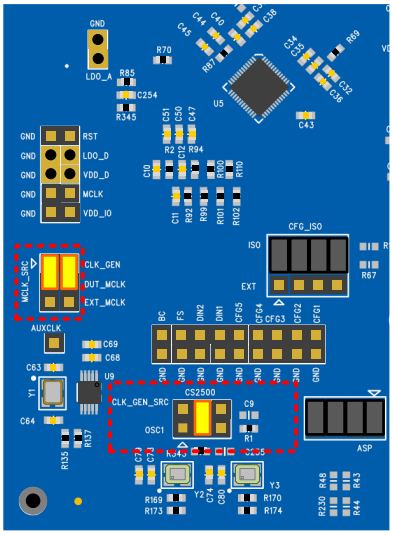
Figure 5: Enabling On board Oscillators

The MCLK source is configured as shown in Table 3.

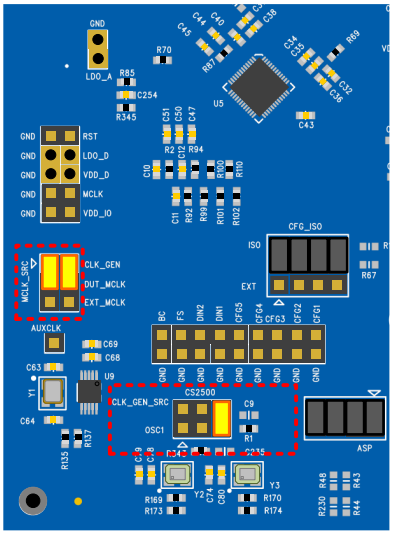
Table 3 MCLK source Jumper Link Config



MCLK source = Dunglass System (Default)



MCLK source = OSC1



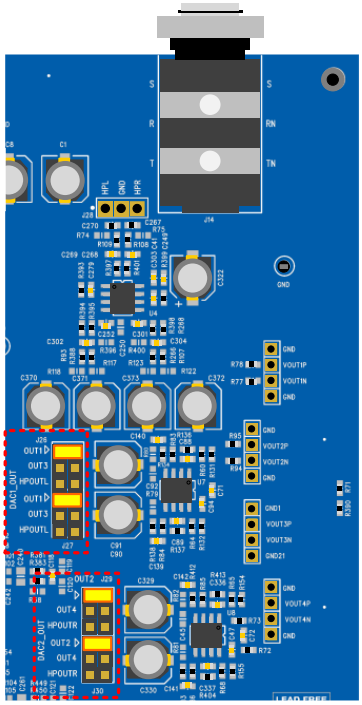
MCLK source = OSC2

1.6 DC4282P-CODEC DAC Output Routing

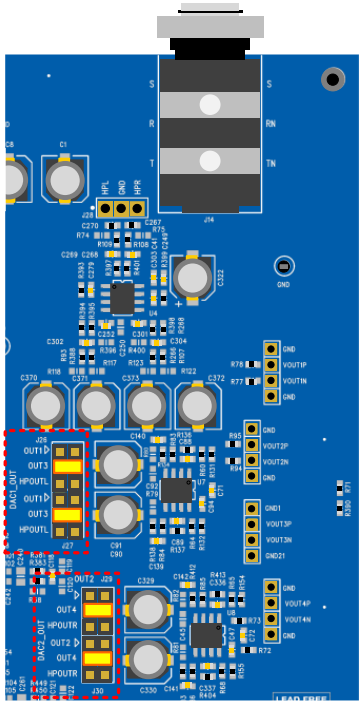
The DC4282P-CODEC board has three routing options for the output of the DAC. The options are configured using J26, J27, J29 & J30. The options are as follows:

- OUT1/OUT2 (Default) – 8 Vrms output on Dunglass OUT1 & OUT2.
    - This is the output of the current-to-voltage buffer/filter
- OUT3/4 – 2.2 Vrms output on Dunglass OUT3 & OUT4.
    - The output of the current-to-voltage buffer/filter is routed to an op-amp line driver with a gain of –11dB.
- HPOUTL/R – 1.76 Vrms single ended headphone output circuit
    - The output of the current-to-voltage buffer/filter is routed to an ended op-amp circuit with a gain of –13dB. The output is routed to a 6.3 mm stereo headphone jack (J14)

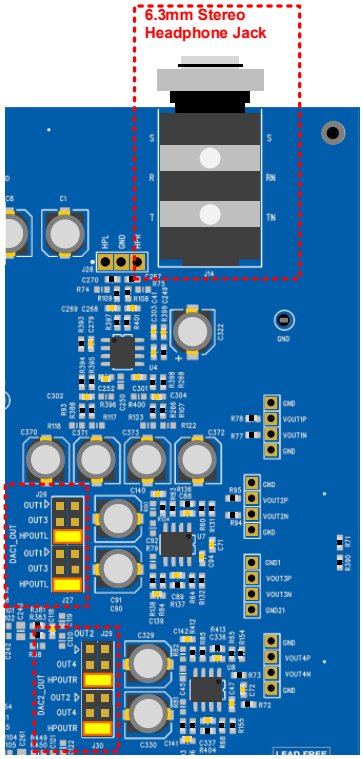
Table 4 DAC Output Routing Jumper Link Config



DAC Output to OUT1/OUT2



DAC Output to OUT3/OUT4



DAC Output to headphone Output

2 Driver Installation and SoundClear Studio Support

2.1 SoundClear Studio

SoundClear Studio (SCS) is a PC/Mac-based tool used to configure Cirrus Logic devices. The tools suite provides support for evaluation and development and can be used with Dunglass system and associated daughter cards.

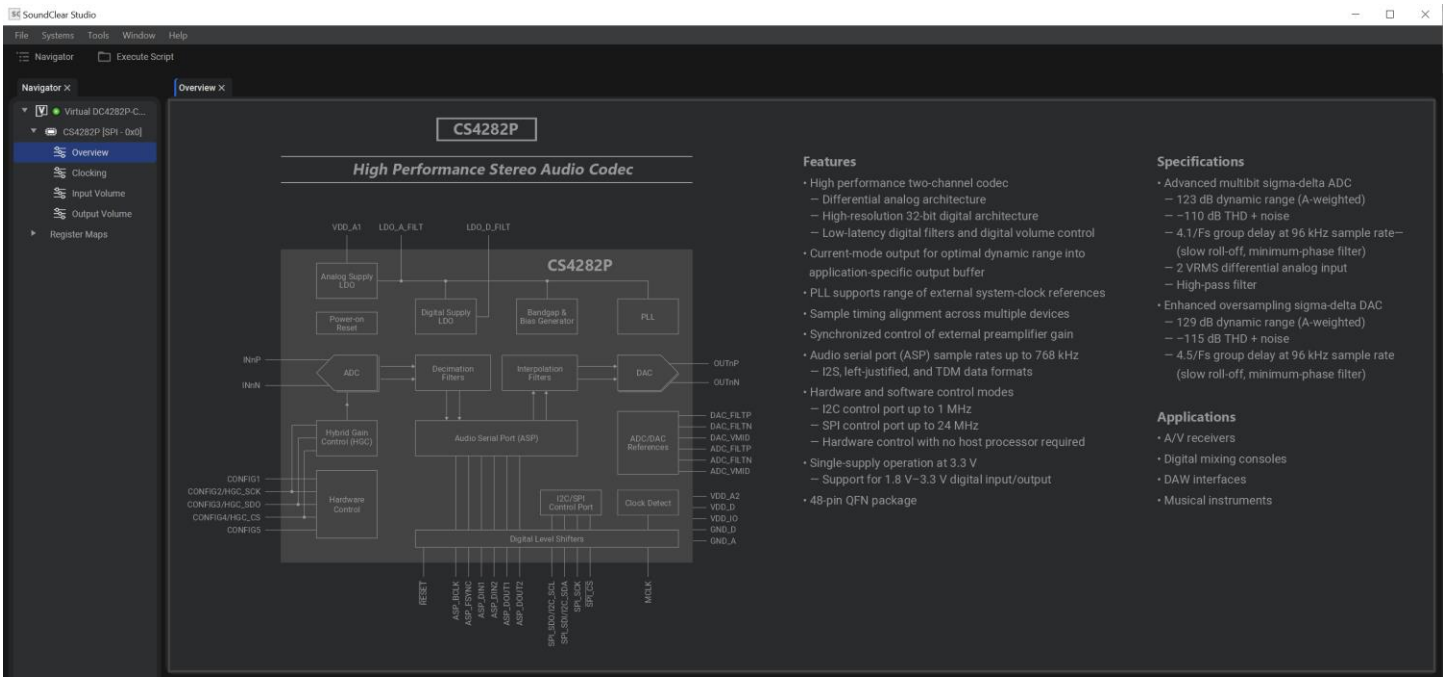


Figure 6: SoundClear Studio

2.1.1 Download SoundClear Studio Software & Drivers

SoundClear Studio and associated software collateral required for the Dunglass system can be downloaded from https://cirrus.com.

- *https://cirrus.com/products/cs4282p/*

The required components are as follows:

- **SoundClear Studio 2.1**. Run the appropriate installer on your Windows or macOS computer to install SoundClear Studio.
- **CS4282P SCS Package**. Install this in SoundClear Studio to incorporate the CS4282P-specific software components in SoundClear Studio. See Section 2.2.1 for details on how to install an SCS package.
- **Jura Windows Setup**. On Windows computers, run the Cirrus Logic USB Audio Setup to install the driver that enables SoundClear Studio to communicate with the Jura board.

2.2 SoundClear Studio Quick Start Guide

2.2.1 Installing Packages

Each daughter card has its own individual SoundClear Studio package that must be installed separately from the main SoundClear Studio Software. These are installed from the main menu using **"File → Install Package..."**. Multiple packages can be installed together by selecting more than one using the file dialog.

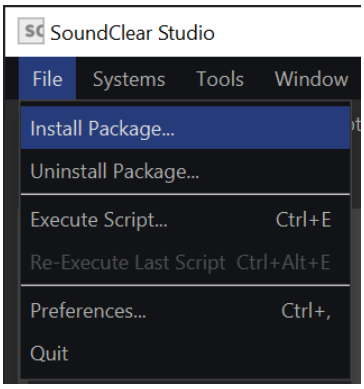


Figure 7: SoundClear Studio – Installing Board Packages

2.2.2 SoundClear Studio User Guide

The SoundClear Studio User Guide can be accessed from the main menu using **"Help → Open Help Contents..."**

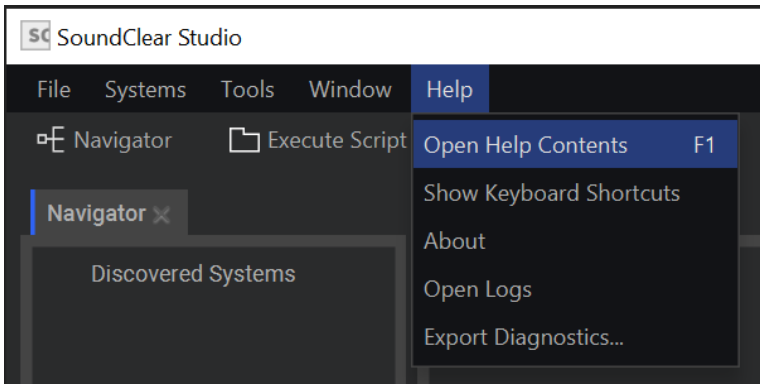


Figure 8: SoundClear Studio – User Guide

2.2.3 Creating a Virtual System

A virtual (non-hardware) version of the system can be created using **“Systems → Add Virtual System..."**

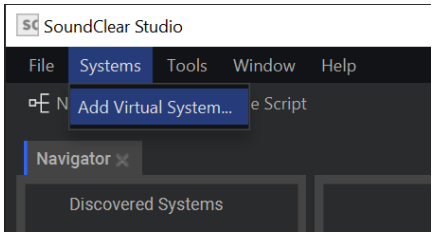


Figure 9: SoundClear Studio – Creating a Virtual System

This opens a dialog box to select an installed system (shown here is the DC4282P-CODEC):

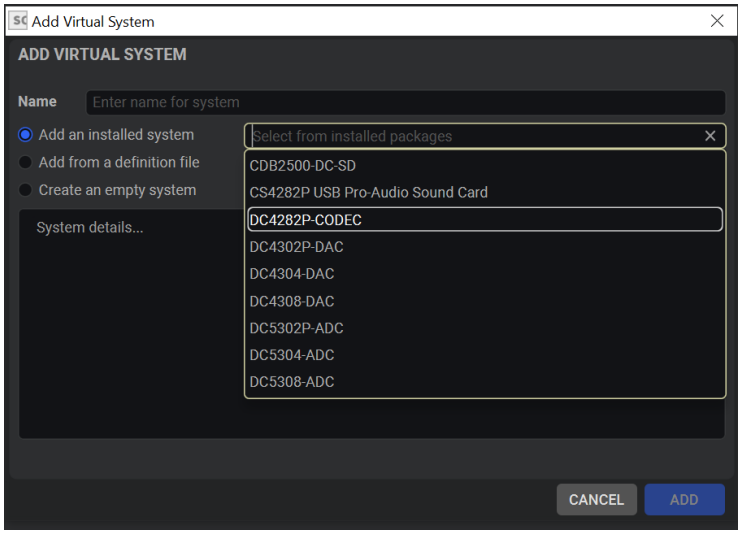


Figure 10: SoundClear Studio – Adding a Virtual System

Once created, a virtual system enables the user to interact with virtual versions of the device register map and helper panels.

2.2.4 Adding an Existing System

SoundClear Studio automatically detects board hardware such as the Jura module and Cirrus Logic devices. In the event of devices not being detected automatically, a device can be added manually. Right click on the system and select **"Add Device…"**

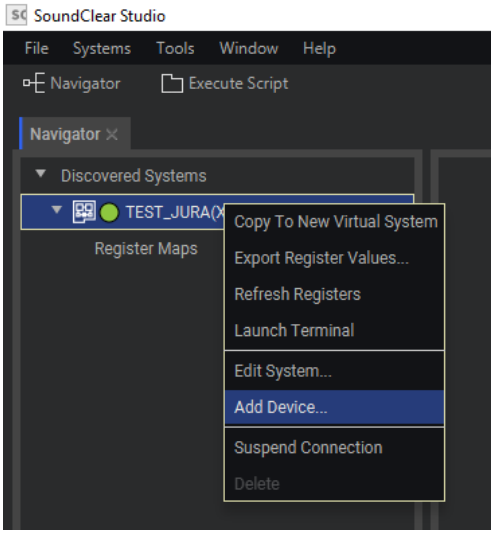


Figure 11: SoundClear Studio – Adding an Existing Device

Then select the device from those installed, along with the protocol and address of the part (this can be edited again by right clicking on the device and selected **"Edit Device..."**):

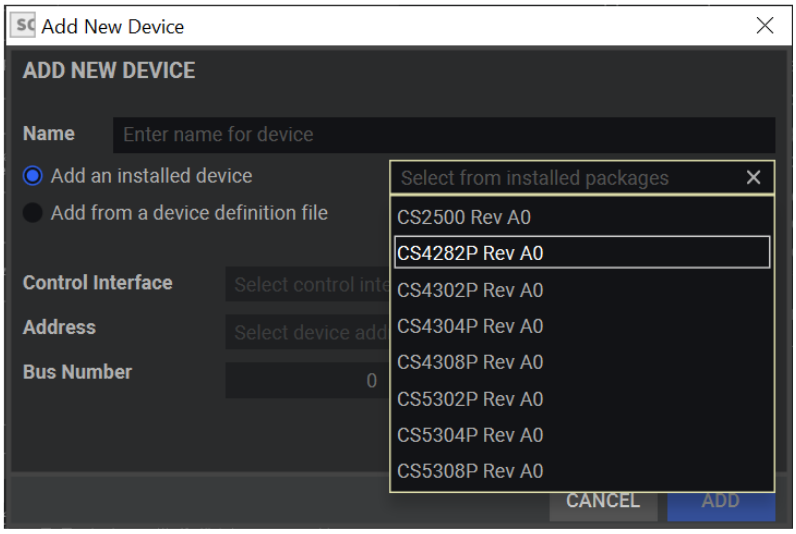


Figure 12: SoundClear Studio – Adding an Existing Device

2.2.5 Executing SoundClear Studio Scripts

SoundClear Studio provides the ability to interact with the device register map using Python scripts. These scripts can sequence register operations to configure the desire states, which can then be executed from SoundClear Studio using **"File→Execute Script…"**

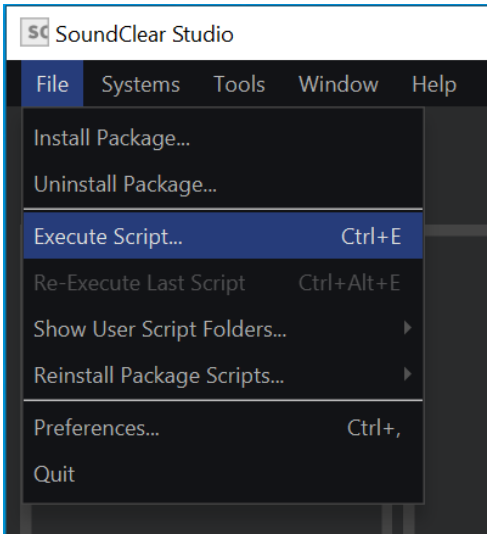


Figure 13: SoundClear Studio – Executing Script

The CS4282P SoundClear Studio package installs a set of scripts to configure the device for common use cases. These are available at <User Documents>\Cirrus Logic\SCS\Scripts\<Package Name>.

The scripts can be accessed via **"File→Show User Script Folder→CS4282P Scripts"**

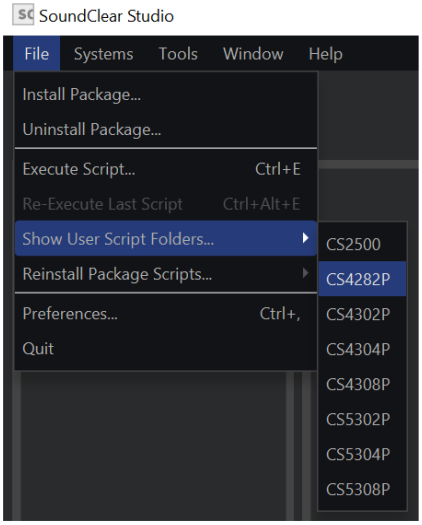


Figure 14: SoundClear Studio – Show User Script Folder

3 DC4282P-CODEC Software Mode Quick Start

After installing the SoundClear Studio software and the CS4282P SCS package, follow the steps below to get up and running quickly:

- Connect the hardware as shown in Figure 2
- Connect USB cable to PC
- Power up the system and ensure JURA OK, 1.8V, 3.3V, VDD_5V LEDs are illuminated.
- Configure signal routing as shown in Table 1
  - For SPDIF output see Section 5
- Start SoundClear Studio
  - SoundClear Studio should auto-detect the DC4282P-CODEC daughter card. If not, follow the procedure specified in Section 2.2.4
- Run one of the scripts from the following location.
  - <User Documents>\Cirrus Logic\SCS\Scripts\<Package Name>.

4 Hardware Mode Control

The Dunglass system supports the hardware control modes for Cirrus Logic high performance ADC, DAC and CODEC devices. These are supported via the rotary switches on the Dunglass system.

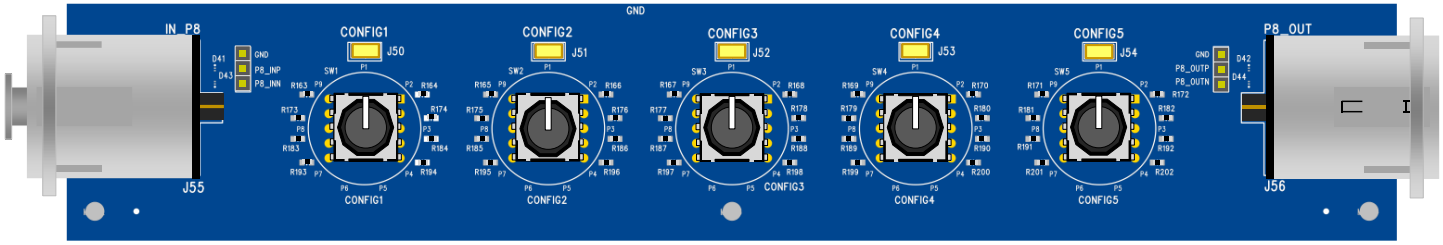


Figure 15: Dunglass Rotary Switches for Hardware Control Mode

Each switch has silkscreen on the board to indicate the position of the switch. Each switch position enables a pull resistor on the respective CONFIG pin to VDD_A or ground.

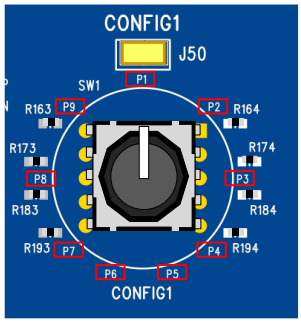


Figure 16: Rotary Switch

Note that, if the rotary switches are reconfigured while the Dunglass system is powered, the daughter card needs to be reset for the changes to take effect. This is done by pushing the DUT RESET button.

Note that Hardware mode is only supported for VDD_IO = 3.3V on the DC4282P-CODEC due to the rotary switch pull-up supply = 3.3V on the Dunglass system.

4.1 Hardware Mode Rotary Switch Settings

The CS4282P supports hardware mode. The rotary switch functions are described in the following tables. Refer to the CS4282P datasheet for further details of the hardware-mode control options.

The CONFIG1 pin selects the ASP operating configuration.

Table 5: CONFIG1 Hardware Control – ASP Configuration

Switch Position	Config Pin Configuration		Description
P1	Pull-up to 3.3V	0 Ω	Software control mode (I2C/SPI)
P2		4.7 kΩ	ASP Primary Mode, 44.1 kHz, 48 kHz sample rate
P3		22 kΩ	ASP Primary Mode, 88.2 kHz, 96 kHz sample rate
P4		100 kΩ	ASP Primary Mode, 176.4 kHz, 192 kHz sample rate
P5	Pull-Down to GND	100 kΩ	ASP Secondary Mode, 176.4 kHz, 192 kHz sample rate
P6		22 kΩ	ASP Secondary Mode, 88.2 kHz, 96 kHz sample rate
P7		4.7 kΩ	ASP Secondary Mode, 44.1 kHz, 48 kHz sample rate
P8		0 Ω	ASP Secondary Mode, autodetect sample rate
P9	No Connection	—	—

1. Autodetect sample rate is only supported in MCLK 256 fs(base), MCLK 512 fs(base) or MCLK 1024 fs(base) clocking configurations.

The CONFIG2 pin selects the ASP format and TDM timeslots option.

Table 6: CONFIG2 Hardware Control – ASP Configuration

Switch Position	Config Pin Configuration		Description
P1	Pull-up to 3.3V	0 Ω	ASP TDM Mode—minimum time slots
P2		4.7 kΩ	ASP TDM Mode—maximum time slots
P3		22 kΩ	—
P4		100 kΩ	—
P5	Pull-Down to GND	100 kΩ	—
P6		22 kΩ	—
P7		4.7 kΩ	ASP Left-Justified Mode
P8		0 Ω	ASP I^2S Mode
P9	No Connection	—	—

The CONFIG3 pin selects the TDM slot selection in TDM Mode.

Table 7: CONFIG3 Hardware Control – TDM Slot Selection

Switch Position	Config Pin Configuration		Description
P1	Pull-up to 3.3V	0 Ω	Slots 14–15
P2		4.7 kΩ	Slots 12–13
P3		22 kΩ	Slots 10–11
P4		100 kΩ	Slots 8–9
P5	Pull-Down to GND	100 kΩ	Slots 6–7
P6		22 kΩ	Slots 4–5
P7		4.7 kΩ	Slots 2–3
P8		0 Ω	Slots 0–1
P9	No Connection	—	—

The CONFIG4 pin selects the clock reference and ASP channel ordering.

Table 8: CONFIG4 Hardware Control – Clocking Configuration

Switch Position	Config Pin Configuration		Clock Reference	PLL	Channel Order
P1	Pull-up to 3.3V	0 Ω	BCLK = 64 fs	Enabled	Default
P2		4.7 kΩ	MCLK = 1024 fs(base)	Bypass	Default
P3		22 kΩ	MCLK = 256 fs(base)	Enabled	Default
P4		100 kΩ	MCLK = 512 fs(base)	Enabled	Default
P5	Pull-Down to GND	100 kΩ	MCLK = 512 fs(base)	Enabled	Reversed
P6		22 kΩ	MCLK = 256 fs(base)	Enabled	Reversed
P7		4.7 kΩ	MCLK = 1024 fs(base)	Bypass	Reversed
P8		0 Ω	BCLK = 64 fs	Enabled	Reversed
P9	No Connection	—	—	—	—

1. fs(base) is the base sample rate.
   fs(base) = 48 kHz for 48 kHz-related sample rates; fs(base) = 44.1 kHz for 44.1 kHz-related sample rates.
2. BCLK 64 fs configuration is only supported in ASP Secondary Mode.

The CONFIG5 pin selects the digital filters. Note that the filter selection is different between ADC and DAC paths.

Table 9: CONFIG5 Hardware Control –ADC Input Digital Filter Selection

Switch Position	Config Pin Configuration		Description
P1	Pull-up to VDD_A	0 Ω	Minimum phase, slow roll-off, HPF bypass
P2		4.7 kΩ	Minimum phase, fast roll-off, HPF bypass
P3		22 kΩ	Linear phase, slow roll-off, HPF bypass
P4		100 kΩ	Linear phase, fast roll-off, HPF bypass
P5	Pull-Down to GND	100 kΩ	Linear phase, fast roll-off, HPF enabled
P6		22 kΩ	Linear phase, slow roll-off, HPF enabled
P7		4.7 kΩ	Minimum phase, fast roll-off, HPF enabled
P8		0 Ω	Minimum phase, slow roll-off, HPF enabled
P9	No Connection	—	—

Table 10: CONFIG5 Hardware Control –DAC Output Digital Filter Selection

Switch Position	Config Pin Configuration		DAC Interpolation Filter		High-Pass Filter (HPF)
			32-48 kHz Sample Rate [1]	88.2-192 kHz Sample Rate	
P1	Pull-up to 3.3V	0 Ω	Minimum phase, slow roll-off	Minimum phase, balanced roll-off	Bypass
P2		4.7 kΩ	Minimum phase, fast roll-off	Minimum phase, fast roll-off	Bypass
P3		22 kΩ	Linear phase, slow roll-off	Linear phase, balanced roll-off	Bypass
P4		100 kΩ	Linear phase, fast roll-off	Linear phase, fast roll-off	Bypass
P5	Pull-Down to GND	100 kΩ	Linear phase, fast roll-off	Linear phase, fast roll-off	Enabled
P6		22 kΩ	Linear phase, slow roll-off	Linear phase, balanced roll-off	Enabled
P7		4.7 kΩ	Minimum phase, fast roll-off	Minimum phase, fast roll-off	Enabled
P8		0 Ω	Minimum phase, slow roll-off	Minimum phase, balanced roll-off	Enabled
P9	No Connection	—	—	—	—

1. Fast roll-off filters are supported for all sample rates. Slow roll-off filters are not valid for 32 kHz sample rate.

5 SPDIF

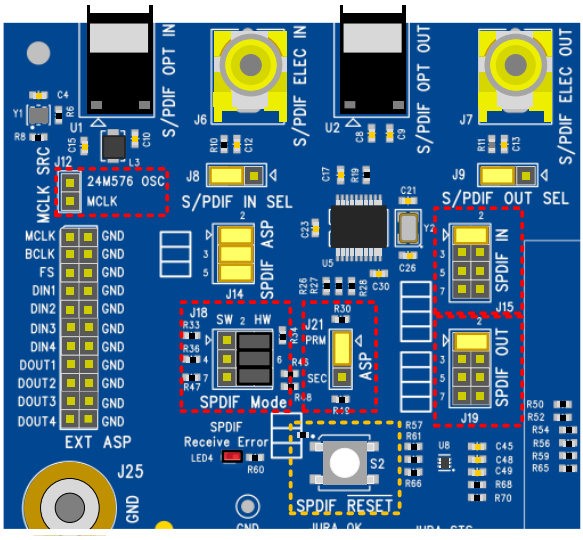
The Dunglass system supports S/PDIF input and output via optical and electrical connectors for sample rates up to 96 kHz (optical) or up to 192 kHz (electrical). The WM8804 S/PDIF transceiver on the Dunglass system can operate in software or hardware mode; in hardware mode, the sample rate is limited to 96 kHz.

Note that when the S/PDIF output is used, the S/PDIF input must be connected to an active source for the WM8804 S/PDIF transceiver to generate the correct MCLK, BCLK and FSYNC clocks.

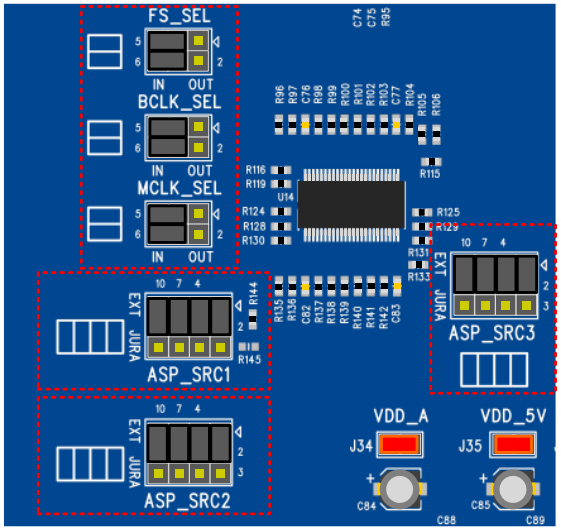
5.1 WM8804 Hardware Mode

To configure the WM8804 S/PDIF transceiver in hardware mode the jumper links on the Dunglass system must be configured as in Table 11.

Table 11 WM8804 Hardware Mode Configuration



S/PDIF Transceiver Configuration



S/PDIF Digital Audio Signal Routing

The SPDIF Receive Error (LED4) is lit when there is no S/PDIF input source present.

If the S/PDIF transceiver is reconfigured while the Dunglass system is powered, the WM8804 needs to be reset for the changes to take effect. The WM8804 can be reset using the SPDIF RESET button.

The CS4282P can be used in software mode or hardware mode for the above S/PDIF transceiver configuration. For this user guide, it is assumed CS4282P hardware mode is used when the WM8804 is in hardware mode.

In CS4282P hardware mode, the rotary switches on the Dunglass system should be configured as shown in Table 12, depending on the sample rate of the SPDIF source.

Note that the daughter card must be reset if the rotary switches have been configured while the Dunglass system is powered. The daughter card can be reset using the DUT RESET button.

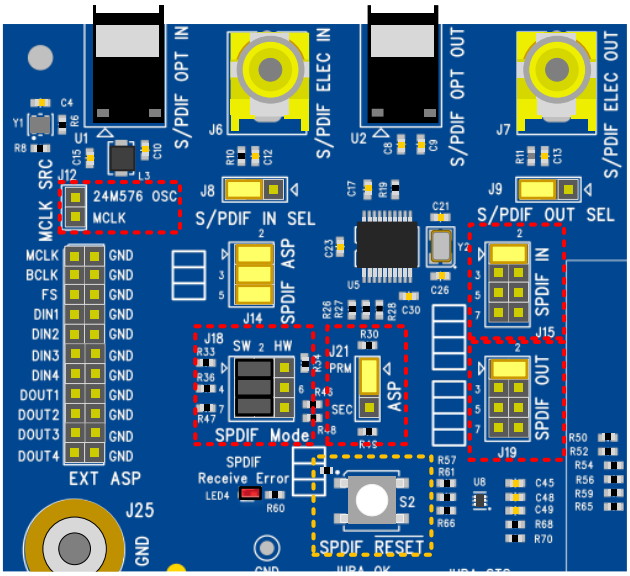
Table 12: Rotary Switch Positions for S/PDIF Input & Output

Rotary Switch	fs = 48kHz/44.1kHz	Fs = 96kHz/88.2kHz
CONFIG1	P7 (ASP Secondary Mode, 44.1 kHz, 48 kHz sample rate)	P6 (ASP Secondary Mode, 88.2 kHz, 96 kHz sample rate)
CONFIG2	P7 (ASP Left-Justified Mode)	P7 (ASP Left-Justified Mode)
CONFIG3	N/A	N/A
CONFIG4	P3 (MCLK = 256 fsb; PLL enabled; Channel order default)	P4 (MCLK = 512 fsb; PLL enabled; Channel order default)
CONFIG5	P8 (Minimum phase, slow roll-off/balanced roll-off filter)	P8 (Minimum phase, slow roll-off/balanced roll-off filter)

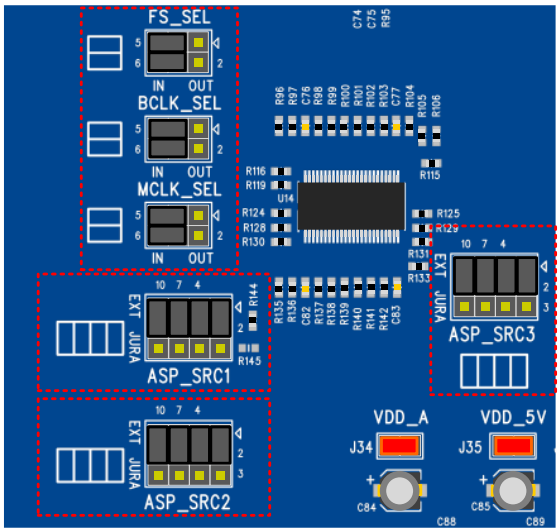
5.2 WM8804 Software Mode

To configure the WM8804 S/PDIF transceiver in software mode the jumper links on the Dunglass system must be configured as in Table 13. Configuring the WM8804 S/PDIF transceiver in software mode allows the SPDIF sample rates of up to 192 kHz to be supported.

Table 13 WM8804 Software Mode Configuration



S/PDIF Transceiver Configuration



S/PDIF Digital Audio Signal Routing

The SPDIF Receive Error (LED4) is lit when there is no S/PDIF input source present.

If the S/PDIF transceiver is reconfigured while the Dunglass system is powered, the WM8804 needs to be reset for the changes to take effect. The WM8804 can be reset using the SPDIF RESET button.

Once the above jumper settings have been implemented, the following SCS scripts can be used to configure the WM8804 transceiver and the CS4282P CODEC for audio playback using the S/PDIF input. The applicable script should be selected according to the sample rate of the SPDIF signal. See Section 2 for further information on running the SCS scripts.

- 48kHz/44.1kHz: **SPDIF_CS4282P_MCLK_256FS_48k_44k1_Secondary_I2S.py**
- 96kHz/88.2kHz: **SPDIF_CS4282P_MCLK_256FS_96k_88k2_Secondary_I2S.py**
- 176.4kHz: **SPDIF_CS4282P_MCLK_128FS_176k4_Secondary_I2S.py**
- 192kHz: **SPDIF_CS4282P_MCLK_128FS_192k_Secondary_I2S.py**

5.3 S/PDIF Transceiver Digital Audio Signal Routing

The WM8804 transceiver converts the S/PDIF input signal to 2-channel I2S or Left Justified format. The output from the S/PDIF receiver must be routed to ASP_DIN1 on the SPDIF IN header.

The WM8804 transceiver converts the 2-channel ASP output to S/PDIF format. The input to the S/PDIF transmitter must be set to ASP_DOUT1 on the SPDIF OUT header

If the WM8804 is configured in software mode, the ASP format is selectable (I2S or Left Justified). In hardware mode, the ASP format is Left-Justified only.

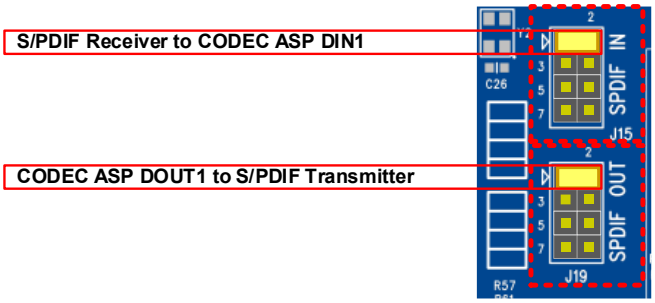


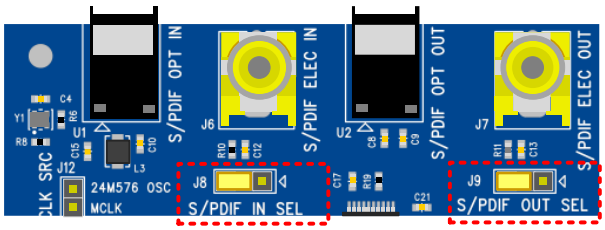
Figure 17: SPDIF Input/Output Jumper Link Configuration

5.4 Selecting Optical or Electrical S/PDIF

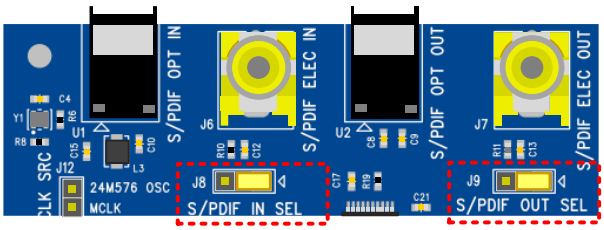
The S/PDIF IN SEL and S/PDIF OUT SEL headers are used to select the optical or electrical S/PDIF interfaces for the respective signal paths. The headers are configured as shown in Table 14.

The Dunglass system supports S/PDIF input/output at sample rates up to 96 kHz (optical) or up to 192 kHz (electrical).

Table 14 SPDIF I/O Configuration



Optical Input & Output



Electrical Input & Output

6 Input and Output Buffer Circuits

6.1 Input Buffer

The analog input channels are supported using external buffer circuits. The buffer circuit implemented on the DC4282P-CODEC daughter card is shown in Figure 18, comprising a high-pass filter and anti-alias filter. The buffer circuit shown produces a full-scale (0 dBFS) output from a 8 V_{RMS} differential input.

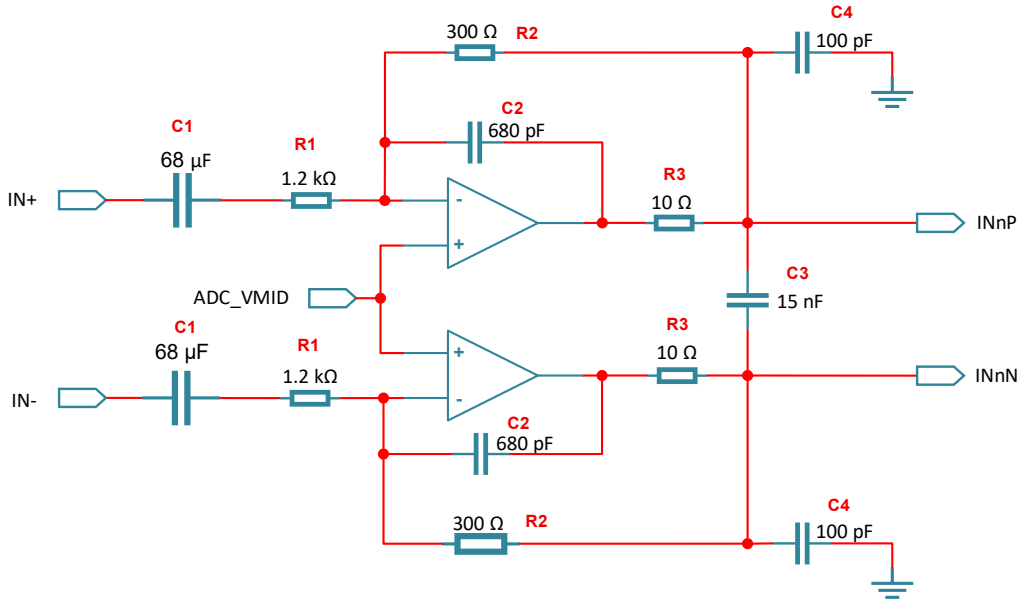


Figure 18: Differential Input Buffer

The high-pass filter is provided by the AC-coupling capacitor C1 and series resistor R1. Using the values shown, the –3 dB cut-off frequency (F_C) can be calculated using the following equation:

$$F_c = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 1200 \times (68 \times 10^{-6})} = 1.95\ Hz$$

The anti-alias filter is provided by the op-amp and associated feedback components. The objective is to provide a flat passband for the audio input bandwidth, and sufficient attenuation at the ADC-modulator sample frequency. The low output impedance of the circuit minimizes the distortion of the signal path.

The typical filter shown provides a –3 dB cut-off frequency around 640 kHz, suitable for the highest CS4282P sample rate of 768 kHz. The attenuation slope of –12 dB/octave results in 42 dB attenuation at the ADC-modulator sample frequency of 6.144 MHz.

The –3 dB cut-off frequency is approximated by the following equation:

$$F_c = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 2(C_3 + C_4)}} = \frac{1}{2\pi\sqrt{300 \times 10 \times 680 \times 10^{-12} \times 2 \times 15 \times 10^{-9}}} = 640\ kHz$$

The gain of the input buffer is determined by the ratio R1/R2. The gain should be configured to provide a full-scale signal of 2 V_{RMS} at the input to the CS4282P. The values shown in Figure 18 provide a ratio of 4; in this configuration, the buffer supports a full-scale input of 8 V_{RMS}.

6.2 Output Buffer

The analog output channels are supported using external buffer circuits. The buffer circuit implemented on the DC4282P-CODEC daughter card is shown in Figure 19, comprising current-to-voltage conversion and out-of-band filtering. The buffer circuit shown produces 8 V_{RMS} differential output from a full-scale (0 dBFS) digital input.

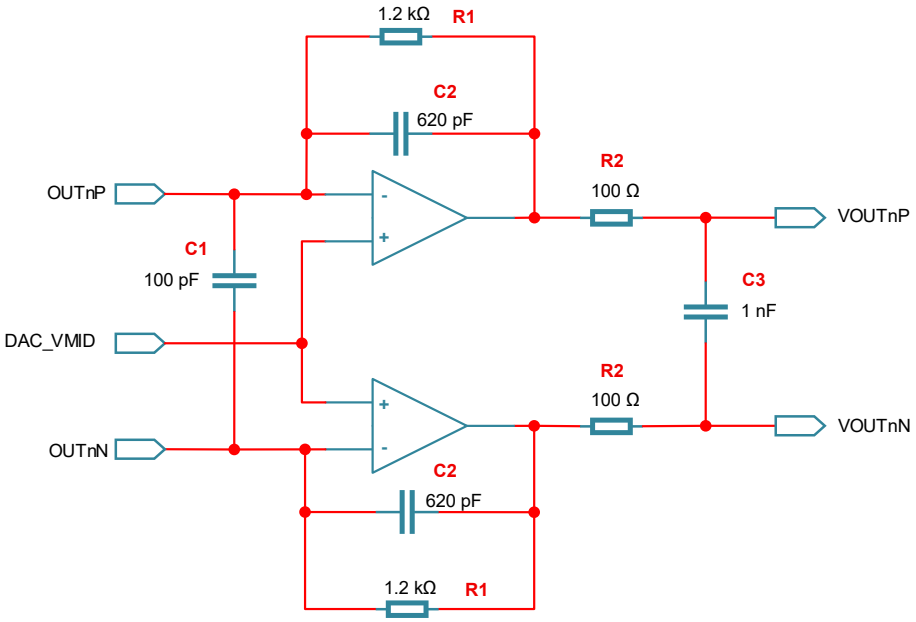


Figure 19: Differential Output Buffer

The full-scale output voltage is determined by the feedback resistor R1. The value of R1 can be calculated using the following equation:

$$R_1(k\Omega) = \frac{Full\_scale\ output\ voltage\ (V_{RMS})}{6.64}$$

The required value of R1 is shown in Table 15 for a range of typical operating configurations. Note that the THD+N performance may be degraded with increased full-scale output voltage.

Table 15 Feedback Resistor (R1) Selection

Full-Scale Output Voltage	Feedback Resistor (R1)
2 V_{RMS}	300 Ω
4 V_{RMS}	600 Ω
8 V_{RMS}	1.2 kΩ

A low-pass filter is provided using R1 and C2. The filter should be designed to provide a flat passband for the audio bandwidth, while attenuating out-of-band noise. The –3 dB cut-off frequency (F_C) can be calculated using the following equation:

$$F_C = \frac{1}{2\pi R_1 C_2}$$

The recommended value of C2 is shown in Table 16 for different values of R1. The recommended configuration provides a –3 dB cut-off around 220 Hz.

Table 16 Feedback Capacitor (C2) Selection

Resistor	Capacitor	-3 dB Cutoff
1.2 kΩ	620 pF	214 kHz
600 Ω	1.2 nF	221 kHz
300 Ω	2.4 nF	221 kHz

Additional filtering is provided using R2 and C3. The recommended components attenuate out-of-band noise, while minimizing the capacitive loading on the op-amp device. Using the values shown, the –3 dB cut-off frequency (F_C) can be calculated using the following equation:

$$F_C = \frac{1}{2\pi R_2 2C_3} = \frac{1}{2 \times \pi \times 100 \times 2 \times 1 \times 10^{-9}} = 795.8\ kHz$$

The component IDs for the filter components on the DC4282P-CODEC daughter card are identified in Table 17.

Table 17 DC4282P-CODEC Component IDs

Output Channel	DAC Output Capacitor (C1)	Feedback Resistor (R1)	Feedback Capacitor (C2)	Out-of-band Filter Resistor (R2)	Out-of-band Filter Capacitor (C3)
OUT1	C103	R380, R382	C247, C248	R381, R383	C118
OUT2	C104	R440, R441	C264, C265	R449, R450	C121

7 Performance Plots

7.1 ADC Performance Plots

ADC Filter Slow Roll-off, Minimum Phase, 48kHz Sample Rate

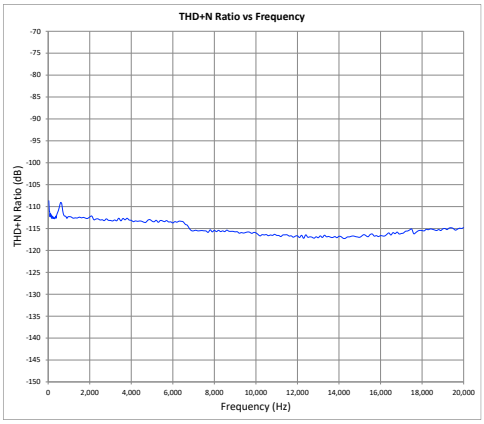


Figure 20: –1dBFS THD+N ratio Vs Frequency

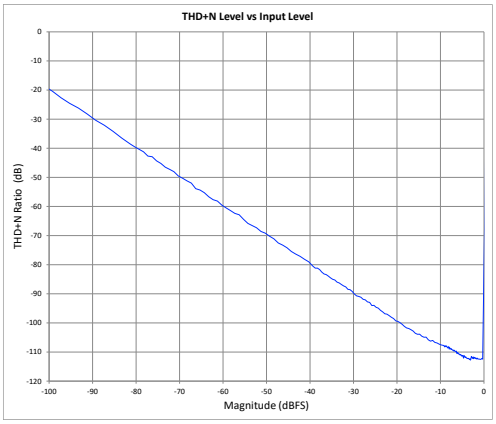


Figure 21: THD+N ratio Vs Magnitude

ADC Filter Slow Roll-off, Minimum Phase, 96kHz Sample Rate

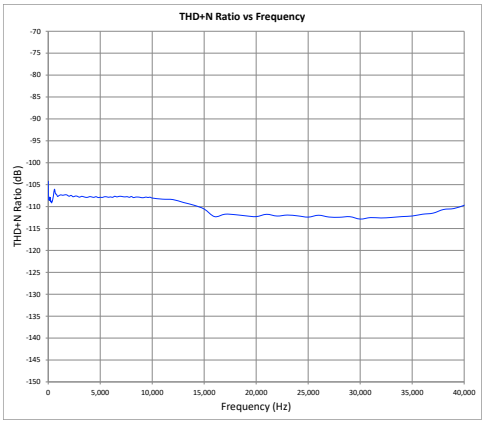


Figure 22: –1dBFS THD+N ratio Vs Frequency

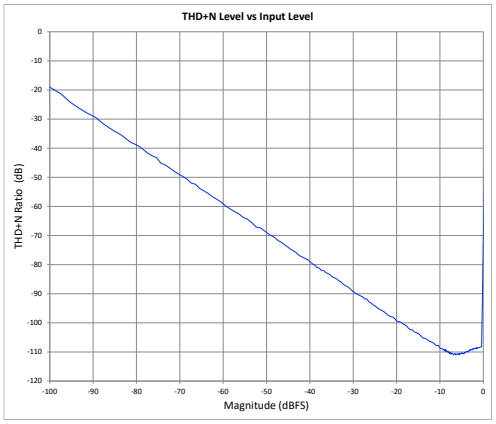


Figure 23: THD+N ratio Vs Magnitude

ADC Filter Slow Roll-off, Minimum Phase, 192kHz Sample Rate

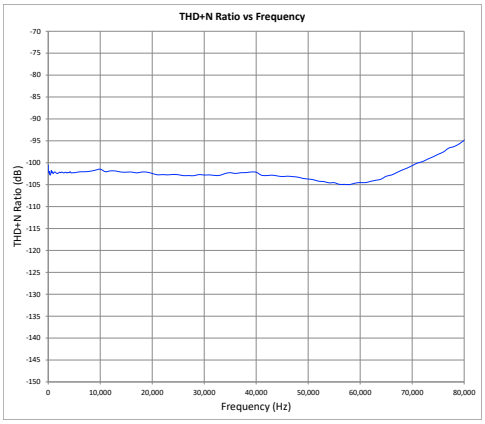


Figure 24: –1dBFS THD+N ratio Vs Frequency

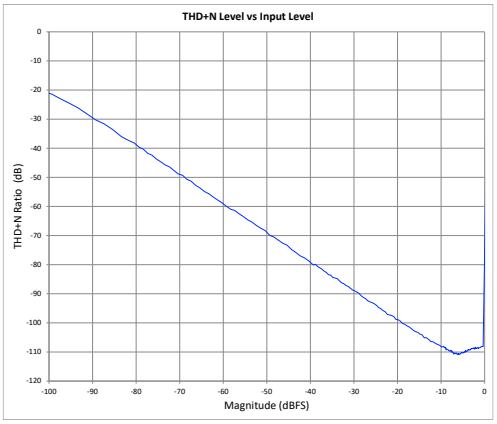


Figure 25: THD+N ratio Vs Magnitude

7.2 DAC Performance Plots

DAC Filter Slow Roll-off, Linear Phase, 48kHz Sample Rate

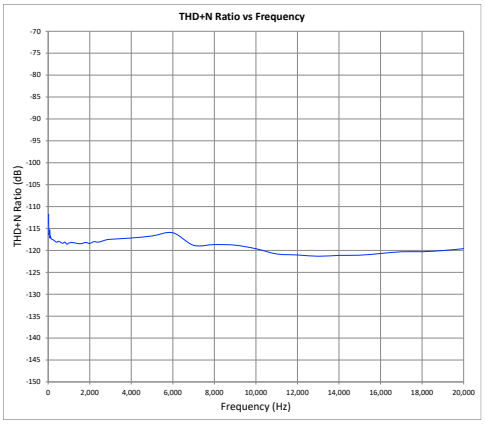


Figure 26: –1dBFS THD+N ratio Vs Frequency

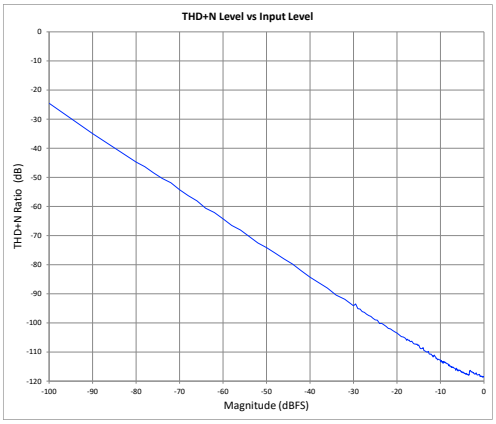


Figure 27: THD+N ratio Vs Magnitude

DAC Filter Slow Roll-off, Linear Phase, 96kHz Sample Rate

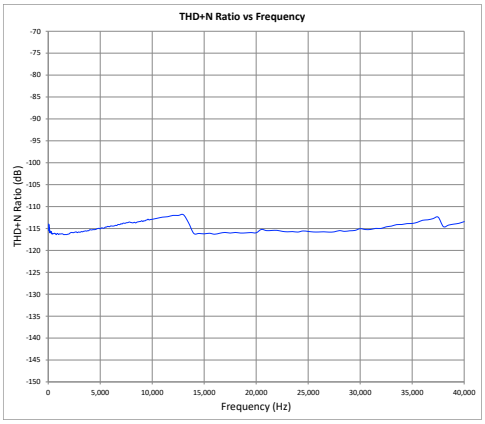


Figure 28: –1dBFS THD+N ratio Vs Frequency

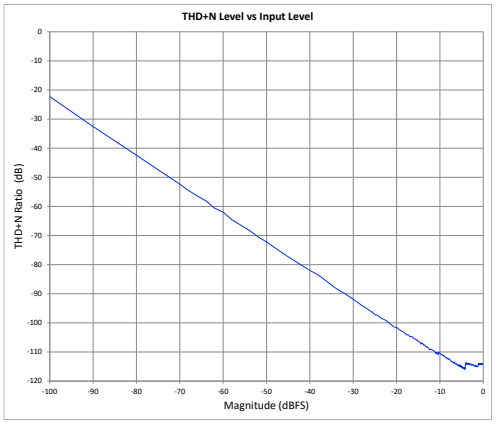


Figure 29: THD+N ratio Vs Magnitude

DAC Filter Slow Roll-off, Linear Phase, 192kHz Sample Rate

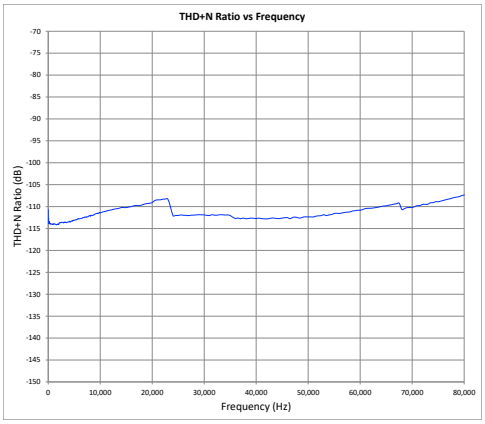


Figure 30: –1dBFS THD+N ratio Vs Frequency

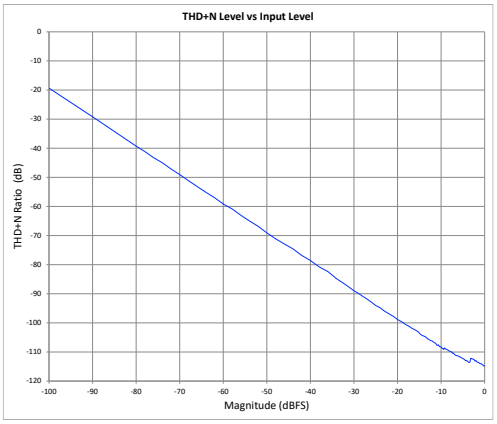


Figure 31:THD+N ratio Vs Magnitude

8 Notices

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Unmodified USB Audio 2.0 Device Software source code is available from www.xmos.ai under XMOS PUBLIC LICENCE: Version 1.

9 Revision History

Revision	Changes
DB1 JUL 2025	• Initial version.

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