DC4304P/4S/8P/8S-DAC User Guide

Introduction

The DC43xx-DAC are daughter cards for the Cirrus Logic Dunglass (CDB-PROAUDIO) system for high performance ADC, DAC and codec devices. This user guide details how to connect the DC43xx-DAC to a Dunglass (CDB-PROAUDIO) system platform and how to get started. The User Guide covers the following daughter cards

- DC4304P-DAC
- DC4304S-DAC
- DC4308P-DAC
- DC4308S-DAC

The default jumper link configuration for DC4308P/8S-DAC is shown in Figure 1 and the default jumper link configuration for DC4304P/4S is shown in Figure 2.

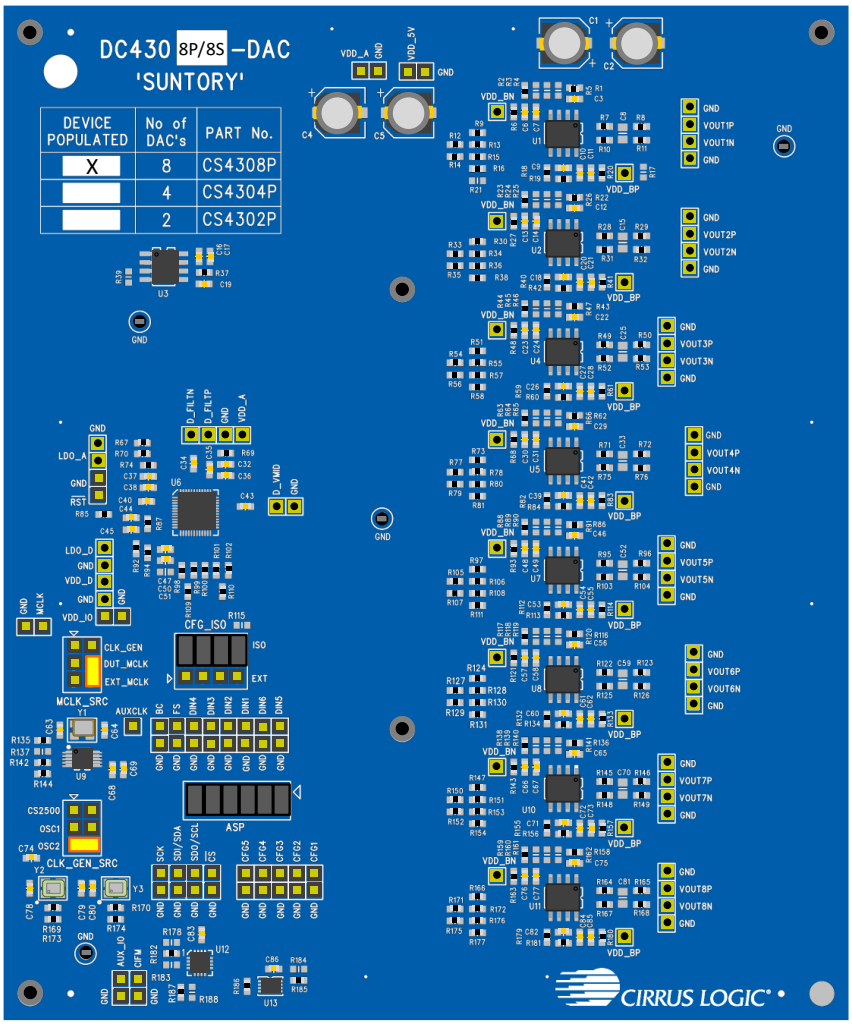


Figure 1: DC4308P/8S-DAC Daughter Card

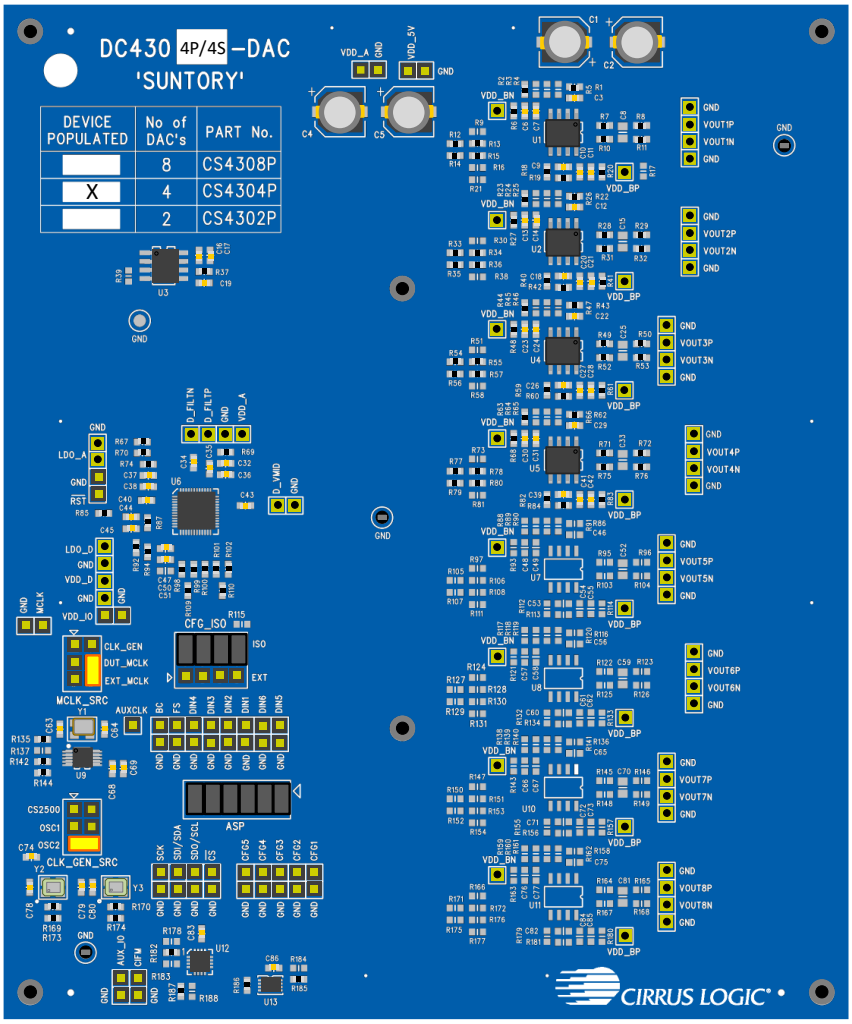


Figure 2: DC4304P/4S-DAC Daughter Card

Table of Contents

1 Hardware Connections

The Dunglass system supports interchangeable daughter cards for a variety of ADC, DAC and codec devices.

Caution:

Daughter cards should not be inserted or removed while the Dunglass system is powered. Fully disconnect or power down external power supply before changing daughter cards.

For more information on the Dunglass (CDB-PROAUDIO) platform, refer to the CDB-PROAUDIO User Guide.

1.1 How to Connect DC430xx-DAC onto the Dunglass System

The DC4304P/4S/8P/8S-DAC is a 4-header daughter card and should be plugged onto DCJ1, DCJ2, DCJ3 & DCJ4. The daughter card connectors are keyed and will only plug in one way. There is also an alignment dot on each board to help with placement.

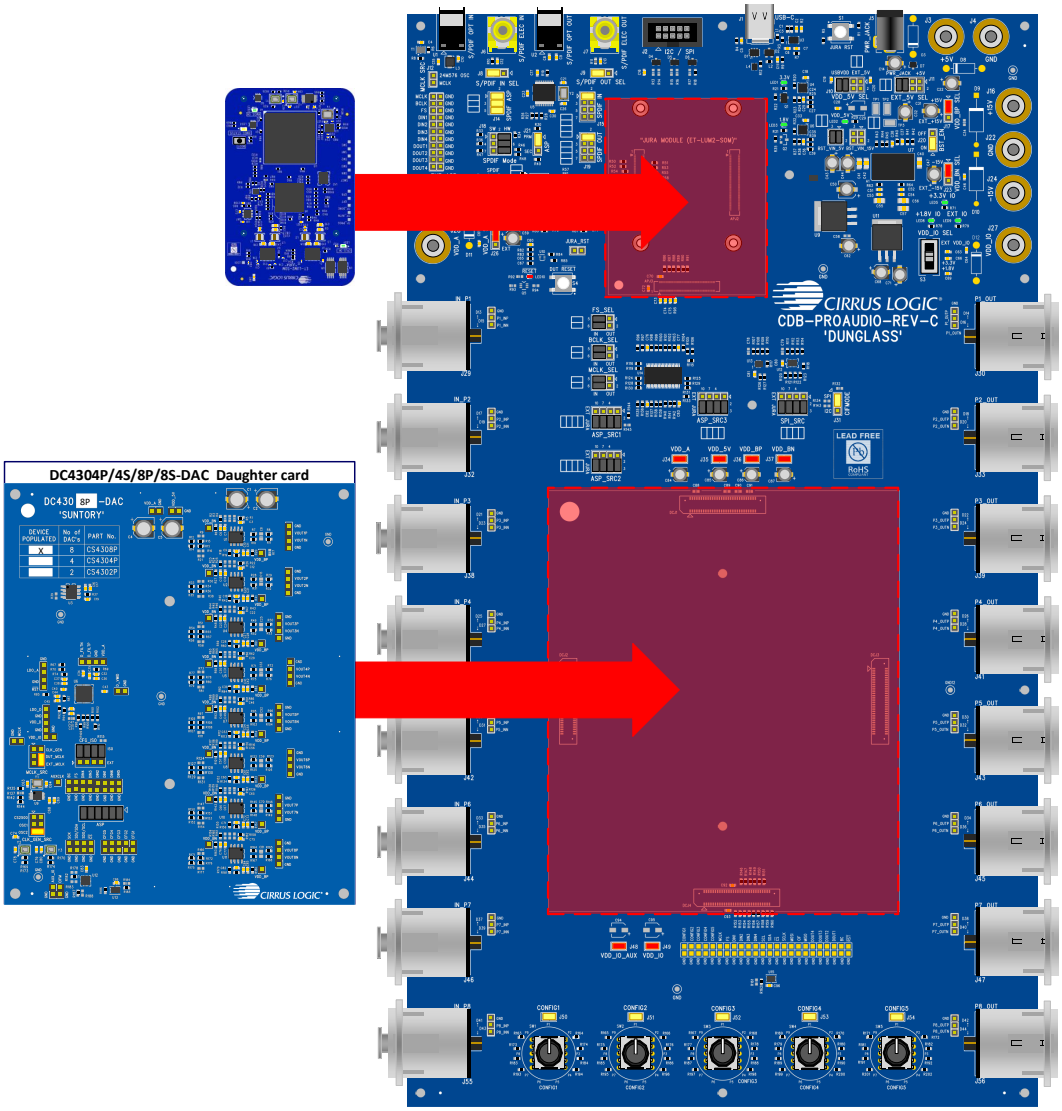


Figure 3: How to Connect DC4304P/4S/8P/8S-DAC onto the Dunglass System

1.2 USB & Power Connection

Dunglass is powered using a 5V external power supply and is controlled via a single USB connection. The Jura module supports the following functions via the USB connection:

- I2C/SPI communications to control device and board.
- Multichannel USB streaming audio (USB class 2).

The Dunglass board is provided with a USB-A to USB-C cable and a 5V wall supply.

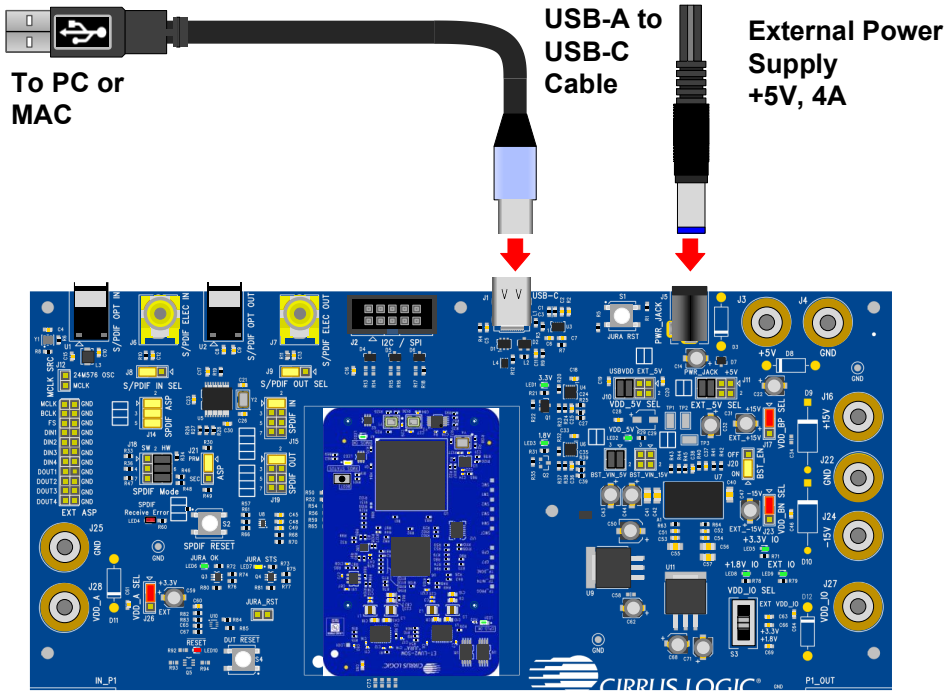


Figure 4: Dunglass (CDB-PROAUDIO) USB & Power Connection

A Total Phase Aardvark connector can be used for I2C/SPI communication. Refer to the CDB-PROAUDIO User Guide for more details.

1.2.1 JURA Module

The Jura module supports I2C/SPI communication to control the Dunglass system and daughter card; it also enables multichannel USB streaming audio (USB audio Class 2).

The Jura module is connected to the Dunglass board as shown below:

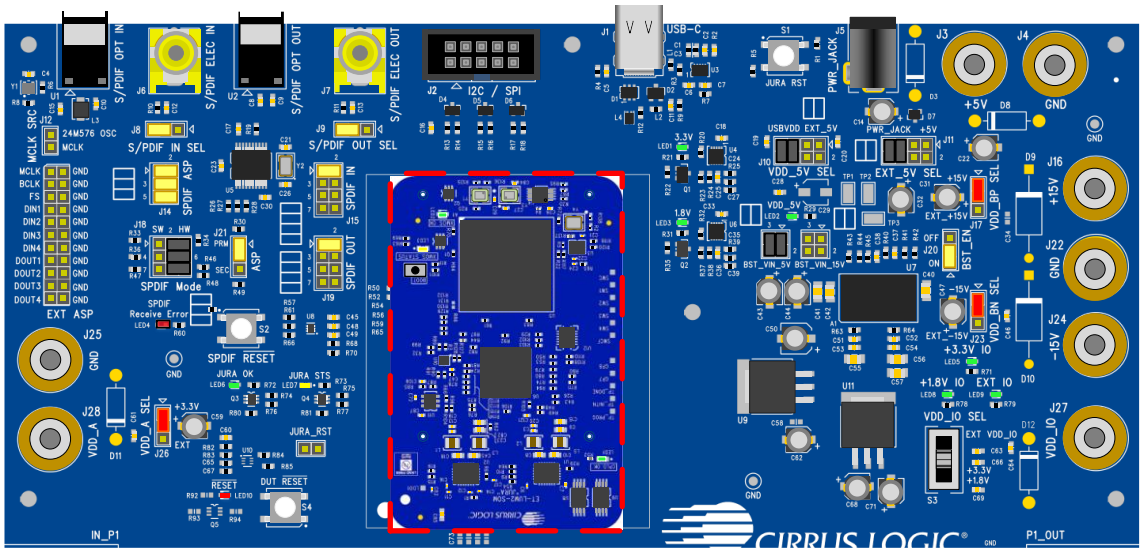


Figure 5: How to Connect JURA Module to Dunglass System

1.2.2 Dunglass Boot Procedure with Jura Module

The USB-C cable must be connected between the Dunglass system and the PC/Mac prior to powering up the board.

The boot time of the Dunglass system varies depending on the version of firmware on the Jura module but is typically in the range of 2 to 5 seconds after applying power to the board.

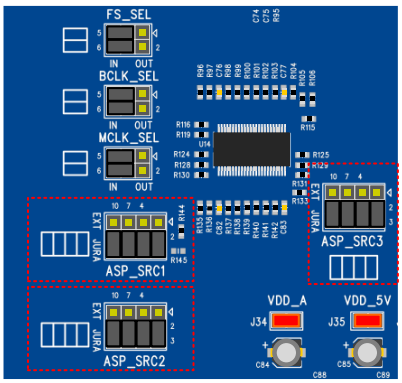
1.3 Routing the Digital Audio PCM Signals

The digital audio PCM paths to the daughter card can be routed from the Jura module, or else from the EXT ASP header and S/PDIF transceiver. The routing is configured using the ASP_SRC1, ASP_SRC2 & ASP_SRC3 headers.

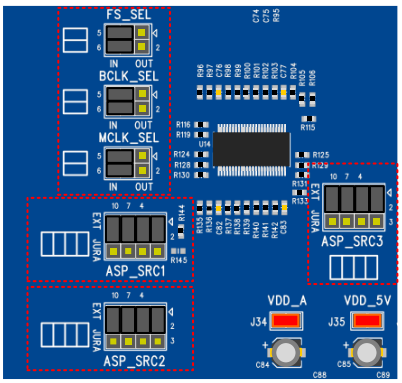
- JURA = Digital audio signals routed from Jura module.
- EXT = Digital audio signals routed from EXT ASP header/SPDIF.

The ASP_SRC1, ASP_SRC2 & ASP_SRC3 headers are configured as shown in Table 1.

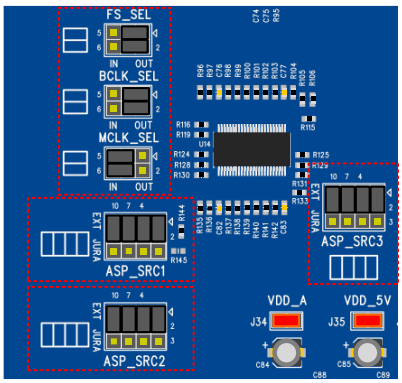
Table 1 Digital Signal Routing



Jura Module Primary Mode



EXT ASP / SPDIF Primary Mode



EXT ASP / SPDIF Secondary Mode

The Jura module always operates in Primary Mode – the MCLK, BCLK and FSYNC are generated by the Jura module, as inputs to the daughter card.

If the digital audio is routed from the EXT ASP header or S/PDIF transceiver, the direction of the MCLK, BCLK, and FSYNC signals are configured using the MCLK_SEL, BCLK_SEL & FS_SEL headers. Each signal is configured independently using the respective header.

- IN = EXT_ASP header or S/PDIF transceiver supports the signal as input to the daughter card
- OUT = EXT_ASP header or S/PDIF transceiver supports the signal as output from the daughter card

Note that the EXT ASP header and S/PDIF transceiver use 3.3 V logic levels; a level shifter is incorporated to interface with the VDD_IO domain on the DC4304P/4S/8P/8S-DAC daughter card.

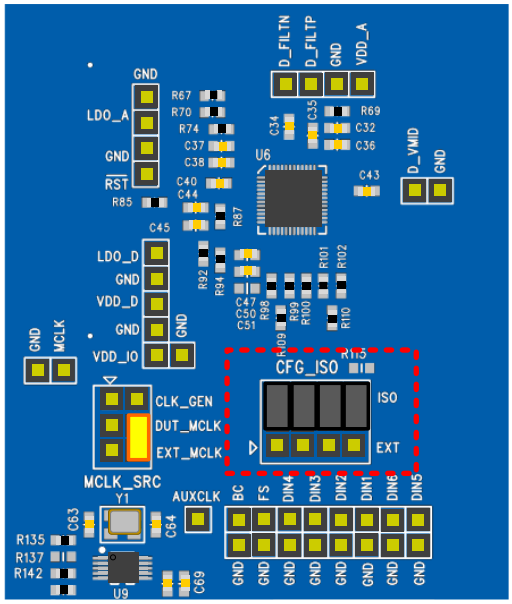
1.4 Selection of Hardware/Software Control Mode

The CS4304P/4S/8P/8S supports Hardware and Software modes. The hardware and software modes are set via the CFG_ISO header on the DC4304P/4S/8P/8S-DAC and the rotary switches on the Dunglass system. The jumper link must be configured as in Table 2.

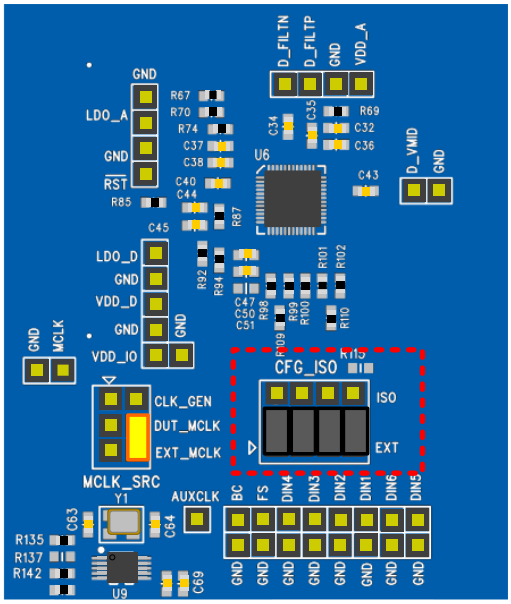
- ISO = Software mode.
- EXT = Hardware mode.

In Hardware mode, rotary switches are used to select the desired configuration. See Section 4 for information on hardware mode.

Table 2 Software/Hardware mode Jumper Link Configuration for DC4304P/4S/8P/8S-DAC



Software Mode Jumper Link Configuration



Hardware Mode Access Jumper Link Configuration

Note that Hardware mode is only supported for VDD_IO = 3.3V on the DC4304P/4S/8P/8S-DAC due to the rotary switch pull-up supply = 3.3V on the Dunglass system.

1.5 DSD Input Connection

The CS4304P/4S/8P/8S supports Direct Stream Digital (DSD) input interface. The DSD interface is supported in software control mode only. Refer to the respective datasheet for further details of DSD interface support.

To configure the DC4304P/4S/8P/8S-DAC for DSD the ASP header link must be removed. With the ASP header link removed, the DSD_CLK can be applied to the BC test point and the DSD Data connected to DIN1–DIN4 for CS4304P/4S and DIN1- DIN6 for CS4308P/8S. Note the MCLK must be synchronous with the DSD_CLK and DSD Data input and should be applied to the MCLK test point.

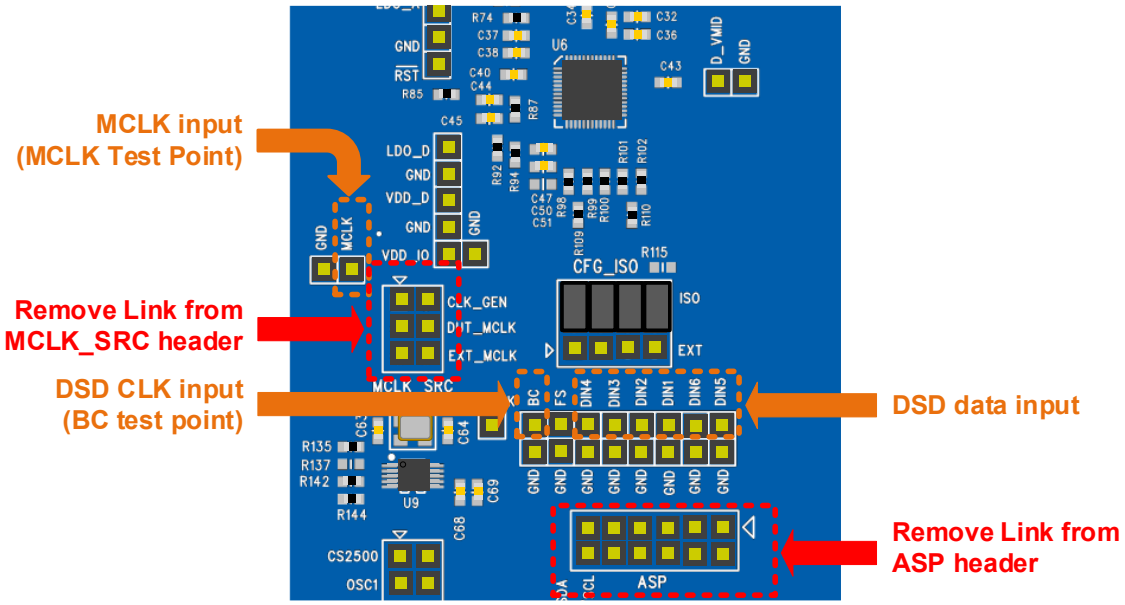


Figure 6: DC4304P/4S/8P/8S-DAC DSD Jumper Link Configuration

The DSD logic levels must be the same as the VDD_IO voltage set on the Dunglass system.

1.6 DC4304P/4S/8P/8S-DAC MCLK Source Selection

The DC4304P/4S/8P/8S-DAC board provides two on-board oscillators that can be used as an MCLK source for the CS4304P/4S/8P/8S. The oscillators are configured for different frequencies; the oscillators are enabled by removing the applicable resistor on the DC4304P/4S/8P/8S-DAC board.

- OSC1 (22.5792 MHz). Enabled by removing R173.
- OSC2 (24.576 MHz). Enabled by removing R174.

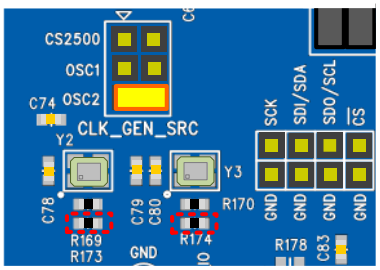
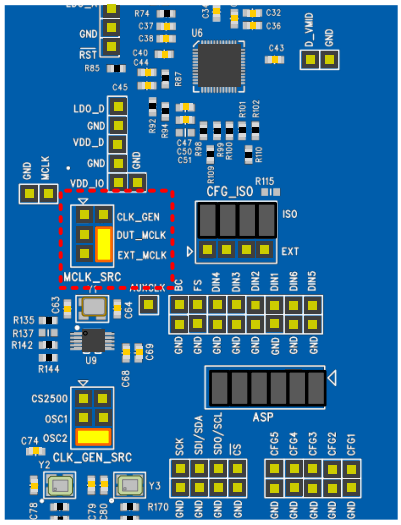


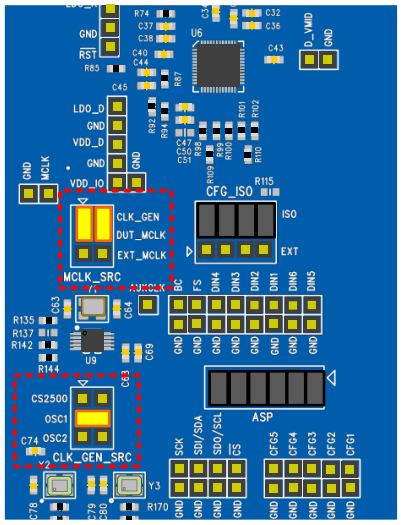
Figure 7: Enabling On board Oscillators

The MCLK source is configured as shown in Table 3.

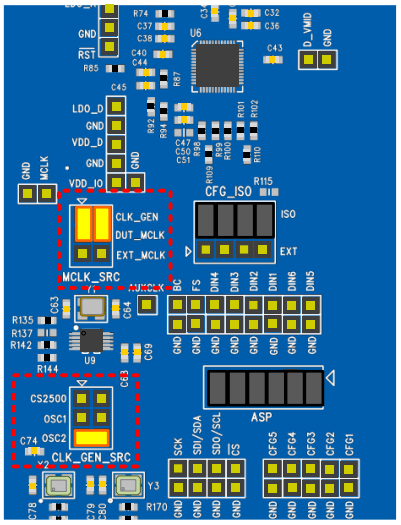
Table 3 MCLK source Jumper Link Config



MCLK source = Dunglass System (Default)



MCLK source = OSC1



MCLK source = OSC2

2 Driver Installation and SoundClear Studio Support

2.1 SoundClear Studio

SoundClear Studio (SCS) is a PC/Mac-based tool used to configure Cirrus Logic devices. The tools suite provides support for evaluation and development and can be used with Dunglass system and associated daughter cards.

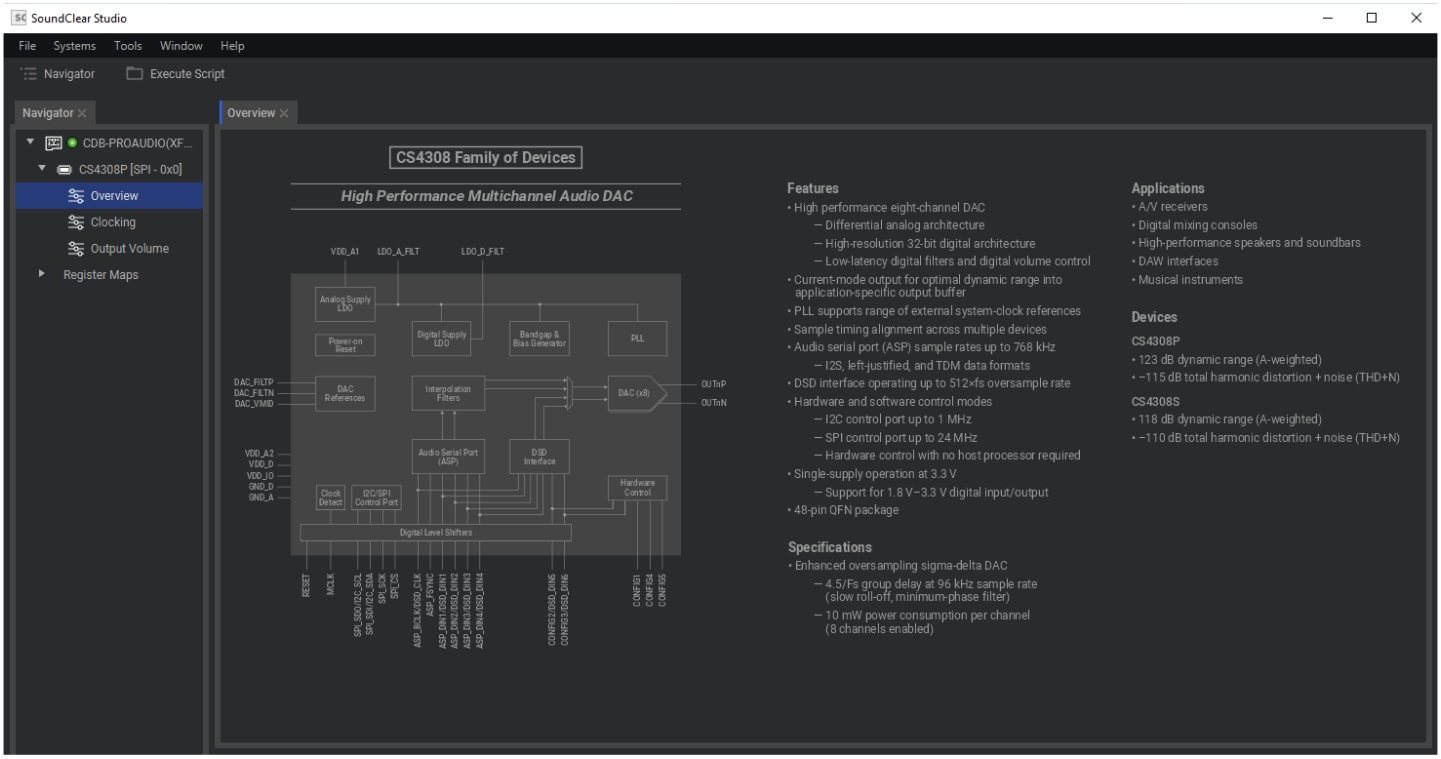


Figure 8: SoundClear Studio

2.1.1 Download SoundClear Studio Software & Drivers

SoundClear Studio and associated software collateral required for the Dunglass system can be downloaded from https://cirrus.com.

- *https://cirrus.com/products/cs4304p/*
- *https://cirrus.com/products/cs4308p/*

The required components are as follows:

- **SoundClear Studio 2.1**. Run the appropriate installer on your Windows or macOS computer to install SoundClear Studio.
- **CS4304 SCS Package**. Install this in SoundClear Studio to incorporate the CS4304-specific software components in SoundClear Studio for CS4304P & CS4304S. See Section 2.2.1 for details on how to install an SCS package.
- **CS4308 SCS Package**. Install this in SoundClear Studio to incorporate the CS4308-specific software components in SoundClear Studio for CS4308P & CS4308S. See Section 2.2.1 for details on how to install an SCS package.
- **Jura Windows Setup**. On Windows computers, run the Cirrus Logic USB Audio Setup to install the driver that enables SoundClear Studio to communicate with the Jura board.

2.2 SoundClear Studio Quick Start Guide

2.2.1 Installing Packages

Each daughter card has its own individual SoundClear Studio package that must be installed separately from the main SoundClear Studio Software. These are installed from the main menu using **"File → Install Package..."**. Multiple packages can be installed together by selecting more than one using the file dialog.

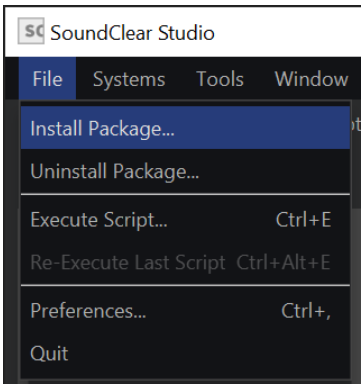


Figure 9: SoundClear Studio – Installing Board Packages

2.2.2 SoundClear Studio User Guide

The SoundClear Studio User Guide can be accessed from the main menu using **"Help → Open Help Contents..."**

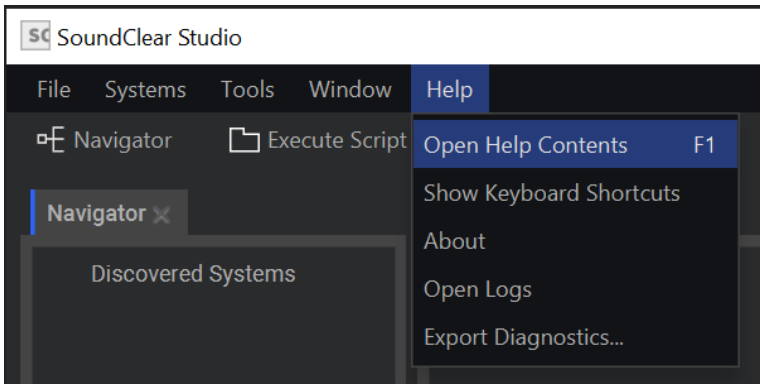


Figure 10: SoundClear Studio – User Guide

2.2.3 Creating a Virtual System

A virtual (non-hardware) version of the system can be created using **“Systems → Add Virtual System..."**

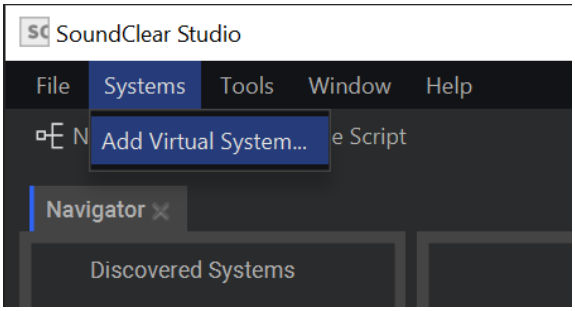


Figure 11: SoundClear Studio – Creating a Virtual System

This opens a dialog box to select an installed system (shown here is the DC4308-DAC):

Note: The DC4308-DAC supports the DC4308P-DAC & DC4308S-DAC boards

Note: The DC4304-DAC supports the DC4304P-DAC & DC4304S-DAC boards

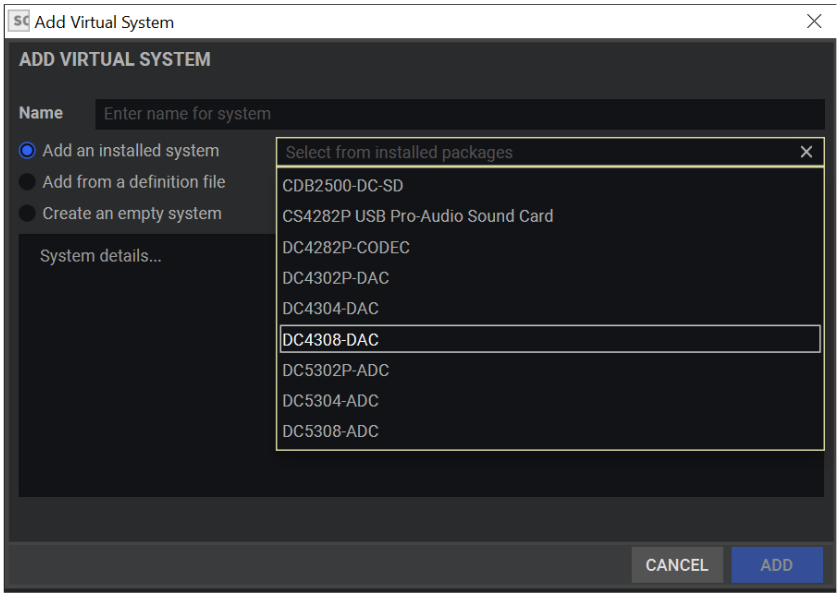


Figure 12: SoundClear Studio – Adding a Virtual System

Once created, a virtual system enables the user to interact with virtual versions of the device register map and helper panels.

2.2.4 Adding an Existing System

SoundClear Studio automatically detects board hardware such as the Jura module and Cirrus Logic devices. In the event of devices not being detected automatically, a device can be added manually. Right click on the system and select **"Add Device…"**

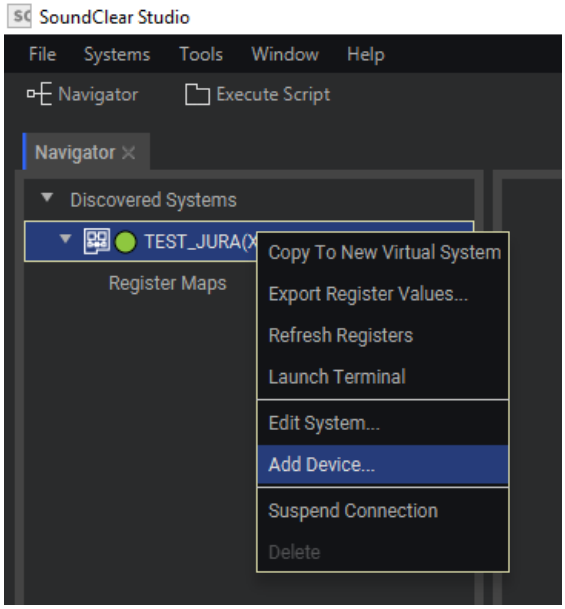


Figure 13: SoundClear Studio – Adding an Existing Device

Then select the device from those installed, along with the protocol and address of the part (this can be edited again by right clicking on the device and selected **"Edit Device..."**):

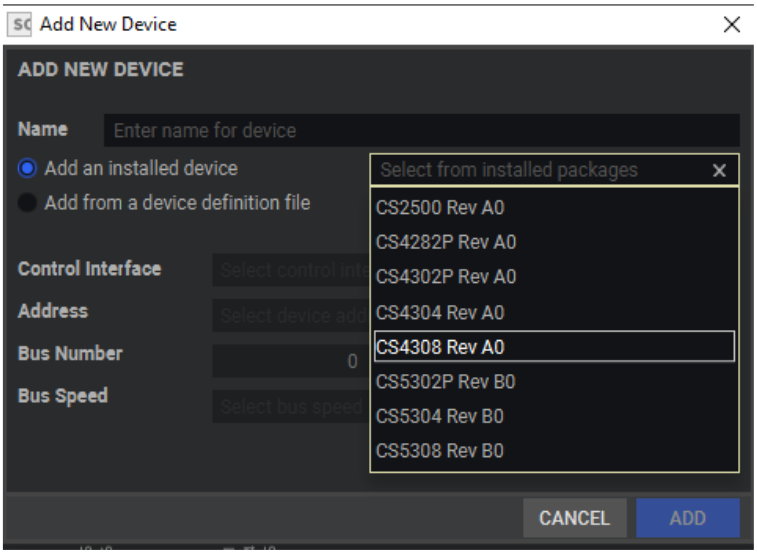


Figure 14: SoundClear Studio – Adding an Existing Device

2.2.5 Executing SoundClear Studio Scripts

SoundClear Studio provides the ability to interact with the device register map using Python scripts. These scripts can sequence register operations to configure the desire states, which can then be executed from SoundClear Studio using **"File→Execute Script…"**

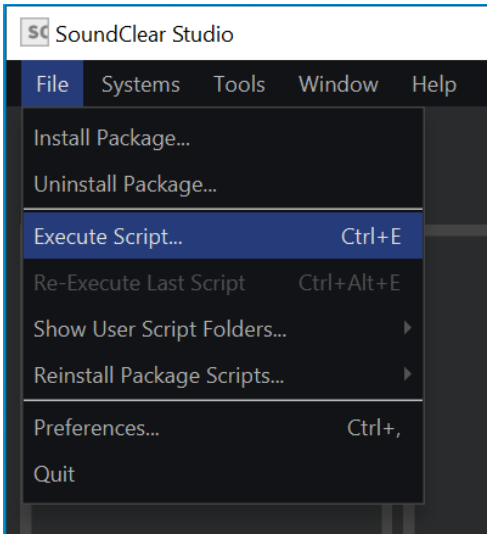


Figure 15: SoundClear Studio – Executing Script

The CS4304 / CS4308 SoundClear Studio package installs a set of scripts to configure the device for common use cases. These are available at <User Documents>\Cirrus Logic\SCS\Scripts\<Package Name>.

The scripts can be accessed via **"File→Show User Script Folder→CS4304 Scripts or CS4308 Scripts"**

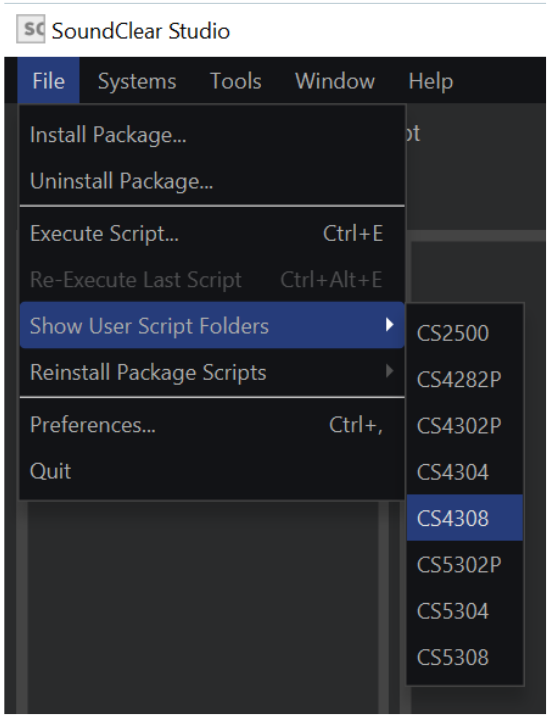


Figure 16: SoundClear Studio – Show User Script Folder

3 DC4304P/4S/8P/8S-DAC Software Mode Quick Start

After installing the SoundClear Studio software and the CS4308 SCS package or CS4304 SCS package, follow the steps below to get up and running quickly:

- Connect the hardware as shown in Figure 3
- Connect USB cable to PC
- Power up the system and ensure JURA OK, 1.8V, 3.3V, VDD_5V LEDs are illuminated.
- Configure signal routing as shown in Table 1
  - For SPDIF output see Section 5
- Start SoundClear Studio
  - SoundClear Studio should auto-detect the DC43xx-DAC daughter card. If not, follow the procedure specified in Section 2.2.4
- Run one of the scripts from the following location.
  - <User Documents>\Cirrus Logic\SCS\Scripts\<Package Name>.

4 Hardware Mode Control

The Dunglass system supports the hardware control modes for Cirrus Logic high performance ADC, DAC and Codec devices. These are supported via the rotary switches on the Dunglass system.

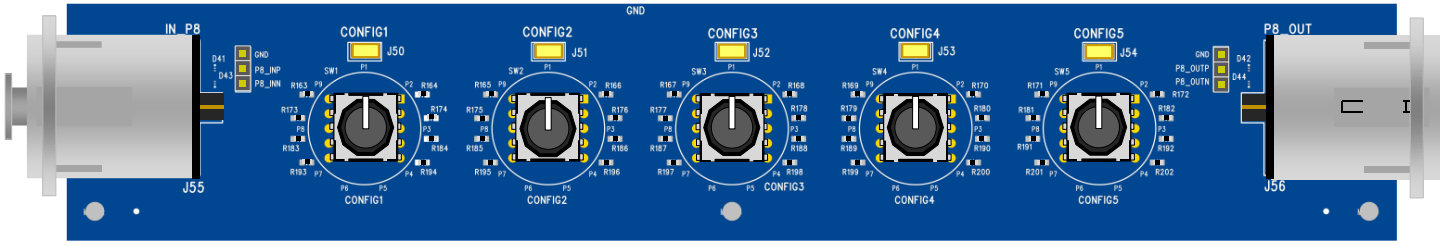


Figure 17: Dunglass Rotary Switches for Hardware Control Mode

Each switch has silkscreen on the board to indicate the position of the switch. Each switch position enables a pull resistor on the respective CONFIG pin to VDD_A or ground.

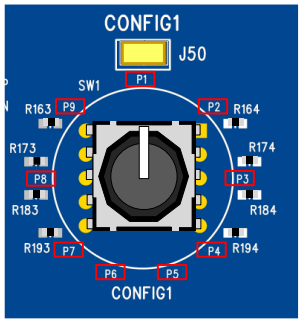


Figure 18: Rotary Switch

Note that, if the rotary switches are reconfigured while the Dunglass system is powered, the daughter card needs to be reset for the changes to take effect. This is done by pushing the DUT RESET button.

Note that Hardware mode is only supported for VDD_IO = 3.3V on the DC4304P/4S/8P/8S-DAC due to the rotary switch pull-up supply = 3.3V on the Dunglass system.

4.1 Hardware Mode Rotary Switch Settings

The CS4304P/4S/8P/8S supports hardware mode. The rotary switch functions are described in the following tables. Refer to the respective datasheet for further details of the hardware-mode control options.

The CONFIG1 pin selects the ASP operating configuration.

Table 4: CONFIG1 Hardware Control – ASP Configuration

Switch Position	Config Pin Configuration		Description
P1	Pull-up to 3.3V	0 Ω	Software control mode (I2C/SPI)
P2		4.7 kΩ	ASP Primary Mode, 44.1 kHz, 48 kHz sample rate
P3		22 kΩ	ASP Primary Mode, 88.2 kHz, 96 kHz sample rate
P4		100 kΩ	ASP Primary Mode, 176.4 kHz, 192 kHz sample rate
P5	Pull-Down to GND	100 kΩ	ASP Secondary Mode, 176.4 kHz, 192 kHz sample rate
P6		22 kΩ	ASP Secondary Mode, 88.2 kHz, 96 kHz sample rate
P7		4.7 kΩ	ASP Secondary Mode, 44.1 kHz, 48 kHz sample rate
P8		0 Ω	ASP Secondary Mode, autodetect sample rate
P9	No Connection		

1. Autodetect sample rate is only supported in MCLK 256 fs(base), MCLK 512 fs(base) or MCLK 1024 fs(base) clocking configurations.

The CONFIG2 pin selects the ASP format and TDM timeslots option.

Table 5: CONFIG2 Hardware Control – ASP Configuration

Switch Position	Config Pin Configuration		Description
P1	Pull-up to 3.3V	0 Ω	ASP TDM Mode—minimum time slots
P2		4.7 kΩ	ASP TDM Mode—maximum time slots
P3		22 kΩ	
P4		100 kΩ	
P5	Pull-Down to GND	100 kΩ	
P6		22 kΩ	
P7		4.7 kΩ	ASP Left-Justified Mode
P8		0 Ω	ASP I^2S Mode
P9	No Connection		

The CONFIG3 pin selects the TDM slot selection in TDM Mode. Slot selection for CS4304P/4S is shown in Table 6; Slot selection for CS4308P/8S is shown in Table 7.

Table 6: CS4304P/4S CONFIG3 Hardware Control – TDM Slot Selection

Switch Position	Config Pin Configuration		Description
P1	Pull-up to 3.3V	0 Ω	Slots 12–15
P2		4.7 kΩ	
P3		22 kΩ	Slots 8–11
P4		100 kΩ	
P5	Pull-Down to GND	100 kΩ	Slots 4–7
P6		22 kΩ	
P7		4.7 kΩ	Slots 0–3
P8		0 Ω	
P9	No Connection		

Table 7: CS4308P/8S CONFIG3 Hardware Control – TDM Slot Selection

Switch Position	Config Pin Configuration		Description
P1	Pull-up to 3.3V	0 Ω	Slots 8–15
P2		4.7 kΩ	
P3		22 kΩ	
P4		100 kΩ	
P5	Pull-Down to GND	100 kΩ	Slots 0–7
P6		22 kΩ	
P7		4.7 kΩ	
P8		0 Ω	
P9	No Connection		

The CONFIG4 pin selects the clock reference and ASP channel ordering.

Table 8: CONFIG4 Hardware Control – Clocking Configuration

Switch Position	Config Pin Configuration		Clock Reference	PLL	Channel Order
P1	Pull-up to 3.3V	0 Ω	BCLK = 64 fs	Enabled	Default
P2		4.7 kΩ	MCLK = 1024 fs(base)	Bypass	Default
P3		22 kΩ	MCLK = 256 fs(base)	Enabled	Default
P4		100 kΩ	MCLK = 512 fs(base)	Enabled	Default
P5	Pull-Down to GND	100 kΩ	MCLK = 512 fs(base)	Enabled	Reversed
P6		22 kΩ	MCLK = 256 fs(base)	Enabled	Reversed
P7		4.7 kΩ	MCLK = 1024 fs(base)	Bypass	Reversed
P8		0 Ω	BCLK = 64 fs	Enabled	Reversed
P9	No Connection				

1. fs(base) is the base sample rate.
   fs(base) = 48 kHz for 48 kHz-related sample rates; fs(base) = 44.1 kHz for 44.1 kHz-related sample rates.
2. BCLK 64 fs configuration is only supported in ASP Secondary Mode.

The CONFIG5 pin selects the digital filter.

Table 9: CONFIG5 Hardware Control – Digital Filter Selection

Switch Position	Config Pin Configuration		DAC Interpolation Filter		High-Pass Filter (HPF)
			32-48 kHz Sample Rate [1]	88.2-192 kHz Sample Rate	
P1	Pull-up to 3.3V	0 Ω	Minimum phase, slow roll-off	Minimum phase, balanced roll-off	Bypass
P2		4.7 kΩ	Minimum phase, fast roll-off	Minimum phase, fast roll-off	Bypass
P3		22 kΩ	Linear phase, slow roll-off	Linear phase, balanced roll-off	Bypass
P4		100 kΩ	Linear phase, fast roll-off	Linear phase, fast roll-off	Bypass
P5	Pull-Down to GND	100 kΩ	Linear phase, fast roll-off	Linear phase, fast roll-off	Enabled
P6		22 kΩ	Linear phase, slow roll-off	Linear phase, balanced roll-off	Enabled
P7		4.7 kΩ	Minimum phase, fast roll-off	Minimum phase, fast roll-off	Enabled
P8		0 Ω	Minimum phase, slow roll-off	Minimum phase, balanced roll-off	Enabled
P9	No Connection				

1. Fast roll-off filters are supported for all sample rates. Slow roll-off filters are not valid for 32 kHz sample rate.

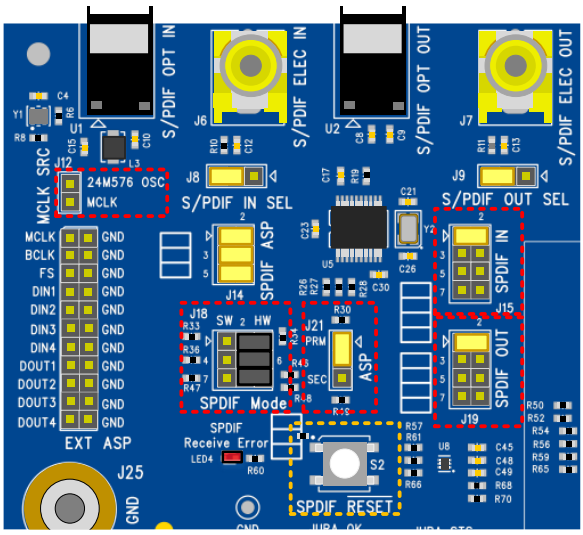
5 SPDIF

The Dunglass system supports S/PDIF input and output via optical and electrical connectors for sample rates up to 96 kHz (optical) or up to 192 kHz (electrical). The WM8804 S/PDIF transceiver on the Dunglass system can operate in software or hardware mode; in hardware mode, the sample rate is limited to 96 kHz.

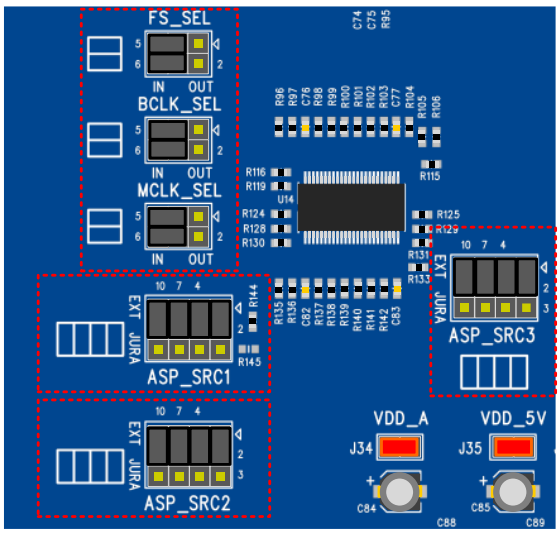
5.1 WM8804 Hardware Mode

To configure the WM8804 S/PDIF transceiver in hardware mode the jumper links on the Dunglass system must be configured as in Table 10.

Table 10 WM8804 Hardware Mode Configuration



S/PDIF Transceiver Configuration



S/PDIF Digital Audio Signal Routing

The SPDIF Receive Error (LED4) is lit when there is no S/PDIF input source present.

If the S/PDIF transceiver is reconfigured while the Dunglass system is powered, the WM8804 needs to be reset for the changes to take effect. The WM8804 can be reset using the SPDIF RESET button.

The CS4304P/4S/8P/8S can be used in software mode or hardware mode for the above S/PDIF transceiver configuration. For this user guide, it is assumed CS43xx hardware mode is used when the WM8804 is in hardware mode.

In CS43xx hardware mode, the rotary switches on the Dunglass system should be configured as shown in Table 11, depending on the sample rate of the SPDIF source.

Note that the daughter card must be reset if the rotary switches have been configured while the Dunglass system is powered. The daughter card can be reset using the DUT RESET button.

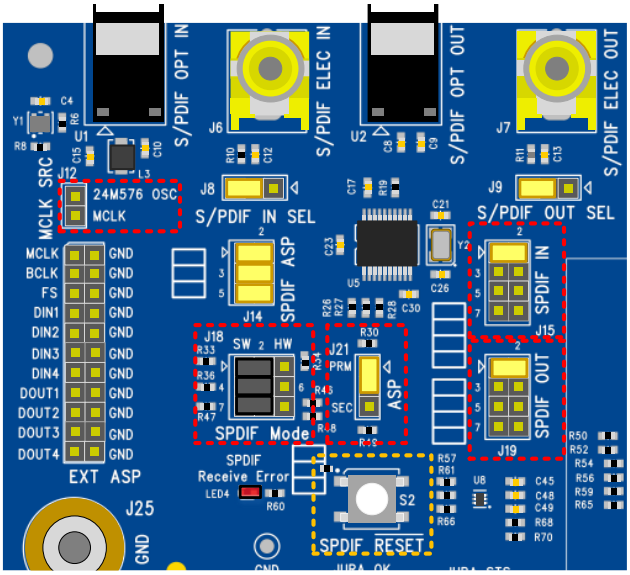
Table 11: Rotary Switch Positions for S/PDIF Input

Rotary Switch		
	fs = 48kHz/44.1kHz	**Fs = 96kHz/88.2kHz**
CONFIG1	P7 (ASP Secondary Mode, 44.1 kHz, 48 kHz sample rate)	P6 (ASP Secondary Mode, 88.2 kHz, 96 kHz sample rate)
CONFIG2	P7 (ASP Left-Justified Mode)	P7 (ASP Left-Justified Mode)
CONFIG3	N/A	N/A
CONFIG4	P3 (MCLK = 256 fsb; PLL enabled; Channel order default)	P4 (MCLK = 512 fsb; PLL enabled; Channel order default)
CONFIG5	P8 (Minimum phase, slow roll-off/balanced roll-off filter)	P8 (Minimum phase, slow roll-off/balanced roll-off filter)

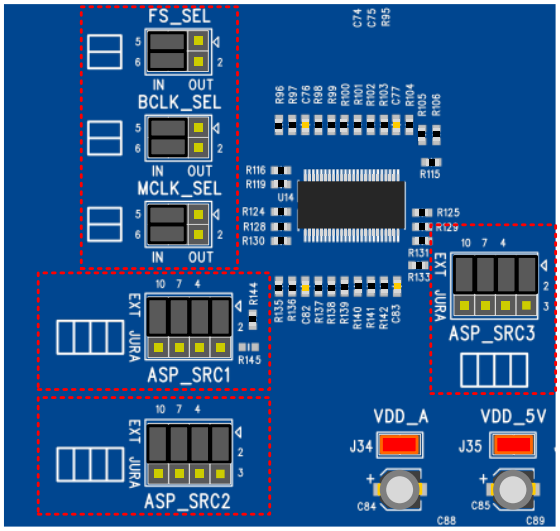
5.2 WM8804 Software Mode

To configure the WM8804 S/PDIF transceiver in software mode the jumper links on the Dunglass system must be configured as in Table 12. Configuring the WM8804 S/PDIF transceiver in software mode allows the SPDIF sample rates of up to 192 kHz to be supported.

Table 12 WM8804 Software Mode Configuration



S/PDIF Transceiver Configuration



S/PDIF Digital Audio Signal Routing

The SPDIF Receive Error (LED4) is lit when there is no S/PDIF input source present.

If the S/PDIF transceiver is reconfigured while the Dunglass system is powered, the WM8804 needs to be reset for the changes to take effect. The WM8804 can be reset using the SPDIF RESET button.

Once the above jumper settings have been implemented, the following SCS scripts can be used to configure the WM8804 transceiver and the CS4304P/4S/8P/8S DAC for audio playback using the S/PDIF input. The applicable script should be selected according to the sample rate of the SPDIF signal. See Section 2 for further information on running the SCS scripts.

- **CS4304P/4S**
  - 48kHz/44.1kHz: **SPDIF_CS4304_MCLK_256FS_48k_44k1_Secondary_I2S.py**
  - 96kHz/88.2kHz: **SPDIF_CS4304_MCLK_256FS_96k_88k2_Secondary_I2S.py**
  - 176.4kHz: **SPDIF_CS4304_MCLK_128FS_176k4_Secondary_I2S.py**
  - 192kHz: **SPDIF_CS4304_MCLK_128FS_192k_Secondary_I2S.py**
- **CS4308P/8S**
  - 48kHz/44.1kHz: **SPDIF_CS4308_MCLK_2565FS_48k_44k1_Secondary_I2S.py**
  - 96kHz/88.2kHz: **SPDIF_CS4308_MCLK_256FS_96k_88k2_Secondary_I2Spy**
  - 176.4kHz: **SPDIF_CS4308_MCLK_128FS_176k4_Secondary_I2S.py**
  - 192kHz: **SPDIF_CS4308_MCLK_128FS_192k_Secondary_I2S.py**

5.3 S/PDIF Transceiver Digital Audio Signal Routing

The WM8804 transceiver converts the S/PDIF input signal to 2-channel I2S or Left Justified format. The output from the S/PDIF Receiver can be routed to any of the four ASP_DIN traces via the SPDIF IN header.

If the WM8804 is configured in software mode, the ASP format is selectable (I2S or Left Justified). In hardware mode, the ASP format is Left-Justified only.

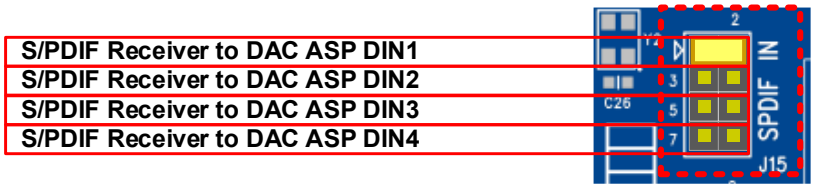


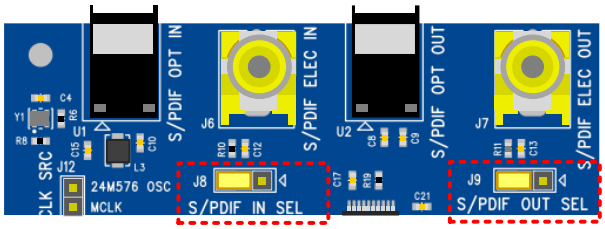
Figure 19: SPDIF IN Jumper Link Configuration

5.4 Selecting Optical or Electrical S/PDIF

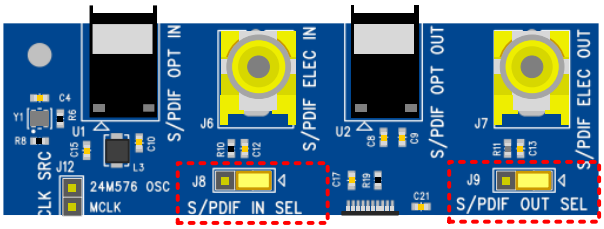
The S/PDIF IN SEL and S/PDIF OUT SEL headers are used to select the optical or electrical S/PDIF interfaces for the respective signal paths. The headers are configured as shown in Table 13.

The Dunglass system supports S/PDIF input/output at sample rates up to 96 kHz (optical) or up to 192 kHz (electrical).

Table 13 SPDIF I/O Configuration



Optical Input & Output



Electrical Input & Output

6 CS4304P/4S DAC Output Summing

The CS4304P/4S supports the option to combine the DAC signal paths in groups of two or four channels; this can be used to achieve enhanced dynamic-range performance on the respective paths.

In the summing configuration, the signal paths are routed and controlled differently to normal operation—the input signals are routed to groups of two or more DACs (depending on the selected configuration), and the grouped paths are each controlled as a single channel.

The DAC output summing is configured using the OUT_SUM_MODE field, as described in the CS4304P/4S datasheet. The summing configurations are described in Table 14.

Table 14 CS4304P/4S DAC Output Summing

Configuration	Description	Output Summing Configuration	Summed Channel Number
Default	4-channel	OUT1–OUT4 as individual outputs	1–4
All DACs combined in groups of two	2-channel input	OUT1+OUT2 OUT3+OUT4	1 2
DACs combined in groups of four	1-channel input	OUT1+OUT2+OUT3+OUT4	1

In summing configuration, the respective analog output connections must be linked externally to achieve the performance enhancement. The analog outputs are current-mode outputs; the external linking of the outputs results in the summing of the respective output signals.

Note that the increased current in the summing configuration affects the choice of components for the output buffer, as described in the following sections.

6.1 CS4304P Output Buffer Circuit

The CS4304P analog output channels are supported using external buffer circuits. A typical buffer circuit is shown in Figure 20, comprising current-to-voltage conversion and out-of-band filtering. The typical buffer circuit shown produces a 2 V_{RMS}. differential output from a full-scale (0 dBFS) digital input.

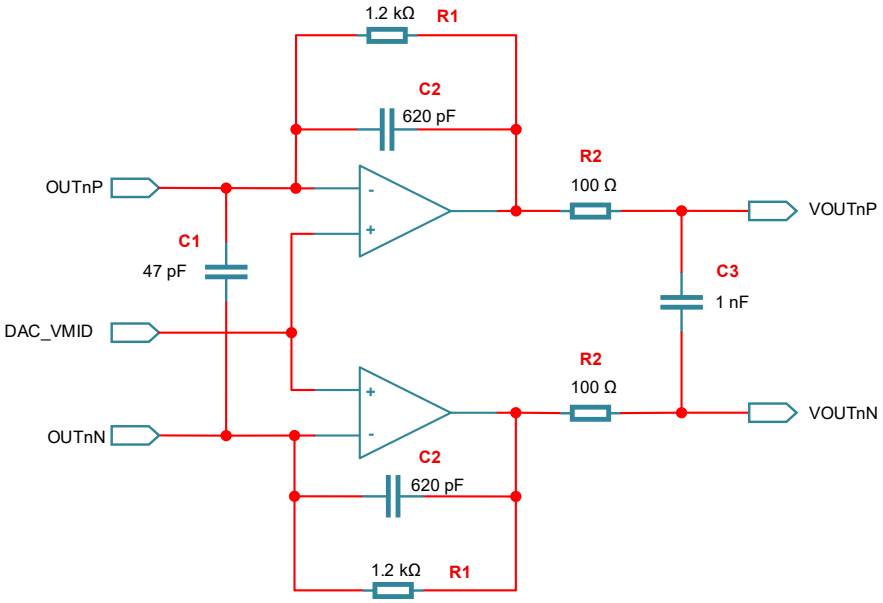


Figure 20: Differential Output Buffer

The full-scale output voltage is determined by the feedback resistor R1. The required value of R1 also depends on whether the outputs are configured in a summing configuration. The value of R1 can be calculated using the following equation:

$$R_1(k\Omega) = \frac{Full\_scale\ output\ voltage\ (V_{RMS})}{(Number\ of\ outputs\ summed\ x\ 1.66)}$$

Note: The number of outputs summed is 1, 2, or 4 depending on the applicable summing configuration.

The required value of R1 is shown in Table 15 for a range of typical operating configurations. Note that the THD+N performance may be degraded with increased full-scale output voltage.

Table 15 Feedback Resistor (R1) Selection

Configuration	Full-Scale Output Voltage		
	2 V_{RMS}	4 V_{RMS}	8 V_{RMS}
No Summing	1.2 kΩ	2.4 kΩ	4.8 kΩ
2 outputs summed	600 Ω	1.2 kΩ	2.4 kΩ
4 outputs summed	300 Ω	600 Ω	1.2 kΩ

A low-pass filter is provided using R1 and C2. The filter should be designed to provide a flat passband for the audio bandwidth, while attenuating out-of-band noise. The –3 dB cut-off frequency (F_C) can be calculated using the following equation:

$$F_C = \frac{1}{2\pi R_1 C_2}$$

The recommended value of C2 is shown in Table 16 for different values of R1. The recommended configuration provides a –3 dB cut-off around 220 Hz.

Table 16 Feedback Capacitor (C2) Selection

Resistor	Capacitor	-3 dB Cutoff
4.8 kΩ	150 pF	221 kHz
2.4 kΩ	300 pF	221 kHz
1.2 kΩ	620 pF	214 kHz
600 Ω	1.2 nF	221 kHz
300 Ω	2.4 nF	221 kHz

Additional filtering is provided using R2 and C3. The recommended components attenuate out-of-band noise, while minimizing the capacitive loading on the op-amp device. Using the values shown, the –3 dB cut-off frequency (F_C) can be calculated using the following equation:

$$F_C = \frac{1}{2\pi R_2 2C_3} = \frac{1}{2 \times \pi \times 100 \times 2 \times 1 \times 10^{-9}} = 795.8\ kHz$$

The recommended value of C1 is 47 pF, assuming output summing is not used. If the outputs are configured in a summing configuration, C1 should be increased to 100 pF.

Table 17 C1 Capacitor Selection

Configuration	Capacitor
No Summing	47 pF
2 outputs summed	100 pF
4 outputs summed	100 pF

6.2 CS4304S Output Buffer Circuit

The CS4304S analog output channels are supported using external buffer circuits. A typical buffer circuit is shown in Figure 21, comprising current-to-voltage conversion and out-of-band filtering. The typical buffer circuit shown produces a 2 V_{RMS}. differential output from a full-scale (0 dBFS) digital input.

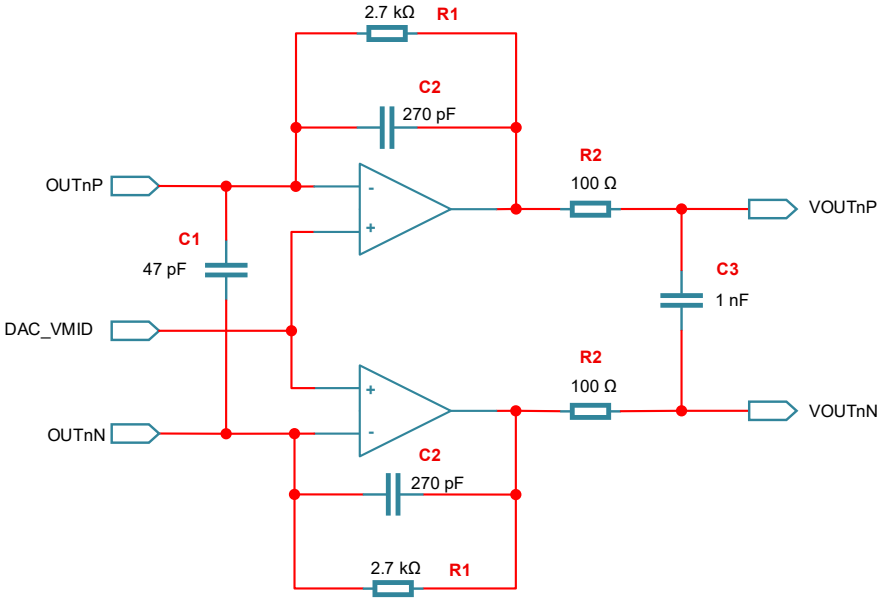


Figure 21: Differential Output Buffer

The full-scale output voltage is determined by the feedback resistor R1. The required value of R1 also depends on whether the outputs are configured in a summing configuration. The value of R1 can be calculated using the following equation:

$$R_1(k\Omega) = \frac{Full\_scale\ output\ voltage\ (V_{RMS})}{(Number\ of\ outputs\ summed\ x\ 0.75)}$$

Note: The number of outputs summed is 1, 2, or 4 depending on the applicable summing configuration.

The required value of R1 is shown in Table 18 for a range of typical operating configurations. Note that the THD+N performance may be degraded with increased full-scale output voltage.

Table 18 Feedback Resistor (R1) Selection

Configuration	Full-Scale Output Voltage		
	2 V_{RMS}	4 V_{RMS}	8 V_{RMS}
No Summing	2.7 kΩ	5.6 kΩ	11 kΩ
2 outputs summed	1.4 kΩ	2.7 kΩ	5.6 kΩ
4 outputs summed	680 Ω	1.4 kΩ	2.7 kΩ

A low-pass filter is provided using R1 and C2. The filter should be designed to provide a flat passband for the audio bandwidth, while attenuating out-of-band noise. The –3 dB cut-off frequency (F_C) can be calculated using the following equation:

$$F_C = \frac{1}{2\pi R_1 C_2}$$

The recommended value of C2 is shown in Table 19 for different values of R1. The recommended configuration provides a –3 dB cut-off around 220 Hz.

Table 19 Feedback Capacitor (C2) Selection

Resistor	Capacitor	-3 dB Cutoff
11 kΩ	68 pF	212 kHz
5.6 kΩ	130 pF	218 kHz
2.7 kΩ	270 pF	218 kHz
1.4 kΩ	510 pF	222 kHz
680 Ω	1.1 nF	212 kHz

Additional filtering is provided using R2 and C3. The recommended components attenuate out-of-band noise, while minimizing the capacitive loading on the op-amp device. Using the values shown, the –3 dB cut-off frequency (F_C) can be calculated using the following equation:

$$F_C = \frac{1}{2\pi R_2 2C_3} = \frac{1}{2 \times \pi \times 100 \times 2 \times 1 \times 10^{-9}} = 795.8\ kHz$$

The recommended value of C1 is 47 pF, assuming output summing is not used. If the outputs are configured in a summing configuration, C1 should be increased to 100 pF.

Table 20 C1 Capacitor Selection

Configuration	Capacitor
No Summing	47 pF
2 outputs summed	100 pF
4 outputs summed	100 pF

6.3 Configuring DC4304P/4S-DAC for DAC Output Summing

The DC4304P/4S-DAC has been designed to support DAC output summing; this is supported using component population options. Note that all the component population options are Imperial 0603 case size.

The following sections describe how to configure the DC4304P/4S-DAC board for different output-summing modes.

6.3.1 Default Configuration: No Output Summing

Figure 22 shows the default external connections to the CS4304P/4S, with no output summing.

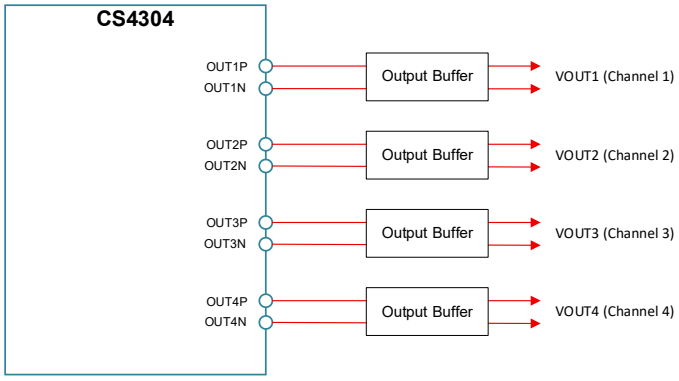


Figure 22: No Output Summing

The CDB-DC4304P/4S component population requirements are described in Table 21.

Table 21 Default Component Population for No Output Summing

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Feedback Resistor (R1)	Feedback Capacitor (C2)	DAC Output Capacitor (C1)
R12, R14, R195, R197, R33, R35, R212, R214, R54, R56, R77, R79, R244, R246, R195, R197, R212, R214, R244, R246,	R198, R203, R215, R220, R231, R235, R247, R252, R225, R226, R209, R217, R192, R200, R241, R249, R192, R200, R209, R217, R241, R249,	R1, R19, R22, R42 R43, R60, R62, R84	C3, C9, C12, C18 C22, C26, C29, C39	C91 C98 C105 C112

The feedback resistance (R1) should be selected as described in Table 15 for CS4304P and Table 18 for CS4304S (see “no summing” configuration). For 2 V_{RMS} full-scale output, the feedback resistance should be 1.2 kΩ for CS4304P and 2.7 kΩ for CS4304S.

The feedback capacitors (C2) should be selected as described in Table 16 for CS4304P and Table 19 for CS4304S and the DAC output capacitor C1 should be selected as described in Table 17 for CS4308P and Table 20 for CS4308S for the chosen resistor value.

6.3.2 Output Summing: DACs Combined in Groups of 2

Figure 23 shows the external connections to the CS4304P/4S when the outputs are summed in groups of 2.

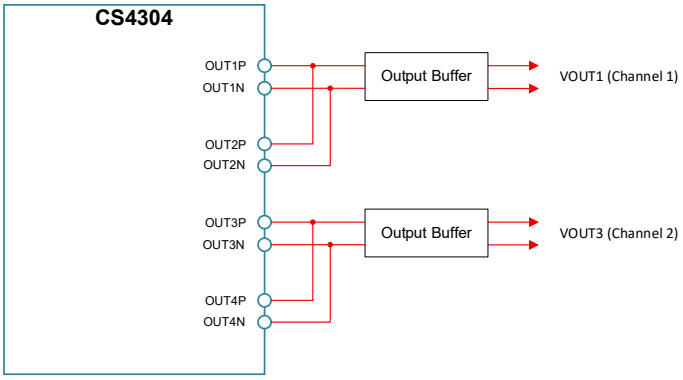


Figure 23: DACs Combined in Groups of 2

The CDB-DC4304P/4S component population requirements are described in Table 22.

Table 22 Component Population for DACs Combined in Groups of 2

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Feedback Resistor (R1)	Feedback Capacitor (C2)	DAC Output Capacitor (C1)
R12, R14, R54, R56 R198, R215, R203, R220 R231, R247, R235, R252 R195, R197	R33, R35, R77, R79 R192, R197, R241, R246	R1, R19, R43, R60	C3, C9, C22, C26	C91 C105

The feedback resistance (R1) should be selected as described in Table 15 for CS4304P and Table 18 for CS4304S (see “2 outputs summed” configuration). For 2 V_{RMS} full-scale output, the feedback resistance should be 600 Ω for CS4304P and 1.4 kΩ for CS4304S.

The feedback capacitors (C2) should be selected as described in Table 16 for CS4304P and Table 19 for CS4304S and the DAC output capacitor C1 should be selected as described in Table 17 for CS4308P and Table 20 for CS4308S for the chosen resistor value.

6.3.3 DACs Combined in a Group of 4

Figure 24 shows the external connections to the CS4304P/4S when the outputs are summed in a group of 4.

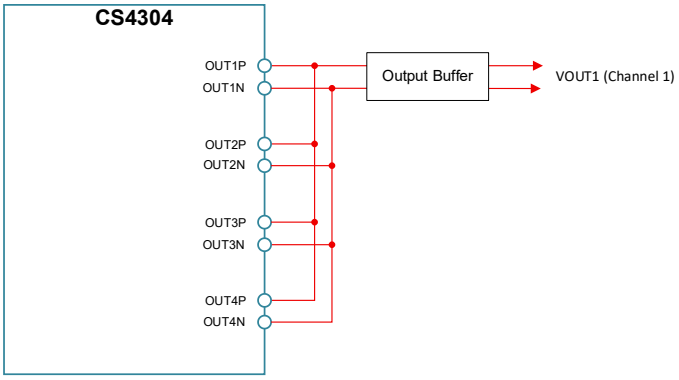


Figure 24: DACs Combined in a Group of 4

The CDB-DC4304P/4S component population requirements are described in Table 23.

Table 23 Component Population for DACs Combined in a Group of 4

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Feedback Resistor (R1)	Feedback Capacitor (C2)	DAC Output Capacitor (C1)
R198, R215, R203, R220 R225, R226, R231, R247 R235, R252, R241, R249, R192, R200, R77, R79,	R12, R14, R33, R35 R54, R56, R195, R197, R244, R246,	R62, R84	C29, C39	C112

The feedback resistance (R1) should be selected as described in Table 15 for CS4304P and Table 18 for CS4304S (see “4 outputs summed” configuration). For 2 V_{RMS} full-scale output, the feedback resistance should be 300 Ω for CS4304P and 680 Ω for CS4304S.

The feedback capacitors (C2) should be selected as described in Table 16 for CS4304P and Table 19 for CS4304S and the DAC output capacitor C1 should be selected as described in Table 17 for CS4308P and Table 20 for CS4308S for the chosen resistor value.

7 CS4308P/8S DAC Output Summing

The CS4308P/8S supports the option to combine the DAC signal paths in groups of two, four, or eight channels; this can be used to achieve enhanced dynamic-range performance on the respective paths. A six-channel summing mode is also supported, with DAC1–DAC4 operating in pairs, with DAC5–DAC8 operating individually.

In the summing configuration, the signal paths are routed and controlled differently to normal operation—the input signals are routed to groups of two or more DACs (depending on the selected configuration), and the grouped paths are each controlled as a single channel.

The DAC output summing is configured using the OUT_SUM_MODE field, as described in the CS4308P/8S datasheet. The summing configurations are described in Table 24.

Table 24 CS4308P/8S DAC Output Summing

Configuration	Description	Output Summing Configuration	Summed Channel Number
Default	8-channel	OUT1–OUT8 as individual outputs	1–8
Four DACs combined in groups of two	6-channel input	OUT1+OUT2 OUT3+OUT4 OUT5 OUT6 OUT7 OUT8	1 2 3 4 5 6
All DACs combined in groups of two	4-channel input	OUT1+OUT2 OUT3+OUT4 OUT5+OUT6 OUT7+OUT8	1 2 3 4
DACs combined in groups of four	2-channel input	OUT1+OUT2+OUT3+OUT4 OUT5+OUT6+OUT7+OUT8	1 2
DACs combined as a group of eight	1-channel input	OUT1+OUT2+OUT3+OUT4+ OUT5+OUT6+OUT7+OUT8	1

In summing configuration, the respective analog output connections must be linked externally to achieve the performance enhancement. The analog outputs are current-mode outputs; the external linking of the outputs results in the summing of the respective output signals.

Note that the increased current in the summing configuration affects the choice of components for the output buffer, as described in the following sections.

7.1 CS4308P Output Buffer Circuit

The CS4308P analog output channels are supported using external buffer circuits. A typical buffer circuit is shown in Figure 25, comprising current-to-voltage conversion and out-of-band filtering. The typical buffer circuit shown produces a 2 V_{RMS}. differential output from a full-scale (0 dBFS) digital input.

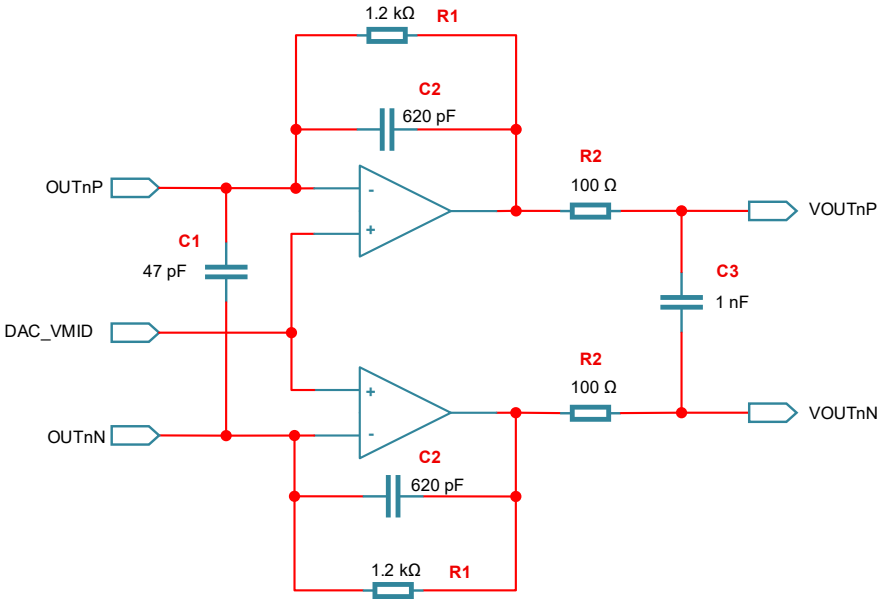


Figure 25: Differential Output Buffer

The full-scale output voltage is determined by the feedback resistor R1. The required value of R1 also depends on whether the outputs are configured in a summing configuration. The value of R1 can be calculated using the following equation:

$$R_1(k\Omega) = \frac{Full\_scale\ output\ voltage\ (V_{RMS})}{(Number\ of\ outputs\ summed\ x\ 1.66)}$$

Note: The number of outputs summed is 1, 2, 4, or 8 depending on the applicable summing configuration.

The required value of R1 is shown in Table 25 for a range of typical operating configurations. Note that the THD+N performance may be degraded with increased full-scale output voltage. Also note that low resistance (e.g., 150 Ω) may be incompatible with some op-amp devices.

Table 25 Feedback Resistor (R1) Selection

Configuration	Full-Scale Output Voltage		
	2 V_{RMS}	4 V_{RMS}	8 V_{RMS}
No Summing	1.2 kΩ	2.4 kΩ	4.8 kΩ
2 outputs summed	600 Ω	1.2 kΩ	2.4 kΩ
4 outputs summed	300 Ω	600 Ω	1.2 kΩ
8 outputs summed	150 Ω	300 Ω	600 Ω

A low-pass filter is provided using R1 and C2. The filter should be designed to provide a flat passband for the audio bandwidth, while attenuating out-of-band noise. The –3 dB cut-off frequency (F_C) can be calculated using the following equation:

$$F_C = \frac{1}{2\pi R_1 C_2}$$

The recommended value of C2 is shown in Table 26 for different values of R1. The recommended configuration provides a –3 dB cut-off around 220 Hz.

Table 26 Feedback Capacitor (C2) Selection

Resistor	Capacitor	-3 dB Cutoff
4.8 kΩ	150 pF	221 kHz
2.4 kΩ	300 pF	221 kHz
1.2 kΩ	620 pF	214 kHz
600 Ω	1.2 nF	221 kHz
300 Ω	2.4 nF	221 kHz
150 Ω	4.7 nF	226 kHz

Additional filtering is provided using R2 and C3. The recommended components attenuate out-of-band noise, while minimizing the capacitive loading on the op-amp device. Using the values shown, the –3 dB cut-off frequency (F_C) can be calculated using the following equation:

$$F_C = \frac{1}{2\pi R_2 2C_3} = \frac{1}{2 \times \pi \times 100 \times 2 \times 1 \times 10^{-9}} = 795.8\ kHz$$

The recommended value of C1 is 47 pF, assuming output summing is not used. If the outputs are configured in a summing configuration, C1 should be increased to 100 pF.

Table 27 C1 Capacitor Selection

Configuration	Capacitor
No Summing	47 pF
2 outputs summed	100 pF
4 outputs summed	100 pF
8 outputs summed	100 pF

7.2 CS4308S Output Buffer Circuit

The CS4308S analog output channels are supported using external buffer circuits. A typical buffer circuit is shown in Figure 26, comprising current-to-voltage conversion and out-of-band filtering. The typical buffer circuit shown produces a 2 V_{RMS}. differential output from a full-scale (0 dBFS) digital input.

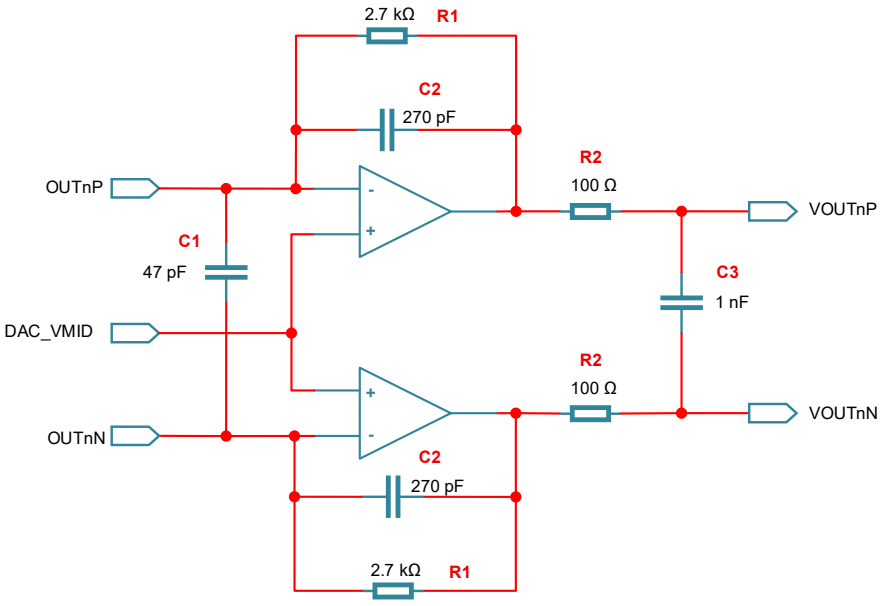


Figure 26: Differential Output Buffer

The full-scale output voltage is determined by the feedback resistor R1. The required value of R1 also depends on whether the outputs are configured in a summing configuration. The value of R1 can be calculated using the following equation:

$$R_1(k\Omega) = \frac{Full\_scale\ output\ voltage\ (V_{RMS})}{(Number\ of\ outputs\ summed\ x\ 0.75)}$$

Note: The number of outputs summed is 1, 2, 4, or 8 depending on the applicable summing configuration.

The required value of R1 is shown in Table 28 for a range of typical operating configurations. Note that the THD+N performance may be degraded with increased full-scale output voltage.

Table 28 Feedback Resistor (R1) Selection

Configuration	Full-Scale Output Voltage		
	2 V_{RMS}	4 V_{RMS}	8 V_{RMS}
No Summing	2.7 kΩ	5.6 kΩ	11 kΩ
2 outputs summed	1.4 kΩ	2.7 kΩ	5.6 kΩ
4 outputs summed	680 Ω	1.4 kΩ	2.7 kΩ
8 outputs summed	360 Ω	680 Ω	1.4 kΩ

A low-pass filter is provided using R1 and C2. The filter should be designed to provide a flat passband for the audio bandwidth, while attenuating out-of-band noise. The –3 dB cut-off frequency (F_C) can be calculated using the following equation:

$$F_C = \frac{1}{2\pi R_1 C_2}$$

The recommended value of C2 is shown in Table 29 for different values of R1. The recommended configuration provides a –3 dB cut-off around 220 Hz.

Table 29 Feedback Capacitor (C2) Selection

Resistor	Capacitor	-3 dB Cutoff
11 kΩ	68 pF	212 kHz
5.6 kΩ	130 pF	218 kHz
2.7 kΩ	270 pF	218 kHz
1.4 kΩ	510 pF	222 kHz
680 Ω	1.1 nF	212 kHz
360 Ω	2.0 nF	221 kHz

Additional filtering is provided using R2 and C3. The recommended components attenuate out-of-band noise, while minimizing the capacitive loading on the op-amp device. Using the values shown, the –3 dB cut-off frequency (F_C) can be calculated using the following equation:

$$F_C = \frac{1}{2\pi R_2 2C_3} = \frac{1}{2 \times \pi \times 100 \times 2 \times 1 \times 10^{-9}} = 795.8\ kHz$$

The recommended value of C1 is 47 pF, assuming output summing is not used. If the outputs are configured in a summing configuration, C1 should be increased to 100 pF.

Table 30 C1 Capacitor Selection

Configuration	Capacitor
No Summing	47 pF
2 outputs summed	100 pF
4 outputs summed	100 pF
8 outputs summed	100 pF

7.3 Configuring DC4308P/8S-DAC for DAC Output Summing

The DC4308P/8S-DAC has been designed to support DAC output summing; this is supported using component population options. Note that all the component population options are Imperial 0603 case size.

The following sections describe how to configure the DC4308P/8S-DAC board for different output-summing modes.

7.3.1 Default Configuration: No Output Summing

Figure 27 shows the default external connections to the CS4308P/8S, with no output summing.

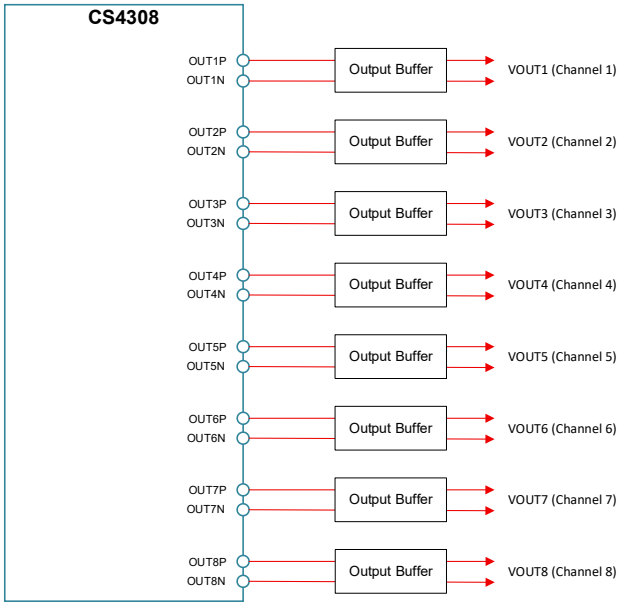


Figure 27: No Output Summing

The CDB-DC4308P component population requirements are described in Table 31.

Table 31 Default Component Population for No Output Summing

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Feedback Resistor (R1)	Feedback Capacitor (C2)	DAC Output Capacitor (C1)
R12, R14, R195, R197, R33, R35, R212, R214, R54, R56, R77, R79, R105, R107, R127, R129 R276, R278, R150, R152 R171, R175, R244, R246, R195, R197, R212, R214 R244, R246, R276, R278	R198, R203, R215, R220, R231, R235, R247, R252, R263, R267, R279, R284, R295, R299, R308, R312, R225, R257, R289, R226, R258, R290, R209, R217, R192, R200, R241, R249, R273, R281 R192, R200, R209, R217 R241, R249, R273, R281	R1, R19, R22, R42 R43, R60, R62, R84 R86, R113, R116, R134 R136, R156, R158, R181	C3, C9, C12, C18 C22, C26, C29, C39 C46, C53, C56, C60 C65, C71, C75, C82	C91 C98 C105 C112 C119 C126 C133 C140

The feedback resistance (R1) should be selected as described in Table 25 for CS4308P and Table 28 for CS4308S (see “no summing” configuration). For 2 V_{RMS} full-scale output, the feedback resistance should be 1.2 kΩ for CS4308P and 2.7 kΩ for CS4308S.

The feedback capacitors (C2) should be selected as described in Table 26 for CS4308P and Table 29 for CS4308S and the DAC output capacitor (C1) should be selected as described in Table 27 for CS4308P and Table 30 for CS4308S for the chosen resistor value.

7.3.2 Output Summing: DACs Combined in Groups of 2

Figure 28 shows the external connections to the CS4308P/8S when the outputs are summed in groups of 2.

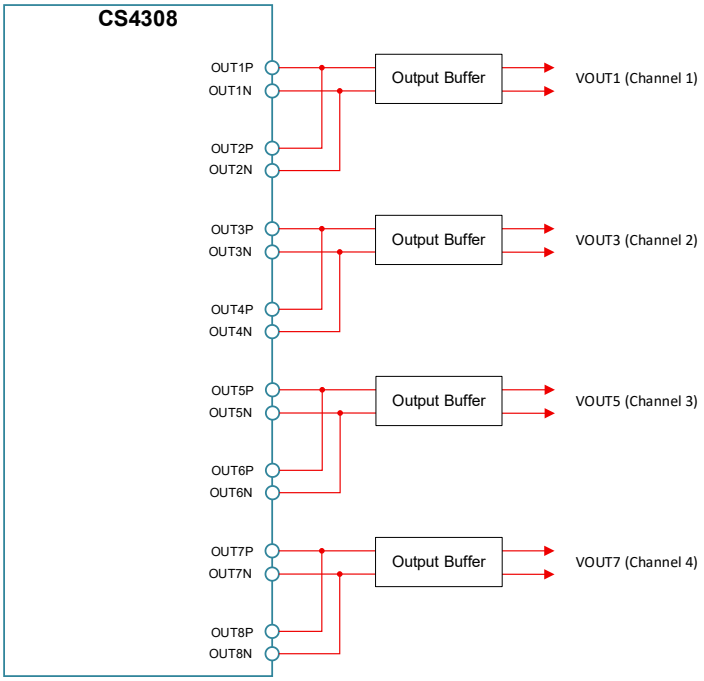


Figure 28: DACs Combined in Groups of 2

The CDB-DC4308P component population requirements are described in Table 32.

Table 32 Component Population for DACs Combined in Groups of 2

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Feedback Resistor (R1)	Feedback Capacitor (C2)	DAC Output Capacitor (C1)
R12, R14, R54, R56 R105, R107, R150, R152 R198, R215, R203, R220 R231, R247, R235, R252 R263, R279, R267, R284 R295, R308, R299, R312 R195, R197	R33, R35, R77, R79 R127, R129, R171, R175 R192, R197, R241, R246 R273, R278	R1, R19, R43, R60 R86, R113, R136, R156	C3, C9, C22, C26 C46, C53, C65, C71	C91 C105 C119 C133

The feedback resistance (R1) should be selected as described in Table 25 for CS4308P and Table 28 for CS4308S (see “2 outputs summed” configuration). For 2 V_{RMS} full-scale output, the feedback resistance should be 600 Ω for CS4308P and 1.4 kΩ for CS4308S.

The feedback capacitors (C2) should be selected as described in Table 26 for CS4308P and Table 29 for CS4308S and the DAC output capacitor (C1) should be selected as described in Table 27 for CS4308P and Table 30 for CS4308S for the chosen resistor value.

7.3.3 DACs Combined in Groups of 4

Figure 24 shows the external connections to the CS4308P/8S when the outputs are summed in groups of 4.

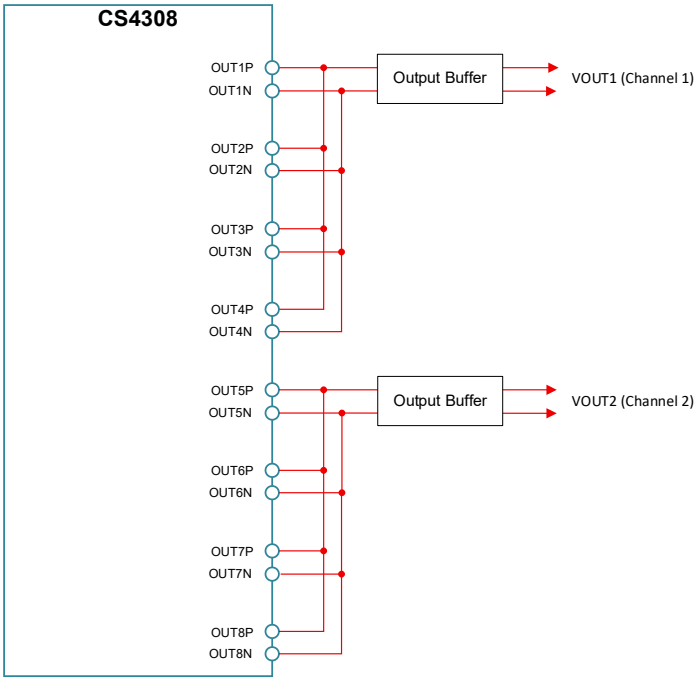


Figure 29: DACs Combined in Groups of 4

The CDB-DC4308P component population requirements are described in Table 33.

Table 33 Component Population for DACs Combined in Groups of 4

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Feedback Resistor (R1)	Feedback Capacitor (C2)	DAC Output Capacitor (C1)
R198, R215, R203, R220 R225, R226, R231, R247 R235, R252, R263, R279 R267, R284, R289, R290 R295, R308, R299, R312 R241, R249, R273, R281 R192, R200, R209, R217 R77, R79, R127, R129	R12, R14, R33, R35 R54, R56, R105, R107 R150, R152, R171, R175 R195, R197, R212, R214 R244, R246, R276, R278	R62, R84, R116, R134	C29, C39, C56, C60	C112 C126

The feedback resistance (R1) should be selected as described in Table 25 for CS4308P and Table 28 for CS4308S (see "4 outputs summed" configuration). For 2 V_{RMS} full-scale output, the feedback resistance should be 300 Ω for CS4308P and 680 Ω for CS4308S.

The feedback capacitors (C2) should be selected as described in Table 26 for CS4308P and Table 29 for CS4308S and the DAC output capacitor (C1) should be selected as described in Table 27 for CS4308P and Table 30 for CS4308S for the chosen resistor value.

7.3.4 DACs Combined in a Group of 8

Figure 30 shows the external connections to the CS4308P/8S when the outputs are summed in a group of 8.

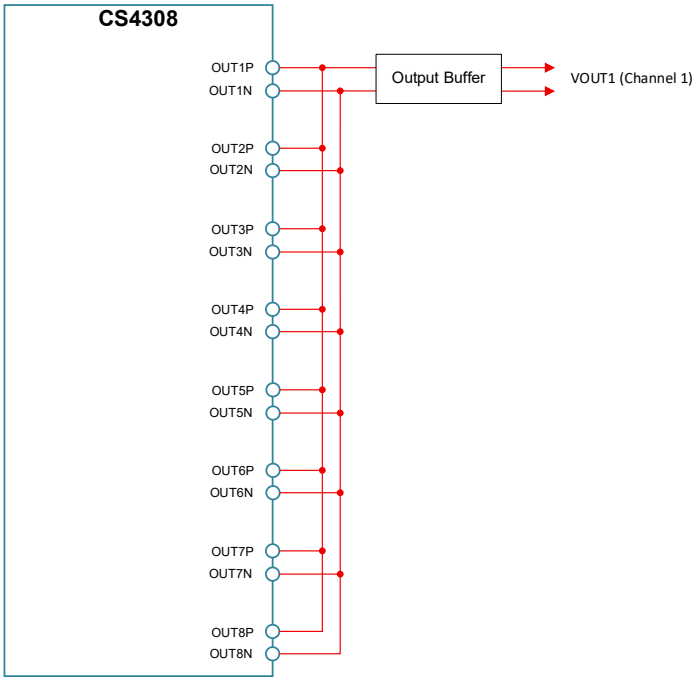


Figure 30: DACs Combined in a Group of 8

The CDB-DC4308P/8S component population requirements are described in Table 34.

Table 34 Component Population for DACs Combined in a Groups of 8

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Feedback Resistor (R1)	Feedback Capacitor (C2)	DAC Output Capacitor (C1)
R12, R14, R195, R197 R198, R203, R215, R220 R225, R226, R231, R247 R235, R252, R263, R279 R267, R284, R289, R290 R295, R308, R299, R312 R241, R249, R273, R281 R257, R258	R33, R35, R54, R56 R77, R79, R105, R107 R127, R129, R150, R152 R192, R200, R209, R217 R171, R175	R1, R19	C3, C9	C91

The feedback resistance (R1) should be selected as described in Table 25 for CS4308P and Table 28 for CS4308S (see “8 outputs summed” configuration). For 2 V_{RMS} full-scale output, the feedback resistance should be 150 Ω for CS4308P and 360 Ω for CS4308S.

The feedback capacitors (C2) should be selected as described in Table 26 for CS4308P and Table 29 for CS4308S and the DAC output capacitor (C1) should be selected as described in Table 27 for CS4308P and Table 30 for CS4308S for the chosen resistor value.

7.3.5 Four DACs Combined in Groups of 2

Figure 31 shows the external connections to the CS4308P/8S when the outputs are summed for 6-channel operation (four DACs combined in groups of 2).

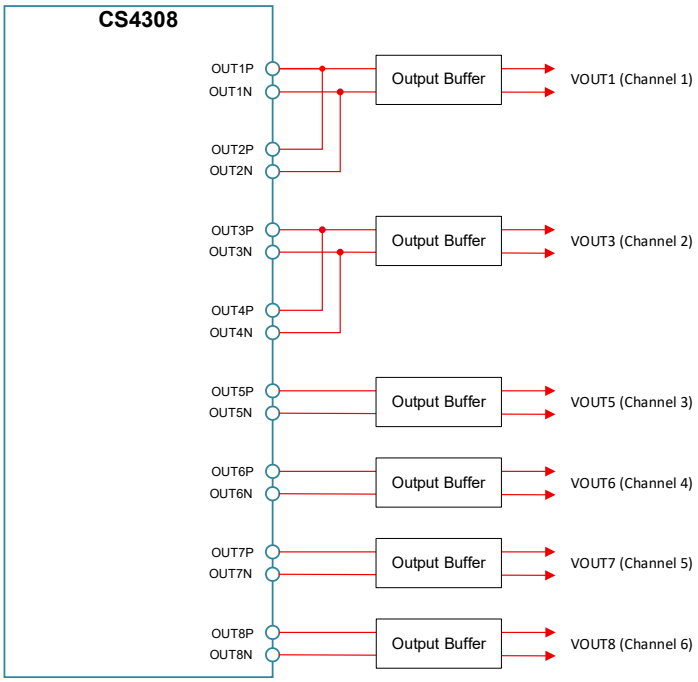


Figure 31: Four DACs Combined in Groups of 2

The CDB-DC4308P/8S component population requirements for the summed outputs are described in Table 35.

Table 35 Component Population – Four DACs Combined in Groups of 2

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Feedback Resistor (R1)	Feedback Capacitor (C2)	DAC Output Capacitor (C1)
R12, R14, R195, R197 R54, R56, R198, R215 R203, R220, R231, R247 R235, R252	R33, R35, R77, R79 R192, R200, R225, R226 R257, R258	R1, R19, R43, R60	C3, C9, C22, C26	C91 C105

The feedback resistance (R1) should be selected as described in Table 25 for CS4308P and Table 28 for CS4308S for CS4308S (see “2 outputs summed” configuration). For 2 V_{RMS} full-scale output, the feedback resistance should be 600 kΩ for CS4308P and 1.4 kΩ for CS4308S.

The CDB-DC4308P/8S component population requirements for the non-summed outputs are described in Table 36.

Table 36 Component Population – OUT5 to OUT8 (No Summing)

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Feedback Resistor (R1)	Feedback Capacitor (C2)	DAC Output Capacitor (C1)
R105, R107, R127, R129 R276, R278, R150, R152 R171, R175	R263, R279, R289, R295 R308, R267, R284, R290 R299, R312, R273, R281	R86, R113, R116, R134 R136, R156, R158, R181	C46, C53, C56, C60 C65, C71, C75, C82	C119 C126 C133 C140

The feedback resistance (R1) should be selected as described in Table 25 for CS4308P and Table 28 for CS4308S (see “no summing” configuration). For 2 V_{RMS} full-scale output, the feedback resistance should be 1.2 kΩ for CS4308P and 2.7 kΩ for CS4308S.

The feedback capacitors (C2) should be selected as described in Table 26 for CS4308P and Table 29 for CS4308S and the DAC output capacitor (C1) should be selected as described in Table 27 for CS4308P and Table 30 for CS4308S for the chosen resistor value.

8 Performance Plots

8.1 DC4304P/8P-DAC Performance Plots

DAC Filter Slow Roll-off, Linear Phase, 48kHz Sample Rate

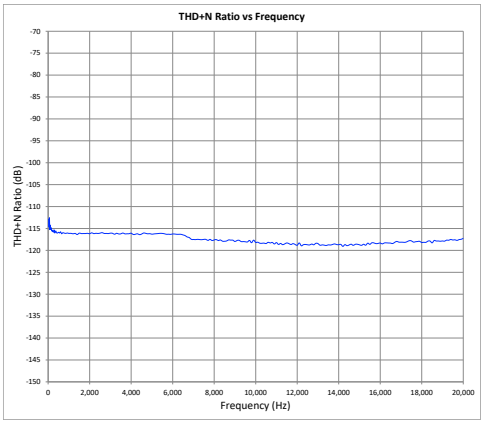


Figure 32: -1dBFS THD+N ratio Vs Frequency

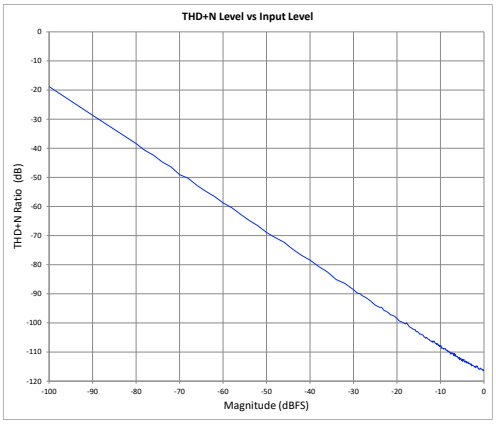


Figure 33: THD+N ratio Vs Magnitude

DAC Filter Slow Roll-off, Linear Phase, 96kHz Sample Rate

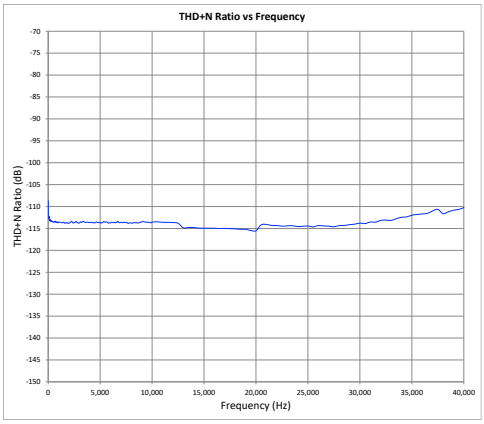


Figure 34: -1dBFS THD+N ratio Vs Frequency

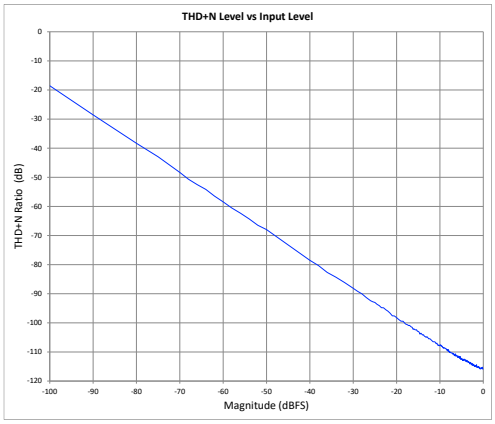


Figure 35: THD+N ratio Vs Magnitude

DAC Filter Slow Roll-off, Linear Phase, 192kHz Sample Rate

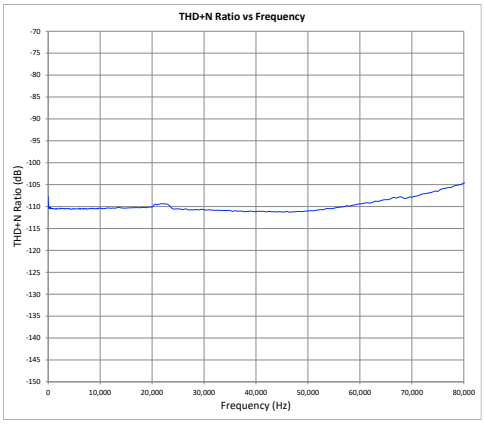


Figure 36: -1dBFS THD+N ratio Vs Frequency

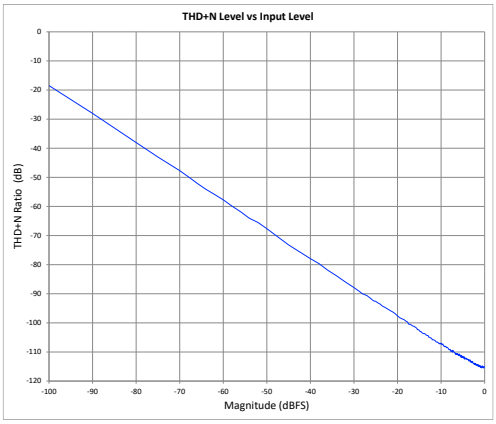


Figure 37: THD+N ratio Vs Magnitude

8.2 DC4304S/8S-DAC Performance Plots

DAC Filter Slow Roll-off, Linear Phase, 48kHz Sample Rate

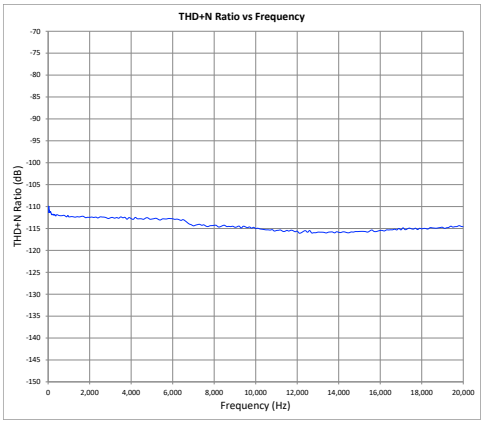


Figure 38: -1dBFS THD+N ratio Vs Frequency

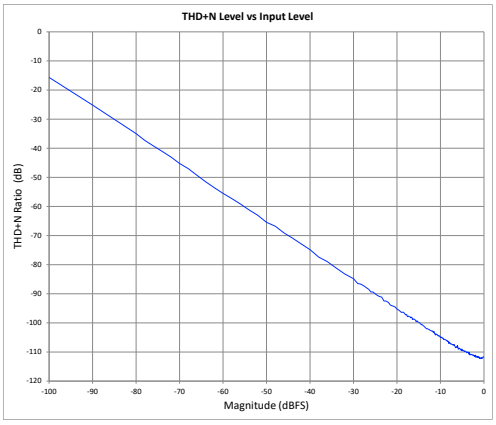


Figure 39: THD+N ratio Vs Magnitude

DAC Filter Slow Roll-off, Linear Phase, 96kHz Sample Rate

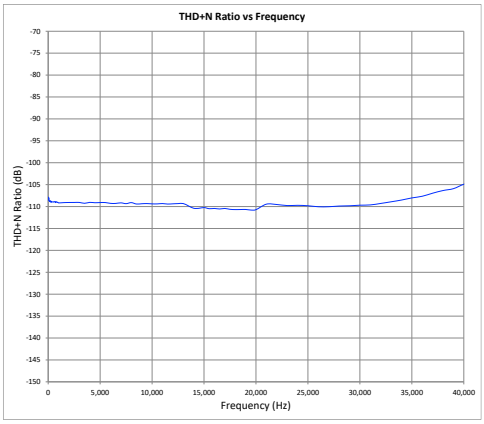


Figure 40: -1dBFS THD+N ratio Vs Frequency

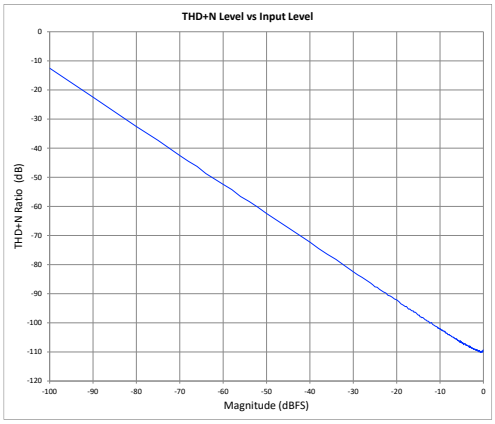


Figure 41: THD+N ratio Vs Magnitude

DAC Filter Slow Roll-off, Linear Phase, 192kHz Sample Rate

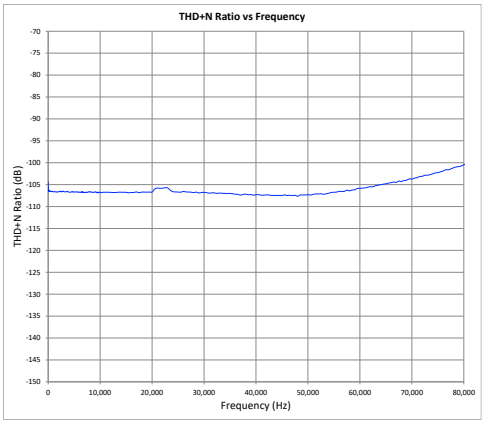


Figure 42: -1dBFS THD+N ratio Vs Frequency

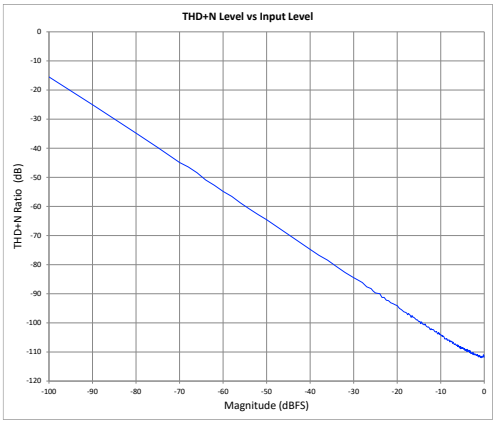


Figure 43:THD+N ratio Vs Magnitude

9 Notices

Jura firmware development utilizes components under the following licenses:

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Unmodified USB Audio 2.0 Device Software source code is available from www.xmos.ai under XMOS PUBLIC LICENCE: Version 1.

10 Revision History

Revision	Changes
DB1 JUN 2024	• Initial version.
DB2 OCT 2024	• Updates in all sections
DB3 OCT 2024	• Diagram Updates
DB4 JAN 2025	• Updates in all sections • Combined user guides for CS4308S, CS4304P & CS4304S into single document
DB4 FEB 2025	• SPDIF SCS script name update • External Components section added
DB5 JUL 2025	• Additional description of output buffer circuits • Performance plots added

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.