DC4332BSE-DAC User Guide

Introduction

The DC4332BSE-DAC is a daughter card used with the Cirrus Logic Dunglass (CDB-PROAUDIO) system to evaluate high performance ADC, DAC, and codec devices. This document details how to connect the DC4332BSE-DAC to the Dunglass (CDB-PROAUDIO) system and how to get started.

The DC4332BSE-DAC, with the default jumper positions, is shown in Figure 1.

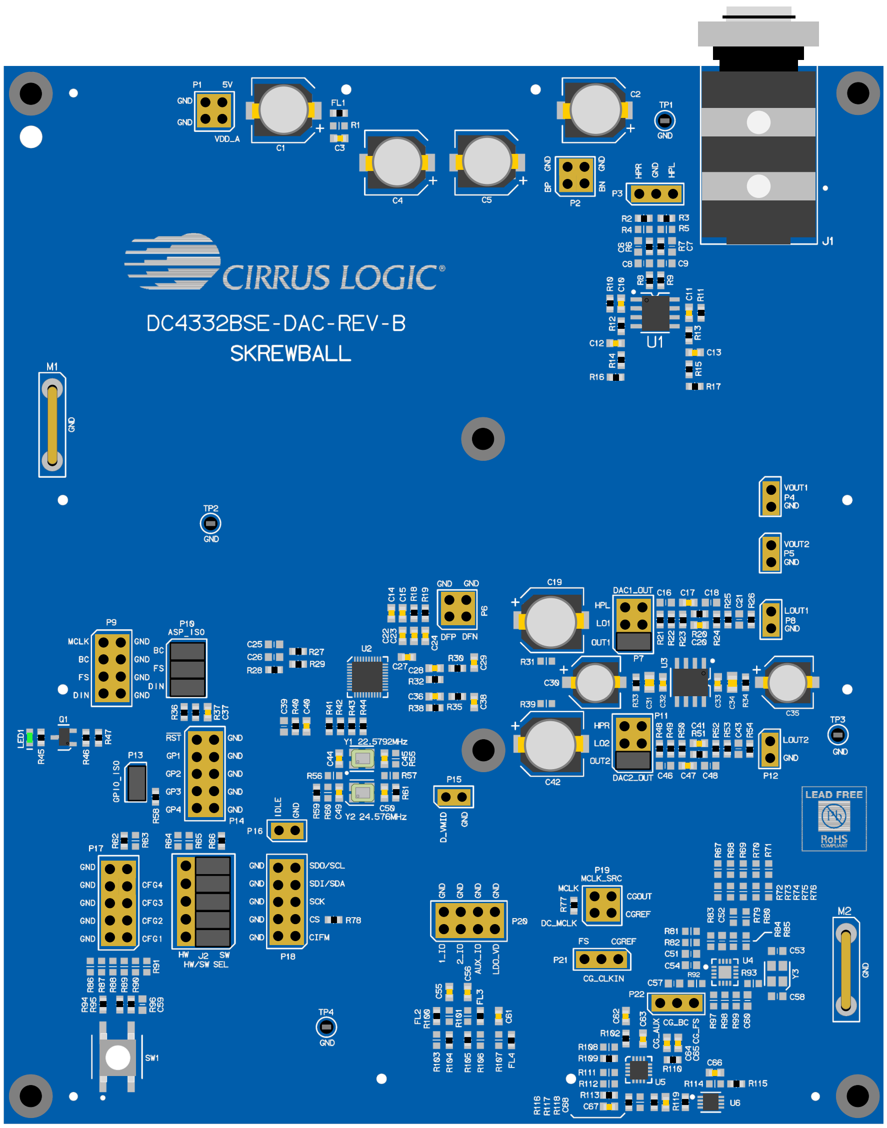

Figure 1: DC4332BSE-DAC Daughter Card

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1 Hardware Connections

The Dunglass system supports interchangeable daughter cards for a variety of ADC, DAC, and codec devices.

Caution:

Daughter cards should not be inserted or removed while the Dunglass system is powered. Fully disconnect or power down external power supply before changing daughter cards.

For more information on the Dunglass (CDB-PROAUDIO) system refer to the CDB-PROAUDIO User Guide[1] .

1.1 How to Connect DC4332BSE-DAC onto the Dunglass System

The DC4332BSE-DAC is a 4-header daughter card that connects to the Dunglass system using headers DCJ1, DCJ2, DCJ3, and DCJ4. A JURA module (described in Section 1.2.1) is also required to be plugged into the Dunglass system. To ensure correct connection, the headers are keyed and alignment dots are visible on each board, as shown in Figure 2.

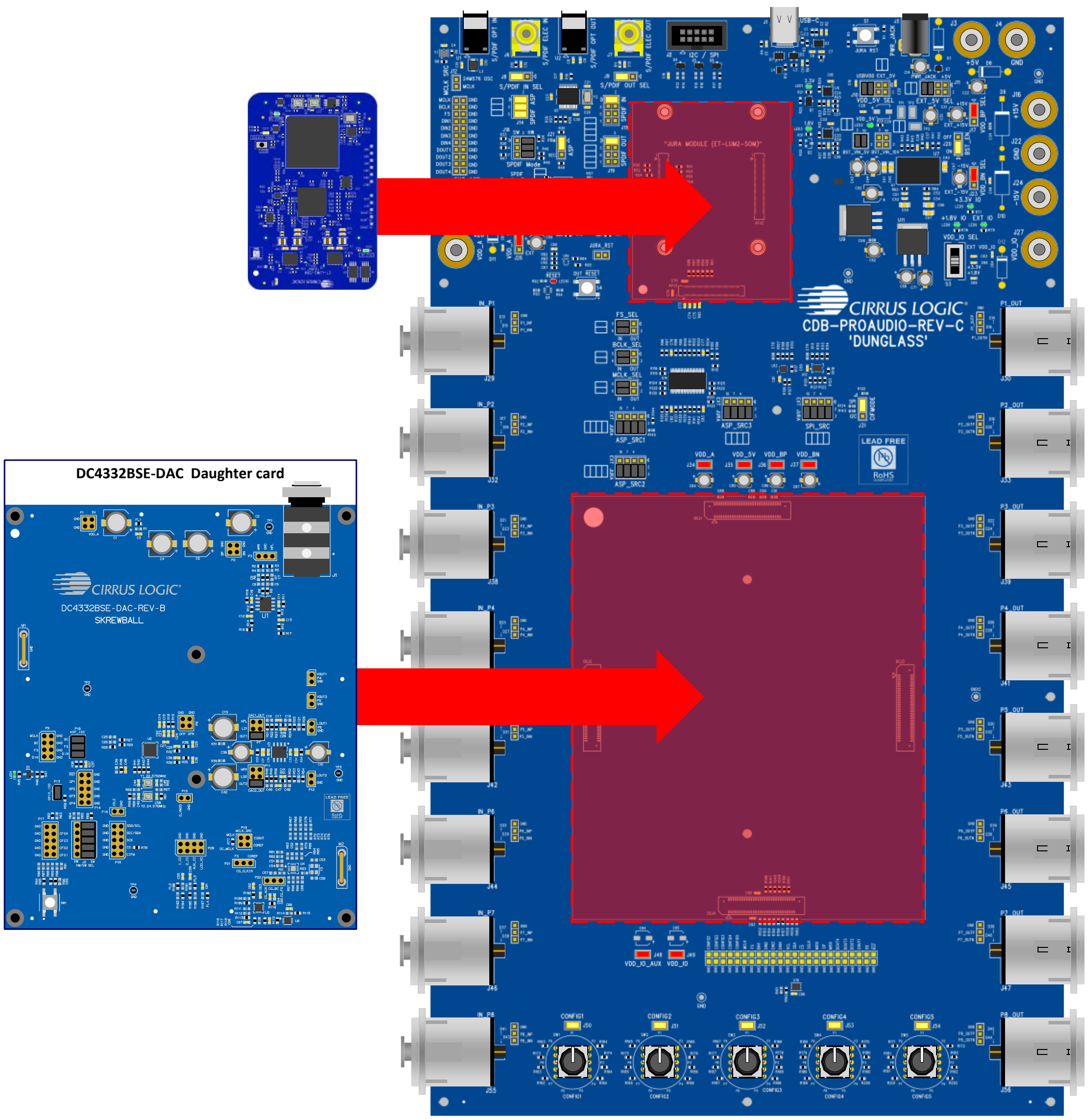

Figure 2: DC4332BSE-DAC Daughter Card and JURA Module Connection to the Dunglass System

1.2 USB and Power Connection

Dunglass is powered using a 5 V external power supply and is controlled via a single USB connection. The JURA module supports the following functions via the USB connection:

- I²C/SPI communications to control device and board
- Multichannel USB streaming audio (USB Class 2)

The Dunglass board is provided with a USB-A to USB-C cable and a 5 V wall supply; connection is illustrated in Figure 3.

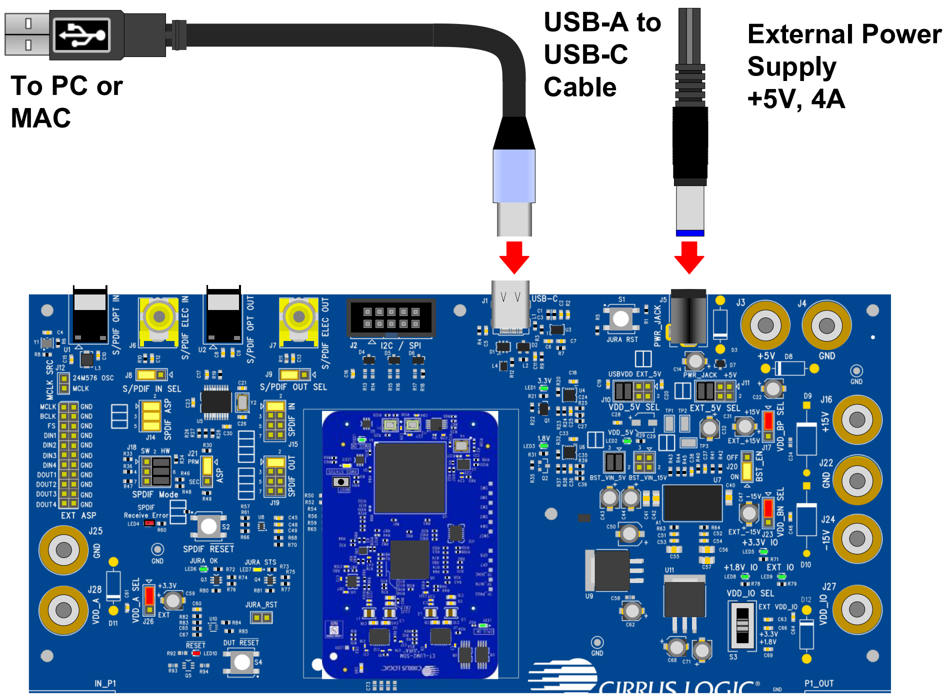

Figure 3: Dunglass (CDB-PROAUDIO) USB and Power Connection

A Total Phase Aardvark connector can be used for I²C/SPI communication. Refer to the CDB-PROAUDIO User Guide[1] for more details.

1.2.1 JURA Module

The JURA module supports I²C/SPI communication to control the Dunglass system and daughter card; it also enables multichannel USB streaming audio (USB audio Class 2).

The JURA module is connected to the Dunglass board as shown in Figure 4:

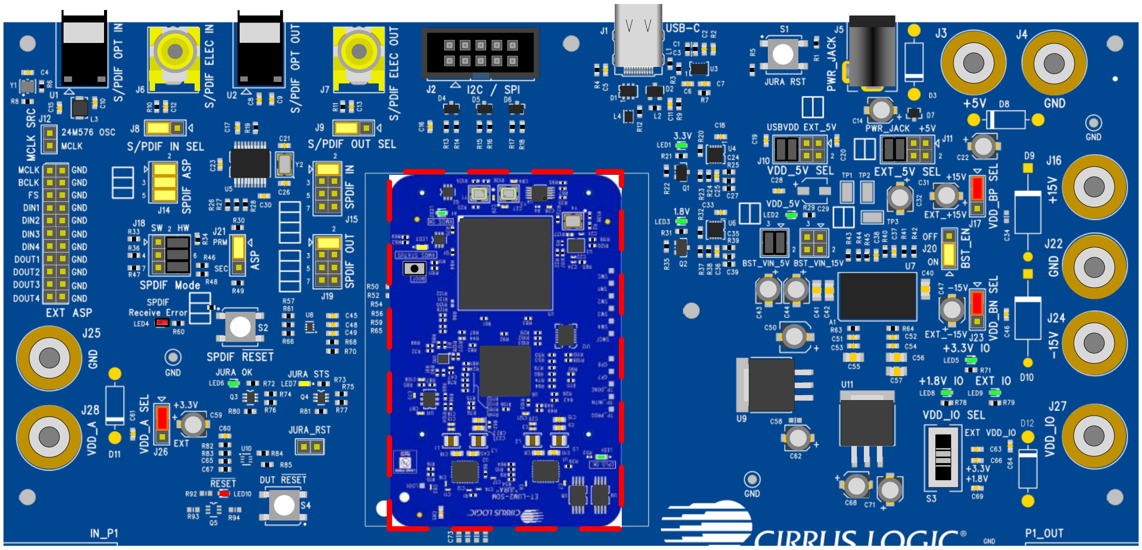

Figure 4: JURA Module Connection to Dunglass System

1.2.2 Dunglass Boot Procedure with JURA Module

The USB-C cable must be connected between the Dunglass system and the PC or Mac® prior to powering up the board.

The boot time of the Dunglass system varies depending on the version of firmware on the JURA module but is typically in the range of 2 s to 5 s after applying power to the board.

1.3 Routing the Digital Audio PCM Signals

The digital audio PCM paths to the daughter card can be routed from the JURA module, or else from the EXT ASP header located on the Dunglass system. The routing is configured using the ASP_SRC1, ASP_SRC2, and ASP_SRC3 headers as follows:

- JURA = Digital audio signals routed from JURA module
- EXT = Digital audio signals routed from EXT ASP header

The ASP_SRC1, ASP_SRC2, and ASP_SRC3 headers are configured for JURA Primary Mode, EXT ASP Primary Mode and EXT ASP Secondary Mode as shown in Figure 5, Figure 6, and Figure 7 respectively.

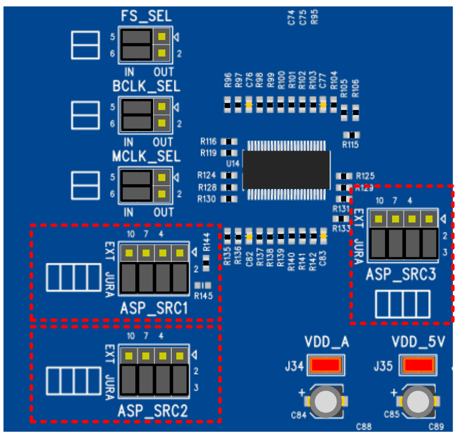

Figure 5: JURA Module Primary Mode

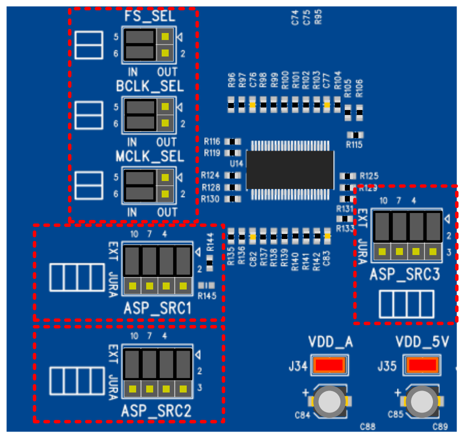

Figure 6: EXT ASP Primary Mode

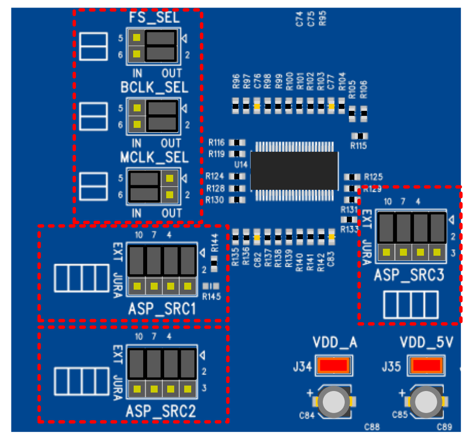

Figure 7: EXT ASP Secondary Mode

The JURA module always operates in Primary Mode – the MCLK, BCLK, and FSYNC clock signals are generated by the JURA module as inputs to the daughter card.

If the digital audio is routed from the EXT ASP header, the direction of the MCLK, BCLK, and FSYNC clock signals are configured using the MCLK_SEL, BCLK_SEL, and FS_SEL headers respectively. Each signal is configured independently, as follows:

- IN = EXT_ASP header supports the signal as input to the daughter card
- OUT = EXT_ASP header supports the signal as output from the daughter card

Note that the EXT ASP header uses 3.3 V logic levels; a level shifter is incorporated to interface with the VDD_IO domain on the DC4332BSE-DAC daughter card.

1.4 Selection of Hardware or Software Control Mode

The CS4332BSE supports hardware and software control modes. The hardware and software modes are set via the HW/SW SEL header on the DC4332BSE-DAC and the rotary switches on the Dunglass system. The Software Mode and Hardware Mode jumper link configurations are shown in Figure 8 and Figure 9.

- SW = Software Mode
- HW = Hardware Mode.

In Hardware Mode, rotary switches are used to select the desired configuration. See Section 4 for information on Hardware Mode.

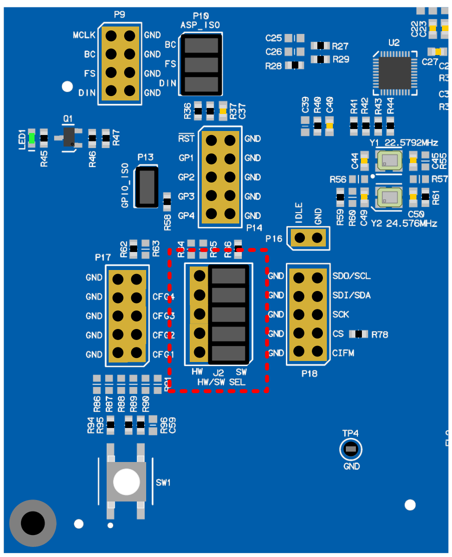

Figure 8: Software Mode Jumper Link Configuration

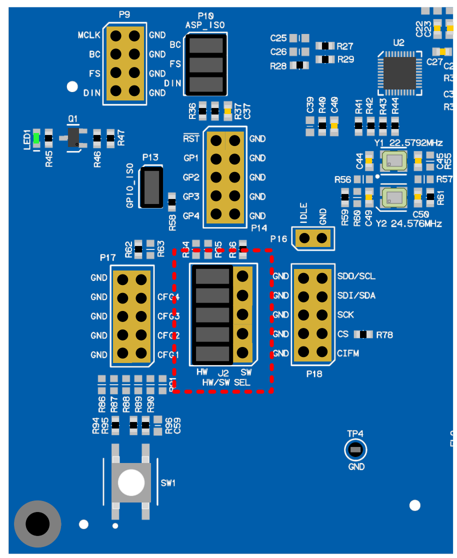

Figure 9: Hardware Mode Jumper Link Configuration

Note that Hardware Mode is only supported for VDD_IO = 3.3 V on the DC4332BSE-DAC due to the 3.3 V rotary switch pull-up supply on the Dunglass system.

1.5 DC4332BSE-DAC System Clocking Source Selection

Clocking for the CS4332BSE is provided using either the MCLK input or the crystal (XTAL) oscillator. The MCLK input is selected by default on the DC4332BSE-DAC. The XTAL oscillator uses one of two external crystals, Y1 or Y2, provided on the DC4332BSE-DAC to generate the system clock. Y1 provides a 22.5792 MHz signal and Y2 provides a 24.576 MHz signal. The oscillators are enabled by configuring resistors on the DC4332BSE-DAC board as follows:

- Y1 (22.5792 MHz). Enabled by removing R138 and R140, and populating R132 and R136.
- Y2 (24.576 MHz). Enabled by removing R138 and R140, and populating R137 and R139.

The clocking source is configured as shown in Figure 10, Figure 11 and Figure 12.

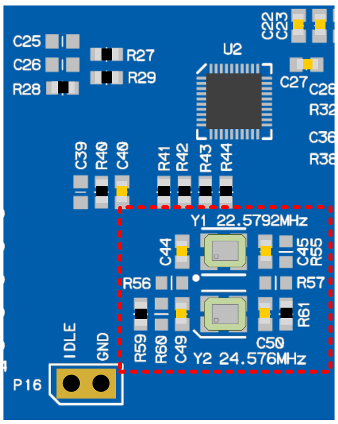

Figure 10: Dunglass System MCLK as clocking source (Default)

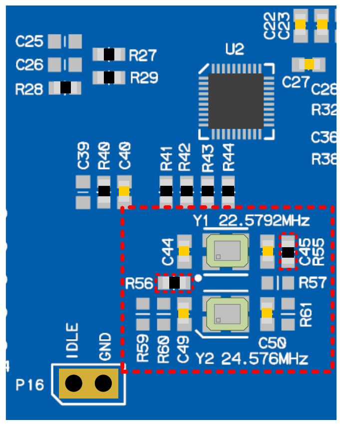

Figure 11: Crystal (XTAL) oscillator Y1 as clocking source

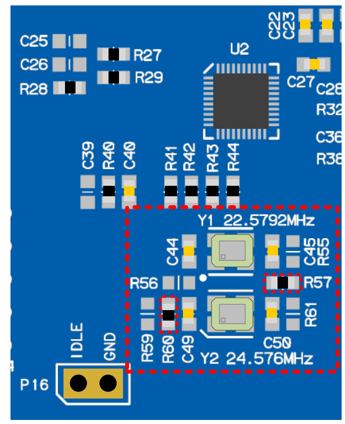

Figure 12: Crystal (XTAL) oscillator Y2 as clocking source

In Hardware Mode, the clocking source is configured using the CONFIG4 pin, as detailed in the CS4332BSE datasheet[2] . In Software Mode, the clocking source is selected using the register field SYSCLK_SRC.

If clocking is provided using the crystal oscillator, the CS4332BSE outputs a clock on the MCLK pin. The frequency of the MCLK output clock matches the crystal oscillator frequency. The output clock can be used to drive other devices.

1.6 DC4332BSE-DAC DAC Output Routing

The DC4332BSE-DAC board has three routing options for the output of the DAC. The options are configured using P7 (DAC1_OUT) and P11 (DAC2_OUT). The options are as follows:

- OUT1/OUT2 (Default) – 1 V_{RMS} output on Dunglass OUT1 and OUT2, shown in Figure 13.
  - This is the output of the current-to-voltage buffer/filter contained within the CS4332BSE.
- LO1/2 – 4.2 V_{RMS} output on Dunglass OUT3 and OUT4, shown in Figure 14.
  - The output of the current-to-voltage buffer/filter is routed to an op-amp line driver with a gain of +12 dB.
- HPL/HPR – 2.1 V_{RMS} single-ended headphone output circuit, shown in Figure 15.
  - The output of the current-to-voltage buffer/filter is routed to a single-ended op-amp circuit with a gain of + 6.4dB. The output is routed to a 6.3 mm stereo headphone jack (J1).

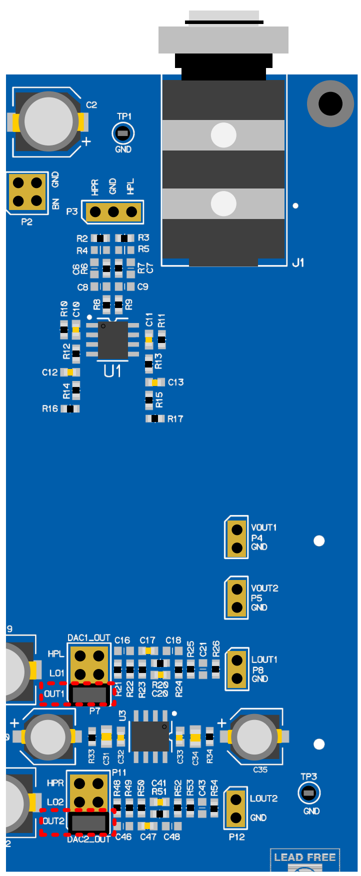

Figure 13: DAC Output to OUT1/OUT2

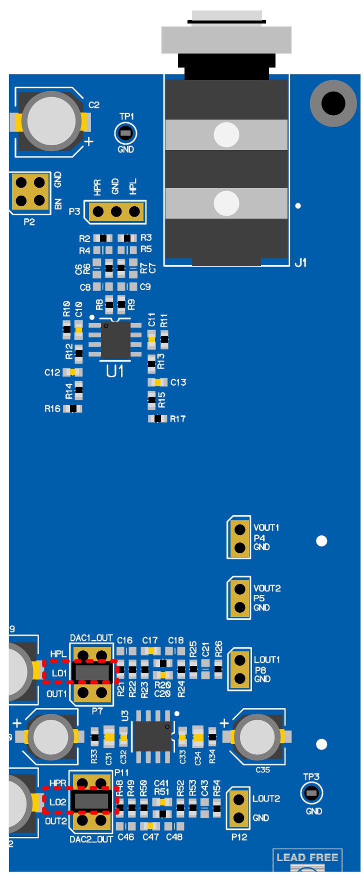

Figure 14: DAC Output to LOUT1/LOUT2

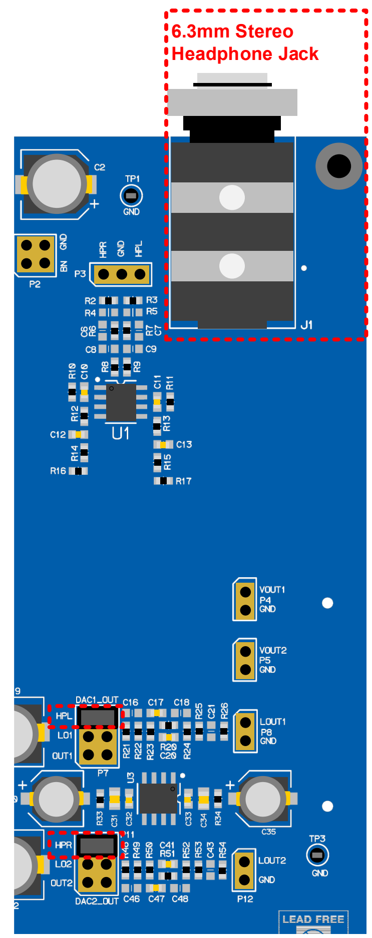

Figure 15: DAC Output to Headphone Output

2 Driver Installation and SoundClear Studio Support

2.1 SoundClear Studio

SoundClear® Studio (SCS) is a PC/Mac®-based tool used to configure Cirrus Logic devices. The tools suite provides support for evaluation and development and can be used with Dunglass system and associated daughter cards.

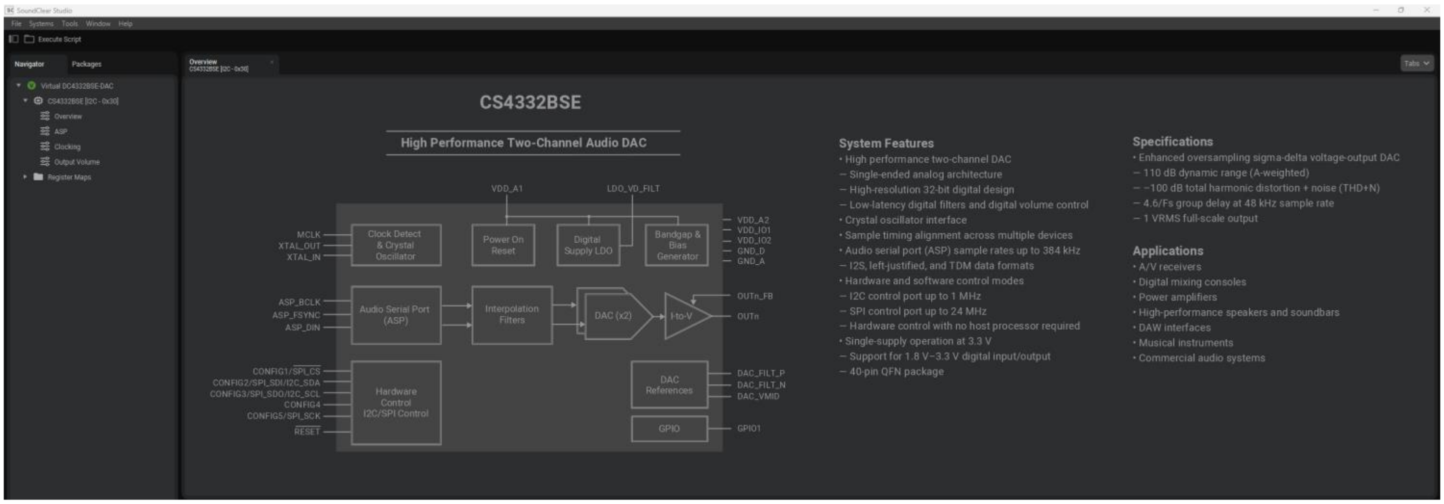

Figure 16: SoundClear Studio

2.1.1 Download SoundClear Studio Software and Drivers

SoundClear Studio and associated software collateral required for the Dunglass system can be downloaded from https://cirrus.com.

The required components are as follows:

- **SoundClear Studio 2.1**. Run the appropriate installer on your Windows® or macOS computer to install SoundClear Studio.
- **CS4332BSE SCS Package**. Install this in SoundClear Studio to incorporate the CS4332BSE-specific software components in SoundClear Studio. See Section 2.2.1 for details on how to install an SCS package.
- **JURA Windows Setup**. On Windows computers, run the Cirrus Logic USB Audio Setup to install the driver that enables SoundClear Studio to communicate with the JURA board.

2.2 SoundClear Studio Quick Start Guide

2.2.1 Installing Packages

Each daughter card has its own individual SoundClear Studio package that must be installed separately from the main SoundClear Studio Software. These are installed from the main menu using **"File → Install Package..."**. Multiple packages can be installed together by selecting more than one using the file dialog.

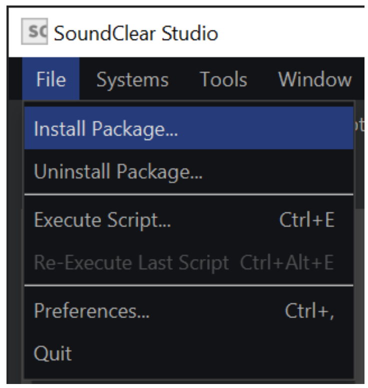

Figure 17: SoundClear Studio – Installing Board Packages

2.2.2 SoundClear Studio User Guide

The SoundClear Studio User Guide can be accessed from the main menu using **"Help → Open Help Contents..."**

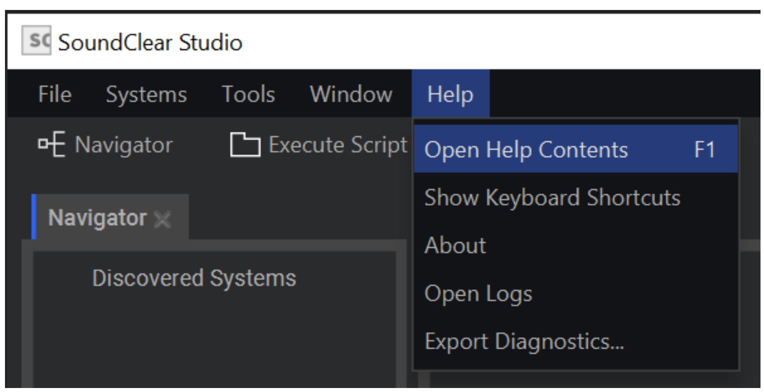

Figure 18: SoundClear Studio – User Guide

2.2.3 Creating a Virtual System

A virtual (non-hardware) version of the system can be created using **“Systems → Add Virtual System..."**

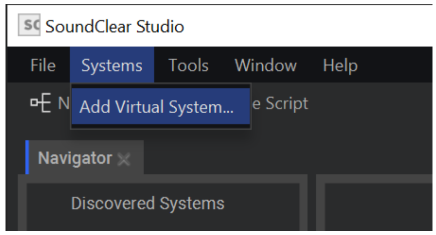

Figure 19: SoundClear Studio – Creating a Virtual System

This opens a dialog box to select an installed system (shown here is the DC4332BSE-DAC):

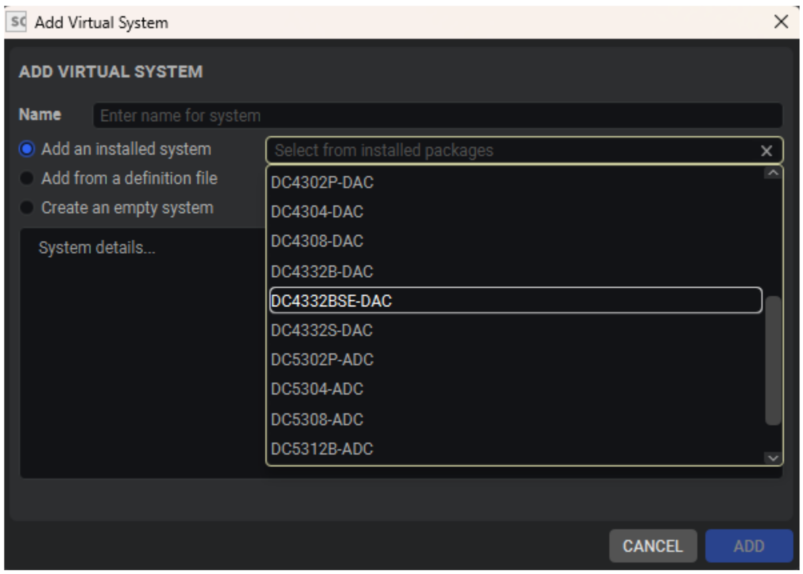

Figure 20: SoundClear Studio – Adding a Virtual System

Once created, a virtual system enables the user to interact with virtual versions of the device register map and helper panels.

2.2.4 Adding an Existing System

SoundClear Studio automatically detects board hardware such as the Jura module and Cirrus Logic devices. In the event of devices not being detected automatically, a device can be added manually. Right click on the system and select **"Add Device…"**

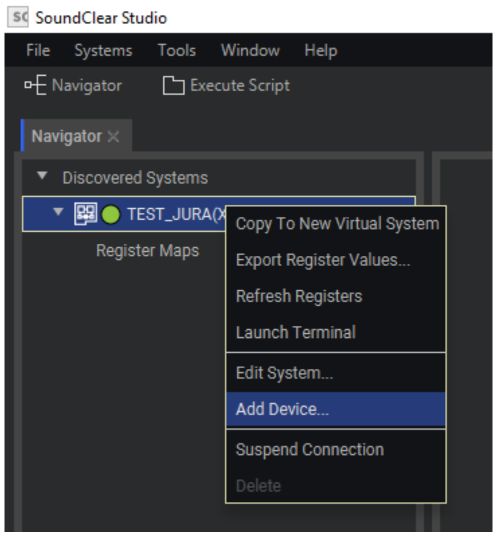

Figure 21: SoundClear Studio – Adding an Existing Device

Then select the device from those installed, along with the protocol and address of the part (this can be edited again by right clicking on the device and selected **"Edit Device..."**):

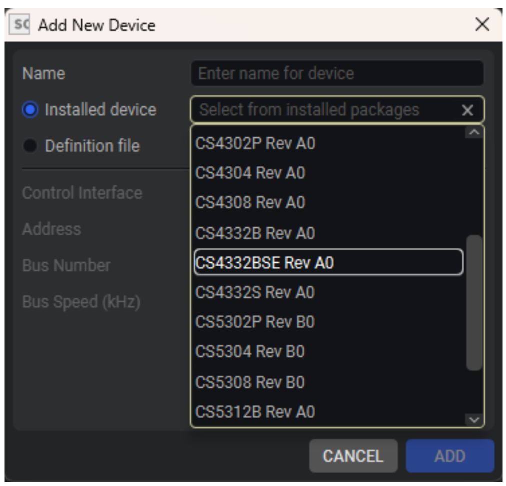

Figure 22: SoundClear Studio – Adding an Existing Device

2.2.5 Executing SoundClear Studio Scripts

SoundClear Studio provides the ability to interact with the device register map using Python® scripts. These scripts can sequence register operations to configure the desire states, which can then be executed from SoundClear Studio using **“File→Execute Script…”**

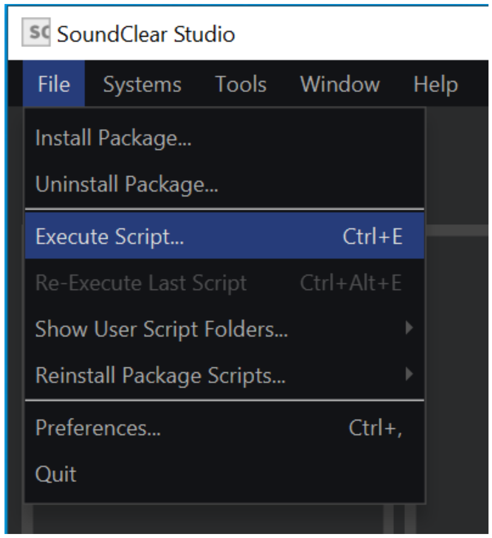

Figure 23: SoundClear Studio – Executing Script

The CS4332BSE SoundClear Studio package installs a set of scripts to configure the device for common use cases. These are available at <User Documents>\Cirrus Logic\SCS\Scripts\<Package Name>.

The scripts can be accessed via **“File→Show User Script Folder→CS4332 Scripts”**

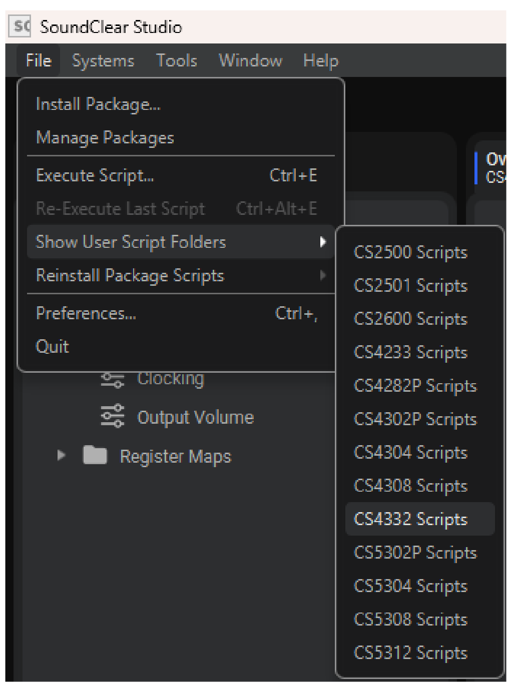

Figure 24: SoundClear Studio – Show User Script Folder

3 DC4332BSE-DAC Software Mode Quick Start

The following steps describe how to start the DC4332BSE-DAC in Software Mode after installing the SoundClear Studio software and the CS4332BSE SCS package:

1. Connect the hardware as shown in Figure 2.
2. Connect the USB cable to the PC.
3. Power up the system and ensure the JURA OK, 1.8 V, 3.3 V, and VDD_5V LEDs are illuminated.
4. Configure signal routing as shown in Section 1.3.
5. Start SoundClear Studio.
   SoundClear Studio should auto-detect the DC4332BSE-DAC daughter card. If not, follow the procedure specified in Section 2.2.4.
6. Run the required script from the following location: <User Documents>\Cirrus Logic\SCS\Scripts\<Package Name>.

4 Hardware Control Mode

The Dunglass system supports Hardware Mode for Cirrus Logic high performance ADC, DAC, and codec devices. These are supported via the rotary switches on the Dunglass system, as illustrated in Figure 25.

Figure 25: Dunglass Rotary Switches for Hardware Control Mode

Each switch has silkscreen on the board to indicate the position of the switch. Each switch position enables a pull resistor on the respective CONFIG pin to VDD_A or ground, as shown in Figure 26.

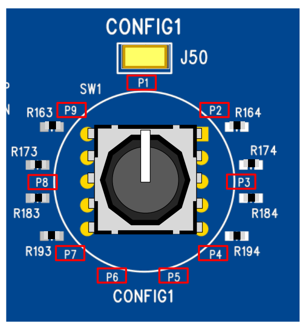

Figure 26: Rotary Switch

If the rotary switches are reconfigured while the Dunglass system is powered, changes will not take effect until the DC4332BSE-DAC is reset by pushing the DUT RESET button.

Note that Hardware Mode is only supported for VDD_IO = 3.3 V on the DC4332BSE-DAC due to the 3.3 V rotary switch pull-up supply on the Dunglass system.

4.1 Hardware Mode Rotary Switch Settings

The CS4332BSE supports Hardware Mode. The rotary switch functions are described in Table 1 to Table 4**Error! Reference source not found.**. Refer to the CS4332BSE datasheet[2] for further details of the Hardware Mode options.

The CONFIG1 pin selects the ASP operating configuration:

Table 1: CONFIG1 Hardware Control – ASP Configuration

Switch Position	Pin Configuration		Description
P1	Pull-up to 3.3 V	0 Ω	Software Control Mode (I^2C/SPI) In I^2C Mode, the pull-up resistor is used to select the device address—see CS4332BSE datasheet. In SPI Mode, it is recommended to use the 100 kΩ pull-up position (P4).
P2		4.7 kΩ	
P3		22 kΩ	
P4		100 kΩ	
P5	Pull-Down to GND	100 kΩ	ASP Primary Mode, 176.4 kHz, 192 kHz sample rate
P6		22 kΩ	ASP Primary Mode, 88.2 kHz, 96 kHz sample rate
P7		4.7 kΩ	ASP Primary Mode, 44.1 kHz, 48 kHz sample rate
P8		0 Ω	ASP Secondary Mode, autodetect sample rate[1]
P9	No Connection	—	—

1. Autodetect sample rate is only supported in MCLK 256 fs(base), MCLK 512 fs(base) or MCLK 1024 fs(base) clocking configurations.

The CONFIG2 pin selects the ASP format and TDM timeslots option:

Table 2: CONFIG2 Hardware Control – ASP Configuration

Switch Position	Pin Configuration		Description
P1	Pull-up to 3.3 V	0 Ω	ASP TDM Mode—minimum time slots, ASP_FSYNC_TYPE = pulse
P2		4.7 kΩ	ASP TDM Mode—maximum time slots, data output on BCLK falling edge (half-cycle mode), ASP_FSYNC_TYPE = pulse
P3		22 kΩ	ASP TDM Mode—maximum time slots, data output on BCLK rising edge (full-cycle mode), ASP_FSYNC_TYPE = pulse
P4		100 kΩ	ASP TDM Mode—minimum time slots, ASP_FSYNC_TYPE = square wave (50% duty cycle)
P5	Pull-Down to GND	100 kΩ	ASP TDM Mode—maximum time slots, data output on BCLK falling edge (half-cycle mode), ASP_FSYNC_TYPE = square wave (50% duty cycle)
P6		22 kΩ	ASP TDM Mode—maximum time slots, data output on BCLK rising edge (full-cycle mode), ASP_FSYNC_TYPE = square wave (50% duty cycle)
P7		4.7 kΩ	ASP Left-Justified Mode
P8		0 Ω	ASP I^2S Mode
P9	No Connection	—	—

The CONFIG3 pin selects the TDM slot selection in TDM Mode:

Table 3: CONFIG3 Hardware Control – TDM Slot Selection

Switch Position	Pin Configuration		Description
P1	Pull-up to 3.3 V	0 Ω	Slots 14–15
P2		4.7 kΩ	Slots 12–13
P3		22 kΩ	Slots 10–11
P4		100 kΩ	Slots 8–9
P5	Pull-Down to GND	100 kΩ	Slots 6–7
P6		22 kΩ	Slots 4–5
P7		4.7 kΩ	Slots 2–3
P8		0 Ω	Slots 0–1
P9	No Connection	—	—

The CONFIG4 pin selects the clock reference and ASP channel ordering:

Table 4: CONFIG4 Hardware Control – Clocking Configuration

Switch Position	Pin Configuration		Clock Reference	Reference Clock Frequency (MHz)	Virtual PAD
P1	Pull-up to 3.3 V	0 Ω	XTAL	1024 fs(base) [1]	Bypassed
P2		4.7 kΩ	XTAL	512 fs(base)	
P3		22 kΩ	MCLK	1024 fs(base)	
P4		100 kΩ	MCLK	512 fs(base)	
P5	Pull-Down to GND	100 kΩ	MCLK	1024 fs(base)	Enabled – Level Detection
P6		22 kΩ	MCLK	512 fs(base)	
P7		4.7 kΩ	MCLK	1024 fs(base)	Enabled – Edge Detection
P8		0 Ω	MCLK	512 fs(base)	
P9	No Connection	—	—	—	—

1. fs(base) is the base sample rate.
fs(base) = 48 kHz for 48 kHz-related sample rates; fs(base) = 44.1 kHz for 44.1 kHz-related sample rates.

5 Output Buffer Circuits

5.1 Output Buffer

The CS4332BSE incorporates a high-performance sigma-delta current-mode DAC with integrated operational amplifiers for current-to-voltage conversion. The external components for the current-to-voltage conversion and out-of-band filtering implemented on the DC4332BSE-DAC daughter card are shown in Figure 27. This circuit produces a 1 V_{RMS} single-ended output from a full-scale (0 dBFS) digital input. This output option is selected by selecting OUT1 and OUT2 as shown in Figure 13

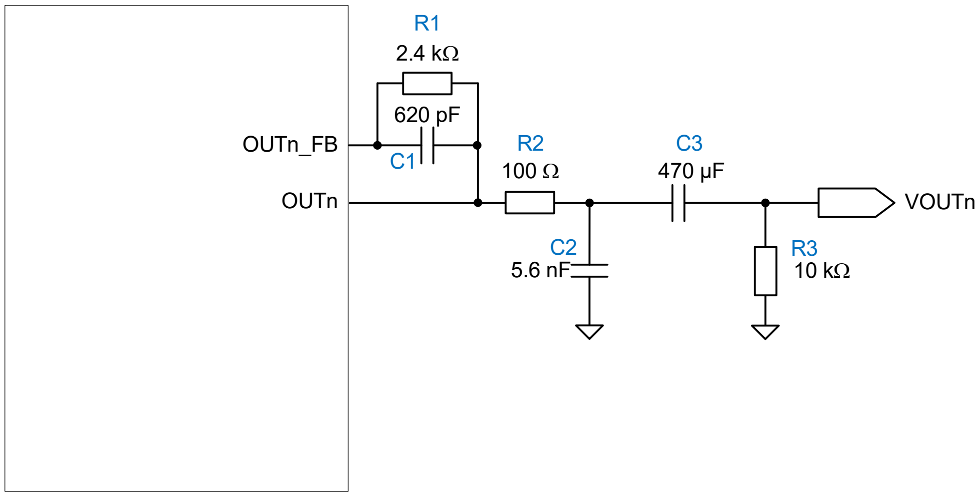

Figure 27: Output Buffer

The feedback resistor, R1 determines the full-scale single-ended output voltage; a maximum output voltage of 1 V_{RMS} is supported at the OUTn pins. R1 is calculated as follows:

$$R_1(k\Omega) = \frac{\text{Full-scale output voltage } (V_{RMS})}{0.418 \text{ mA}_{RMS}} = \frac{1}{0.418\times10^{-3}} = 2.4 \text{ k}\Omega$$

The filter is provided by the integrated operational amplifiers and associated feedback components C1 and R1. The objective is to provide a flat passband for the audio output bandwidth. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi\times2400\times620\times10^{-12}} = 107 \text{ kHz}$$

R2 and C2 create an output filter to reduce out-of-band noise of the output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_2 C_2} = \frac{1}{2\pi\times100\times5.6\times10^{-9}} = 284 \text{ kHz}$$

R3 and C3 form a high-pass filter, which removes the DC bias of the voltage output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_3 C_3} = \frac{1}{2\pi\times10\times10^3\times470\times10^{-6}} = 0.03 \text{ kHz}$$

5.1.1 Active Line Driver Circuit

Additionally, the DC4332BSE-DAC has an active line driver circuit, as shown in Figure 28. This circuit produces a 4.2 V_{RMS} output from a full-scale (0 dBFS) digital input. This output option is selected by selecting LO1 and LO2 as shown in Figure 14

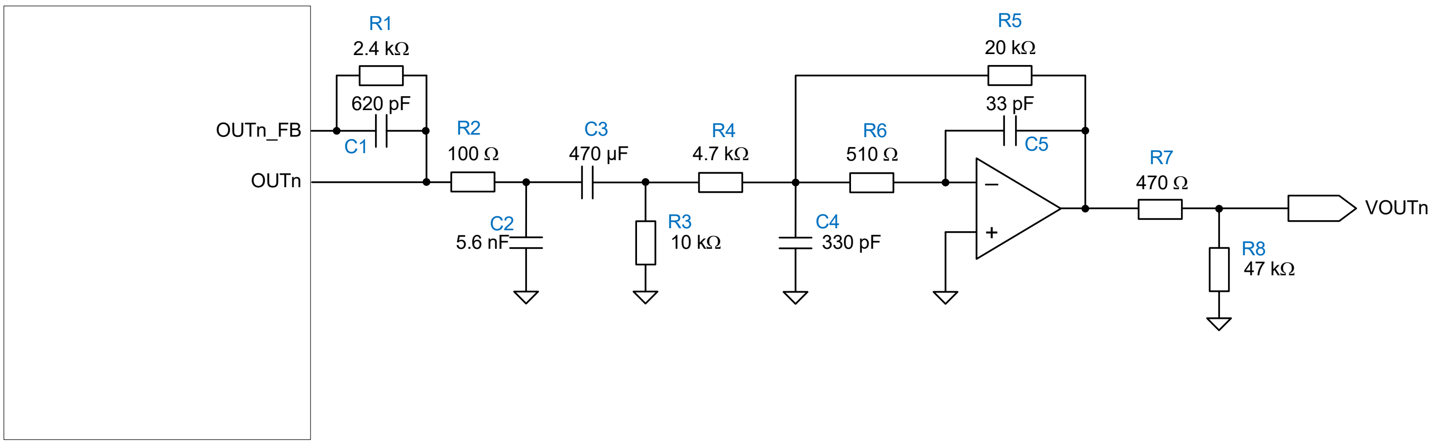

Figure 28: Active Line Driver Circuit

The feedback resistor, R1 determines the full-scale single-ended output voltage; a maximum output voltage of 1 V_{RMS} is supported at the OUTn pins. R1 is calculated as follows

$$R_1 = \frac{\text{Max Output Voltage } (V_{RMS})}{0.418\text{mA}_{RMS}} = \frac{1}{0.418\times10^{-3}} = 2.4\ \text{k}\Omega$$

The filter is provided by the integrated operational amplifiers and associated feedback components C1 and R1. The objective is to provide a flat passband for the audio output bandwidth. The cut-off frequency of the filter is calculated as follows:

$$F_c = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\times\pi\times2400\times620\times10^{-12}} = 107\ \text{kHz}$$

R2 and C2 create an output filter to reduce out-of-band noise of the output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_2 2C_2} = \frac{1}{2\pi\times100\times5.6\times10^{-9}} = 284\ \text{kHz}$$

C3 removes the DC bias of the CS4332BSE output and forms a high pass filter with parallel resistance of R3 and R4. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi(R_3||R_4)C_3} = \frac{1}{2\times\pi\times\left(\frac{10\times10^3\times4.7\times10^3}{10\times10^3+4.7\times10^3}\right)\times470\times10^{-6}} = 0.1\ \text{Hz}$$

R4 and C4 create a low pass filter. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_4 C_4} = \frac{1}{2\times\pi\times4.7\times10^3\times330\times10^{-12}} = 102.6\ \text{kHz}$$

R5, R6 and C5 create a low pass filter within the OPAMP feedback loop. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi(R_6+R_5)C_5} = \frac{1}{2\times\pi\times(510+20\times10^3)\times33\times10^{-12}} = 235.1\ \text{kHz}$$

The gain of the output buffer is determined by the ratio R4 and R5.

$$\text{Gain} = \frac{R_5}{R_4} = \frac{20\times10^3}{4.7\times10^3} = 4.2$$

5.1.2 Active Headphone Circuit

The DC4332BSE-DAC has a 6.3 mm stereo headphone jack that is controlled by an active circuit, as shown in Figure 29. This circuit produces a 2.1 V_{RMS} output from a full-scale (0 dBFS) digital input. This output option is selected by selecting HPR and HPL as shown in Figure 15.

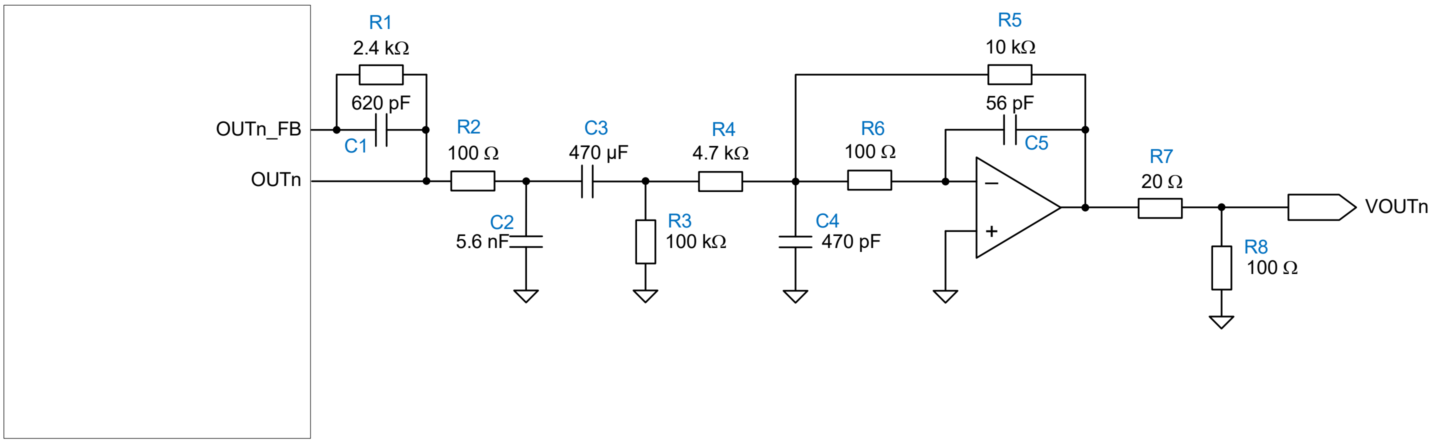

Figure 29 Active Headphone Circuit

The feedback resistor, R1 determines the full-scale single-ended output voltage; a maximum output voltage of 1 V_{RMS} is supported at the OUTn pins. R1 is calculated as follows

$$R_1 = \frac{\text{Max Output Voltage }(V_{RMS})}{0.418\text{mA}_{RMS}} = \frac{1}{0.418\times10^{-3}} = 2.4\text{ k}\Omega$$

The filter is provided by the integrated operational amplifiers and associated feedback components C1 and R1. The objective is to provide a flat passband for the audio output bandwidth. The cut-off frequency of the filter is calculated as follows:

$$F_c = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\times\pi\times2400\times620\times10^{-12}} = 107\text{ kHz}$$

R2 and C2 create an output filter to reduce out-of-band noise of the output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_2 C_2} = \frac{1}{2\pi\times100\times2.2\times10^{-9}} = 723\text{ kHz}$$

C3 removes the DC bias of the CS4332BSE output and forms a high pass filter with parallel resistance of R3 and R4. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi(R_3||R_4)C_3} = \frac{1}{2\times\pi\times\left(\frac{100\times10^3\times4.7\times10^3}{100\times10^3+4.7\times10^3}\right)\times470\times10^{-6}} = 0.75\text{ Hz}$$

R4 and C4 create a low pass filter. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_4 C_4} = \frac{1}{2\times\pi\times4.7\times10^3\times470\times10^{-9}} = 72\text{ kHz}$$

R5, R6 and C5 create a low pass filter within the OPAMP feedback loop. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi(R_5+R_6)C_5} = \frac{1}{2\times\pi\times\left(10\times10^3+100\right)\times56\times10^{-12}} = 281\ \text{kHz}$$

The gain of the output buffer is determined by the ratio R4 and R5.

$$\text{Gain} = \frac{R_5}{R_4} = \frac{10\times10^3}{4.7\times10^3} = 2.1$$

6 Notices

JURA firmware development utilizes components under the following licenses:

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Unmodified USB Audio 2.0 Device Software source code is available from www.xmos.ai under XMOS PUBLIC LICENCE: Version 1.

7 References

[1] Cirrus Logic, CDB-PROAUDIO_DS1352DB; Dunglass System (CDB-PROAUDIO)

[2] Cirrus Logic, CS4332BSE_DS1430; High Performance Two-Channel Audio DAC Datasheet

8 Revision History

Revision	Changes
DB1 MAY 2026	• Initial version.

Contacting Cirrus Logic Support
For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.