DC5302P/4P/4S/8P/8S-ADC User Guide

Introduction

The DC53xx-ADC are daughter cards for the Cirrus Logic Dunglass (CDB-PROAUDIO) system for high performance ADC, DAC and codec devices. This user guide details how to connect the DC53xx-ADC to a Dunglass (CDB-PROAUDIO) system platform and how to get started. The User Guide covers the following daughter cards:

- DC5302P-ADC
- DC5304P-ADC
- DC5304S-ADC
- DC5308P-ADC
- DC5308S-ADC

The default jumper link configuration for DC5308P/8S-ADC is shown in Figure 1.

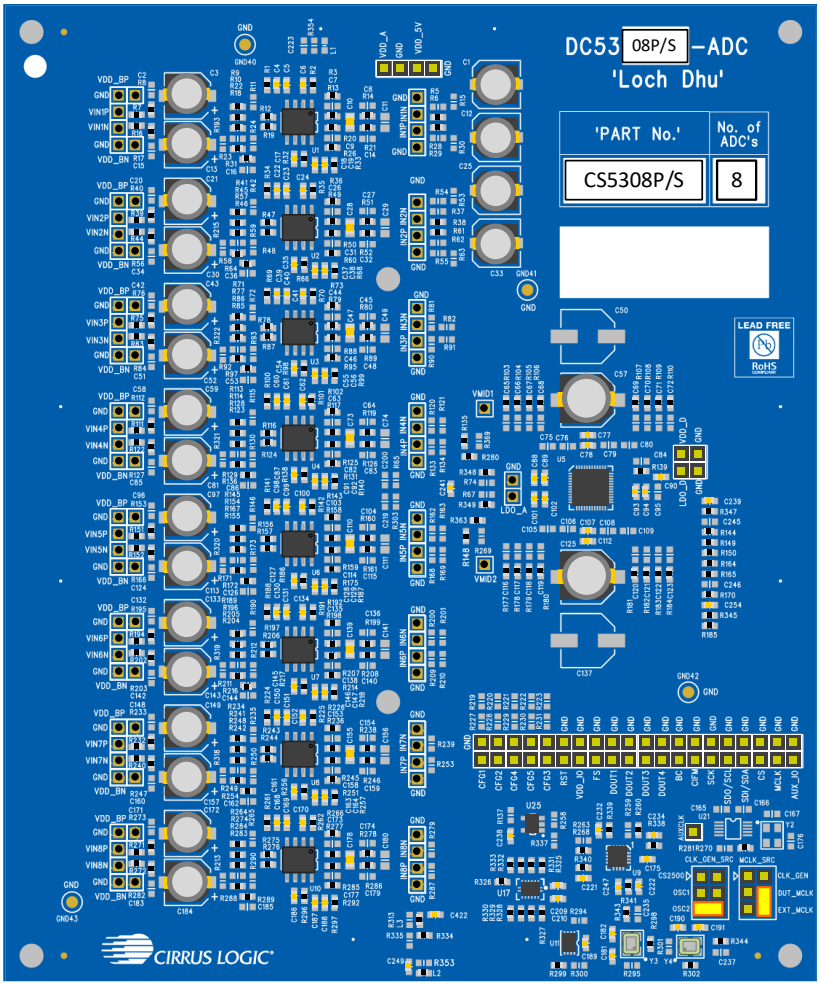


Figure 1: DC5308P/8S-ADC Daughter Card

The default jumper link configuration for DC5304P/4S-ADC is shown in Figure 2.

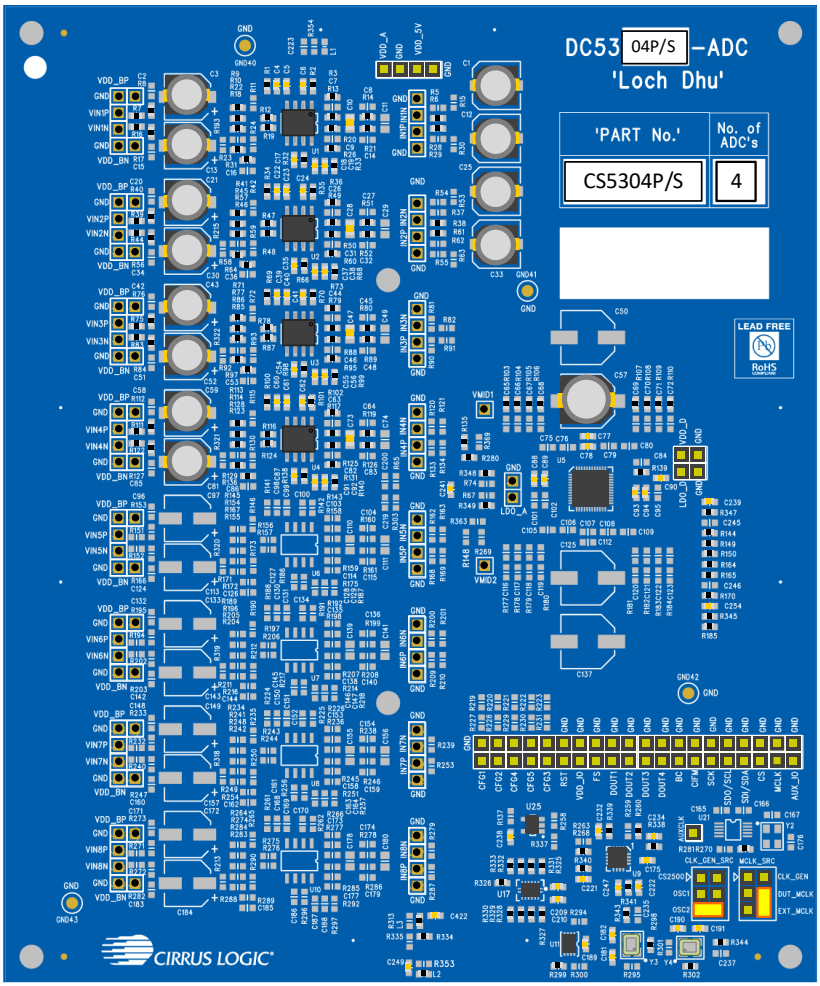


Figure 2: DC5304P/4S-ADC Daughter Card

The default jumper link configuration for DC5302P-ADC is shown in Figure 3.

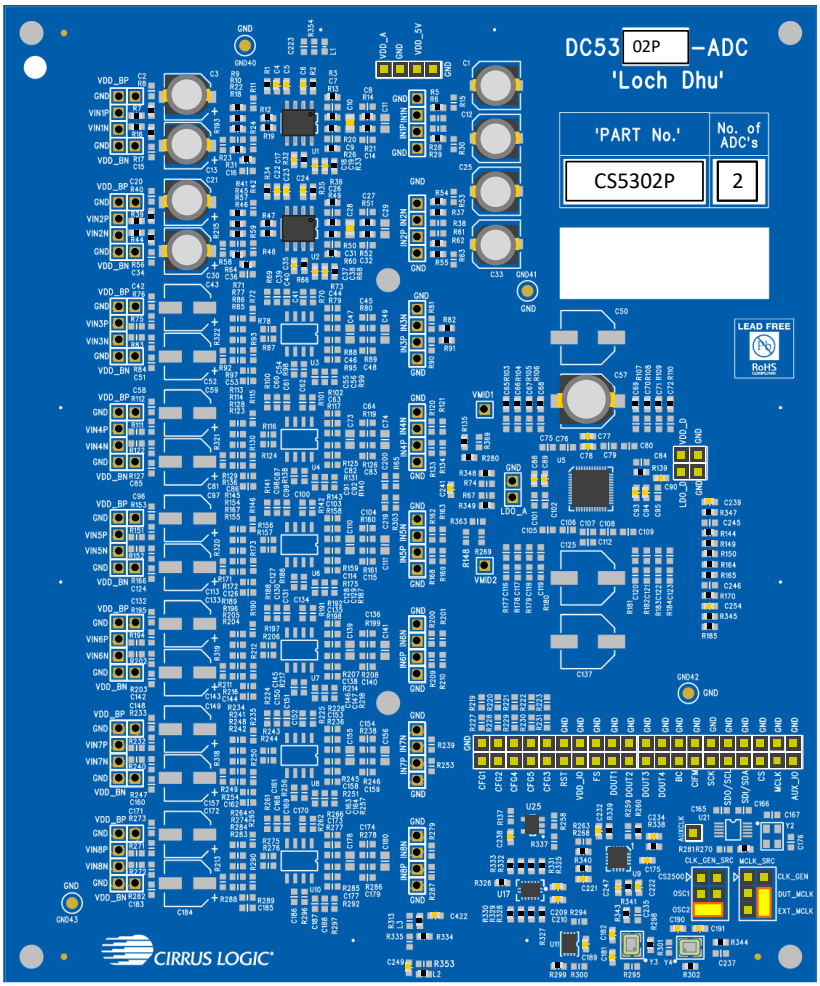


Figure 3: DC5302P-ADC Daughter Card

Table of Contents

1 Hardware Connections

The Dunglass system supports interchangeable daughter cards for a variety of ADC, DAC and codec devices.

Caution:

Daughter cards should not be inserted or removed while the Dunglass system is powered. Fully disconnect or power down external power supply before changing daughter cards.

For more information on the Dunglass (CDB-PROAUDIO) platform, refer to the CDB-PROAUDIO User Guide.

1.1 How to Connect DC530xx-ADC onto the Dunglass System

The DC5302P/4P/4S/8P/8S-ADC is a 4-header daughter card and should be plugged onto DCJ1, DCJ2, DCJ3 & DCJ4. The daughter card connectors are keyed and will only plug in one way. There is also an alignment dot on each board to help with placement.

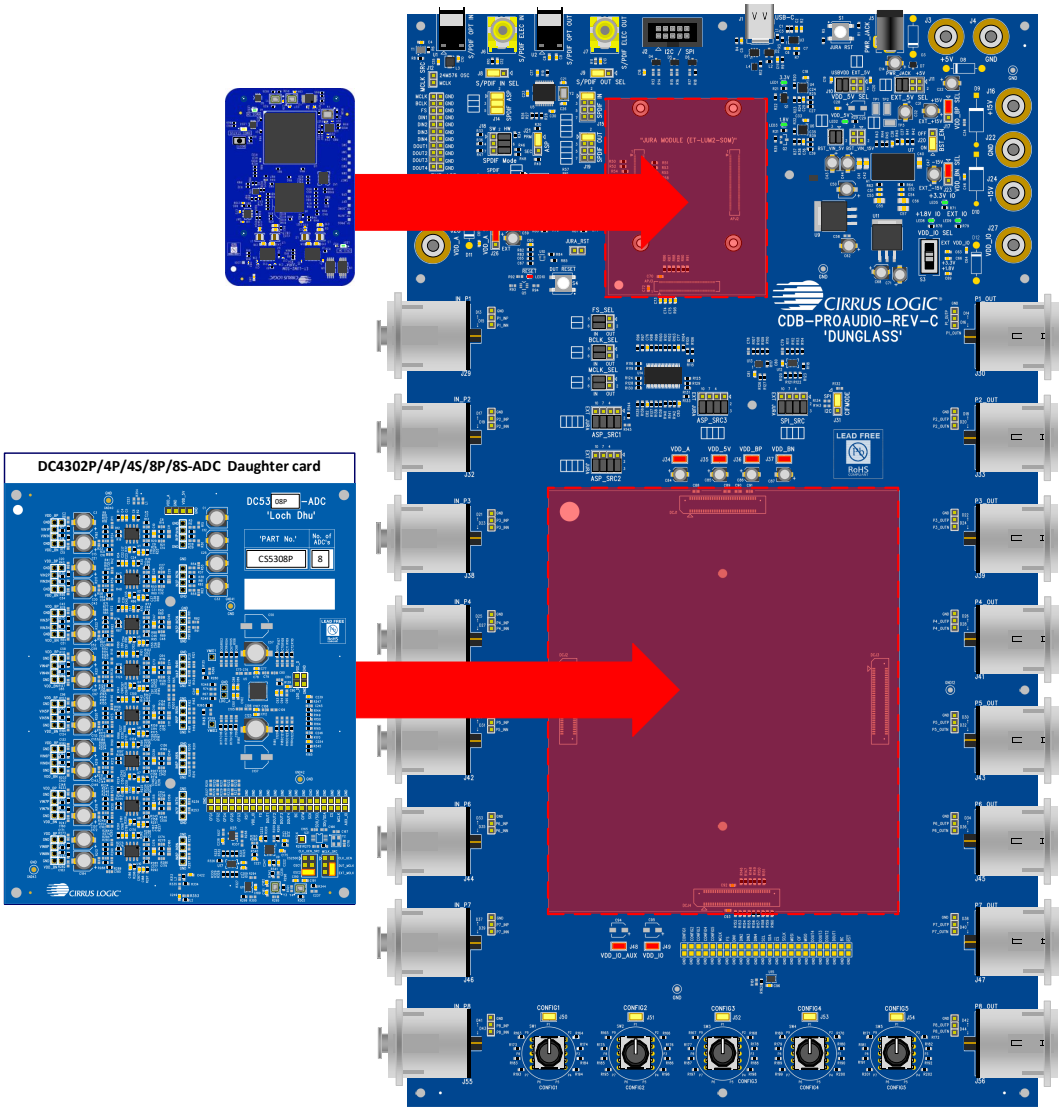


Figure 4: How to Connect DC5302P/P/4S/8P/8S-ADC onto the Dunglass System

1.2 USB & Power Connection

Dunglass is powered using a 5V external power supply and is controlled via a single USB connection. The Jura module supports the following functions via the USB connection:

- I2C/SPI communications to control device and board.
- Multichannel USB streaming audio (USB class 2).

The board is provided with a USB-A to USB-C cable and a 5V wall supply.

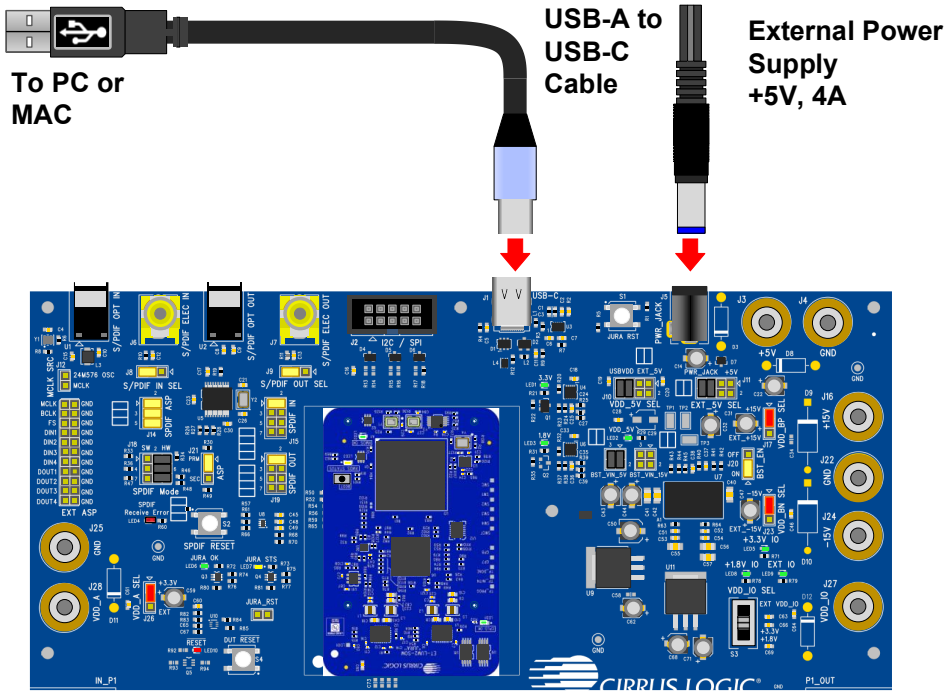


Figure 5: Dunglass (CDB-PROAUDIO) USB & Power Connection

A Total Phase Aardvark connector can be used for I2C/SPI communication. Refer to the CDB-PROAUDIO User Guide for more details.

1.2.1 JURA Module

The Jura module supports I2C/SPI communication to control the Dunglass system and daughter card; it also enables multichannel USB streaming audio (USB audio Class 2).

The Jura module is connected to the Dunglass board as shown below:

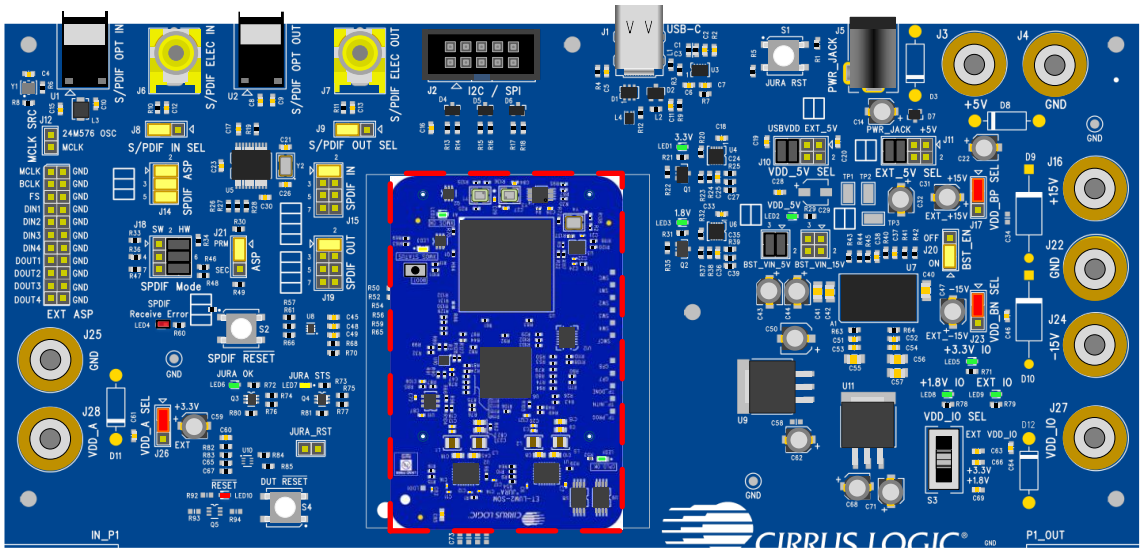


Figure 6: How to Connect JURA Module to Dunglass System

1.2.2 Dunglass Boot Procedure with Jura Module

The USB-C cable must be connected between the Dunglass system and the PC/Mac prior to powering up the board.

The boot time of the Dunglass system varies depending on the version of firmware on the Jura module but is typically in the range of 2 to 5 seconds after applying power to the board.

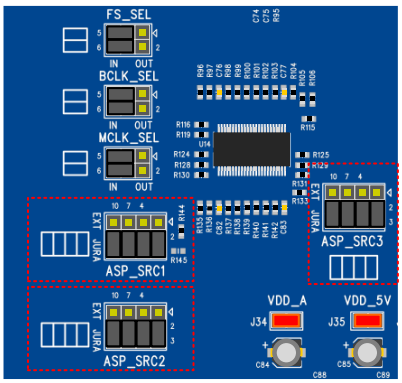
1.3 Routing the Digital Audio Signals

The digital audio PCM paths to the daughter card can be routed from the Jura module, or else from the EXT ASP header and S/PDIF transceiver. The routing is configured using the ASP_SRC1, ASP_SRC2 & ASP_SRC3 headers.

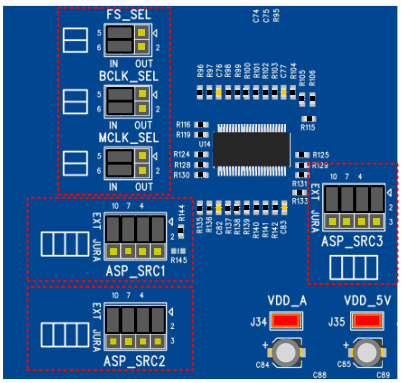
- JURA = Digital audio signals routed from Jura module.
- EXT = Digital audio signals routed from EXT ASP header/SPDIF.

The ASP_SRC1, ASP_SRC2 & ASP_SRC3 headers are configured as shown in Table 1.

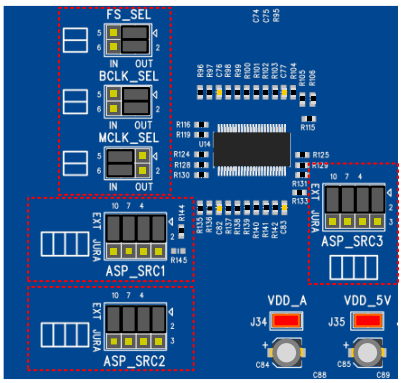
Table 1 Digital Signal Routing



Jura Module Primary Mode



EXT ASP / SPDIF Primary Mode



EXT ASP / SPDIF Secondary Mode

The Jura module always operates in Primary Mode – the MCLK, BCLK and FSYNC are generated by the Jura module, as inputs to the daughter card.

If the digital audio is routed from the EXT ASP header or S/PDIF transceiver, the direction of the MCLK, BCLK, and FSYNC signals are configured using the MCLK_SEL, BCLK_SEL & FS_SEL headers. Each signal is configured independently using the respective header.

- IN = EXT_ASP header or S/PDIF transceiver supports the signal as input to the daughter card
- OUT = EXT_ASP header or S/PDIF transceiver supports the signal as output from the daughter card

Note that the EXT ASP header and S/PDIF transceiver use 3.3 V logic levels; a level shifter is incorporated to interface with the VDD_IO domain on the DC5302P/4P/4S/8P/8S-ADC daughter card.

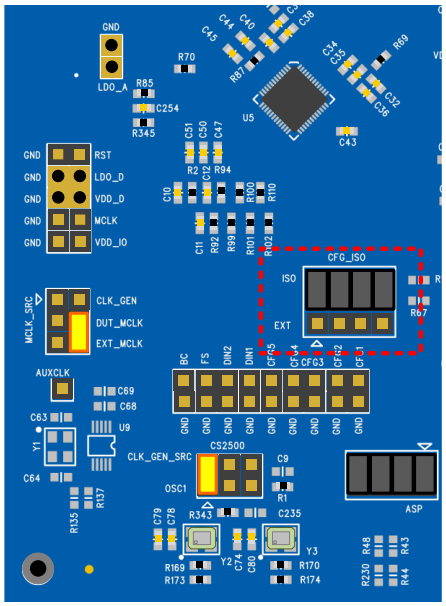
1.4 Selection of Hardware/Software Control Mode

The CS4282P supports Hardware and Software modes. The hardware and software modes are set via the CFG_ISO header on the DC4282P-CODEC and the rotary switches on the Dunglass system. The jumper link must be configured as in Table 2.

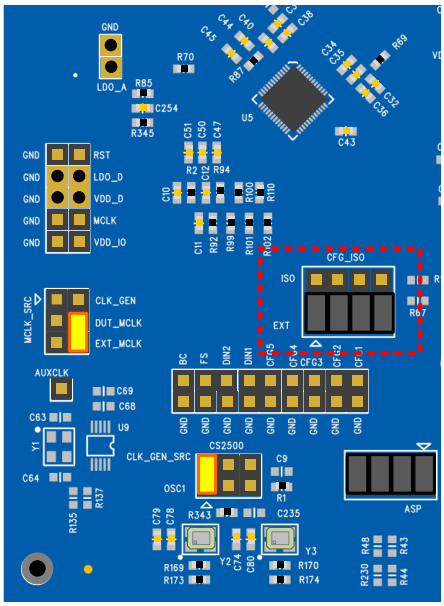
- ISO = Software mode.
- EXT = Hardware mode.

In Hardware mode, rotary switches are used to select the desired configuration. See Section 4 for information on hardware mode.

Table 2 Software/Hardware mode Jumper Link Configuration for DC4282P-CODEC



Software Mode Jumper Link Configuration



Hardware Mode Access Jumper Link Configuration

Note that Hardware mode is only supported for VDD_IO = 3.3V on the DC5302P/4P/4S/8P/8S-ADC daughter card due to the rotary switch pull-up supply = 3.3V on the Dunglass system.

1.5 DC5302P/4P/4S/8P/8S-ADC MCLK Source Selection

The DC5302P/4P/4S/8P/8S-ADC board provides two on-board oscillators that can be used as an MCLK source for the CS5302P/4P/4S/8P/8S. The oscillators are configured for different frequencies; the oscillators are enabled by removing the applicable resistor on the DC5302P/4P/4S/8P/8S-ADC board.

- OSC1 (11.2896 MHz). Enabled by removing R298.
- OSC2 (12.288 MHz). Enabled by removing R302.

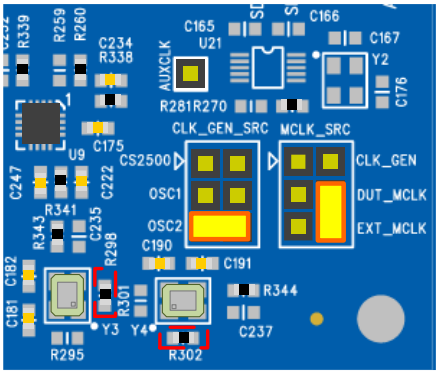
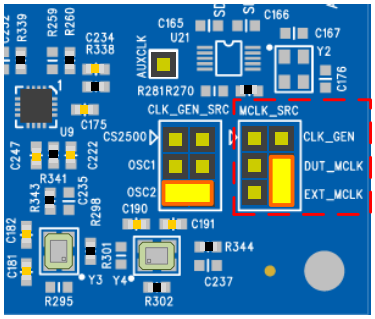


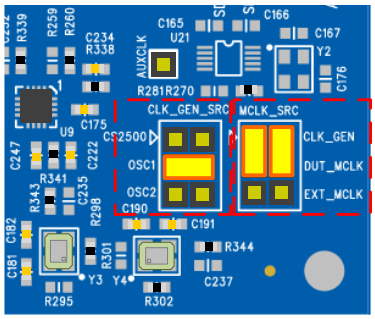
Figure 7: Enabling On-board Oscillators

The MCLK source is configured as shown in Table 3.

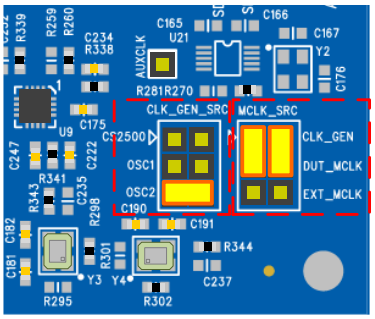
Table 3 MCLK Source Jumper Link Config



MCLK source = Dunglass System (Default)



MCLK source = OSC1



MCLK source = OSC2

2 Driver Installation and SoundClear Studio Support

2.1 SoundClear Studio

SoundClear Studio (SCS) is a PC/Mac-based tool used to configure Cirrus Logic devices. The tools suite provides support for evaluation and development and can be used with Dunglass system and associated daughter cards.

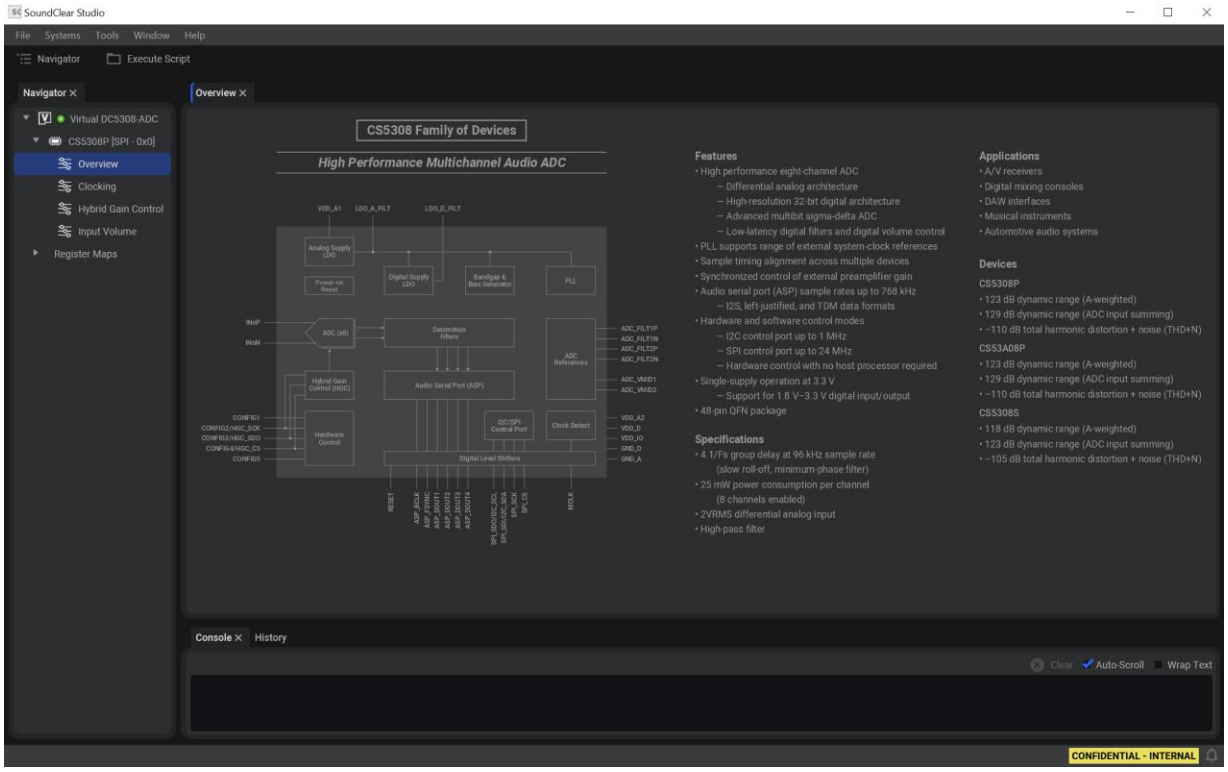


Figure 8: SoundClear Studio

2.1.1 Download SoundClear Studio Software & Drivers

SoundClear *Studio* and associated software collateral required for the Dunglass system can be downloaded from *https://cirrus.com*.

- https://cirrus.com/products/cs5302p/
- https://cirrus.com/products/cs5304p/
- https://cirrus.com/products/cs5308p/

The required components are as follows:

- **SoundClear Studio 2.1.** Run the appropriate installer on your Windows or macOS computer to install SoundClear Studio.
- **CS5302P SCS Package.** Install this in SoundClear Studio to incorporate the CS5302-specific software components in SoundClear Studio for CS5302P. See Section 2.2.1 for details on how to install an SCS package.
- **CS5304 SCS Package.** Install this in SoundClear Studio to incorporate the CS5304-specific software components in SoundClear Studio for CS5304P & CS5304S. See Section 2.2.1 for details on how to install an SCS package.
- **CS5308 SCS Package.** Install this in SoundClear Studio to incorporate the CS5308-specific software components in SoundClear Studio for CS5308P & CS5308S. See Section 2.2.1 for details on how to install an SCS package.
- **Jura Windows Setup.** On Windows computers, run the Cirrus Logic USB Audio Setup to install the driver that enables SoundClear Studio to communicate with the Jura board.

2.2 SoundClear Studio Quick Start Guide

2.2.1 Installing Packages

Each daughter card has its own individual SoundClear Studio package that must be installed separately from the main SoundClear Studio Software. These are installed from the main menu using **"File → Install Package..."**. Multiple packages can be installed together by selecting more than one using the file dialog.

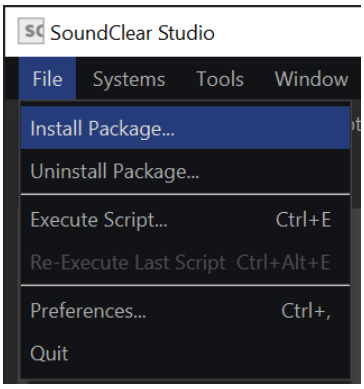


Figure 9: SoundClear Studio – Installing Board Packages

2.2.2 SoundClear Studio User Guide

The SoundClear Studio User Guide can be accessed from the main menu using **"Help → Open Help Contents..."**

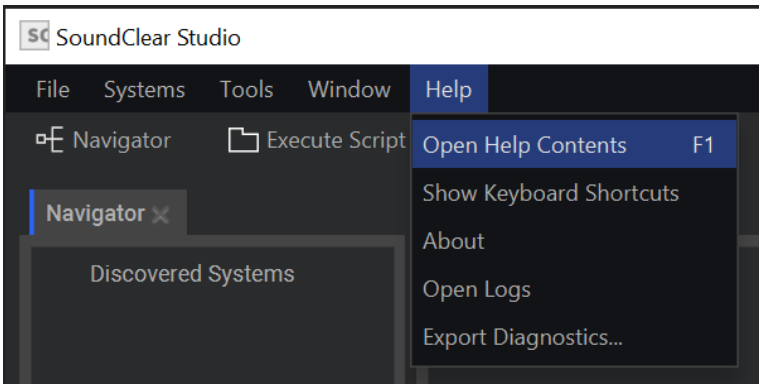


Figure 10: SoundClear Studio – User Guide

2.2.3 Creating a Virtual System

A virtual (non-hardware) version of the system can be created using **“Systems → Add Virtual System..."**

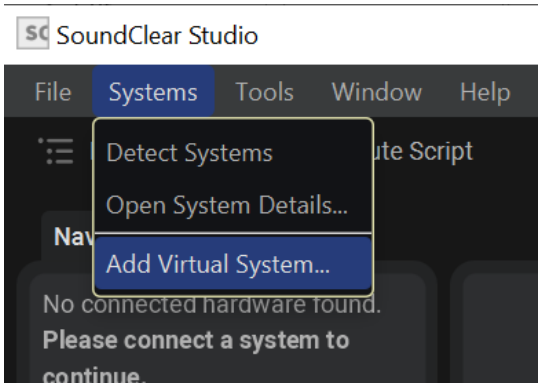


Figure 11: SoundClear Studio – Creating a Virtual System

This opens a dialog to select an installed system (shown here is the DC5308-ADC):

Note: The DC5308-ADC supports the DC5308P-ADC & DC5308S-ADC boards

Note: The DC5304-ADC supports the DC5304P-ADC & DC5304S-ADC boards

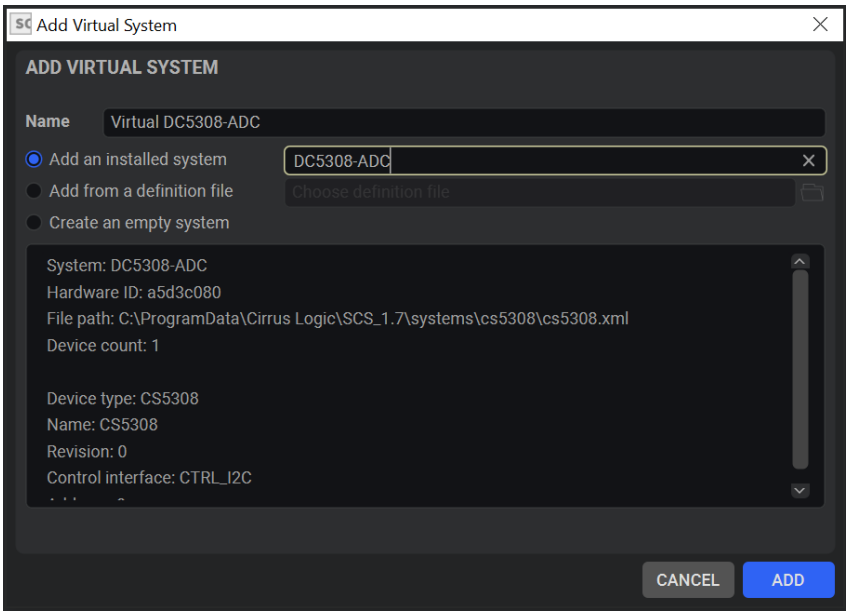


Figure 12: SoundClear Studio – Adding a Virtual System

Once created, a virtual system enables the user to interact with virtual versions of the device register map and helper panels.

2.2.4 Adding an Existing System

SoundClear Studio automatically detects board hardware such as the Jura module and Cirrus Logic devices. In the event of devices not being detected automatically, a device can be added manually. Right click on the system and select **"Add Device…"**

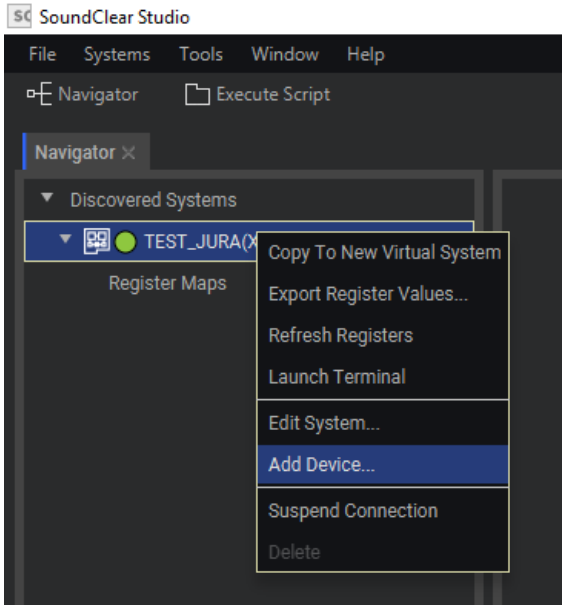


Figure 13: SoundClear Studio – Adding an Existing System

Then select the device from those installed, along with the protocol and address of the part (this can be edited again by right clicking on the device and selected **"Edit Device..."**):

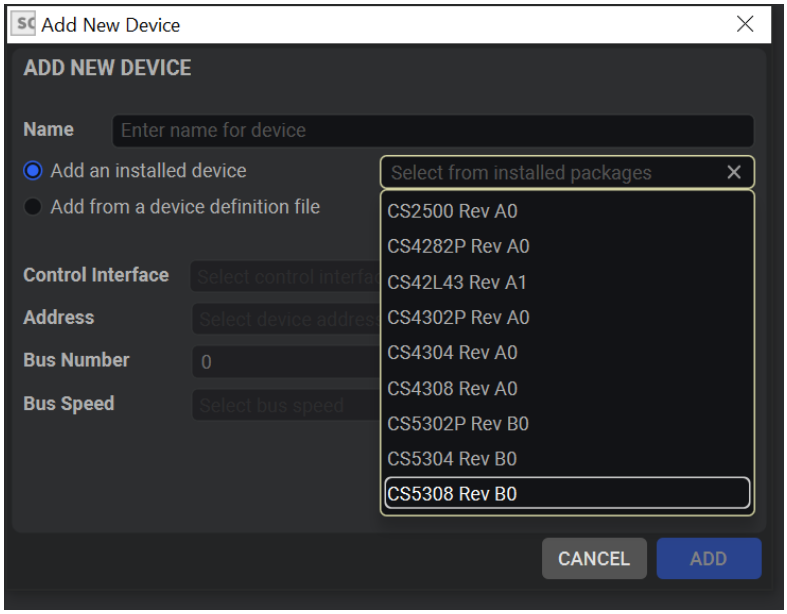


Figure 14: SoundClear Studio – Adding an Existing System

2.2.5 Executing SoundClear Studio Scripts

SoundClear Studio provides the ability to interact with the device register map using Python scripts. These scripts can sequence register operations to configure the desire into desired states, which can then be executed from SoundClear Studio using **"File→Execute Script…"**

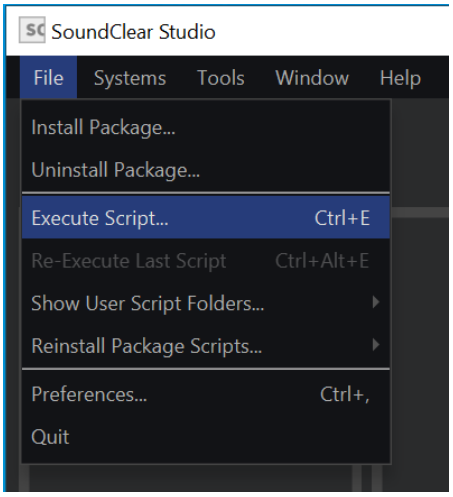


Figure 15: SoundClear Studio – Executing Script

The DC5308P-ADC SoundClear Studio package installs a set of scripts to configure the device for common use cases. The scripts are available at <User Documents>\Cirrus Logic\SCS\Scripts\<Package Name>.

The CS5308P scripts can be accessed from SoundClear Studio using **"File→Show User Script Folder→CS5308P"**

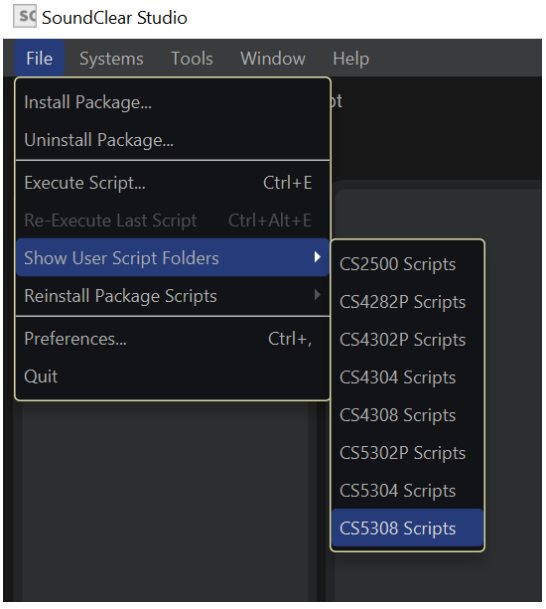


Figure 16: SoundClear Studio – Show User Script Folder

3 DC5302P/4P/4S/8P/8S-ADC Software Mode Quick Start

After installing the SoundClear Studio software and the applicable CS5308, CS5304, or CS5302P SCS package, follow the steps below to get up and running quickly:

- Connect the hardware as shown in Figure 4.
- Connect USB cable to PC
- Power up the system and ensure JURA OK, 1.8V, 3.3V, VDD_5V LEDs are illuminated.
- Configure signal routing as shown in Table 1
  - For SPDIF output see Section 5
- Start SoundClear Studio
  - SoundClear Studio should auto-detect the DC53xx-ADC daughter card. If not, follow the procedure specified in Section 2.2.4
- Run one of the scripts from the following location.
  - <User Documents>\Cirrus Logic\SCS\Scripts\<Package Name>.

4 Hardware Mode Control

The Dunglass system supports the hardware control modes for Cirrus Logic high performance ADC, DAC and Codec devices. These are supported via the rotary switches on the Dunglass system.

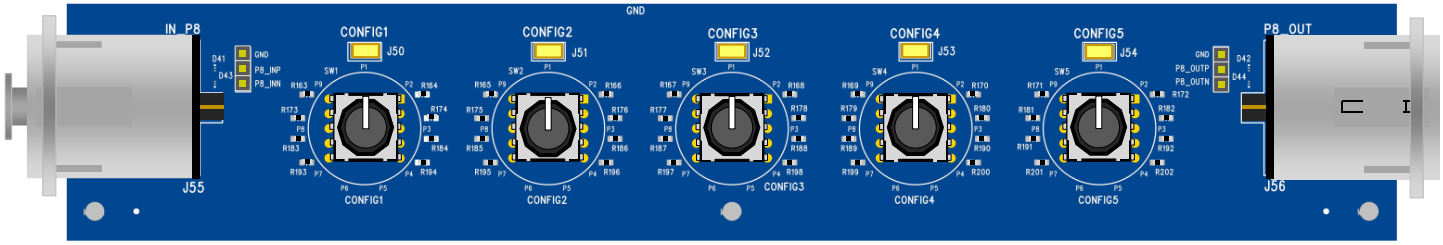


Figure 17: Dunglass Rotary Switches for Hardware Control Mode

Each switch has silkscreen on the board to indicate the position of the switch. Each switch position enables a pull resistor on the respective CONFIG pin to VDD_A or ground.

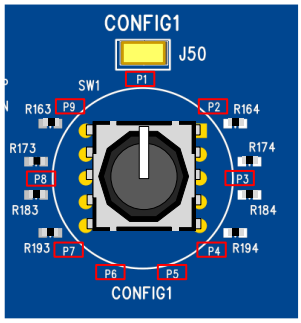


Figure 18: Rotary Switch

Note that, if the rotary switches are reconfigured while the Dunglass system is powered, the daughter card needs to be reset for the changes to take effect. This is done by pushing the DUT RESET button.

4.1 Hardware Mode Rotary Switch Settings

The rotary switch functions are described in the following tables. Refer to the CS5302P/4P/4S/8P/8S datasheet for further details of the hardware-mode control options.

The CONFIG1 pin selects the ASP operating configuration.

Table 4: CONFIG1 Hardware Control – ASP Configuration

Switch Position	Config Pin Configuration		Description
P1	Pull-up to VDD_A	0 Ω	Software control mode (I2C/SPI)
P2		4.7 kΩ	ASP Primary Mode, 44.1 kHz, 48 kHz sample rate
P3		22 kΩ	ASP Primary Mode, 88.2 kHz, 96 kHz sample rate
P4		100 kΩ	ASP Primary Mode, 176.4 kHz, 192 kHz sample rate
P5	Pull-Down to GND	100 kΩ	ASP Secondary Mode, 176.4 kHz, 192 kHz sample rate
P6		22 kΩ	ASP Secondary Mode, 88.2 kHz, 96 kHz sample rate
P7		4.7 kΩ	ASP Secondary Mode, 44.1 kHz, 48 kHz sample rate
P8		0 Ω	ASP Secondary Mode, autodetect sample rate
P9	No Connection	—	—

The CONFIG2 pin selects the ASP format and TDM timeslots option.

Table 5: CONFIG2 Hardware Control – ASP Configuration

Switch Position	Config Pin Configuration		Description
P1	Pull-up to VDD_A	0 Ω	ASP TDM Mode—minimum time slots
P2		4.7 kΩ	ASP TDM Mode—maximum time slots, data output on BCLK falling edge (half-cycle mode)
P3		22 kΩ	ASP TDM Mode—maximum time slots, data output on BCLK rising edge (full-cycle mode)
P4		100 kΩ	—
P5	Pull-Down to GND	100 kΩ	—
P6		22 kΩ	—
P7		4.7 kΩ	ASP Left-Justified Mode
P8		0 Ω	ASP I^2S Mode
P9	No Connection	—	—

The CONFIG3 pin selects the TDM slot selection in TDM Mode.

Table 6: CONFIG3 Hardware Control – TDM Slot Selection

Switch Position	Config Pin Configuration		Description – CS5302P	Description – CS5304P/4S	Description – CS5308P/8S
P1	Pull-up to 3.3V	0 Ω	Slots 14–15	Slots 12–15	Slots 8–15
P2		4.7 kΩ	Slots 12–13		
P3		22 kΩ	Slots 10–11	Slots 8–11	
P4		100 kΩ	Slots 8–9		
P5	Pull-Down to GND	100 kΩ	Slots 6–7	Slots 4–7	Slots 0–7
P6		22 kΩ	Slots 4–5		
P7		4.7 kΩ	Slots 2–3	Slots 0–3	
P8		0 Ω	Slots 0–1		
P9	No Connection	—	—	—	—

The CONFIG4 pin selects the ASP channel ordering.

Table 7: CONFIG4 Hardware Control – ASP Channel Order

Switch Position	Config Pin Configuration		Channel Order
P1	Pull-up to VDD_A	0 Ω	—
P2		4.7 kΩ	Default
P3		22 kΩ	—
P4		100 kΩ	—
P5	Pull-Down to GND	100 kΩ	—
P6		22 kΩ	—
P7		4.7 kΩ	Reversed
P8		0 Ω	—
P9	No Connection	—	—

The CONFIG5 pin selects the digital filter.

Table 8: CONFIG5 Hardware Control – Digital Filter Selection

Switch Position	Config Pin Configuration		Description
P1	Pull-up to VDD_A	0 Ω	Minimum phase, slow roll-off, HPF bypass
P2		4.7 kΩ	Minimum phase, fast roll-off, HPF bypass
P3		22 kΩ	Linear phase, slow roll-off, HPF bypass
P4		100 kΩ	Linear phase, fast roll-off, HPF bypass
P5	Pull-Down to GND	100 kΩ	Linear phase, fast roll-off, HPF enabled
P6		22 kΩ	Linear phase, slow roll-off, HPF enabled
P7		4.7 kΩ	Minimum phase, fast roll-off, HPF enabled
P8		0 Ω	Minimum phase, slow roll-off, HPF enabled
P9	No Connection	—	—

5 SPDIF Out

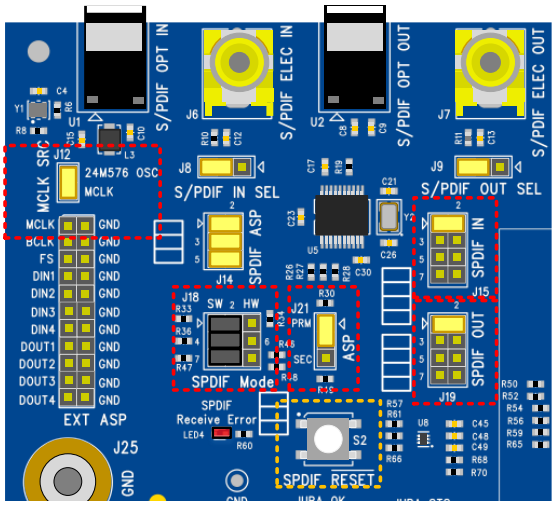
The DC5302P/4P/4S/8P/8S-ADC daughtercard supports S/PDIF output via optical and electrical connectors in software mode for sample rates up to 96 kHz (optical) or up to 192 kHz (electrical). The Dunglass system supports S/PDIF output at 48 kHz, 96 kHz, and 192 kHz sample rates.

5.1 WM8804 Software Mode

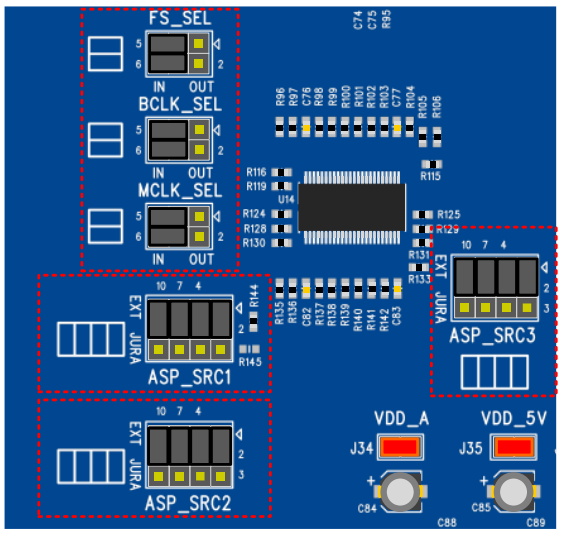
To configure the WM8804 S/PDIF transceiver in software mode the jumper links on the Dunglass system must be configured as in Table 9. Configuring the WM8804 S/PDIF transceiver in software mode allows the SPDIF sample rates of up to 192 kHz to be supported.

Table 9 WM8804 Software Mode Configuration

Populate J12 Link or apply a 22.5792MHz clock to MCLK



S/PDIF Transceiver Configuration



S/PDIF Digital Audio Signal Routing

The SPDIF Receive Error (LED4) is lit when there is no S/PDIF input source present.

If the S/PDIF transceiver is reconfigured while the Dunglass system is powered, the WM8804 needs to be reset for the changes to take effect. The WM8804 can be reset using the SPDIF RESET button.

Once the above jumper settings have been implemented, the following SCS scripts can be used to configure the WM8804 transceiver and the CS5302P/4P/4S/8P/8S ADC for audio streaming to S/PDIF output. The applicable script should be selected according to the sample rate of the SPDIF signal. See Section 2.2.5 for further information on running the SCS scripts.

- **CS5302P**
  - **SPDIF_CS5302P_MCLK_24M576_22M5792_48k_44k1_Primary_I2S.py**
  - **SPDIF_CS5302P_MCLK_24M576_22M5792_96k_88k2_Primary_I2S.py**
  - **SPDIF_CS5302P_MCLK_24M576_22M5792_192k_176k4_Primary_I2S.py**
- **CS5304P/4S**
  - **SPDIF_CS5304_MCLK_24M576_22M5792_48k_44k1_Primary_I2S.py**
  - **SPDIF_CS5304_MCLK_24M576_22M5792_96k_88k2_Primary_I2S.py**
  - **SPDIF_CS5304_MCLK_24M576_22M5792_192k_176k4_Primary_I2S.py**

- **CS5308P/8S**
  - **SPDIF_CS5308_MCLK_24M576_22M5792_48k_44k1_Primary_I2S.py**
  - **SPDIF_CS5308_MCLK_24M576_22M5792_96k_88k2_Primary_I2S.py**
  - **SPDIF_CS5308_MCLK_24M576_22M5792_192k_176k4_Primary_I2S.py**

5.2 Digital Audio Signal Routing to S/PDIF Transceiver

The signal source for the S/PDIF output transmitter is configured using the SPDIF OUT header; the source can be selected from any of the ASP_DOUTn pins from the ADC device.

Note the ASP_DOUTn pins support Channels 1–2, 3–4, 5–6, and 7–8 respectively.

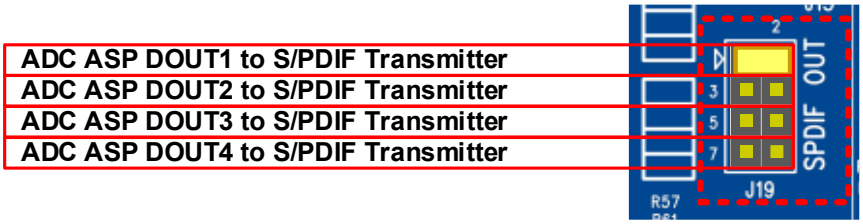


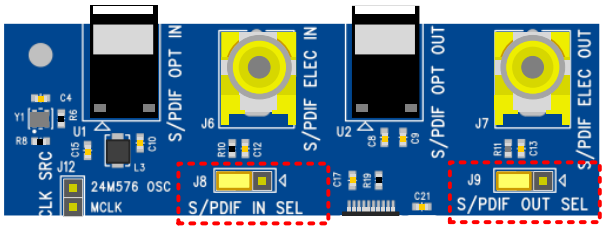
Figure 19: SPDIF OUT Jumper Link Configuration

5.3 Selecting Optical or Electrical S/PDIF

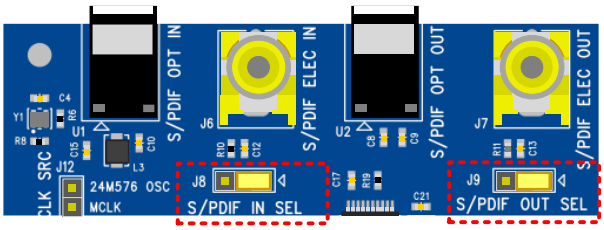
The S/PDIF IN SEL and S/PDIF OUT SEL headers are used to select the optical or electrical S/PDIF interfaces for the respective signal paths. The headers are configured as shown in Table 10.

The Dunglass system supports S/PDIF input/output at sample rates up to 96 kHz (optical) or up to 192 kHz (electrical).

Table 10 SPDIF I/O Configuration



Optical Input & Output



Electrical Input & Output

6 ADC Input Summing (CS5304P/4S/8P/8S)

The ADC signal paths can be combined in groups of two, four, or eight channels; this can be used to achieve enhanced dynamic-range performance on the respective paths.

The ADC input summing is configured using IN_SUM_MODE. Note that IN_SUM_MODE should not be changed while GLOBAL_EN is set. The GLOBAL_EN bit should always be cleared before writing to IN_SUM_MODE.

The supported summing options for CS5304P and CS5304S are described in Table 11.

Table 11 CS5304P/4S ADC Input Summing

Configuration	Description	Input Summing Configuration
Default	4-channel input	ADC1–ADC4 as individual outputs
ADCs combined in groups of two	2-channel input	ADC1+ADC2 ADC3+ADC4
ADCs combined in groups of four	1-channel input	ADC1+ADC2+ADC3+ADC4

The supported summing options for CS5308P and CS5308S are described in Table 12.

Table 12 CS5308P/8S ADC Input Summing

Configuration	Description	Input Summing Configuration
Default	8-channel input	ADC1–ADC4 as individual outputs
ADCs combined in groups of two	4-channel input	ADC1+ADC2 ADC3+ADC4
ADCs combined in groups of four	2-channel input	ADC1+ADC2+ADC3+ADC4
ADCs combined as a group of eight	1-channel input	ADC1+ADC2+ADC3+ADC4+ADC5+ADC6+ADC7+ADC8

If the ADC paths are combined, the respective analog input connections must be linked together to provide the same input to each of the respective ADC channels. Typical connections are shown in Section 6.2 and Section 6.3.

The combined ADC paths are configured using the control registers associated with the lowest-numbered ADC in the group. For example, the ADC3+ADC4 group is configured using the IN3/ADC3 control registers.

6.1 Input Buffer Circuit

The analog input channels are supported using external buffer circuits. The buffer circuit implemented on the DC5302P/4P/4S/8P/8S-ADC daughter card is shown in Figure 20, comprising a high-pass filter and anti-alias filter. The buffer circuit shown produces a full-scale (0 dBFS) output from a 8 V_{RMS} differential input.

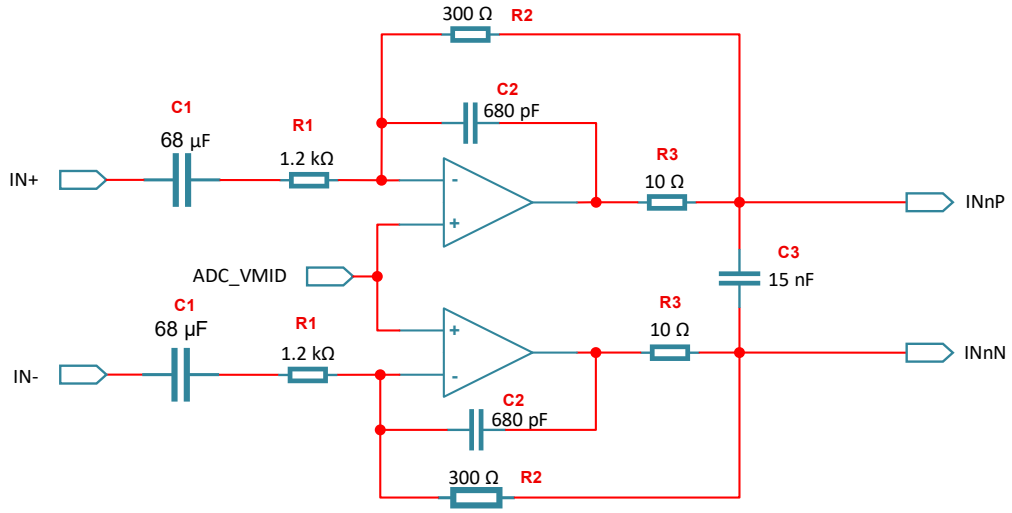


Figure 20: Differential Input Buffer

If ADC input summing is used, the input buffer should be modified with additional capacitors C4 as shown in Figure 21.

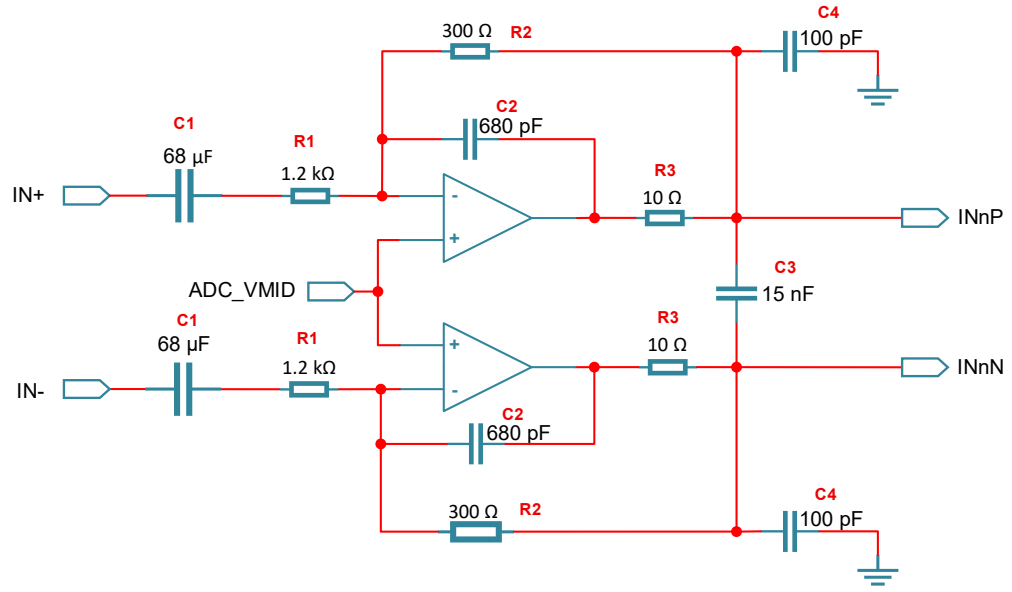


Figure 21: Differential Input Buffer for Input Summing

In the summing configuration, an additional 15 nF capacitor C5 should also be placed between each pair of INnP/N pins. These capacitors should be as close as possible to the input pins of the CS530x.

The summing configurations for CS5304P and CS5304S are shown in Section 6.2.

The summing configurations for CS5308P and CS5308S are shown in Section 6.3.

6.2 Configuring DC5304P/4S-ADC for Input Summing

6.2.1 Default Configuration: No Input Summing

Figure 22 shows the default external connections to the CS5304P/4S, with no input summing.

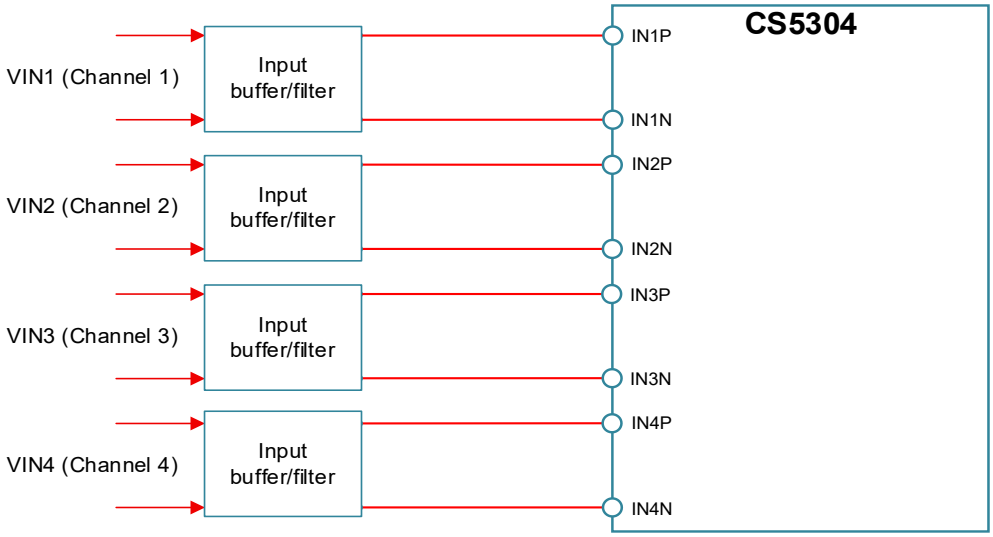


Figure 22: No Output Summing

In this default configuration, the input buffer circuit should be as shown in Figure 20.

The CDB-DC5304P/4S component population requirements are described in Table 13.

Table 13 Default Component Population (No Input Summing)

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Unpopulated 100 pF Capacitor C4	Unpopulated 15 nF Capacitor C5
R28, R6, R61, R38, R80, R89, R119, R126	R30, R63, R15, R53, R90, R133, R81, R120, R134, R121	C8, C14, C45, C48	C75, C76, C79, C80

6.2.2 ADC Input Summing: ADC inputs Combined in Groups of 2

Figure 23 shows the external connections to the CS5304P/4S when the inputs are summed in groups of 2.

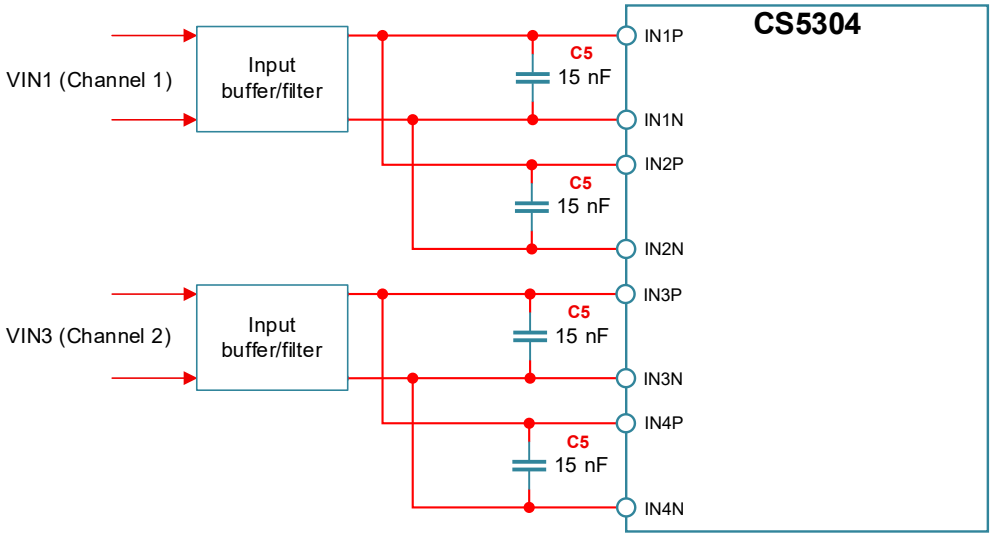


Figure 23: ADC Inputs Combined in Groups of 2

In this summing configuration, the input buffer circuit should be as shown in Figure 21.

The CDB-DC5304P/4S component population requirements are described in Table 14.

Table 14 Component Population for ADC Inputs Combined in Groups of 2

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Unpopulated 100 pF Capacitor C4	Unpopulated 15 nF Capacitor C5
R28, R6, R80, R89, R30, R63, R15, R53, R90, R133, R81, R120	R61, R38, R119, R126, R134, R121	C8, C14, C45, C48	C75, C76, C79, C80

6.2.3 ADC Input Summing: ADC inputs Combined in a Group of 4

Figure 24 shows the external connections to the CS5304P/4S when the inputs are summed in a group of 4.

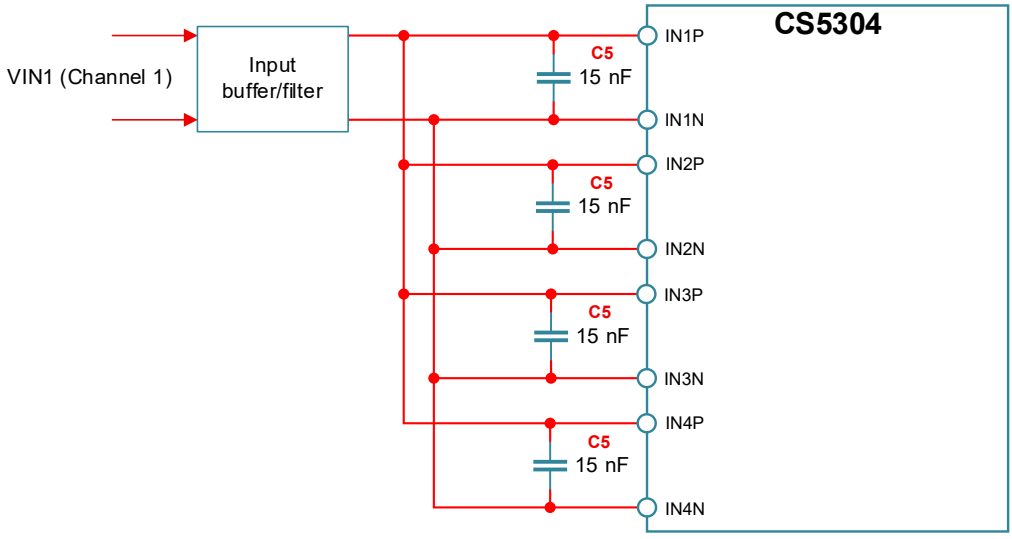


Figure 24: ADC Inputs Combined in a Group of 4

In this summing configuration, the input buffer circuit should be as shown in Figure 21.

The CDB-DC5304P/4S component population requirements are described in Table 15.

Table 15 Component Population for ADC Inputs Combined in a Group of 4

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Unpopulated 100 pF Capacitor C4	Unpopulated 15 nF Capacitor C5
R28, R6, R30, R63, R15, R53, R90, R133, R81, R120, R134, R121	R61, R38, R80, R89, R119, R126	C8, C14, C45, C48	C75, C76, C79, C80

6.3 Configuring DC5308P/8S-ADC for Input Summing

6.3.1 Default Configuration: No Input Summing

Figure 25 shows the default external connections to the CS5308P/8S, with no input summing.

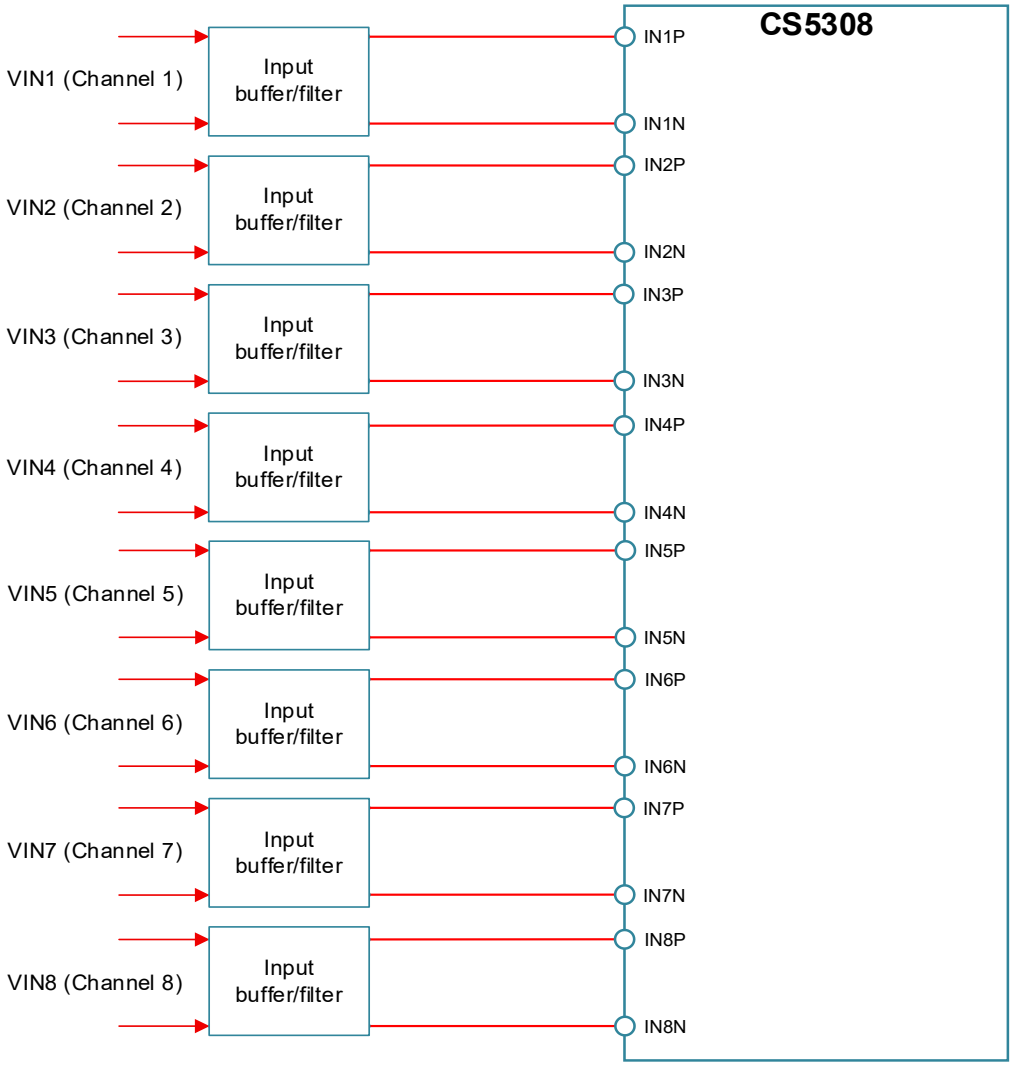


Figure 25: No Output Summing

In this default configuration, the input buffer circuit should be as shown in Figure 20.

The CDB-DC5308P/8S component population requirements are described in Table 16.

Table 16 Default Component Population (No Input Summing)

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Unpopulated 100 pF Capacitor C4	Unpopulated 15 nF Capacitor C5
R28, R6, R61, R38, R80, R89, R119, R126, R160, R161, R199, R208, R238, R246, R278, R286	R30, R63, R15, R53, R90, R133, R81, R120, R134, R169, R121, R163, R168, R209, R162, R200, R253, R287, R239, R279, R210, R201	C8, C14, C45, C48, C104, C115, C154, C159	C75, C76, C79, C80, C105, C106, C108, C109

6.3.2 ADC Input Summing: ADC inputs Combined in Groups of 2

Figure 26 shows the external connections to the CS5308P/8S when the inputs are summed in groups of 2.

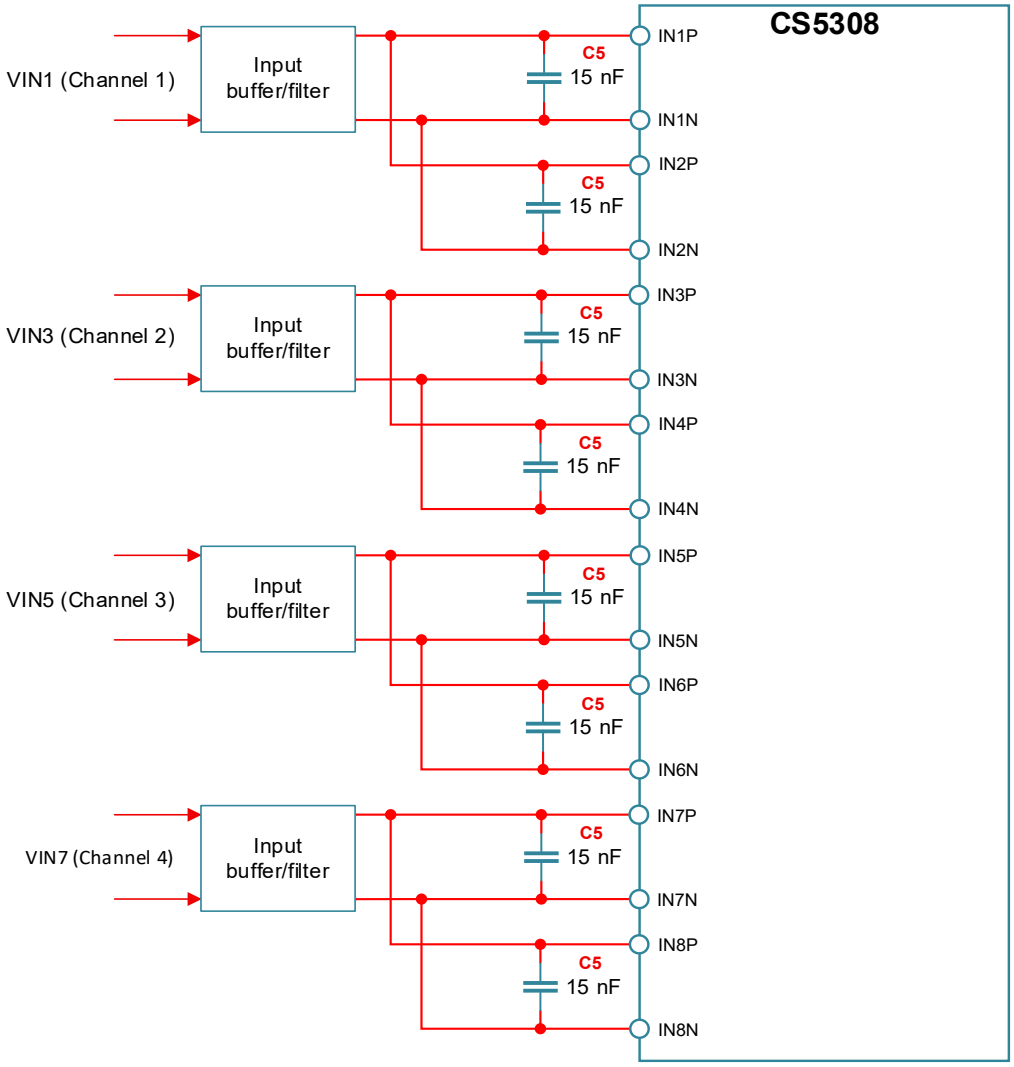


Figure 26: ADC Inputs Combined in Groups of 2

In this summing configuration, the input buffer circuit should be as shown in Figure 21.

The CDB-DC5308P/8S component population requirements are described in Table 17.

Table 17 Component Population for ADC Inputs Combined in Groups of 2

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Unpopulated 100 pF Capacitor C4	Unpopulated 15 nF Capacitor C5
R28, R6, R80, R89, R30, R63, R15, R53, R90, R133, R81, R120, R160, R161, R168, R209, R162, R200, R238, R246, R253, R287, R239, R279	R61, R38, R119, R126 R199, R208, R278, R286, R134, R169, R121, R163, R210, R201	C8, C14, C45, C48, C104, C115, C154, C159	C75, C76, C79, C80, C105, C106, C108, C109

6.3.3 ADC Input Summing: ADC inputs Combined in Groups of 4

Figure 27 shows the external connections to the CS5308P/8S when the inputs are summed in groups of 4.

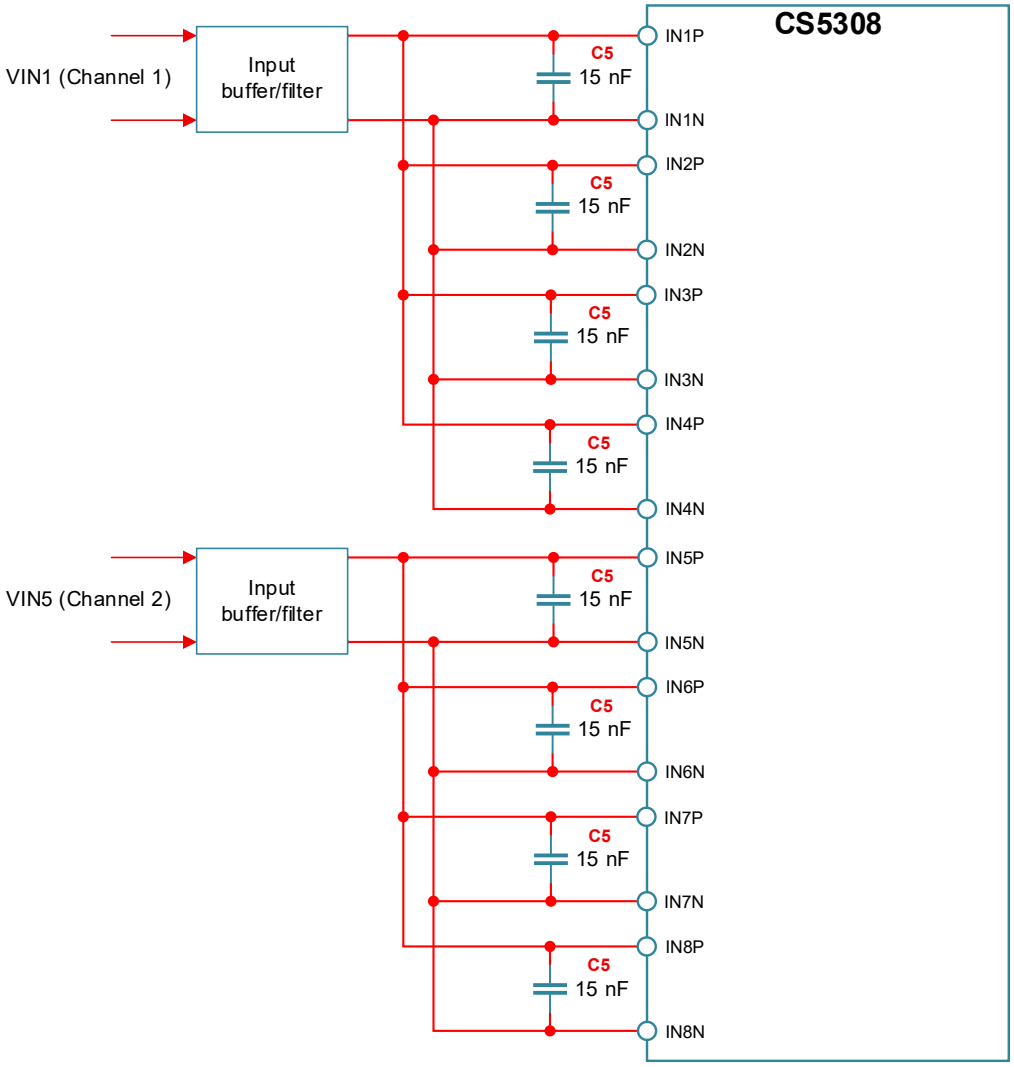


Figure 27: ADC Inputs Combined in Groups of 4

In this summing configuration, the input buffer circuit should be as shown in Figure 21.

The CDB-DC5308P/8S component population requirements are described in Table 18.

Table 18 Component Population for ADC Inputs Combined in Groups of 4

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Unpopulated 100 pF Capacitor C4	Unpopulated 15 nF Capacitor C5
R28, R6, R30, R63, R15, R53, R90, R133, R81, R120, R160, R161, R168, R209, R162, R200, R253, R287, R239, R279, R134, R210, R121, R201	R61, R38, R80, R89, R119, R126, R199, R208, R238, R246, R278, R286, R169, R163	C8, C14, C45, C48, C104, C115, C154, C159	C75, C76, C79, C80, C105, C106, C108, C109

6.3.4 ADC Input Summing: ADC inputs Combined in a Group of 8

Figure 28 shows the external connections to the CS5308P/8S when the inputs are summed in a group of 8.

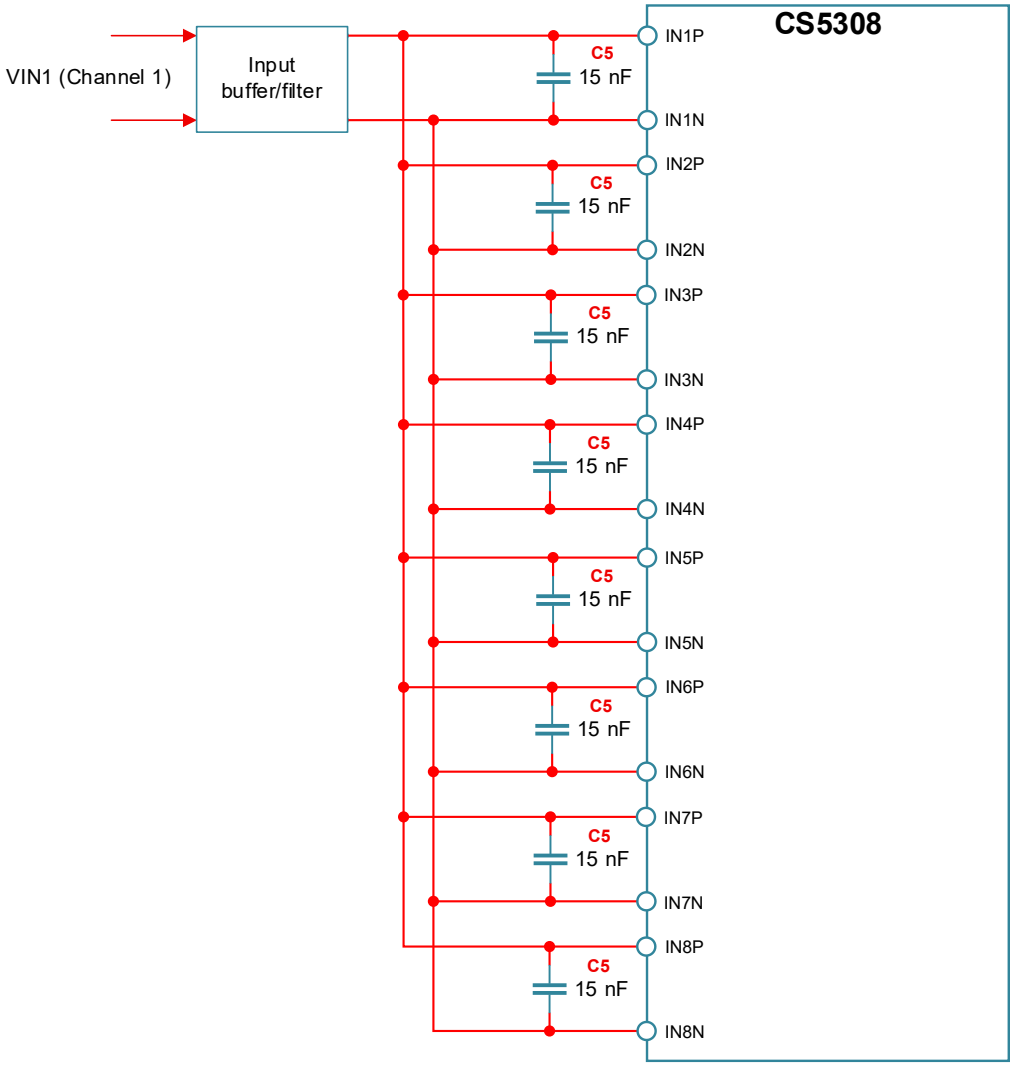


Figure 28: ADC Inputs Combined in a Group of 8

In this summing configuration, the input buffer circuit should be as shown in Figure 21.

The CDB-DC5308P/8S component population requirements are described in Table 19.

Table 19 Component Population for ADC Inputs Combined in a Group of 8

Populated 0 Ω Resistor	Unpopulated 0 Ω Resistor	Unpopulated 100 pF Capacitor C4	Unpopulated 15 nF Capacitor C5
R28, R6, R30, R63, R15, R53, R90, R133, R81, R120, R134, R169, R121, R163, R168, R209, R162, R200, R253, R287, R239, R279, R210, R201	R61, R38, R80, R89, R119, R126, R160, R161, R199, R208, R238, R246, R278, R266	C8, C14, C45, C48, C104, C115, C154, C159	C75, C76, C79, C80, C105, C106, C108, C109

7 Performance Plots

7.1 DC5302P-ADC Performance Plots

ADC Filter Slow Roll-off, Minimum Phase, 48kHz Sample Rate

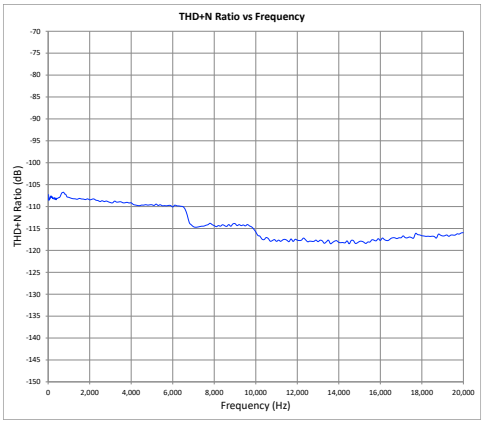


Figure 29: -1dBFS THD+N ratio Vs Frequency

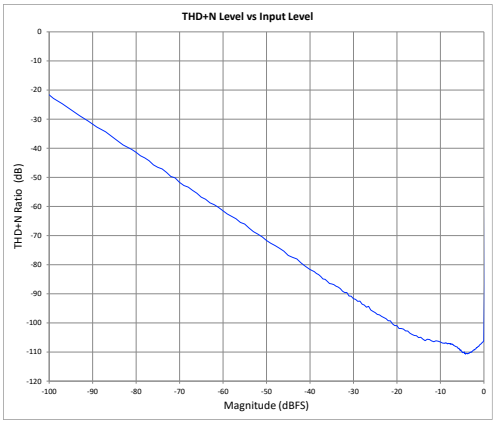


Figure 30: THD+N ratio Vs Magnitude

ADC Filter Slow Roll-off, Minimum Phase, 96kHz Sample Rate

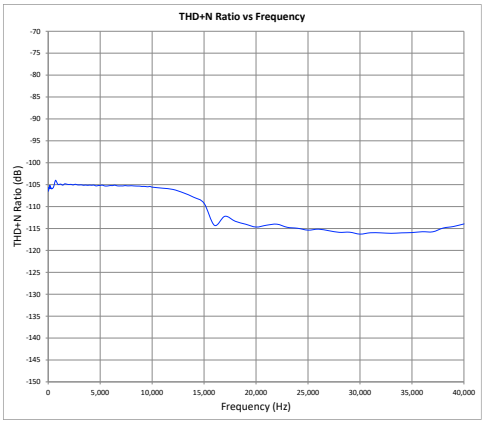


Figure 31: -1dBFS THD+N ratio Vs Frequency

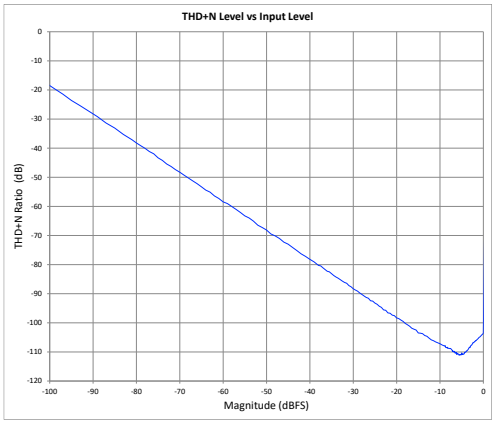


Figure 32: THD+N ratio Vs Magnitude

ADC Filter Slow Roll-off, Minimum Phase, 192kHz Sample Rate

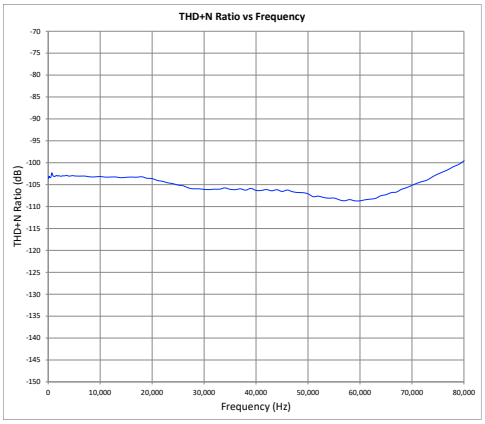


Figure 33: -1dBFS THD+N ratio Vs Frequency

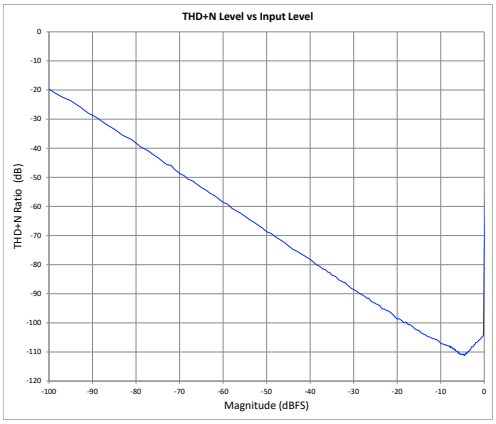


Figure 34: THD+N ratio Vs Magnitude

7.2 DC5304P/8P-ADC Performance Plots

ADC Filter Slow Roll-off, Minimum Phase, 48kHz Sample Rate

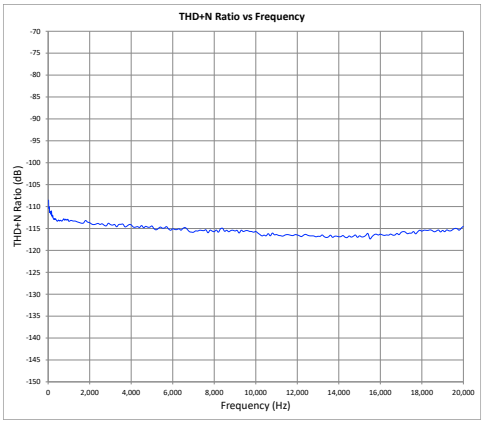


Figure 35: -1dBFS THD+N ratio Vs Frequency

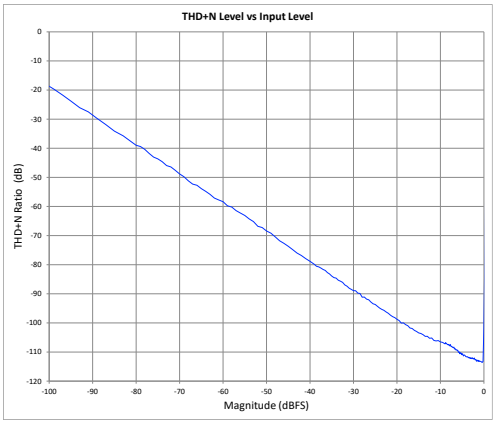


Figure 36: THD+N ratio Vs Magnitude

ADC Filter Slow Roll-off, Minimum Phase, 96kHz Sample Rate

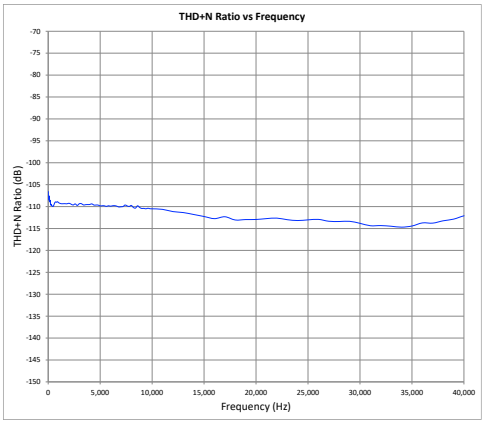


Figure 37: -1dBFS THD+N ratio Vs Frequency

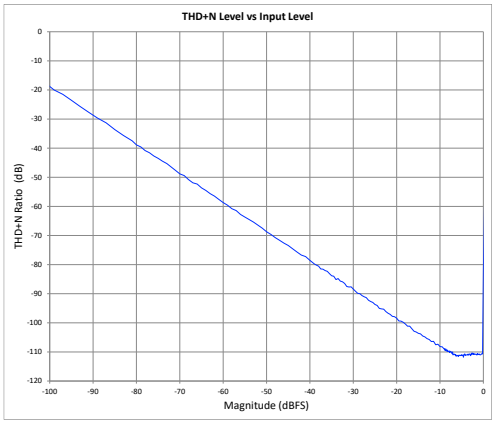


Figure 38: THD+N ratio Vs Magnitude

ADC Filter Slow Roll-off, Minimum Phase, 192kHz Sample Rate

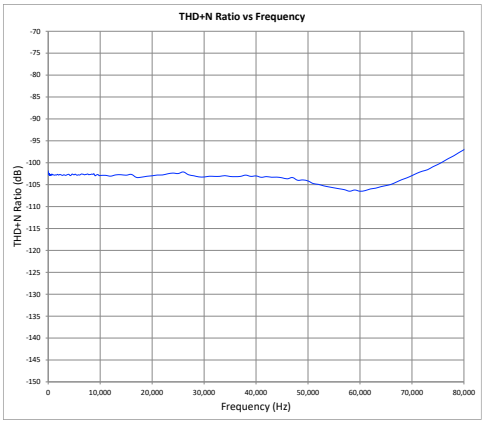


Figure 39: -1dBFS THD+N ratio Vs Frequency

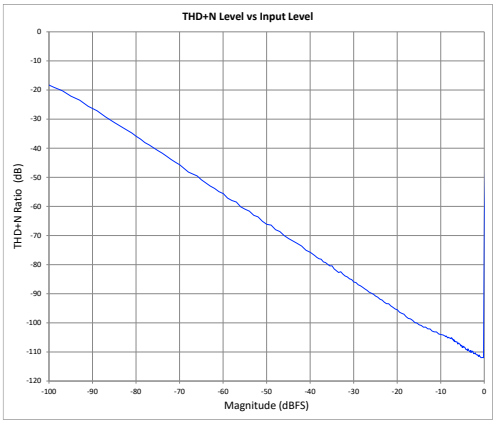


Figure 40:THD+N ratio Vs Magnitude

7.3 DC5304S/8S-ADC Performance Plots

ADC Filter Slow Roll-off, Minimum Phase, 48kHz Sample Rate

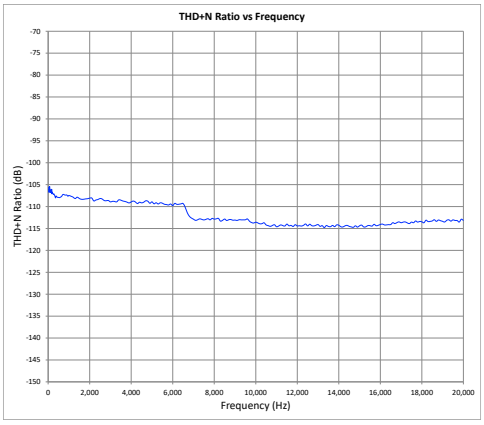


Figure 41: -1dBFS THD+N ratio Vs Frequency

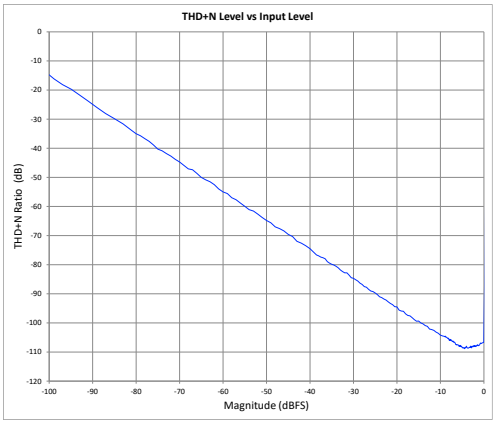


Figure 42: THD+N ratio Vs Magnitude

ADC Filter Slow Roll-off, Minimum Phase, 96kHz Sample Rate

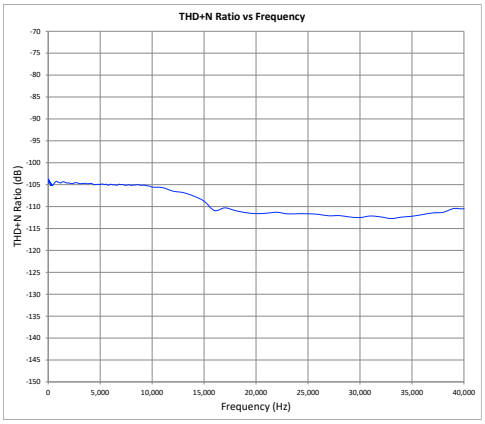


Figure 43: -1dBFS THD+N ratio Vs Frequency

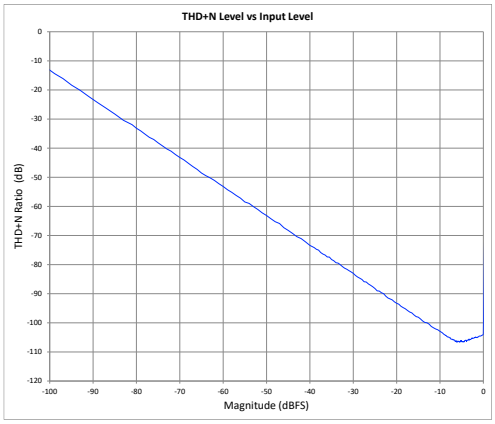


Figure 44: THD+N ratio Vs Magnitude

ADC Filter Slow Roll-off, Minimum Phase, 192kHz Sample Rate

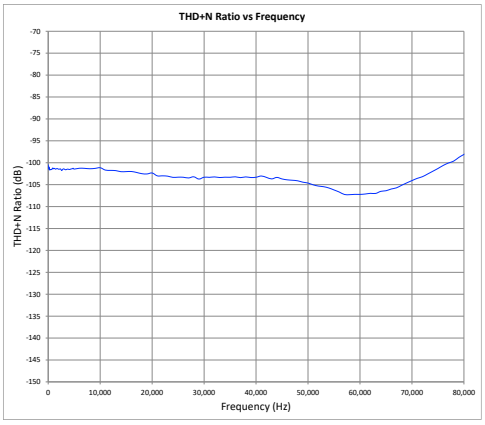


Figure 45: -1dBFS THD+N ratio Vs Frequency

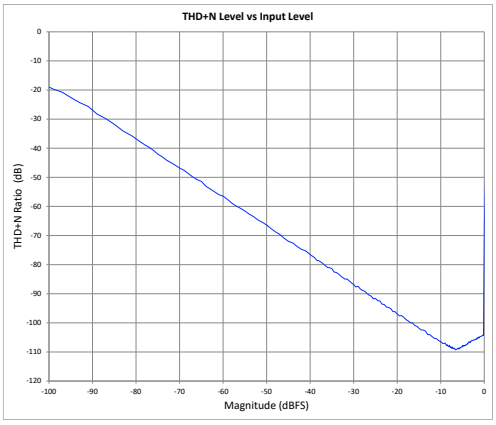


Figure 46:THD+N ratio Vs Magnitude

8 Notices

Jura firmware development utilizes components under the following licenses:

1. XMOS PUBLIC LICENCE: Version 1, available at www.xmos.ai/license-agreements/
2. The MIT License, available at www.github.com/microsoft/uf2/blob/master/LICENSE.txt. Copyright © Microsoft Corporation

Unmodified USB Audio 2.0 Device Software source code is available from www.xmos.ai under XMOS PUBLIC LICENCE: Version 1.

9 Revision History

Revision History

Revision	Changes
R1 JUNE 2023	• Initial version.
R2 OCT 2023	• Updated description for executing SCS scripts
R3 JUL 2025	• Updated to include CS5302P, CS5304P, CS5304S & CS5308S boards • How to configure ADC input summing mode added • Performance plots for CS5302P, CS5304P/8P & CS5304S/8S added

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.