

DC5312BSE-ADC User Guide

Introduction

The DC5312BSE-ADC is a daughter card used with the Cirrus Logic Duglass (CDB-PROAUDIO) system to evaluate high performance ADC, DAC, and codec devices. This document details how to connect the DC5312BSE-ADC to the Duglass (CDB-PROAUDIO) system and how to get started.

The DC5312BSE-ADC, with the default jumper positions, is shown in Figure 1.

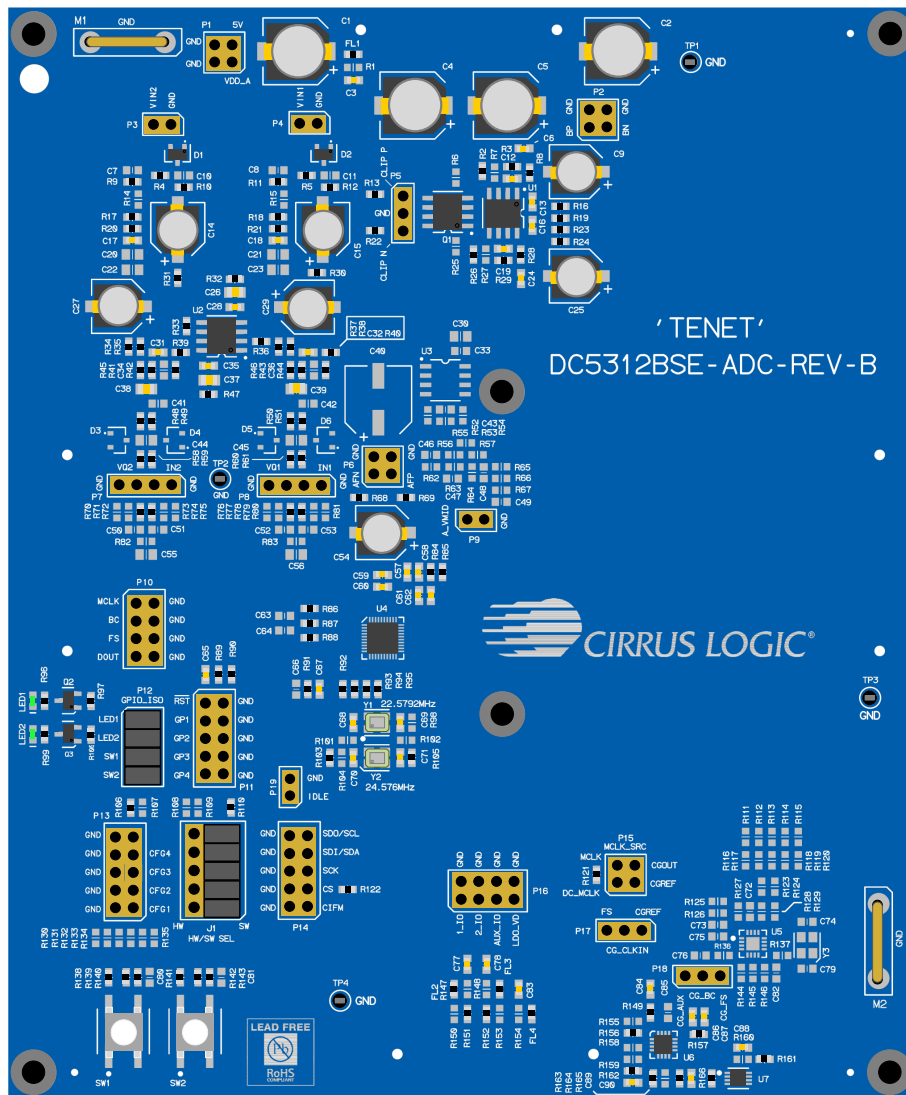


Figure 1: DC5312BSE-ADC Daughter Card

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1 Hardware Connections

The Dunglass system supports interchangeable daughter cards for a variety of ADC, DAC, and codec devices.

Caution:

Daughter cards should not be inserted or removed while the Dunglass system is powered. Fully disconnect or power down external power supply before changing daughter cards.

For more information on the Dunglass (CDB-PROAUDIO) system refer to the CDB-PROAUDIO User Guide^[1].

1.1 How to Connect DC5312BSE-ADC onto the Dunglass System

The DC5312BSE-ADC is a 4-header daughter card that connects to the Dunglass system using headers DCJ1, DCJ2, DCJ3, and DCJ4. A JURA module (described in Section 1.2.1) is also required to be plugged into the Dunglass system. To ensure correct connection, the headers are keyed and alignment dots are visible on each board, as shown in Figure 2.

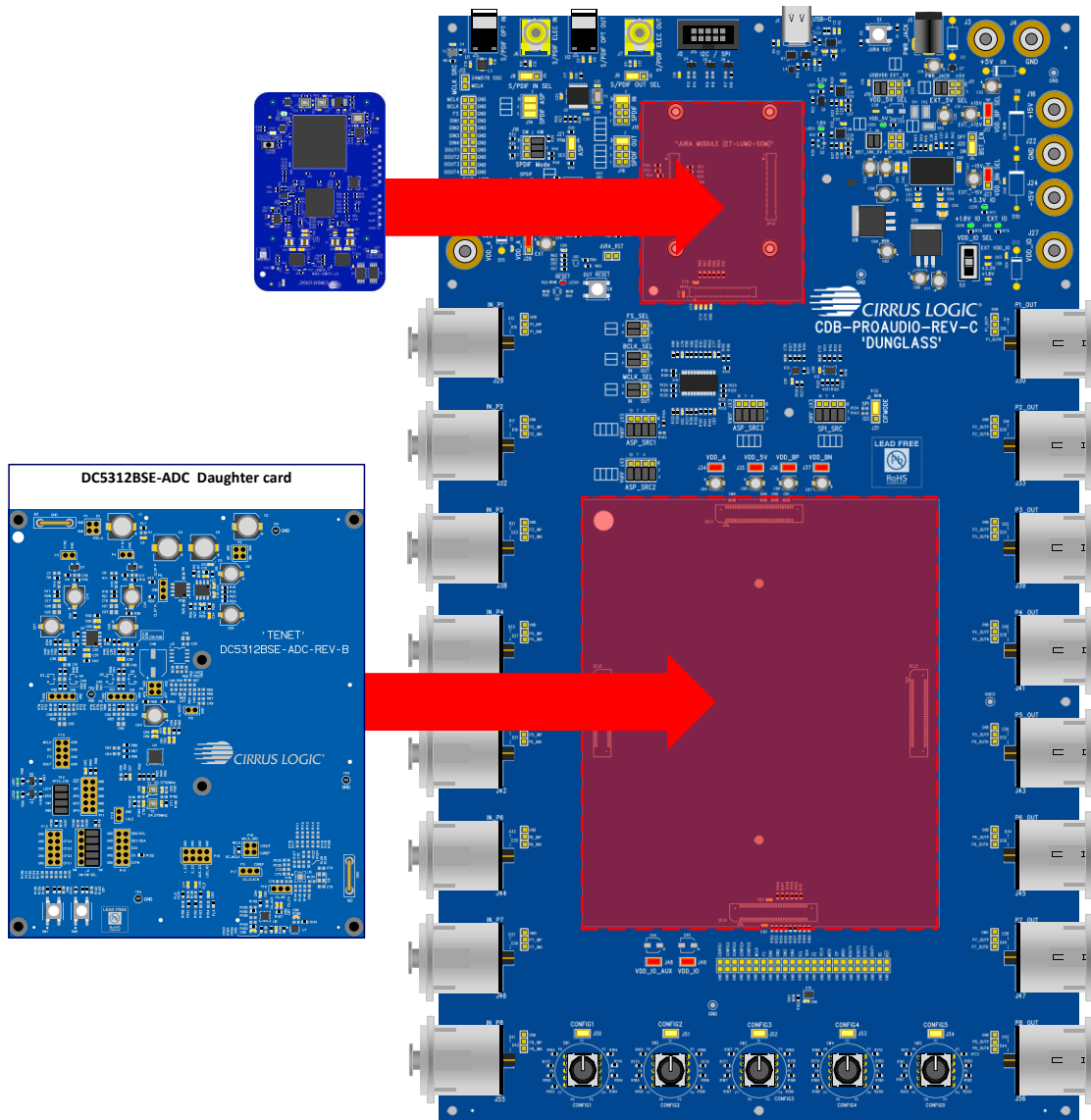


Figure 2: DC5312BSE-ADC Daughter Card and JURA Module Connection to the Dunglass System

1.2 USB and Power Connection

Dunglass is powered using a 5 V external power supply and is controlled via a single USB connection. The JURA module supports the following functions via the USB connection:

- I²C/SPI communications to control device and board
- Multichannel USB streaming audio (USB Class 2)

The Dunglass board is provided with a USB-A to USB-C cable and a 5 V wall supply; connection is illustrated in Figure 3.

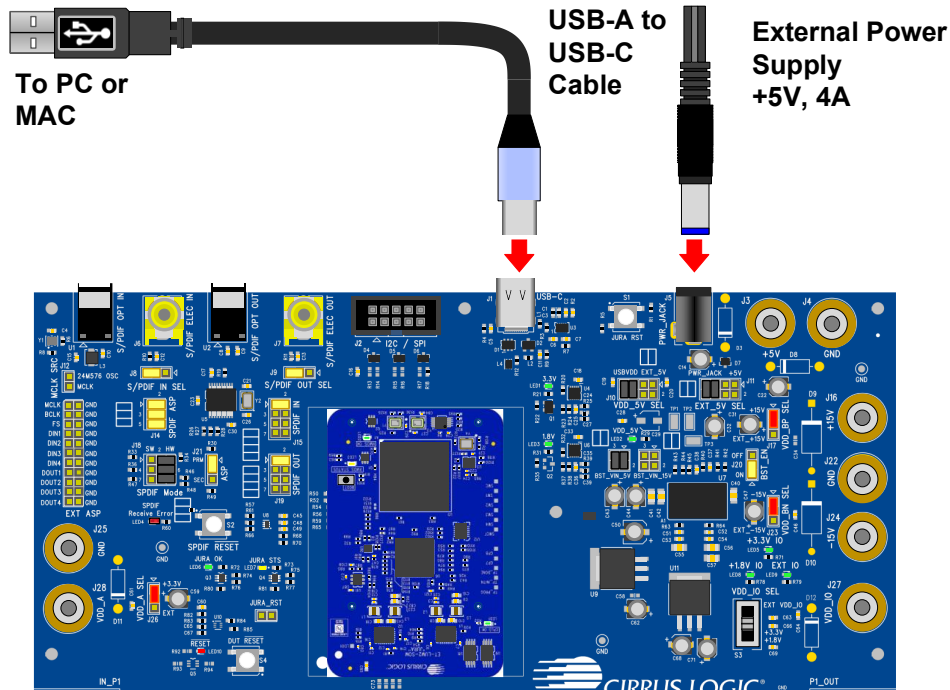


Figure 3: Dunglass (CDB-PROAUDIO) USB and Power Connection

A Total Phase Aardvark connector can be used for I²C/SPI communication. Refer to the CDB-PROAUDIO User Guide^[1] for more details.

1.2.1 JURA Module

The JURA module supports I²C/SPI communication to control the Dunglass system and daughter card; it also enables multichannel USB streaming audio (USB audio Class 2).

The JURA module is connected to the Dunglass board as shown in Figure 4:

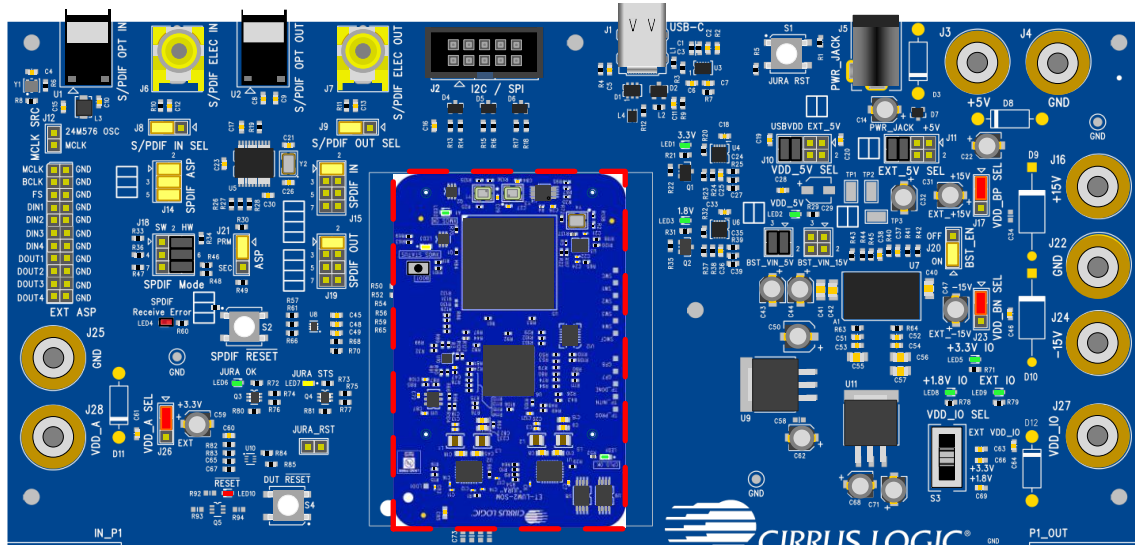


Figure 4: JURA Module Connection to Dunglass System

1.2.2 Dunglass Boot Procedure with JURA Module

The USB-C cable must be connected between the Dunglass system and the PC or Mac[®] prior to powering up the board.

The boot time of the Dunglass system varies depending on the version of firmware on the JURA module but is typically in the range of 2 s to 5 s after applying power to the board.

1.3 Routing the Digital Audio PCM Signals

The digital audio PCM paths to the daughter card can be routed from the JURA module, or else from the EXT ASP header located on the Dunglass system. The routing is configured using the ASP_SRC1, ASP_SRC2, and ASP_SRC3 headers as follows:

- JURA = Digital audio signals routed from JURA module
- EXT = Digital audio signals routed from EXT ASP header

The ASP_SRC1, ASP_SRC2, and ASP_SRC3 headers are configured for JURA Primary Mode, EXT ASP Primary Mode and EXT ASP Secondary Mode as shown in Figure 5, Figure 6, and Figure 7 respectively.

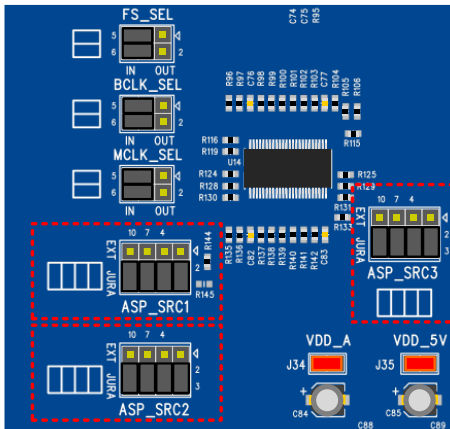


Figure 5: JURA Module Primary Mode

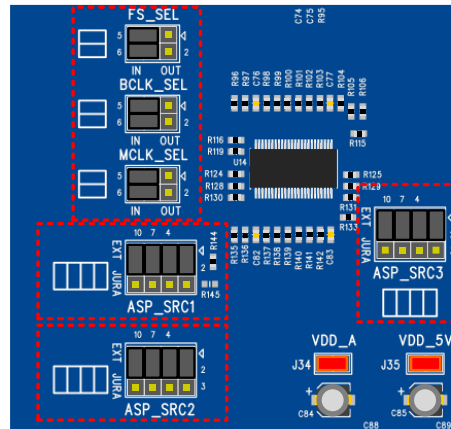


Figure 6: EXT ASP Primary Mode

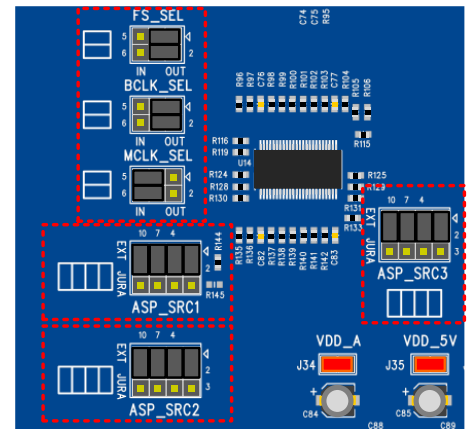


Figure 7: EXT ASP Secondary Mode

The JURA module always operates in Primary Mode – the MCLK, BCLK, and FSYNCK clock signals are generated by the JURA module as inputs to the daughter card.

If the digital audio is routed from the EXT ASP header, the direction of the MCLK, BCLK, and FSYNCK clock signals are configured using the MCLK_SEL, BCLK_SEL, and FS_SEL headers respectively. Each signal is configured independently, as follows:

- IN = EXT ASP header supports the signal as input to the daughter card
- OUT = EXT ASP header supports the signal as output from the daughter card

Note that the EXT ASP header uses 3.3 V logic levels; a level shifter is incorporated to interface with the VDD_IO domain on the DC5312BSE-ADC daughter card.

1.4 Selection of Hardware or Software Control Mode

The CS5312BSE supports hardware and software control modes. The hardware and software modes are set via the HW/SW SEL header on the DC5312BSE-ADC and the rotary switches on the Dunglass system. The Software Mode and Hardware Mode jumper link configurations are shown in Figure 8 and Figure 9.

- SW = Software Mode
- HW = Hardware Mode.

In Hardware Mode, rotary switches are used to select the desired configuration. See Section 4 for information on Hardware Mode.

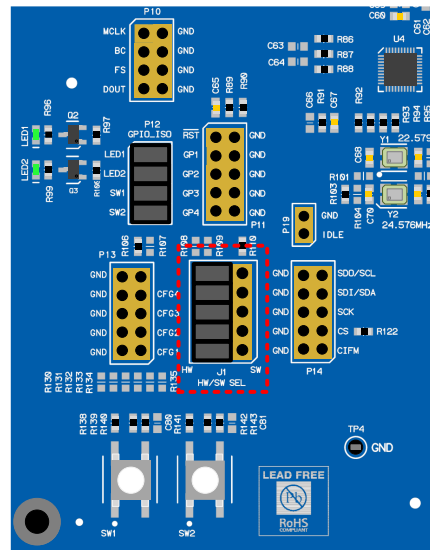
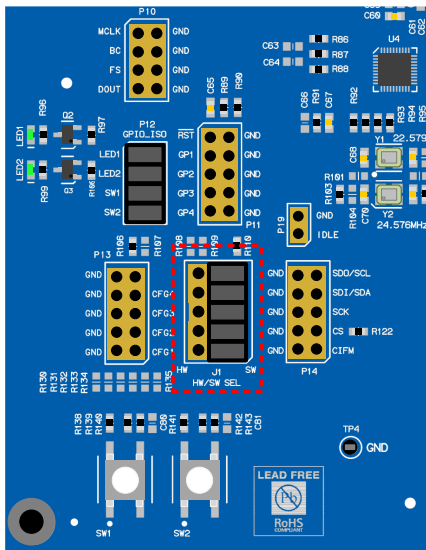


Figure 8: Software Mode Jumper Link Configuration

Figure 9: Hardware Mode Jumper Link Configuration

Note that Hardware Mode is only supported for VDD_IO = 3.3 V on the DC5312BSE-ADC due to the 3.3 V rotary switch pull-up supply on the Dunglass system.

1.5 DC5312BSE-ADC System Clocking Source Selection

Clocking for the CS5312BSE is provided using either the MCLK input or the crystal (XTAL) oscillator. The MCLK input is selected by default on the DC5312BSE-ADC. The XTAL oscillator uses one of two external crystals, Y1 or Y2, provided on the DC5312BSE-ADC to generate the system clock. Y1 provides a 22.5792 MHz signal and Y2 provides a 24.576 MHz signal. The oscillators are enabled by configuring resistors on the DC5312BSE-ADC board as follows:

- Y1 (22.5792 MHz). Enabled by removing R138 and R140, and populating R132 and R136.
- Y2 (24.576 MHz). Enabled by removing R138 and R140, and populating R137 and R139.

The clocking source is configured as shown in Figure 10, Figure 11 and Figure 12.

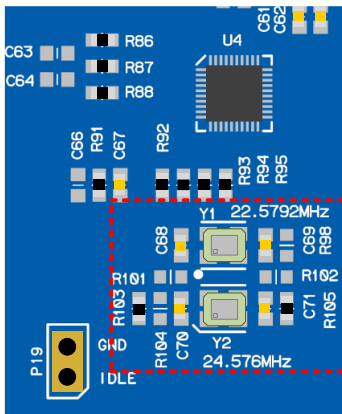


Figure 10: Dunglass System MCLK as clocking source (Default)

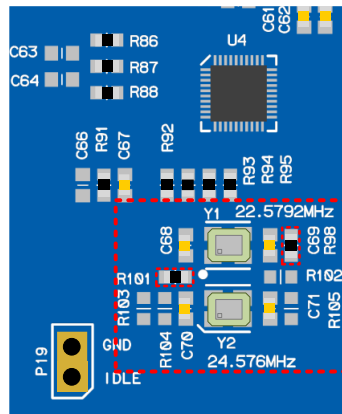


Figure 11: Crystal (XTAL) oscillator Y1 as clocking source

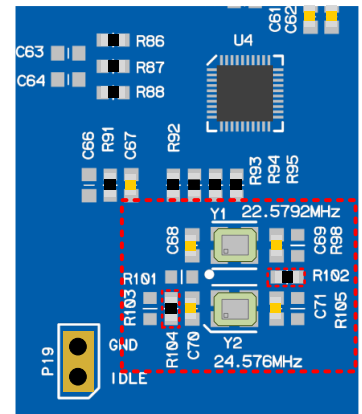


Figure 12: Crystal (XTAL) oscillator Y2 as clocking source

In Hardware Mode, the clocking source is configured using the CONFIG4 pin, as detailed in the CS5312BSE datasheet^[2]. In Software Mode, the clocking source is selected using the register field SYSCLK_SRC.

If clocking is provided using the crystal oscillator, the CS5312BSE outputs a clock on the MCLK pin. The frequency of the MCLK output clock matches the crystal oscillator frequency. The output clock can be used to drive other devices.

2 Driver Installation and SoundClear Studio Support

2.1 SoundClear Studio

SoundClear® Studio (SCS) is a PC/Mac®-based tool used to configure Cirrus Logic devices. The tools suite provides support for evaluation and development and can be used with Duglass system and associated daughter cards.

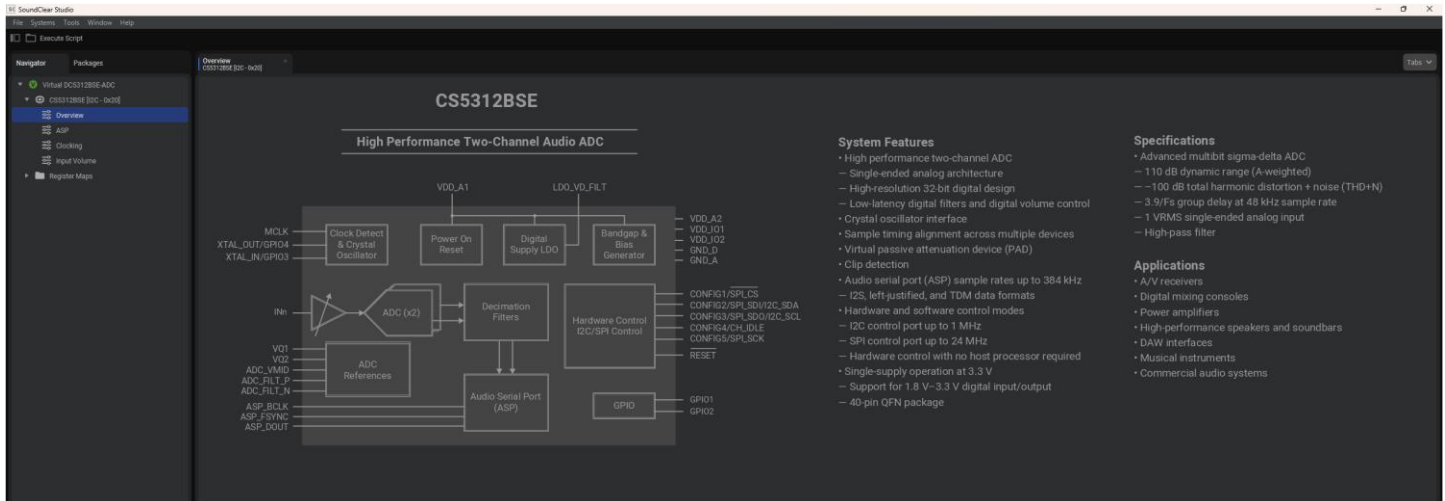


Figure 13: SoundClear Studio

2.1.1 Download SoundClear Studio Software and Drivers

SoundClear Studio and associated software collateral required for the Duglass system can be downloaded from <https://cirrus.com>.

The required components are as follows:

- **SoundClear Studio 2.1.** Run the appropriate installer on your Windows® or macOS computer to install SoundClear Studio.
- **CS5312BSE SCS Package.** Install this in SoundClear Studio to incorporate the CS5312BSE-specific software components in SoundClear Studio. See Section 2.2.1 for details on how to install an SCS package.
- **JURA Windows Setup.** On Windows computers, run the Cirrus Logic USB Audio Setup to install the driver that enables SoundClear Studio to communicate with the JURA board.

2.2 SoundClear Studio Quick Start Guide

2.2.1 Installing Packages

Each daughter card has its own individual SoundClear Studio package that must be installed separately from the main SoundClear Studio Software. These are installed from the main menu using **"File → Install Package..."**. Multiple packages can be installed together by selecting more than one using the file dialog.

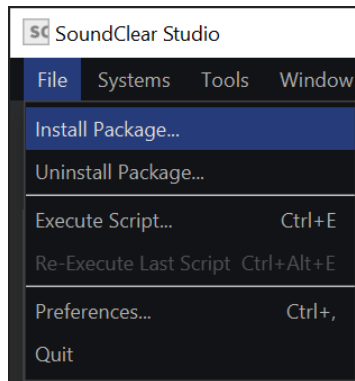


Figure 14: SoundClear Studio – Installing Board Packages

2.2.2 SoundClear Studio User Guide

The SoundClear Studio User Guide can be accessed from the main menu using **"Help → Open Help Contents..."**

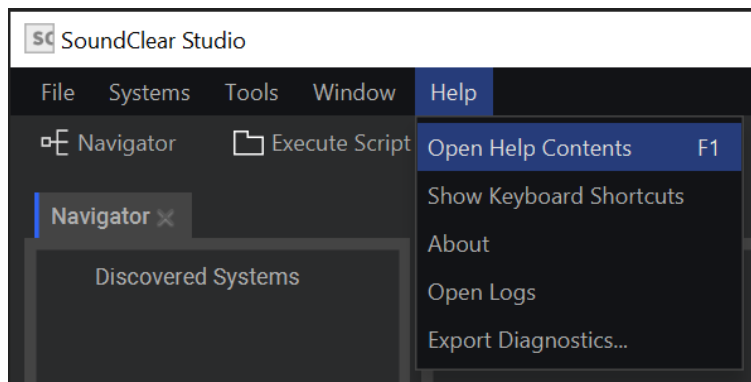


Figure 15: SoundClear Studio – User Guide

2.2.3 Creating a Virtual System

A virtual (non-hardware) version of the system can be created using “**Systems** → **Add Virtual System...**”

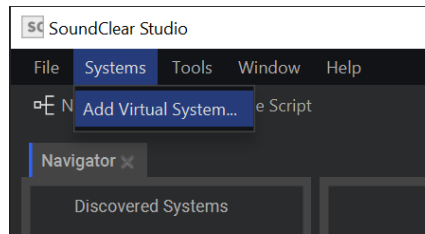


Figure 16: SoundClear Studio – Creating a Virtual System

This opens a dialog box to select an installed system (shown here is the DC5312BSE-ADC):

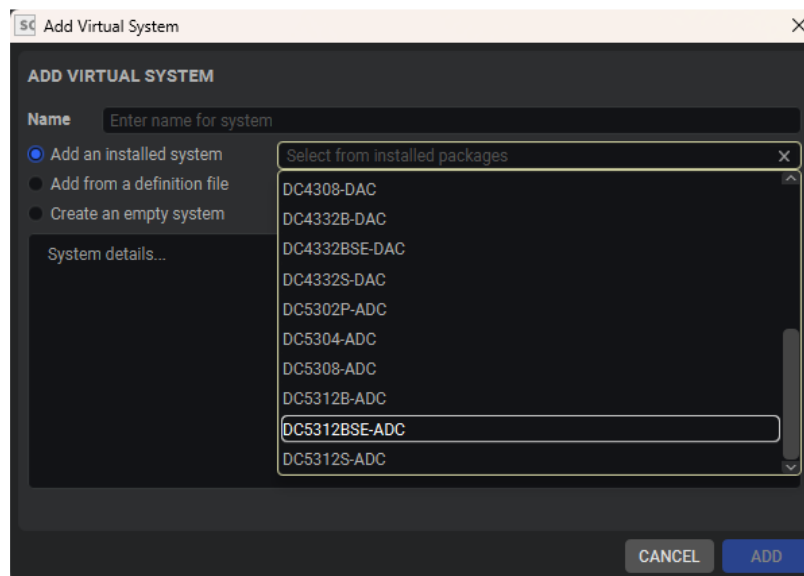


Figure 17: SoundClear Studio – Adding a Virtual System

Once created, a virtual system enables the user to interact with virtual versions of the device register map and helper panels.

2.2.4 Adding an Existing System

SoundClear Studio automatically detects board hardware such as the Jura module and Cirrus Logic devices. In the event of devices not being detected automatically, a device can be added manually. Right click on the system and select “Add Device...”

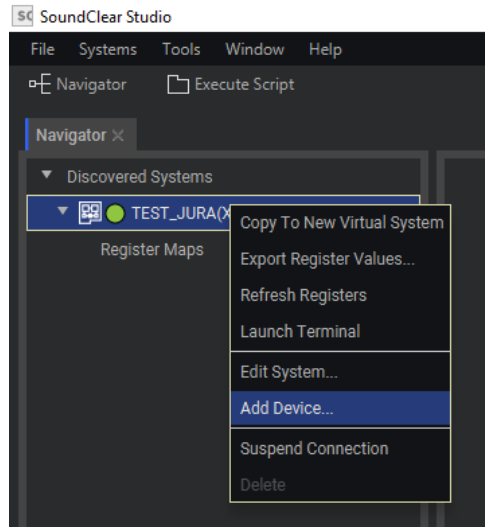


Figure 18: SoundClear Studio – Adding an Existing Device

Then select the device from those installed, along with the protocol and address of the part (this can be edited again by right clicking on the device and selected “Edit Device...”):

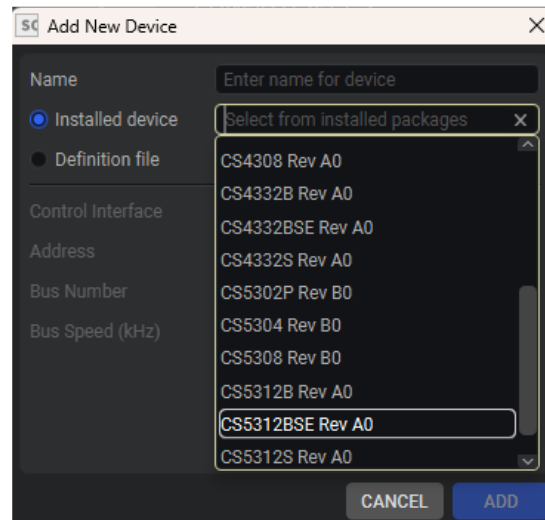


Figure 19: SoundClear Studio – Adding an Existing Device

2.2.5 Executing SoundClear Studio Scripts

SoundClear Studio provides the ability to interact with the device register map using Python® scripts. These scripts can sequence register operations to configure the desired states, which can then be executed from SoundClear Studio using “File→Execute Script...”

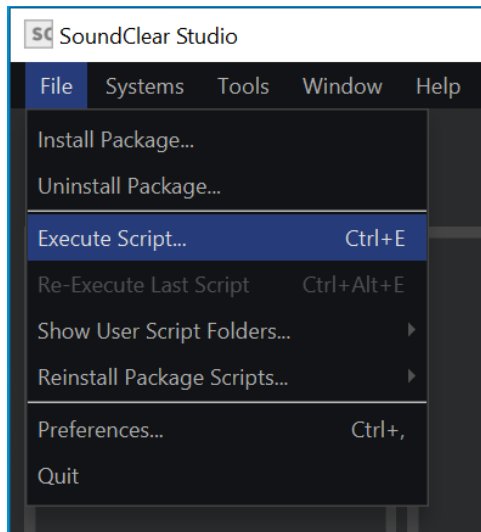


Figure 20: SoundClear Studio – Executing Script

The CS5312BSE SoundClear Studio package installs a set of scripts to configure the device for common use cases. These are available at <User Documents>\Cirrus Logic\SCS\Scripts\<Package Name>.

The scripts can be accessed via “File→Show User Script Folder→CS5312 Scripts”

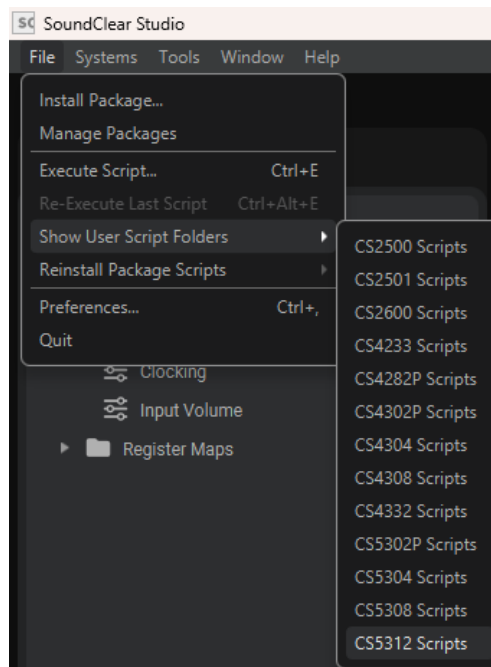


Figure 21: SoundClear Studio – Show User Script Folder

3 DC5312BSE-ADC Software Mode Quick Start

The following steps describe how to start the DC5312BSE-ADC in Software Mode after installing the SoundClear Studio software and the CS5312BSE SCS package:

1. Connect the hardware as shown in Figure 2.
2. Connect the USB cable to the PC.
3. Power up the system and ensure the JURA OK, 1.8 V, 3.3 V, and VDD_5V LEDs are illuminated.
4. Configure signal routing as shown in Section 1.3.
5. Start SoundClear Studio.
SoundClear Studio should auto-detect the DC5312BSE-ADC daughter card. If not, follow the procedure specified in Section 2.2.4.
6. Run the required script from the following location: <User Documents>\Cirrus Logic\SCS\Scripts\<Package Name>.

4 Hardware Control Mode

The Duglass system supports Hardware Mode for Cirrus Logic high performance ADC, DAC, and codec devices. These are supported via the rotary switches on the Duglass system, as illustrated in Figure 22.



Figure 22: Duglass Rotary Switches for Hardware Control Mode

Each switch has silkscreen on the board to indicate the position of the switch. Each switch position enables a pull resistor on the respective CONFIG pin to VDD_A or ground, as shown in Figure 23.

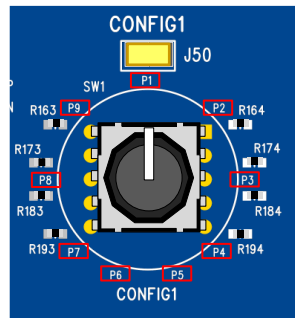


Figure 23: Rotary Switch

If the rotary switches are reconfigured while the Duglass system is powered, changes will not take effect until the DC5312BSE-ADC is reset by pushing the DUT RESET button.

Note that Hardware Mode is only supported for VDD_IO = 3.3 V on the DC5312BSE-ADC due to the 3.3 V rotary switch pull-up supply on the Duglass system.

4.1 Hardware Mode Rotary Switch Settings

The CS5312BSE supports Hardware Mode. The rotary switch functions are described in Table 1 to Table 4. Refer to the CS5312BSE datasheet^[2] for further details of the Hardware Mode options.

The CONFIG1 pin selects the ASP operating configuration:

Table 1: CONFIG1 Hardware Control – ASP Configuration

Switch Position	Pin Configuration		Description
P1	Pull-up to 3.3 V	0 Ω	Software Control Mode (I ² C/SPI)
P2		4.7 kΩ	In I ² C Mode, the pull-up resistor is used to select the device address—see CS5312BSE datasheet.
P3		22 kΩ	In SPI Mode, it is recommended to use the 100 kΩ pull-up position (P4).
P4		100 kΩ	
P5	Pull-Down to GND	100 kΩ	ASP Primary Mode, 176.4 kHz, 192 kHz sample rate
P6		22 kΩ	ASP Primary Mode, 88.2 kHz, 96 kHz sample rate
P7		4.7 kΩ	ASP Primary Mode, 44.1 kHz, 48 kHz sample rate
P8		0 Ω	ASP Secondary Mode, autodetect sample rate ¹
P9	No Connection	—	—

- Autodetect sample rate is only supported in MCLK 256 fs(base), MCLK 512 fs(base) or MCLK 1024 fs(base) clocking configurations.

The CONFIG2 pin selects the ASP format and TDM timeslots option:

Table 2: CONFIG2 Hardware Control – ASP Configuration

Switch Position	Pin Configuration		Description
P1	Pull-up to 3.3 V	0 Ω	ASP TDM Mode—minimum time slots, ASP_FSYNC_TYPE = pulse
P2		4.7 kΩ	ASP TDM Mode—maximum time slots, data output on BCLK falling edge (half-cycle mode), ASP_FSYNC_TYPE = pulse
P3		22 kΩ	ASP TDM Mode—maximum time slots, data output on BCLK rising edge (full-cycle mode), ASP_FSYNC_TYPE = pulse
P4		100 kΩ	ASP TDM Mode—minimum time slots, ASP_FSYNC_TYPE = square wave (50% duty cycle)
P5	Pull-Down to GND	100 kΩ	ASP TDM Mode—maximum time slots, data output on BCLK falling edge (half-cycle mode), ASP_FSYNC_TYPE = square wave (50% duty cycle)
P6		22 kΩ	ASP TDM Mode—maximum time slots, data output on BCLK rising edge (full-cycle mode), ASP_FSYNC_TYPE = square wave (50% duty cycle)
P7		4.7 kΩ	ASP Left-Justified Mode
P8		0 Ω	ASP I ² S Mode
P9	No Connection	—	—

The CONFIG3 pin selects the TDM slot selection in TDM Mode:

Table 3: CONFIG3 Hardware Control – TDM Slot Selection

Switch Position	Pin Configuration		Description
P1	Pull-up to 3.3 V	0 Ω	Slots 14–15
P2		4.7 kΩ	Slots 12–13
P3		22 kΩ	Slots 10–11
P4		100 kΩ	Slots 8–9
P5	Pull-Down to GND	100 kΩ	Slots 6–7
P6		22 kΩ	Slots 4–5
P7		4.7 kΩ	Slots 2–3
P8		0 Ω	Slots 0–1
P9	No Connection	—	—

The CONFIG4 pin selects the clock reference and ASP channel ordering:

Table 4: CONFIG4 Hardware Control – Clocking Configuration

Switch Position	Pin Configuration		Clock Reference	Reference Clock Frequency (MHz)	Virtual PAD
P1	Pull-up to 3.3 V	0 Ω			Bypassed
P2		4.7 k Ω	XTAL	512 fs(base)	
P3		22 k Ω			
P4		100 k Ω	MCLK	512 fs(base)	
P5	Pull-Down to GND	100 k Ω			Enabled – Level Detection
P6		22 k Ω	MCLK	512 fs(base)	
P7		4.7 k Ω			Enabled – Edge Detection
P8		0 Ω	MCLK	512 fs(base)	
P9	No Connection	—	—	—	—

- fs(base) is the base sample rate.
fs(base) = 48 kHz for 48 kHz-related sample rates; fs(base) = 44.1 kHz for 44.1 kHz-related sample rates.

5 Input and Output Buffer Circuits

5.1 Input Buffer

The analog input channels are supported using external buffer circuits. The buffer circuit, comprising a high-pass filter and anti-alias filter, implemented on the DC5312BSE-ADC daughter card is shown in Figure 24. The buffer circuit shown produces a full-scale (0 dBFS) output from a 1 V_{RMS} single-ended input.

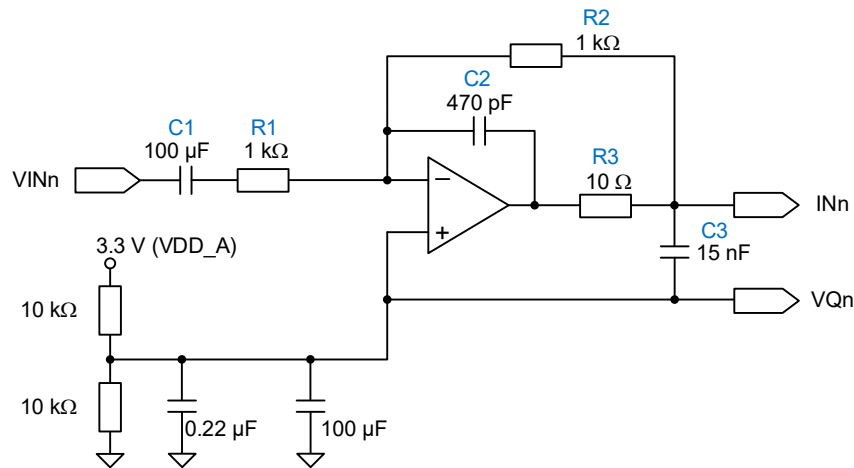


Figure 24: Input Buffer

The high-pass filter is provided by the AC-coupling capacitor C1 and series resistor R1. Using the values shown in Figure 24, the –3 dB cut-off frequency (F_c) can be calculated using the following equation:

$$F_c = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 1000 \times (100 \times 10^{-6})} = 1.59 \text{ Hz}$$

The anti-alias filter is provided by the op-amp and associated feedback components. The objective is to provide a flat passband for the audio input bandwidth, and sufficient attenuation at the ADC-modulator sample frequency. The low output impedance of the circuit minimizes the distortion of the signal path.

The typical filter shown provides a –3 dB cut-off frequency around 424 kHz, suitable for the highest CS5312BSE sample rate of 384 kHz. The attenuation slope of –12 dB/octave results in 42 dB attenuation at the ADC-modulator sample frequency of 6.144 MHz.

The –3 dB cut-off frequency is approximated by the following equation:

$$F_c = \frac{1}{2\pi \sqrt{R_2 R_3 C_2 2C_3}} = \frac{1}{2\pi \sqrt{1000 \times 10 \times 470 \times 10^{-12} \times 2 \times 15 \times 10^{-9}}} = 424 \text{ kHz}$$

The gain of the input buffer is set by R1 and R2. The gain should be configured to provide a full-scale signal of 1 V_{RMS} at the input to the CS5312BSE. The values shown in Figure 24 provide a ratio of 1; in this configuration, the buffer supports a full-scale input of 1 V_{RMS}.

6 Notices

JURA firmware development utilizes components under the following licenses:

1. XMOS PUBLIC LICENCE: Version 1, available at www.xmos.ai/license-agreements/
2. The MIT License, available at www.github.com/microsoft/uf2/blob/master/LICENSE.txt. Copyright © Microsoft Corporation

Unmodified USB Audio 2.0 Device Software source code is available from www.xmos.ai under XMOS PUBLIC LICENCE: Version 1.

7 References

- [1] Cirrus Logic, CDB-PROAUDIO_DS1352DB; Dungle System (CDB-PROAUDIO)
- [2] Cirrus Logic, CS5312BSE_DS1433; High Performance Two-Channel Audio ADC Datasheet

8 Revision History

Revision	Changes
DB1 MAY 2026	• Initial version.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest you, go to www.cirrus.com.

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