CDB40L5x-Q100

CDB40L5x-Q100 Board User Guide

Introduction

The CDB40L5x-Q100 is a platform for testing and evaluating the CS40L51, CS40L52, and CS40L53 devices. This document describes using CDB40L5x-Q100 boards with various supported configurations.

Table of Contents

1 Introduction

This user guide is applicable to the CDB40L51/CDB40L52/CDB40L53 evaluation boards, collectively referred to as the CDB40L5x customer development boards. The CDB40L5x-Q100 (also referred to as a CDB) is a daughter card for the Lochnagar 2 development platform. Each CDB has two of the same device (i.e., two CS40L51 devices, two CS40L52 devices, or two CS40L53 devices).

1.1 Features

The CDB40L5x-Q100 + Lochnagar 2 system includes the following features:

- Supports 2 CS40L5x devices – one configured for internal-boost amplifier supply, and one for an external supply
- USB Connection to PC via SCS
- Tuning user interface
- Support for I2C control ports
- Test point access to GPIO
- High power rails for internal boost (device 1/U1/HAP1) and external (device 2/ U2/HAP2) power supplies
- Configuration of system power supply via jumpers

2 Quick Start Guide with SoundClear Studio (SCS)

For more information on how to get started with SCS, see Application Note *AN0687 – CS40L5x SCS User Guide*.

2.1 Required Hardware for Quick Start

1. 1 Lochnagar 2
2. 1 CDB40L5x-Q100
3. 1 USB-B to USB-A cable to connect host (i.e. laptop) to Lochnagar 2 board

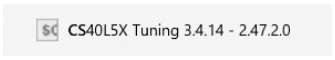
2.2 Required Software for Quick Start

1. SCS Haptics Tuning Dependencies Installer
2. CS40L5x Tuning BSP

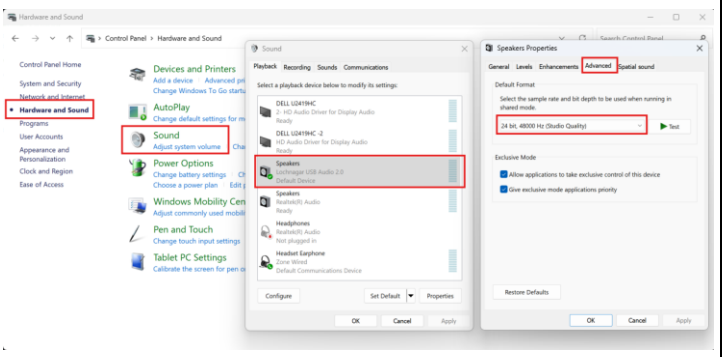
2.3 Quick Start Procedure

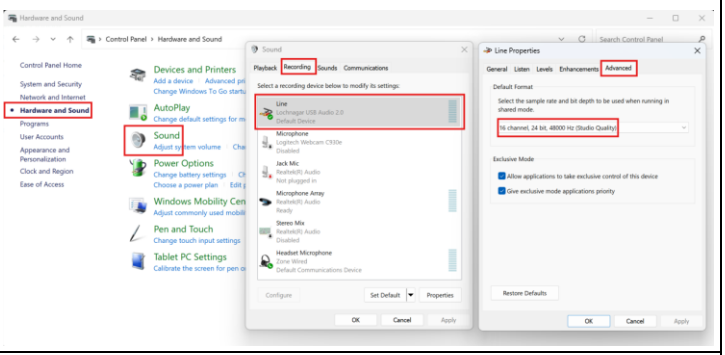
1. Install the required software
   - Install the SCS Haptics Tuning Dependencies Installer.
   - Install the CS40L5X Tuning Base BSP

Contact your Cirrus Logic applications representative for assistance in sourcing or installing this software.



2. Ensure that the sound card is configured correctly for both recording and playback.

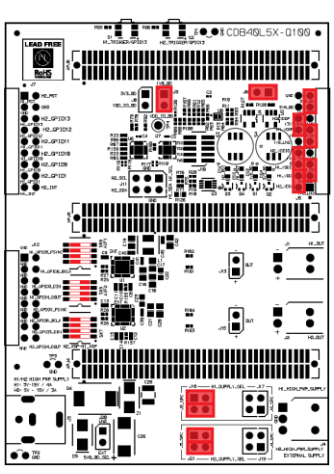


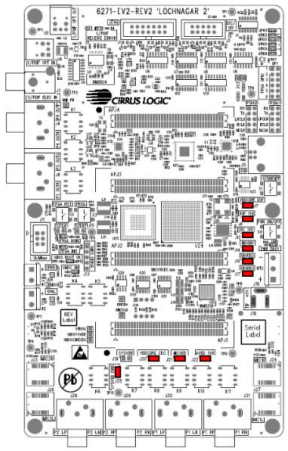


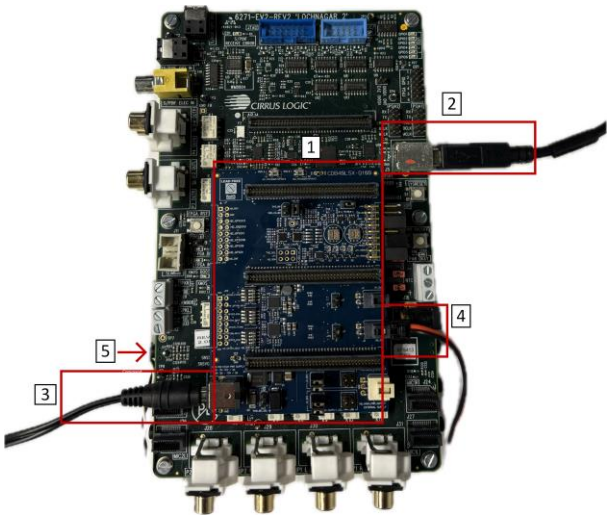
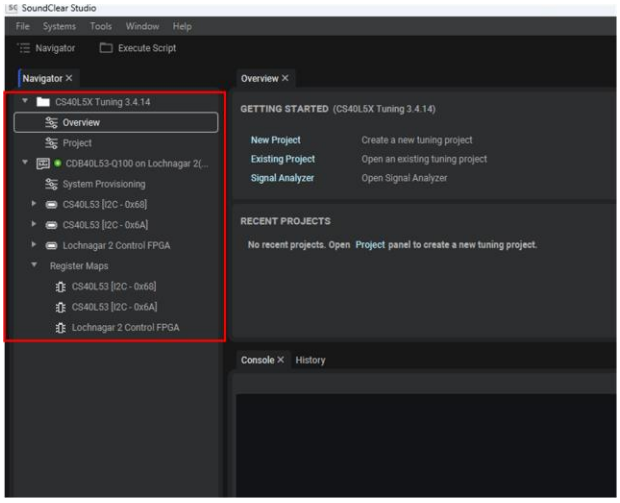
3. Ensure that the jumpers on the CDB40L5x-Q100 board are correct. For most cases, the configuration shown on the right will work; this is the default jumper placement.

The populated jumpers are shown in Red. The switches SW6, SW5, and SW7 should be configured as follows:

Switch	SW6 (top)	SW5 (middle)	SW7 (bottom)
Configuration	All on	All off	All on





4. Connect the CDB40L5x-Q100 to Lochnagar 2 and PC. • Place CDB40L5x-Q100 onto Lochnagar 2 to plug in using APJ1, APJ2, and APJ3. • Connect the Lochnagar 2 to the PC using a USB-A cable. • Connect a 3.3 V – 15 V power supply to CDB40L5x-Q100. A 12 V / 5 A power supply is recommended by default. • Connect an actuator to H1_OUT and/or H2_OUT (J1 and/or J2) on the CDB40L5X board. • (Optional, but recommended) Connect the analog output of an accelerometer into the Lochnagar 2 board (J35 on the bottom side).	
5. Open the CS40L5X Tuning application and the CS40L5x devices will appear in the Navigator. Refer to Section 6.1 for information on project creation.	

3 Hardware Overview

3.1 Board Diagram

An overview of the CDB40L5x-Q100 board is shown in the following figure.

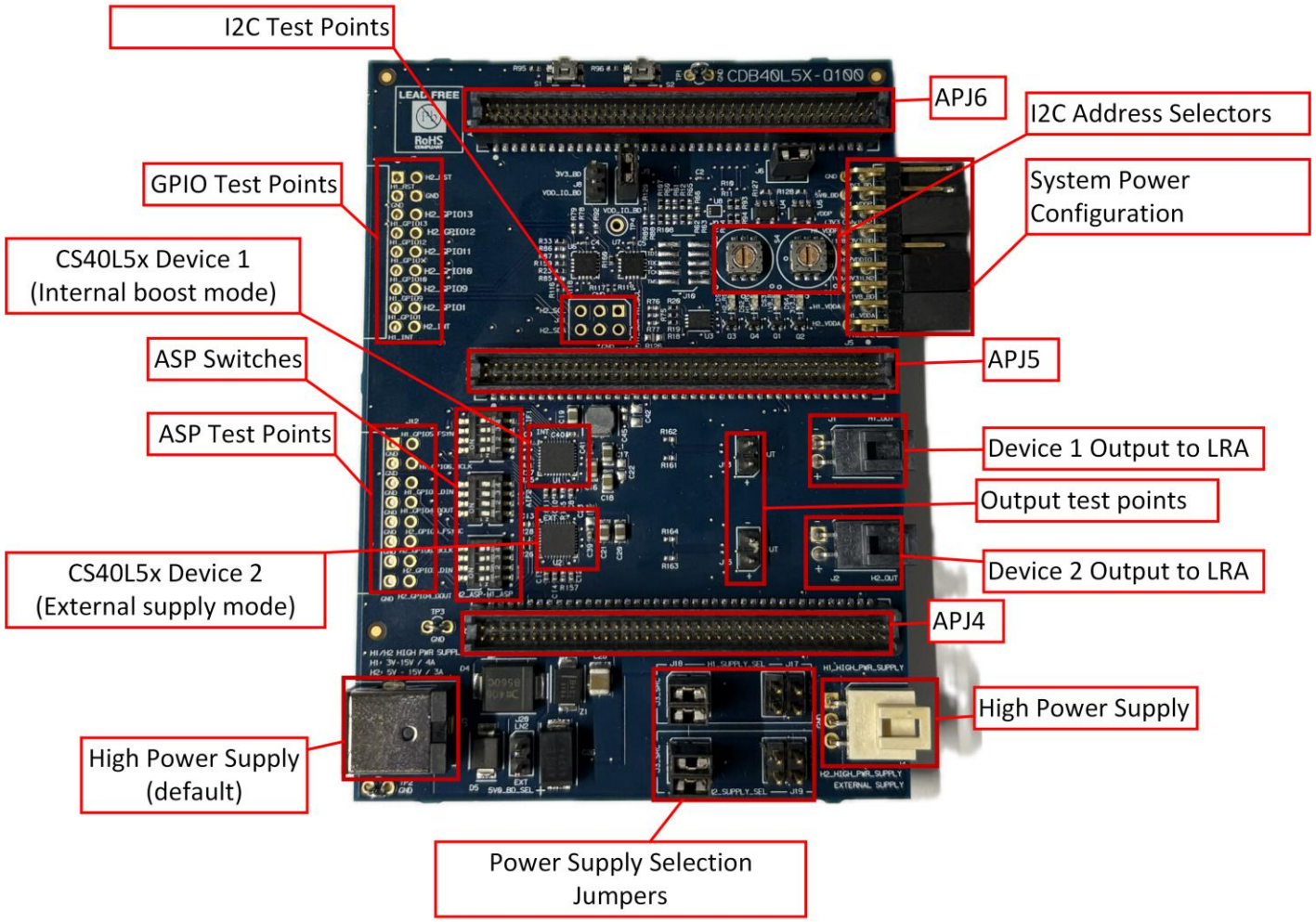


Figure 1 Board Diagram

3.2 Block Diagram

The following block diagram shows more details of the connections between the Lochnagar 2 development platform and the CDB40L5x-Q100 board.

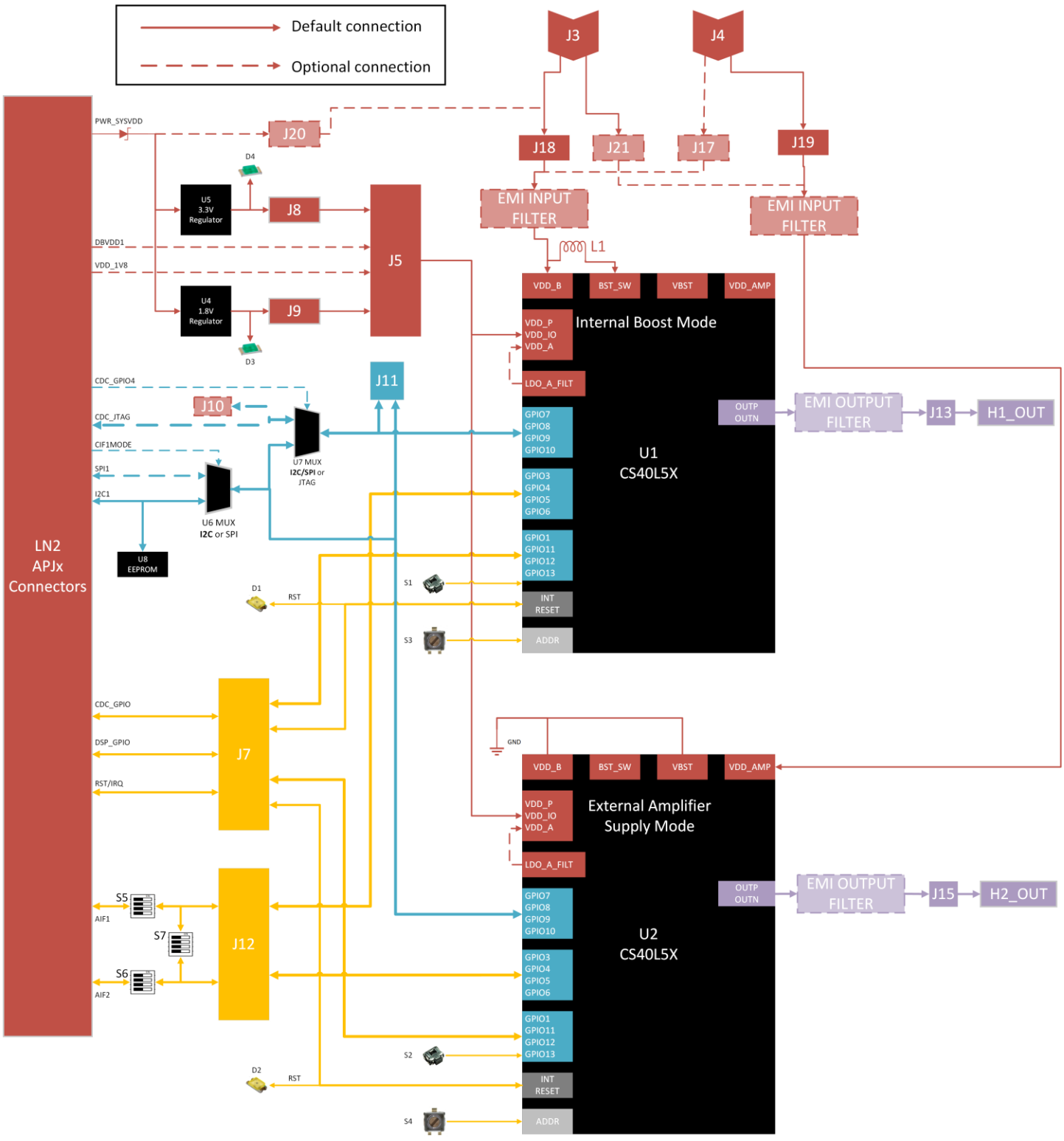


Figure 2 Block Diagram

4 DC Power Supply Configurations

4.1 Board Supply

The Lochnagar 2 board supplies 5 V power to CDB40L5x-Q100 by default. Regulators on the CDB40L5x-Q100 are used to generate 1.8 V and 3.3 V rails from the 5 V power. The 1.8 V, 3.3 V, and 5 V rails are routed to the CS40L5x devices via J5.

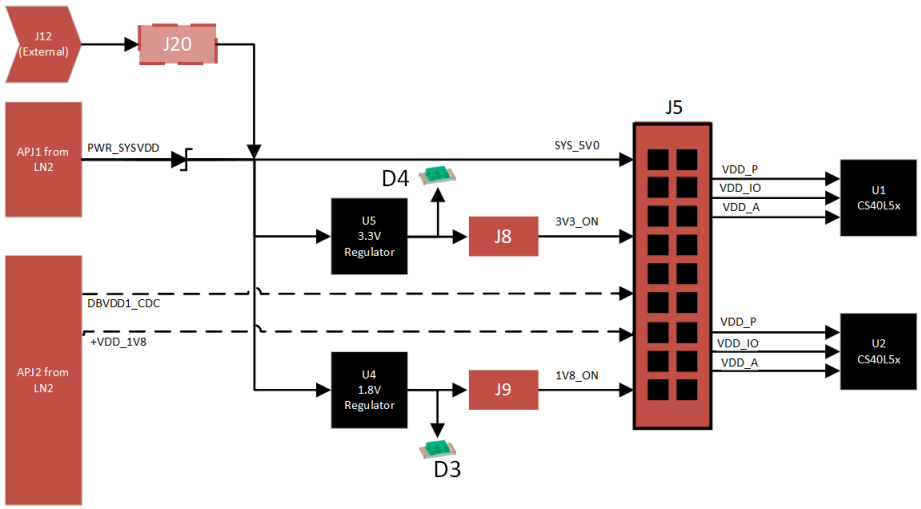


Figure 3 Board Supply

4.1.1 Board supply from LN2 (default)

By default, the LN2 provides a 5 V supply to the CDB40L5x-Q100 board. This supply is used to provide I/O power rails. Ensure J20 is not populated (default).

4.2 Amplifier Supply

The Class D amplifier can be powered from the internal boost converter or from an external supply. Device 1 is powered using the internal boost converter and Device 2 is powered directly from an external power supply.

The amplifier power supply for each device can be provided through J3 or J4. The power source for Device 1 is selected using J17 and J18; the power source for Device 2 is selected using J19 and J21, as shown in the table below.

Note that the amplifier supply for Device 1 (boost converter) is supported in the range 3 V – 15 V; the amplifier supply for Device 2 (external supply) is supported in the range 5 V – 15 V.

Table 1 Amplifier Supply

Device 1 Supply	Board Configuration
J3	J17 unpopulated, J18 populated
J4	J17 populated, J18 unpopulated

Device 2 Supply	Board Configuration
J3	J19 unpopulated, J21 populated
J4	J19 populated, J21 unpopulated

The J17, J18, J19, and J21 configuration is illustrated in the figure below.

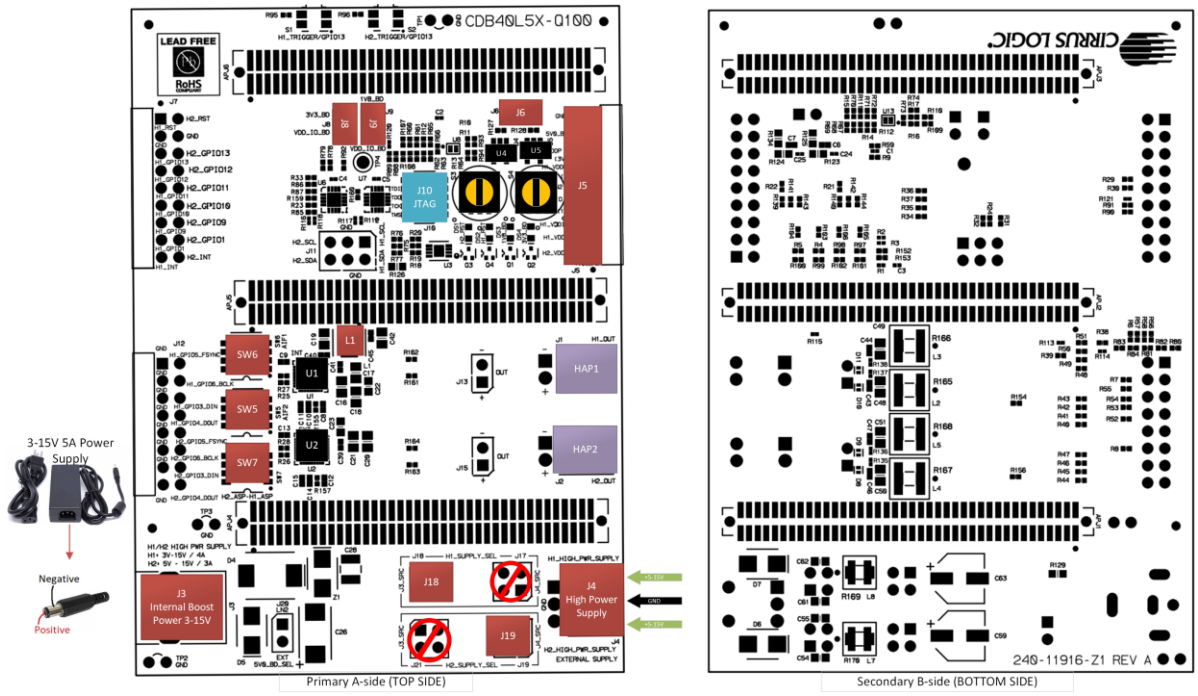


Figure 4 Example Amplifier Supply Configuration

Note:

Each device (U1/U2) requires 2.5 A for a 12V input. If both devices are being used, then use a 5 A power supply

4.3 Device Supplies (VDD_P, VDD_IO, VDD_A)

The CS40L5x devices require power supplies for always-on circuits (VDD_P) and digital input/output (VDD_IO). The analog supply can be provided externally (VDD_A) or generated using the internal regulator.

The device power connections are configured using J5 jumpers. The default configuration is shown in the following figure (VDD_P=3.3V, VDD_IO=1.8V, VDD_A=external 1.8V).

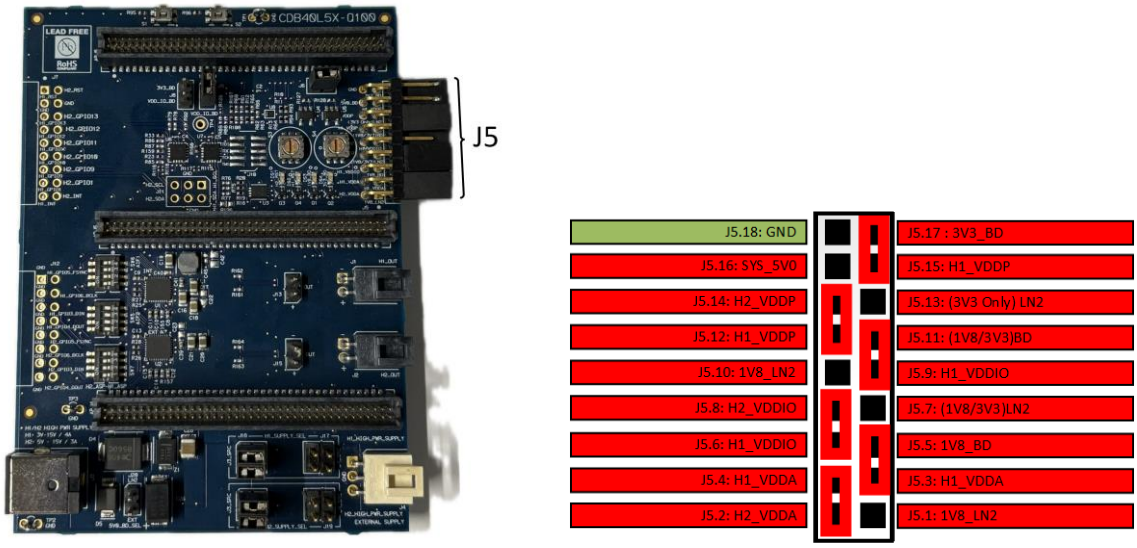


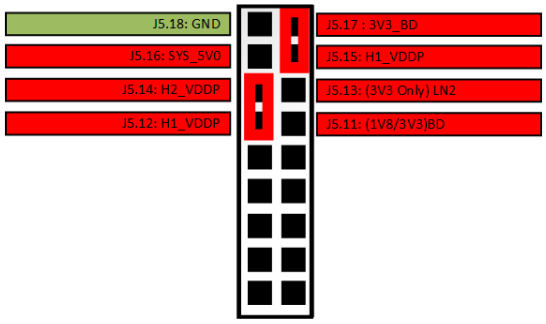
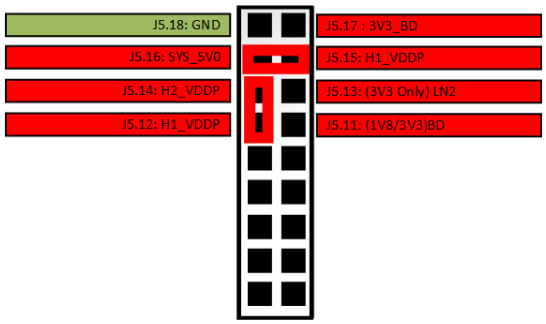
Figure 5 J5 Configuration - VDD_P, VDD_IO, VDD_A

Alternative power-supply configurations are described below.

4.3.1 System Supply (VDD_P)

VDD_P supports 3.3 V and 5 V supplies. The U1 and U2 devices can have different VDD_P supplies, but using the same supply is recommended. The VDD_P configuration is selected using J5 jumpers as follows:

Table 2 J5 Configuration - VDD_P

To configure VDD_P = 3.3 V (default): • Ensure J5.15 – J5.17 are connected • Ensure J5.12 – J5.14 are connected	
To configure VDD_P = 5 V: • Ensure J5.15 – J5.16 are connected • Ensure J5.12 – J5.14 are connected	

4.3.2 Digital I/O Supply (VDD_IO)

VDD_IO supports 1.8 V and 3.3 V supplies. The U1 and U2 can have different VDD_IO supplies, but using the same supply is recommended. The VDD_IO configuration is supported using the J5 jumpers as shown in the figure below. The VDD_IO voltage (at pin J5.11) is selected by populating either J8 or J9.

- To configure VDD_IO for 1.8 V, populate J9 (default). J8 should be unpopulated.
- To configure VDD_IO for 3.3 V, populate J8. J9 should be unpopulated.

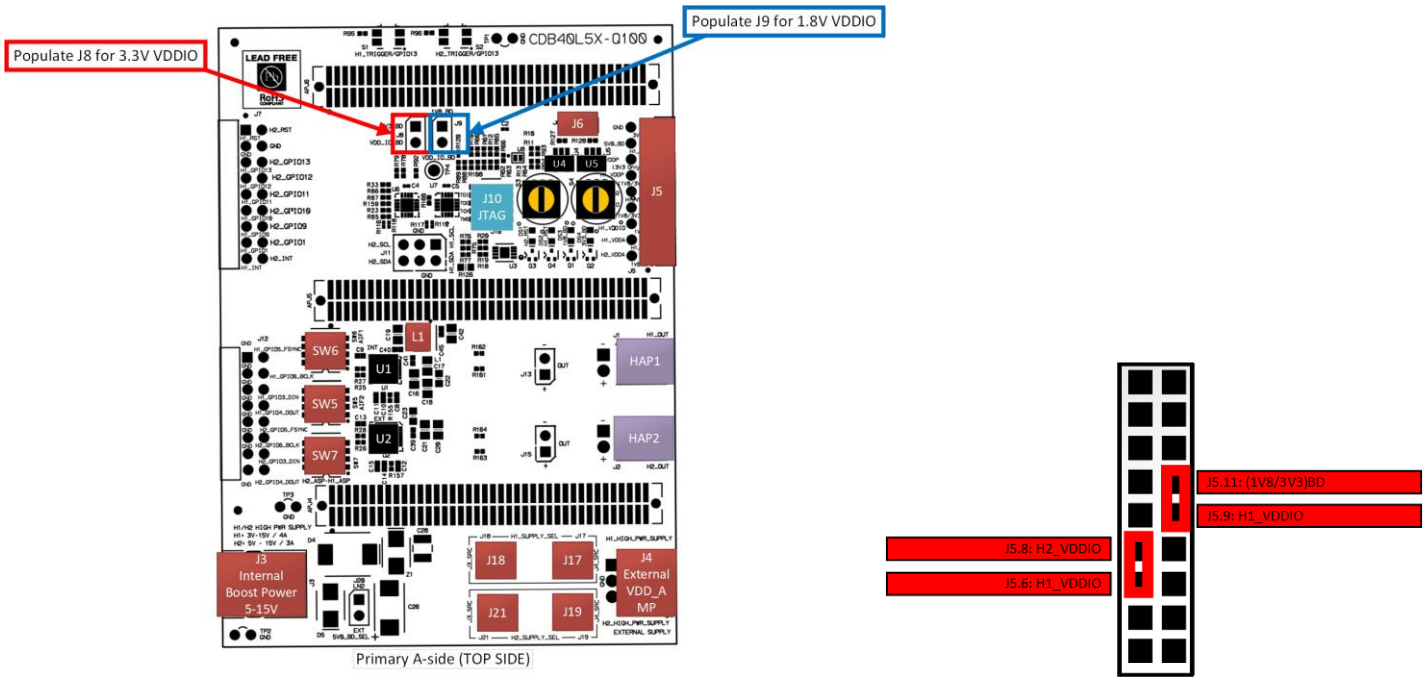
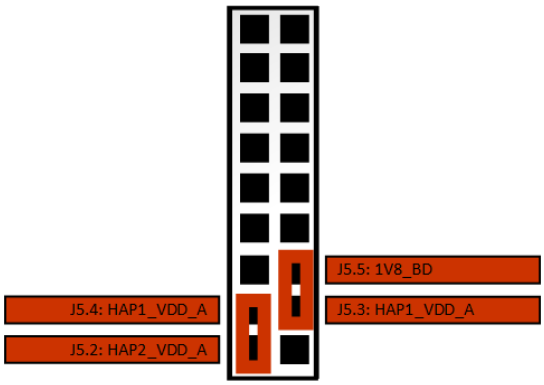
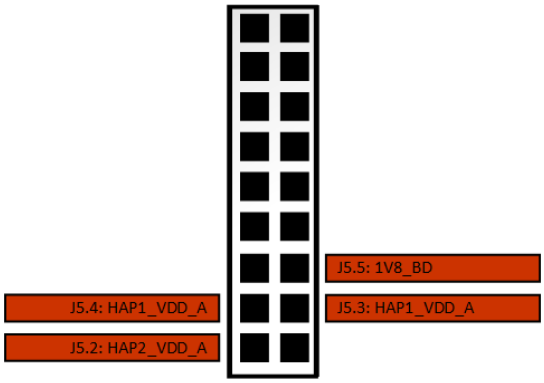


Figure 6 VDD_IO Selection - J8 or J9

4.3.3 Analog Supply (VDD_A)

VDD_A (1.8V) can be provided externally, or else provided from the internal regulator via the LDO_A_FILT output pin.

Table 3 J5 Configuration - VDD_A

To configure external VDD_A (default): • Ensure R155 and R157 are not populated • Ensure J5.3 – J5.5 are connected • Ensure J5.2 – J5.4 are connected	
To configure VDD_A from internal regulator: • Populate R155 and R157 with 0 Ω resistors (this connects VDD_A to LDO_A_FILT) • Remove J5.3 – J5.5 • Remove J5.2 – J5.4	

5 Device Interfaces

CDB40L5x-Q100 serves as a bridge to interface with CS40L5x through a Lochnagar 2 board. The following tables and figures describe the connections between the CDB40L5x-Q100 board, the CS40L5x devices, and the Lochnagar 2 APJ connectors, as well as the test points for external drive or monitoring. Note: R135 and R136 must be populated to enable the VMON test points for HAP1. R137 and R138 should be populated to enable the VMON test points for HAP2. They are located on the top layer.

Table 4 Test Point Color Code

Color	Test Point
Red	Power
Green	Ground
Yellow	GPIO
Blue	I2C Control Port
Purple	Output
Orange	Output Sense

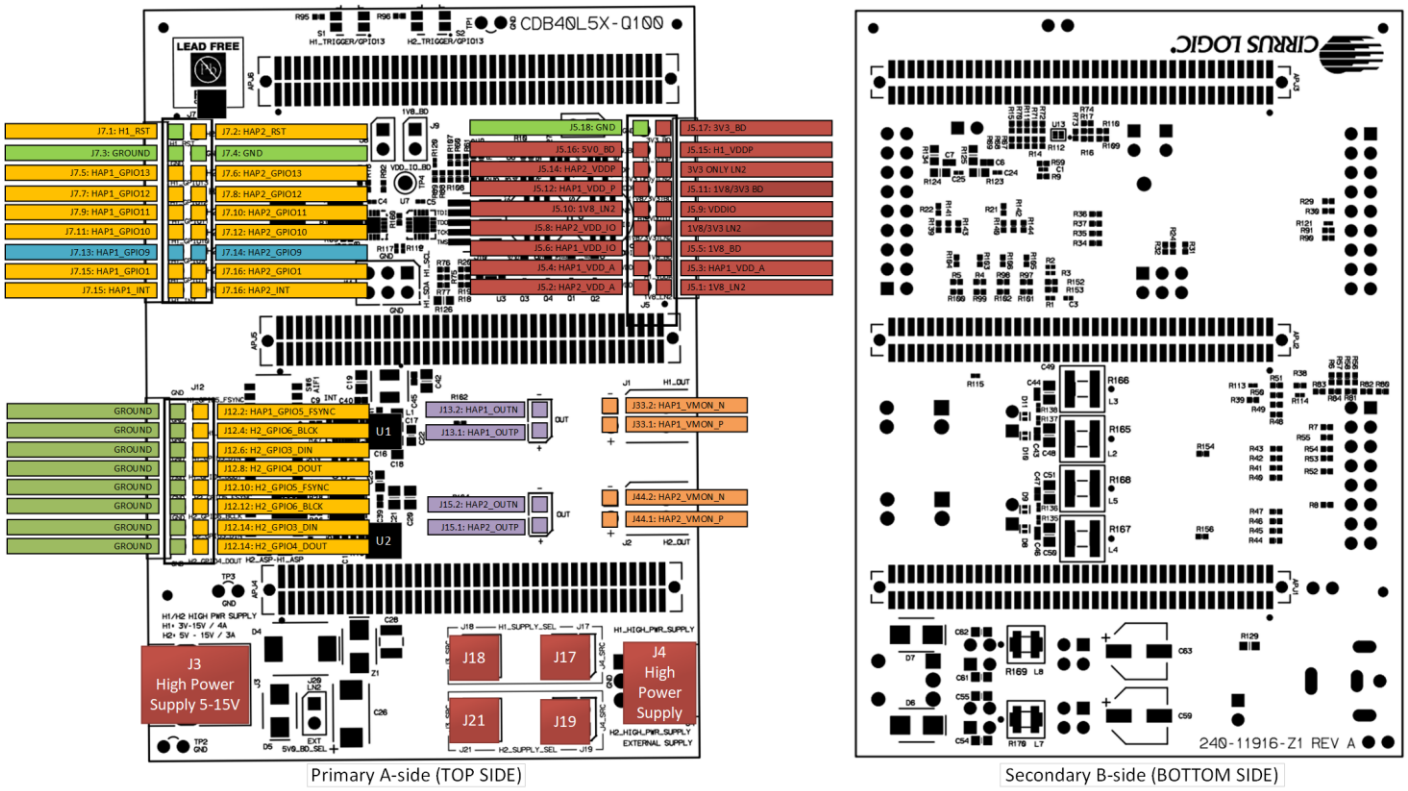


Figure 7 GPIO and Power Test Points

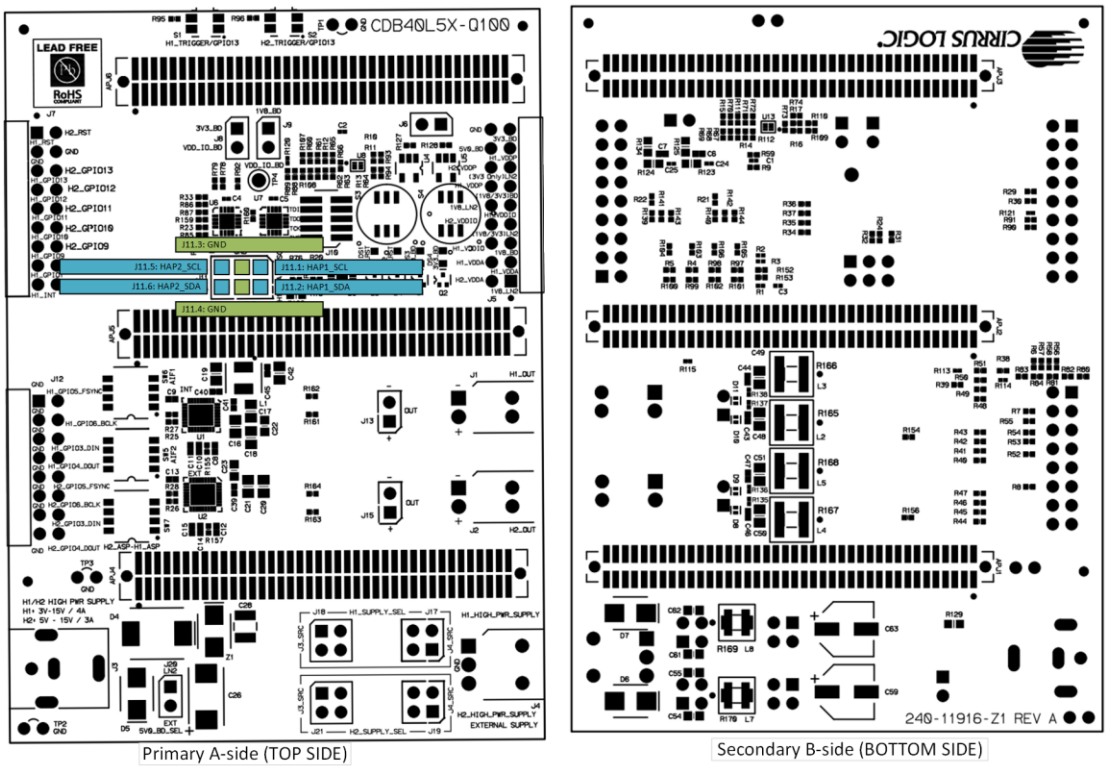


Figure 8 I2C Bus Test Points

Table 5 Test Point Connections

Board Test Points	CS40L5x Pin	CS40L5x Function	APJ Connection to U1: CS40L5x		APJ Connection to U2: CS40L5x	
			Default configuration	***Alternate configurations***	***Default configuration***	***Alternate configurations***
J7.1: H1_RST **J7.2: H2_RST**	**20**	**RESET**	CDC_RST (APJ2.76 / APJ5.76)	CDC_REFCLK_GPIO2 (APJ2.14 / APJ5.14) DSP_GPIO3 (APJ3.57 / APJ6.57) DSP_GPIO5 (APJ3.61 / APJ6.61) DSP_GPIO6 (APJ3.63 / APJ6.63)	CDC_RST (APJ2.76 / APJ5.76)	CS40L5x Haptics 1 Alternate Configuration
J11.1: H1_SCL **J11.5: H2_SCL**	**11**	**I2C_SCL**	I2C1_SCL (APJ2.40 / APJ5.40)	None	I2C1_SCL (APJ2.40 / APJ5.40)	None
		SPI_MISO	SPI1_MISO (APJ2.63 / APJ5.63)	None	SPI1_MISO (APJ2.63 / APJ5.63)	None
J11.2: H1_SDA **J11.6: H2_SDA**	**12**	**I2C_SDA**	I2C1_SDA (APJ2.39 / APJ5.39)	None	I2C1_SDA (APJ2.39 / APJ5.39)	None
		SPI_MOSI	SPI1_MOSI (APJ2.66 / APJ5.66)	None	SPI1_MOSI (APJ2.66 / APJ5.66)	None
J7.13: H1_GPIO9 **J7.14 H2_GPIO9**	**8**	SPI_SCK	SPI2_SCLK (APJ3.11 / APJ6.11)	SPI1_SCLK (APJ2.65 / APJ5.65)	SPI2_SCLK (APJ3.11 / APJ6.11)	SPI1_SCLK (APJ2.65 / APJ5.65)
		GPIO9	CDC_GPIO4 (APJ2.5 / APJ5.5)	None	CDC_GPIO4 (APJ2.5 / APJ5.5)	None
J7.11: H1_GPIO10 **J7.12: H2_GPIO10**	**9**	SPI_SS	None	SPI1_SS (APJ2.61/APJ5.61) SPI2_SS (APJ3.13 / APJ6.13)	None	CS40L5x Haptics 1 Alternate Configuration
		GPIO10	CDC_GPIO4 (APJ5.5 / APJ3.59)	None	CDC_GPIO5 (APJ5.7 / APJ3.61)	None
J7.9: H1_GPIO11 **J7.10: H2_GPIO11**	**13**	**GPIO11**	CDC_REFCLK_GPIO2 (APJ2.14/ APJ5.14)	None	CDC_REFCLK_GPIO2 (APJ2.14 / APJ5.14)	None
J7.7: H1_GPIO12 **J7.8: H2_GPIO12**	**14**	**GPIO12**	CDC_GPIO3 (APJ2.52 / APJ5.52)	None	CDC_GPIO3 (APJ2.52 / APJ5.52)	None
J7.5: H1_GPIO13 **J7.6: H2_GPIO13**	**15**	**GPIO13**	CDC_GPIO1 (APJ2.26 / APJ5.26)	None	CDC_GPIO1 (APJ2.26 / APJ5.26)	None
J7.15: H1_GPIO1 **J7.17: H2_GPIO1**	**3**	**GPIO1**	CDC_GPIO5 (APJ2.5 / APJ5.5)	None	CDC_GPIO5 (APJ2.5 / APJ5.5)	None
J12.6: H1_GPIO3_DIN **J12.14: H2_GPIO3_DIN**	**4**	GPIO3	None	None	None	None
		ASP_DIN	CDC_AIF1RXDAT (APJ2.32)	CDC_AIF2RXDAT (APJ2.15)	CDC_AIF2RXDAT (APJ2.15)	CDC_AIF1RXDAT (APJ2.32)
J12.8: H1_GPIO4_DOUT **J12.16: H2_GPIO4_DOUT**	**5**	GPIO4	None	None	None	None
		ASP_DOUT	CDC_AIF1TXDAT (APJ2.24)	CDC_AIF2TXDAT (APJ2.13)	CDC_AIF2TXDAT (APJ2.13)	CDC_AIF1TXDAT (APJ2.24)

Board Test Points	CS40L5x Pin	CS40L5x Function	APJ Connection to U1: CS40L5x		APJ Connection to U2: CS40L5x	
J12.2: H1_GPIO5_FSYNC J12.10: H2_GPIO5_FSYNC	**6**	GPIO5	None	None	None	None
		ASP_FSYNC	CDC_AIF1LRCLK (APJ2.34 / APJ5.34)	CDC_AIF2LRCLK (APJ2.16 / APJ5.16)	CDC_AIF2LRCLK (APJ2.16 / APJ5.16)	CDC_AIF1LRCLK (APJ2.34 / APJ5.34)
J12.4: H1_GPIO6_BCLK J12.12: H2_GPIO6_BCLK	**7**	GPIO6	None	None	None	None
		ASP_BCLK	CDC_AIF1RXBCLK (APJ2.36 / APJ5.36)	CDC_AIF2BCLK (APJ2.17 / APJ5.17)	CDC_AIF2BCLK (APJ2.17 / APJ5.17)	CDC_AIF1RXBCLK (APJ2.36 / APJ5.36)
J7.17: H1_INT J7.18: H2_INT	**16**	**INT**	CDC_IRQ (APJ2.3 / APJ5.3)	DSP_IRQ (APJ3.62 / APJ6.62) DSP_GPIO4 (APJ3.59 / APJ6.59) DSP_GPIO5 (APJ3.61 / APJ6.61)	DSP_IRQ (APJ3.62 / APJ6.62)	CDC_IRQ (APJ2.3 / APJ5.3) CDC_GPIO4 (APJ2.5 / APJ5.5) DSP_GPIO6 (APJ3.63 / APJ6.63)
J17.2: HAP1_VDD_B J17.4: HAP1_VDD_B J18.2: HAP1_VDD_B J18.4: HAP1_VDD_B	**2**	**VDD_B**	N/A	PWR_SYSVDD if J20, J18 are populated (APJ1.1 / APJ1.2 / APJ1.4 / APJ4.1 / APJ4.2 / APJ4.4)	N/A	PWR_SYSVDD (if J20, J18 are populated) (APJ1.1 / APJ1.2 / APJ1.4 / APJ4.1 / APJ4.2 / APJ4.4)
J19.2: HAP2_VDD_AMP J19.4: HAP2_VDD_AMP J21.2: HAP2_VDD_AMP J21.4: HAP2_VDD_AMP	**31**	**VDD_AMP**	N/A	PWR_SYSVDD if J20, J21 are populated (APJ1.1 / APJ1.2 / APJ1.4 / APJ4.1 / APJ4.2 / APJ4.4)	N/A	PWR_SYSVDD (if J20, J21 are populated) (APJ1.1 / APJ1.2 / APJ1.4 / APJ4.1 / APJ4.2 / APJ4.4)
L1: HAP1_BST_SW	**34**	**BST_SW**	—	—	—	—
J5.12: H1_VDDP J5.14: H2_VDDP	**24**	**VDD_P**	—	—	—	—
J5.6: H1_VDDIO J5.9: H2_VDDIO J5.8: H2_VDDIO	**10**	**VDD_IO**	—	—	—	—
J5.2: H2_VDDA J5.3: H1_VDDA J5.5: H1_VDDA	**22**	**VDD_A**	—	—	—	—
J1.2: HAP1_OUT+ J2.2: HAP2_OUT+	**29**	**OUTP**	—	—	—	—
J1.1: HAP1_OUT- J2.1: HAP2_OUT-	**30**	**OUTN**	—	—	—	—

5.1 Control Interfaces

The CS40L5x incorporates a control port, supporting I2C or SPI modes of operation. By default, CDB40L5x-Q100 is configured for I2C operation.

5.1.1 Reset

The reset pins on the U1 and U2 devices are independent and are not connected to each other.

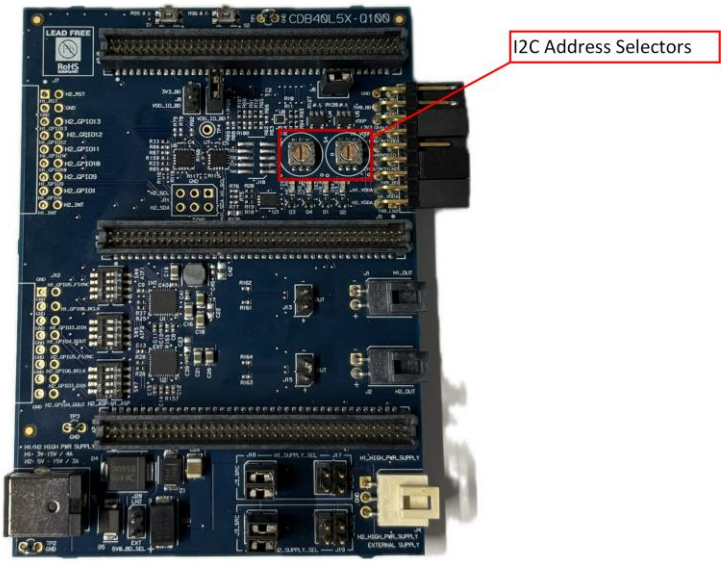
To trigger a manual reset, momentarily short following pins on J7:

- For U1, short J7.1 and J7.3 momentarily
- For U2, short J7.2 and J7.4 momentarily

5.1.2 I²C Interface

CDB40L5x-Q100 uses the Lochnagar 2 I2C1 interface. In order to allow many devices to share a single two-wire control bus, every device target on the bus has a unique 8-bit target address. This I2C address is determined by the position of switches S3 and S4; the switch position is read on entering the Standby State from the Reset State or Hibernate State.

Table 6 I2C Target Address

CDB Orientation	Use the following switch position		
	Position	S3: Address for U1	S4: Address for U2
		0x60	0x62
		0x64	0x66
		0x68 (default)	0x6A (default)
		0x6C	0x6E

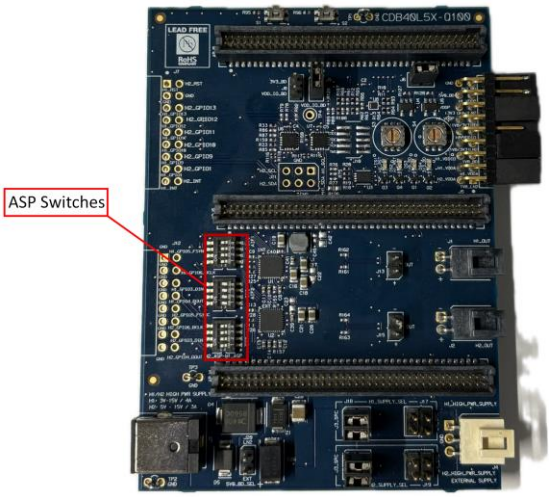
5.1.3 SPI Interface

To use the SPI interface, contact your Cirrus Logic representative for details.

5.2 Tuning Interface

5.2.1 Audio Serial Port (ASP) Interface

Tuning requires the ASP interface to be enabled (default) and connected to the LN2 board. The ASP is connected to the Lochnagar 2 audio interface using DIP switches as described below.

<table>
<tr><th>CDB DIP Switches for ASP</th><th>Description</th></tr>
<tr><td> 
</td><td>
<table>
<tr><th>Switch</th><th>ON Position</th><th>OFF Position</th></tr>
<tr><td>S5</td><td>Connects the ASP in U2 to the Lochnagar 2 Audio Interface 2</td><td>Disconnects the U2 ASP from Lochnagar 2 Audio Interface 2 (default)</td></tr>
<tr><td>S6</td><td>Connects the ASP in U1 to the Lochnagar 2 Audio Interface 1 (default)</td><td>Disconnects the U1 ASP from Lochnagar 2 Audio Interface 1</td></tr>
<tr><td>S7</td><td>Connects U1 and U2 ASP pins together (default)</td><td>Disconnects U1 and U2 ASP pins</td></tr>
</table>
</td></tr>
</table>

6 Software Configuration

6.1 Creating an SCS Project and Device Configuration

When starting SCS, first a project must be created. The project will contain the tunings and waveforms created for a haptics actuator/system. The tuning process is shown below.

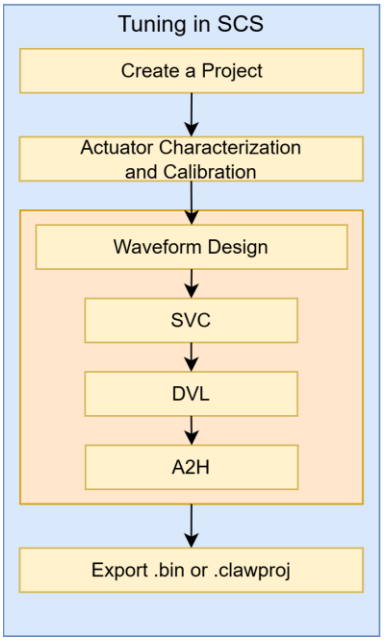
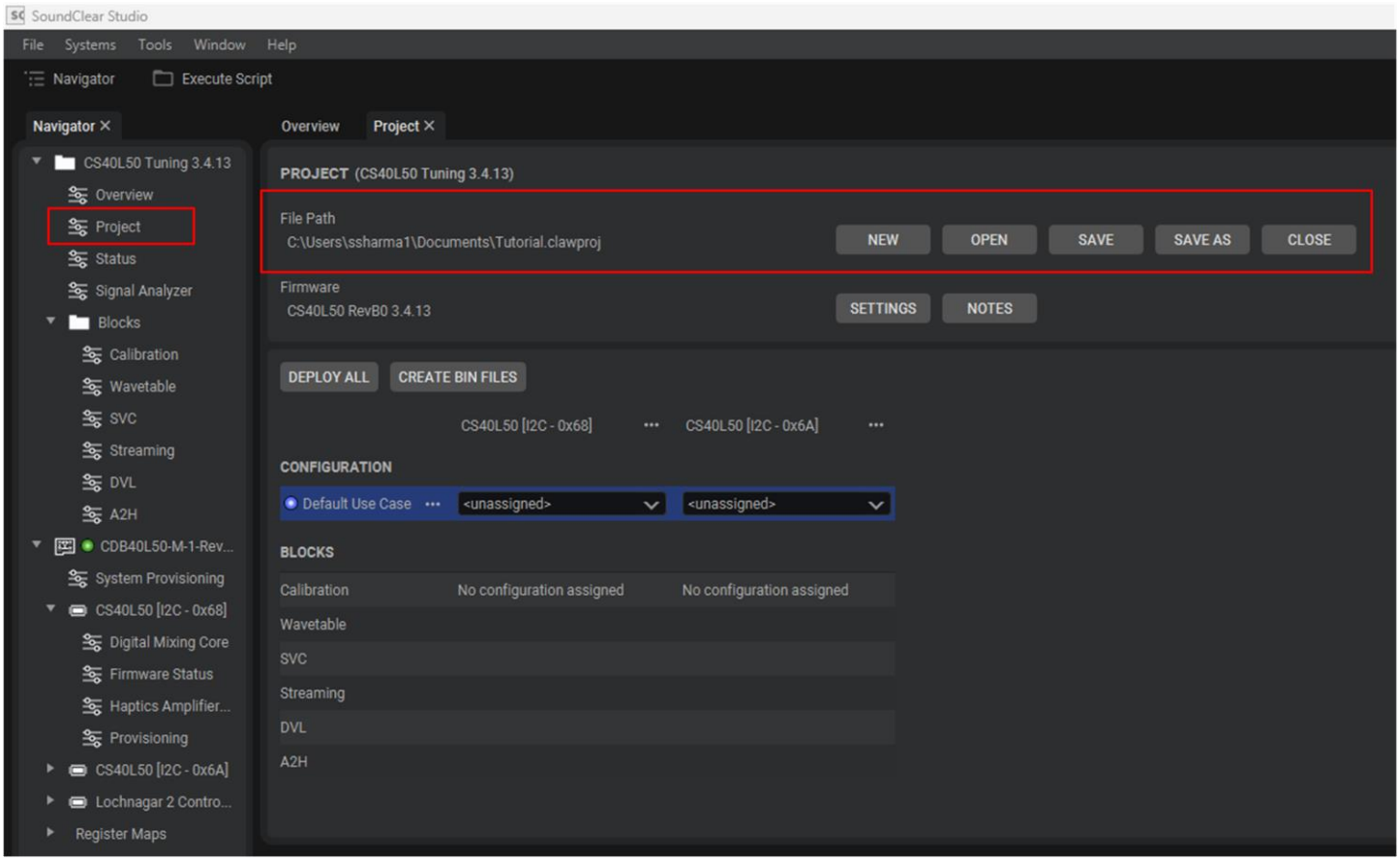


Figure 9 SCS Tuning Process

To create a new project in SCS, navigate to the project tab in the navigator and then create a new project. Once the project is created the system can be configured. The configuration for each device can be set in the Project tab.



The following definitions are applicable in SoundClear Studio and throughout this document.

- Each CS40L5X available on the given tuning platform is considered a **Device.**
- Each device can be assigned a tuning **Configuration**.
- Each configuration consists of tuning blocks (SVC, DVL, etc.) with a number of tunable parameters. The tuned parameter values for each block are considered **Presets.**

A configuration is a container of presets that can be applied to a device all at once. Different combinations of presets can be created for different configurations, and configurations can be applied across multiple devices on the hardware. Single configurations cannot be exported out of a Tuning Project, that is the purpose of an SCS project. The project will hold all associated configurations to the device. See Application Note *AN0687 – CS40L5x SCS User Guide* for more information.

7 Revision History

Revision	Changes
DB1 DEC 2025	• Initial release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.