CDB82L46-DC High Coast System Daughter Card User Guide

Introduction

The High Coast system is a hardware platform for configuring and evaluating the Cirrus Logic CS82L4x analog front-end (AFE) devices. It comprises the High Coast motherboard (CDB82L4X-MB) and a daughter card. Separate daughter cards are available for the 1-channel (CDB82L41-DC), 4-channel (CDB82L44-DC), and 6-channel (CDB82L46-DC) products.

This document describes the features and usage of the High Coast daughtercard CDB82L46-DC. For descriptions of the CDB82L4X-MB motherboard and the other daughter cards, see the respective user guides.

The CDB82L46-DC daughter card incorporates a CS82L46 six-channel analog frontend (AFE), see Figure 1.

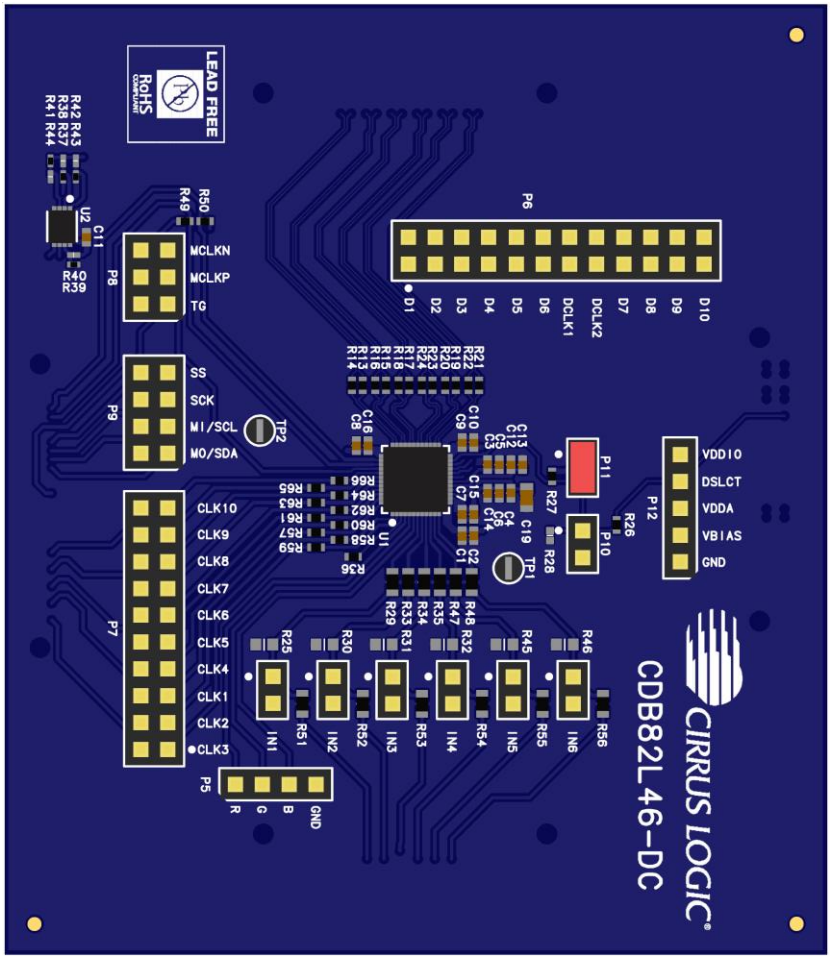

Figure 1. CDB82L46-DC Daughter Card

Table of Contents

1 Motherboard Connection

Caution:

The daughter card must not be inserted or removed while the High Coast system is powered. Fully disconnect or power down all external power supplies before connecting or removing a daughter card.

The CDB82L46-DC daughter card mounts to the High Coast motherboard via the DC1, DC2, DC3, and DC4 connectors. For further details, refer to the High Coast system motherboard user guide.

To mount the daughter card, ensure the DC1–DC4 connectors of the daughter card align with the respective connectors on the High Coast motherboard. Once aligned, apply downwards pressure on each side of the daughter card until seated. After mounting, device signals are accessible from the High Coast motherboard. For details on the operation of the High Coast motherboard, refer to the High Coast motherboard user guide.

The correct position and orientation of the CDB82L46-DC daughter card is shown in Figure 2.

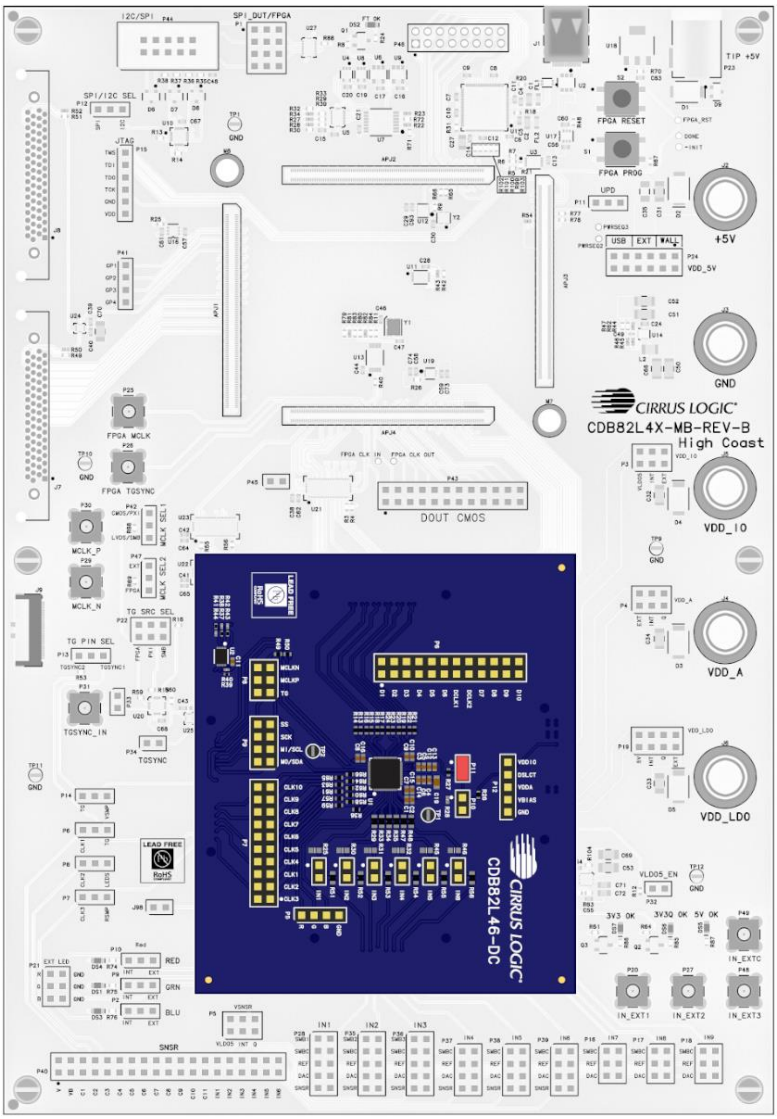

Figure 2. Motherboard Connection

2 Test Points

The CDB82L46-DC daughter card provides a comprehensive set of test points for monitoring device signals. The test points are grouped by function, as shown in Figure 3.

Ground connections, including test points TP1 and TP2, are identified with a green GND symbol in Figure 3. Note that oscilloscope probe ground leads can be connected to hoop test points TP1 and TP2.

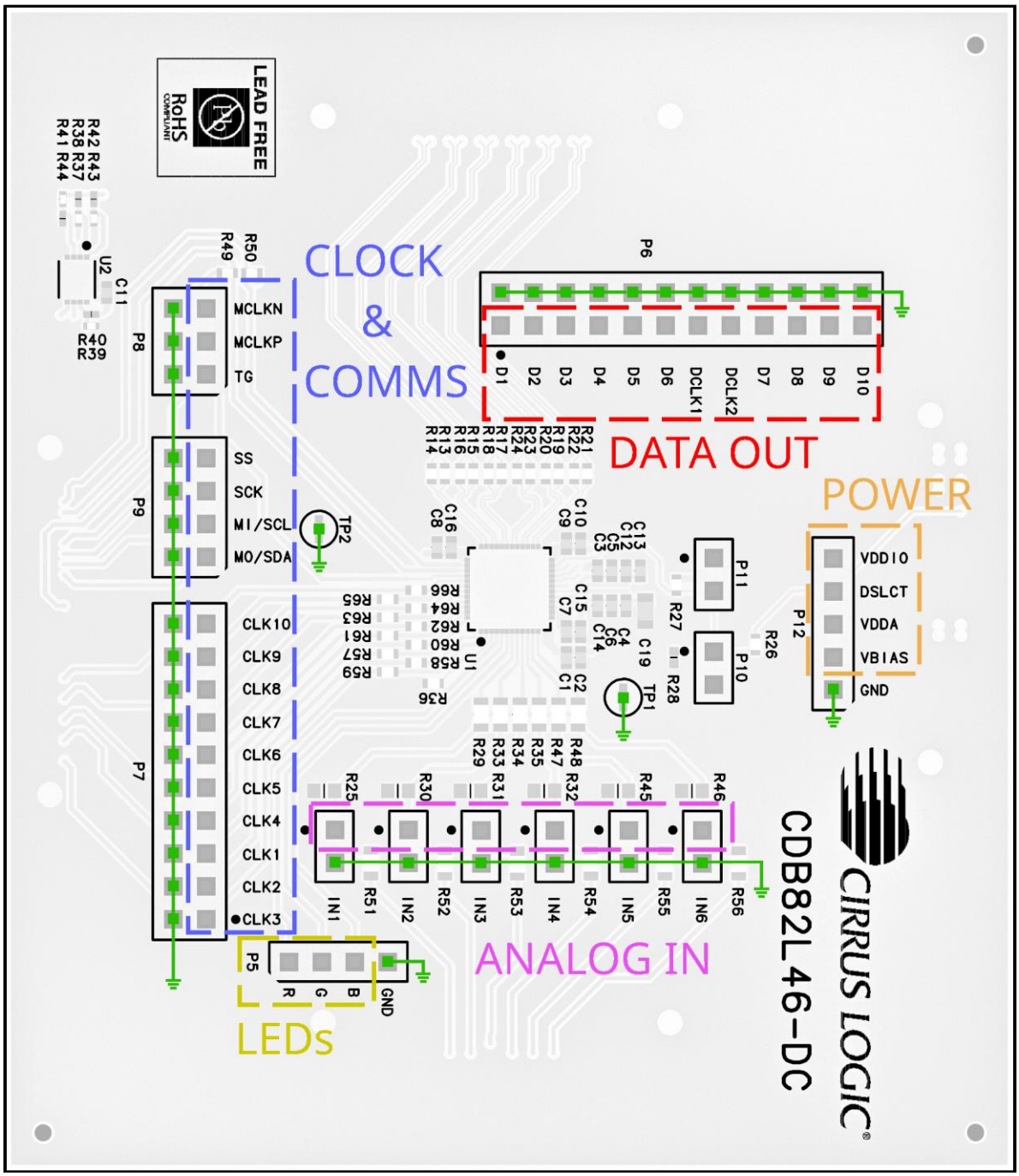

Figure 3. Test Points

All test points are labeled on the daughter card. The mapping between the daughter-card label and CS82L46 pin is shown in Table 1.

Table 1. Test Point Mapping

Daughter Card Label	CS82L46 Pin Name	Notes
MCLKN	MCLK_EXT_N	
MCLKP	MCLK_EXT/MCLK_EXT_P	
SS	$\overline{\text{SPI\_CS}}$	
SCK	SPI_SCK	
MI/SCL	SPI_SDO/I2C_SCL	
MO/SDA	SPI_SDI/I2C_SDA	
TG	TGSYNC1/VSMP_EXT	
CLK1	CLKOUT1/LEDR_EN/TGSYNC2	
CLK2	CLKOUT2/LEDG_EN/LED_START	
CLK3	CLKOUT3/LEDB_EN/RSMP_EXT	
CLK4	CLKOUT4	
CLK5	CLKOUT5	
CLK6	CLKOUT6	
CLK7	CLKOUT7	
CLK8	CLKOUT8	
CLK9	CLKOUT9	
CLK10	CLKOUT10	
D1	DOUT1_P/DOUT1	CMOS configuration only - see Section 5.
D2	DOUT1_N/DOUT2	CMOS configuration only - see Section 5.
D3	DOUT2_P/DOUT3	CMOS configuration only - see Section 5.
D4	DOUT2_N/DOUT4	CMOS configuration only - see Section 5.
D5	DOUT3_P/DOUT5	CMOS configuration only - see Section 5.
D6	DOUT3_N/DOUT6	CMOS configuration only - see Section 5.
DCLK1	DCLKOUT_P/DCLKOUT1	CMOS configuration only - see Section 5.
DCLK2	DCLKOUT_N/DCLKOUT2	CMOS configuration only - see Section 5.
D7	DOUT4_P/DOUT7	CMOS configuration only - see Section 5.
D8	DOUT4_N/DOUT8	CMOS configuration only - see Section 5.
D9	DOUT5_P/DOUT9	CMOS configuration only - see Section 5.
D10	DOUT5_N/DOUT10	CMOS configuration only - see Section 5.
VDDIO	VDD_IO	
DSLCT	DSLCT	
VDDA	VDD_A	
VBIAS	VBIAS	
IN1	IN1	
IN2	IN2	
IN3	IN3	
IN4	IN4	
IN5	IN5	
IN6	IN6	
R	ILED_R	
G	ILED_G	
B	ILED_B	

3 DSLCT Pin

The CS82L46 provides a control port, supporting I2C or SPI modes of operation. The control port is automatically configured in I2C Mode or SPI Mode following the first valid I2C/SPI activity detected after power-on reset.

- In I2C Mode, the DSLCT pin sets the I2C address.
- In SPI Mode, the DSLCT pin determines whether the register map is in Flat Mode 0, Flat Mode 1, or Banked Mode.

The DSLCT pin is connected to headers P10 and P11. To configure the control interface using the DSLCT pin, place a jumper on P10 or P11 as described in Table 2.

Table 2. DSLCT Jumper Configuration

Jumper Position	I2C Address (W/R)	SPI Mode
P11	0x36/0x37	Flat Mode 0
P10	0x34/0x35	Banked Mode
No Jumper		Flat Mode 1

The locations of headers P10 and P11 are shown in Figure 4

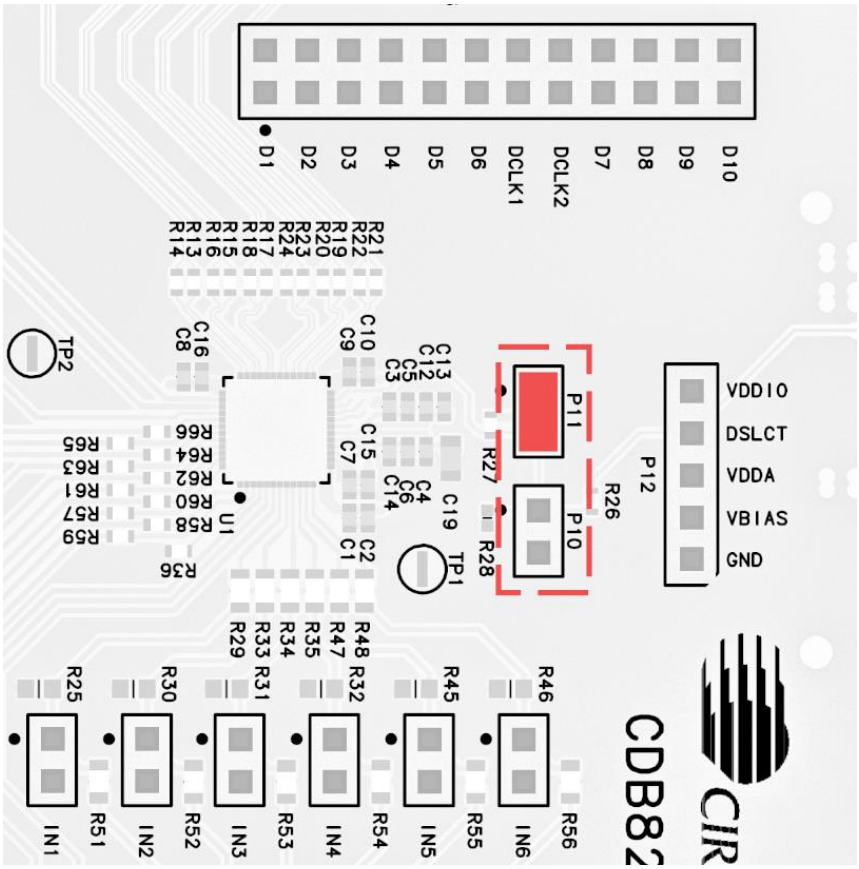

Figure 4. DSLCT Pin Headers

Note: The DSLCT pin state is read by the CS82L46 device after power-on reset. After changing the DSLCT jumper, power-cycle all device supplies to ensure any changes take effect.

4 Analog Inputs

4.1 Analog Input DC/AC Coupling

By default, analog inputs (IN1–IN6) are DC coupled to the CS82L46 through 0 Ω resistors R29, R33, R34, R35, R47, and R48. The resistor sites are highlighted in red in Figure 6.

To configure the board for AC-coupled input, replace the 0 Ω resistors with capacitors, as illustrated in Figure 5. The required capacitor package size is 0603 (1608 metric).

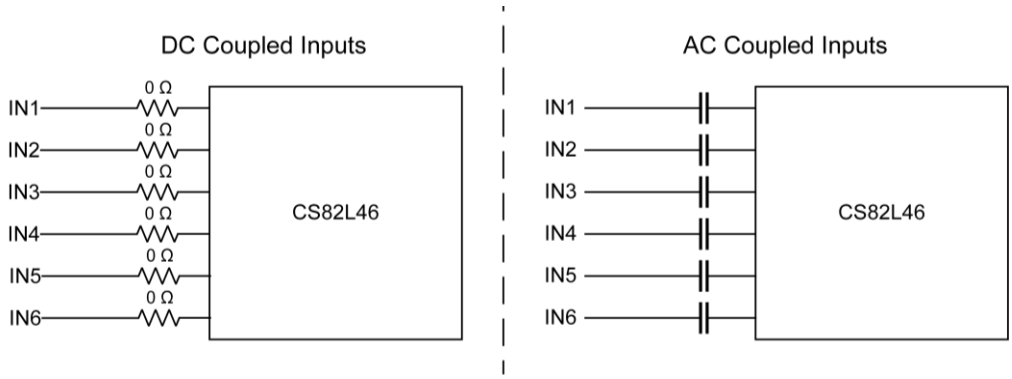

Figure 5. DC/AC Coupled Inputs

4.2 Analog Input Termination

The CS82L46 provides a high-impedance termination for the analog inputs (IN1–IN6). If required, parallel termination resistors can be incorporated by populating R25, R30, R31, R32, R45, and R46. The resistor sites are highlighted in blue in Figure 6.

The recommended termination resistor value is 49.9 Ω, to match the 50 Ω controlled impedance of the analog input traces on the PCB. The required termination resistor package size is 0603 (1608 metric).

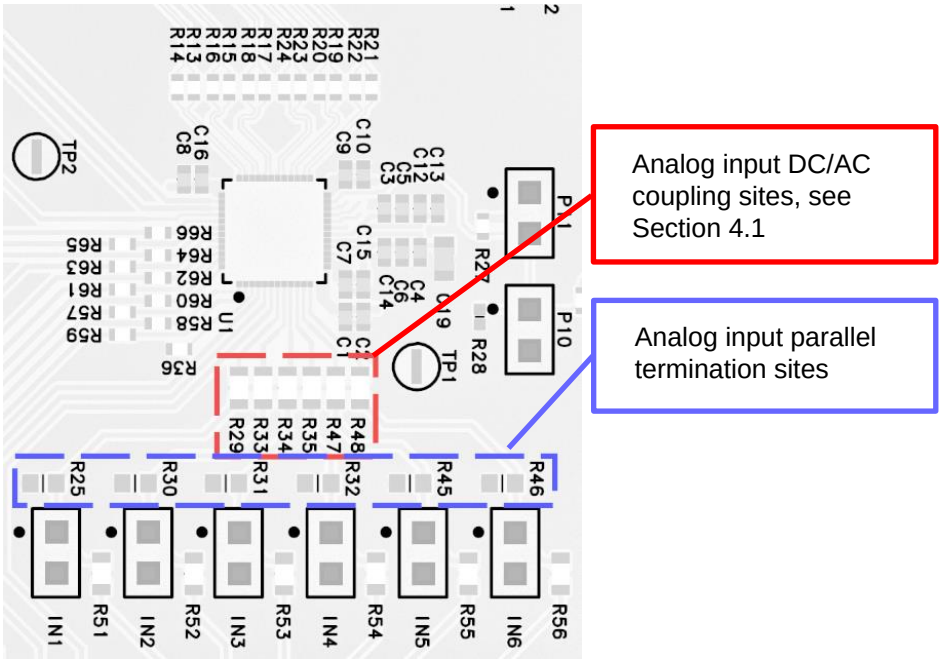

Figure 6. Analog Input Coupling and Termination

5 LVDS/CMOS Data Output

The CDB82L46-DC daughter card can be configured for either LVDS or CMOS data output.

To change the configuration, components must be removed or populated as shown in Table 3.

Table 3. LVDS/CMOS Board Modifications

		LVDS → CMOS		CMOS → LVDS	
Board Location	**Ref Des**	**Action**	**Value (Ω)**	**Action**	**Value (Ω)**
Top	R14	Remove		Populate	0
Top	R13	Remove		Populate	0
Top	R16	Remove		Populate	0
Top	R15	Remove		Populate	0
Top	R18	Remove		Populate	0
Top	R17	Remove		Populate	0
Top	R24	Remove		Populate	0
Top	R23	Remove		Populate	0
Top	R20	Remove		Populate	0
Top	R19	Remove		Populate	0
Top	R22	Remove		Populate	0
Top	R21	Remove		Populate	0
Bottom	R1	Populate	33	Remove	
Bottom	R2	Populate	33	Remove	
Bottom	R3	Populate	33	Remove	
Bottom	R4	Populate	33	Remove	
Bottom	R5	Populate	33	Remove	
Bottom	R6	Populate	33	Remove	
Bottom	R7	Populate	33	Remove	
Bottom	R8	Populate	33	Remove	
Bottom	R9	Populate	33	Remove	
Bottom	R10	Populate	33	Remove	
Bottom	R11	Populate	33	Remove	
Bottom	R12	Populate	33	Remove	

The top-side resistor sites are highlighted in red in Figure 7. The bottom-side resistor sites are located directly underneath the top-side resistors (on the reverse side of the board).

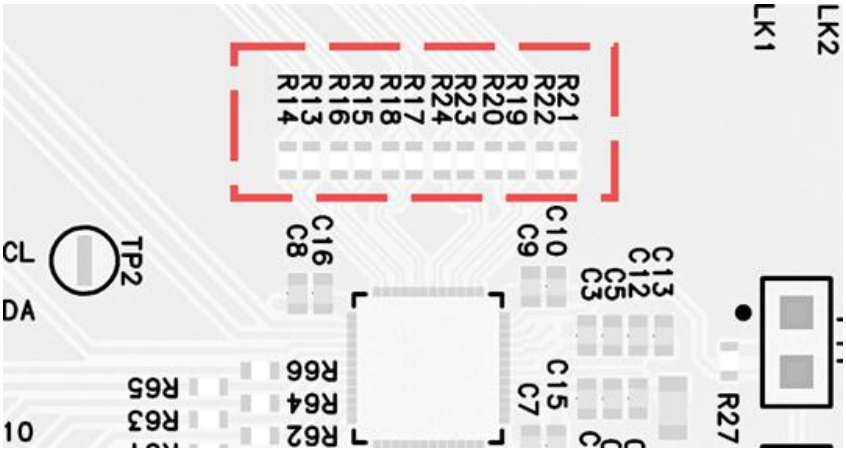

Figure 7. LVDS Top-Side Resistors Location

6 SoundClear Studio Support

SoundClear® Studio (SCS) is a Windows®/MacOS® application used to configure Cirrus Logic devices. SCS provides support for evaluation and development and can be used to communicate with the CDB82L46-DC daughter card when it is mounted on a High Coast motherboard. When SCS is launched, it automatically detects the selected communication protocol (I2C/SPI), and the I2C address/SPI Register Map Mode.

For download and installation details, including script execution, refer to the High Coast (CDB82L4X-MB) motherboard user guide.

7 Revision History

Revision History

Revision	Changes
R1 OCT 2024	• Initial version.
R2 MAY 2025	• Inclusion of CDB82L41-DC details. • Updates due to new revision (REV-B) motherboard. • SCS SPI Flat Mode 1 section updates.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.