AN0681

# CS40L5x Schematic and Layout Guidelines

## Introduction

The CS40L5x is an advanced haptic driver with waveform memory, integrated DSP, and closed-loop algorithms. This document describes the schematic and layout guidelines for the CS40L51, CS40L52, and the CS40L53 devices.

## Table of Contents

# 1 CS40L5x Pinout

The pinout of the CS40L5x is shown in the Figure below (Top View, through package). Note that the corner pad between Pin 1 and Pin 34 should not be connected externally and should not have any traces, planes, or vias under it.

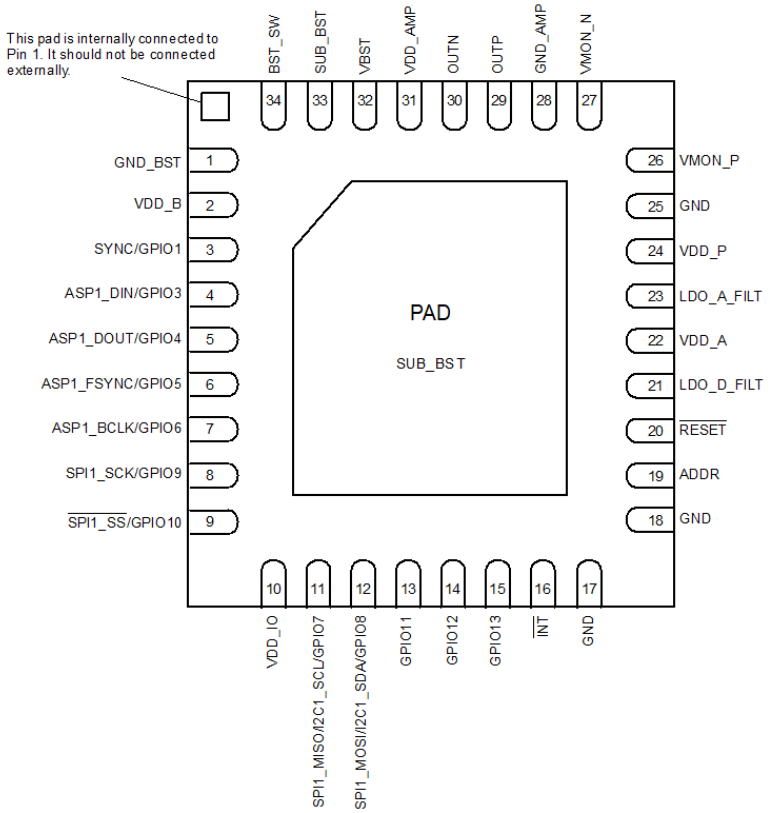



**Figure 1 Pinout Diagram**

## 2 CS40L5x Schematic Guidelines

This section describes the different connection configurations that are supported by the CS40L5x device. It covers the different power supply configurations, data and control interfaces, and output and monitoring connections.

There are two typical connections for the CS40L5x device: *internal boost configuration* or *external amplifier supply configuration*. These two configurations are related to the high-power supply connections as described in the High-Current Supply Connections section.

The typical connections for CS40L5x in *internal boost configuration* are shown in the following figure. The optional configurations and allowed selections are provided with their respective notation.

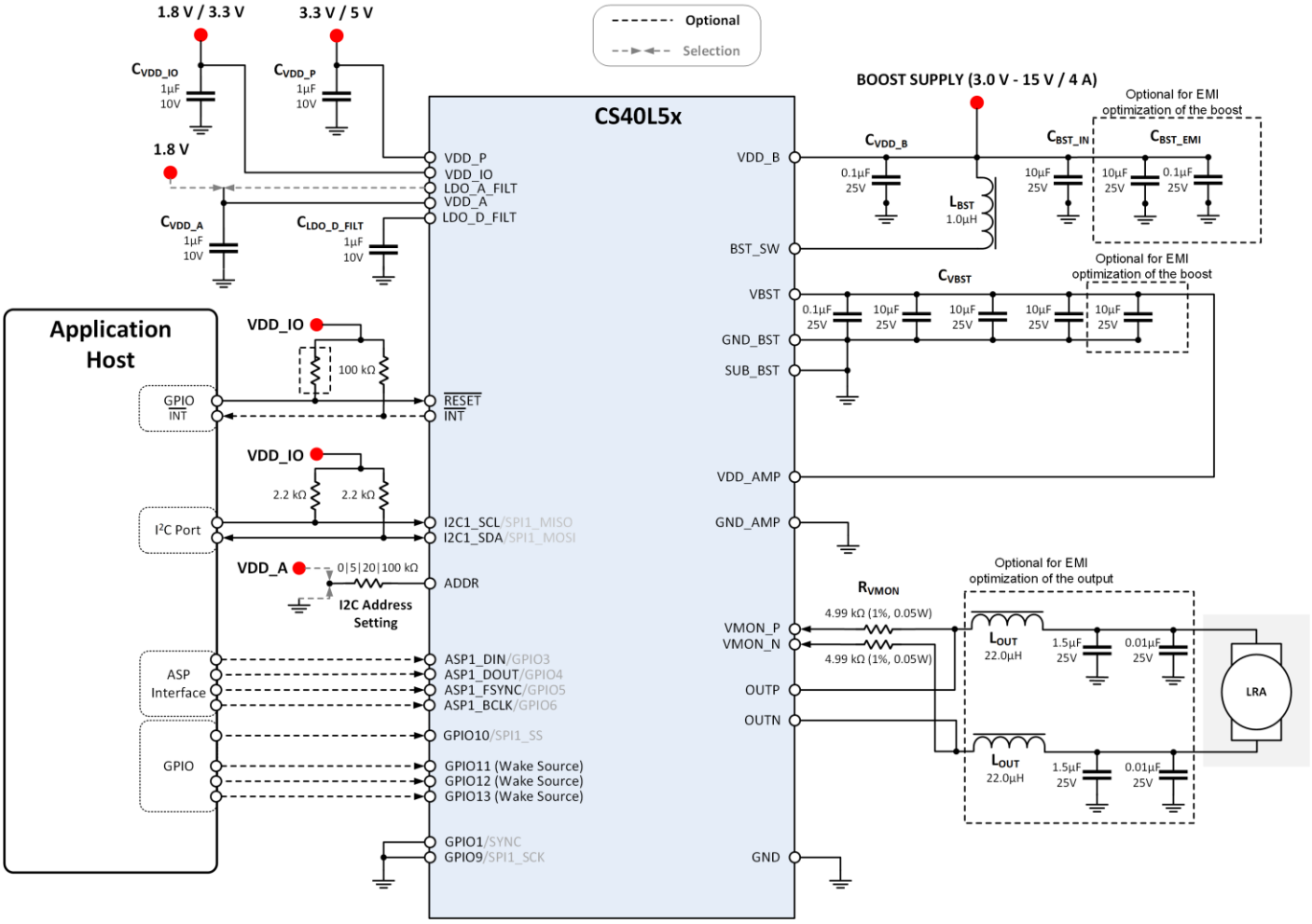



**Figure 2 CS40L5x Typical Connection Diagram - Internal Boost**

The typical connections for CS40L5x in *external amplifier supply configuration* are shown in the following figure. The optional configurations and allowed selections are provided with their respective notation.

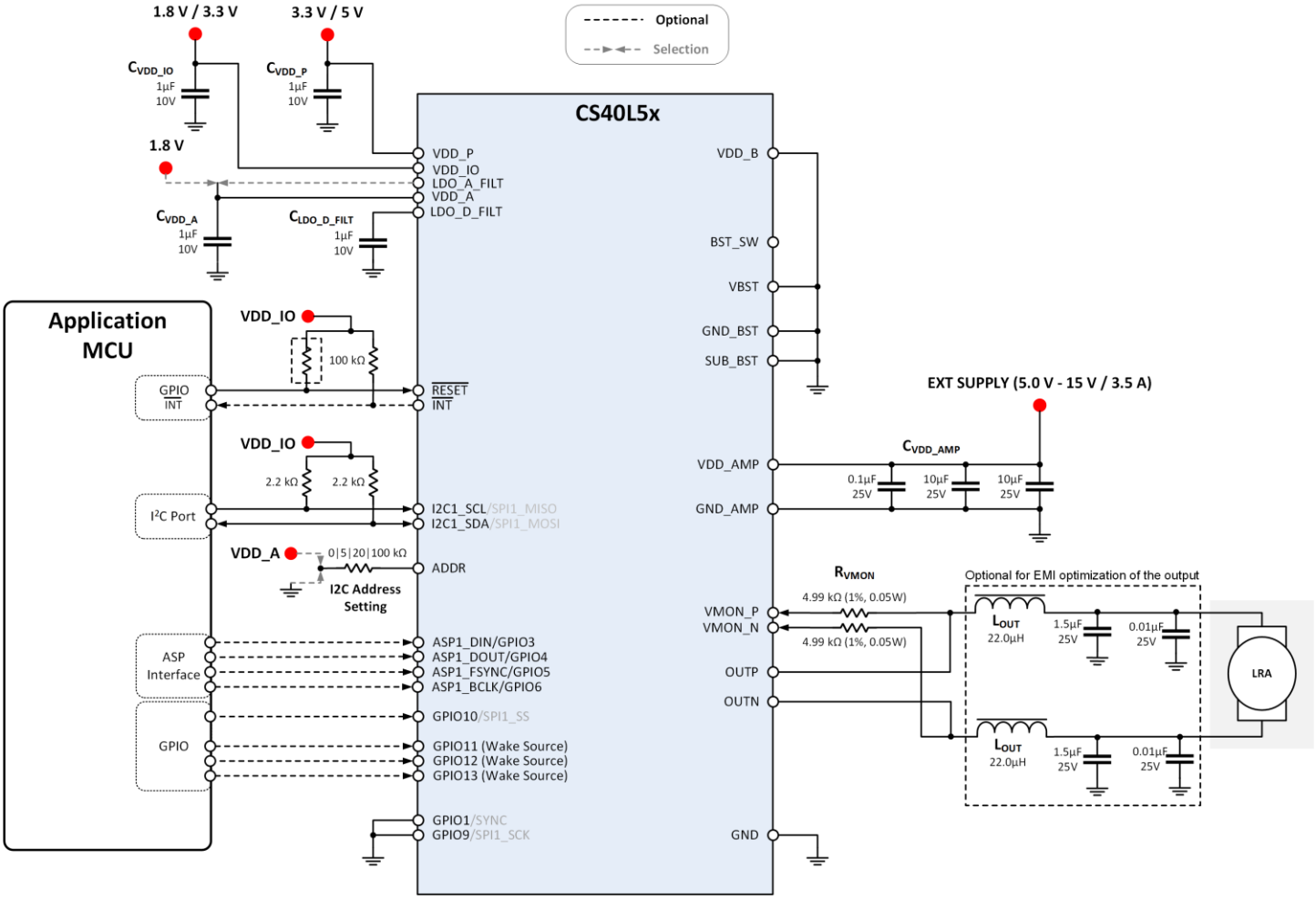



**Figure 3 CS40L5x Typical Connection Diagram - External Amplifier Supply**

## 2.1 Recommended External Components

Cirrus Logic recommends the following external components for use with the CS40L5x device.

The recommended external components for CS40L5x in *internal boost configuration* are provided in the following table.

**Table 1 Recommended External Components - Internal Boost**

| Component | Value | Quantity | Manufacturer | Part Number | Dimension (mm) | | | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | | L | W | H | |
| $C_{VDD\_P}$ | 1 µF | x1 | Taiyo Yuden | LMK105BJ105MVHF | 1.0 | 0.50 | 0.55 | Rated Voltage: 10 V, Temperature Characteristics: X5R |
| $C_{VDD\_IO}$ | 1 µF | x1 | Taiyo Yuden | LMK105BJ105MVHF | 1.0 | 0.50 | 0.55 | Rated Voltage: 10 V, Temperature Characteristics: X5R |
| $C_{VDD\_A}$ | 1 µf | x1 | Taiyo Yuden | LMK105BJ105MVHF | 1.0 | 0.50 | 0.55 | Rated Voltage: 10 V, Temperature Characteristics: X5R |
| $C_{LDO\_D\_FILT}$ | 1 µF | x1 | Taiyo Yuden | LMK105BJ105MVHF | 1.0 | 0.50 | 0.55 | Rated Voltage: 10 V, Temperature Characteristics: X5R |
| $C_{VDD\_B}$ | 0.1 µF | x1 | Samsung | CL05B104KO5VPNC | 0.6 | 0.30 | 0.3 | Rated Voltage: 25 V, Temperature Characteristics: X5R |
| $C_{BST\_IN}$ | 10 µF | x1 | Taiyo Yuden | EMK212BBJ106KGHT | 2.0 | 1.25 | 1.35 | Rated Voltage: 16 V, Temperature Characteristics: X5R |
| $L_{BST}$ | 1 µH | x1 | Murata | LQH44PH1R0MPRL | 4.0 | 4.0 | 1.8 | Rated DC Current: 3.2 A ($I_{rms}$) / 4.3 A ($I_{sat}$), DC resistance: 30 mΩ (max) |
| $C_{VBST}$ | 10 µF | x3 | Murata | EMK212BBJ106KGHT | 2.0 | 1.25 | 1.35 | Rated Voltage: 16 V, Temperature Characteristics: X5R |
| $C_{VBST}$ | 0.1 µF | x1 | Samsung | CL05B104KO5VPNC | 1.0 | 0.50 | 0.55 | Rated Voltage: 16 V, Temperature Characteristics: X7R |
| $R_{VMON}$ | 4.99 kΩ | x2 | Vishay Dale | CRCW04024K99FKED | 1.0 | 0.50 | 0.40 | Rated Power: 1/16 W, Tolerance: 1% |

The recommended external components for CS40L5x in *external amplifier supply configuration* are provided in the following table.

**Table 2 Recommended External Components - External Amplifier Supply**

| Component | Value | Quantity | Manufacturer | Part Number | Dimension (mm) | | | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | | L | W | H | |
| $C_{VDD\_P}$ | 1 µF | x1 | Taiyo Yuden | LMK105BJ105MVHF | 1.0 | 0.5 | 0.55 | Rated Voltage: 10 V, Temperature Characteristics: X5R |
| $C_{VDD\_IO}$ | 1 µF | x1 | Taiyo Yuden | LMK105BJ105MVHF | 1.0 | 0.5 | 0.55 | Rated Voltage: 10 V, Temperature Characteristics: X5R |
| $C_{VDD\_A}$ | 1 µf | x1 | Taiyo Yuden | LMK105BJ105MVHF | 1.0 | 0.5 | 0.55 | Rated Voltage: 10 V, Temperature Characteristics: X5R |
| $C_{LDO\_D\_FILT}$ | 1 µF | x1 | Taiyo Yuden | LMK105BJ105MVHF | 1.0 | 0.5 | 0.55 | Rated Voltage: 10 V, Temperature Characteristics: X5R |
| $C_{VDD\_AMP}$ | 0.1 µF | x1 | Samsung | CL05B104KO5VPNC | 1.0 | 0.5 | 0.55 | Rated Voltage: 16 V, Temperature Characteristics: X7R |
| $C_{VDD\_AMP}$ | 10 µF | x2 | Taiyo Yuden | EMK212BBJ106KGHT | 2.0 | 1.25 | 1.35 | Rated Voltage: 16 V, Temperature Characteristics: X5R |
| $R_{VMON}$ | 4.99 kΩ | x2 | Vishay Dale | CRCW04024K99FKED | 1.0 | 0.50 | 0.40 | Rated Power: 1/16 W, Tolerance: 1% |

## 2.2 Power Supply Connections

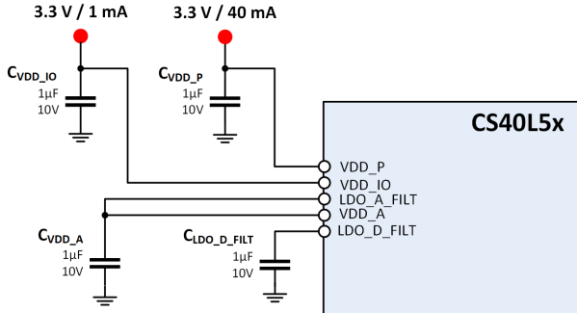
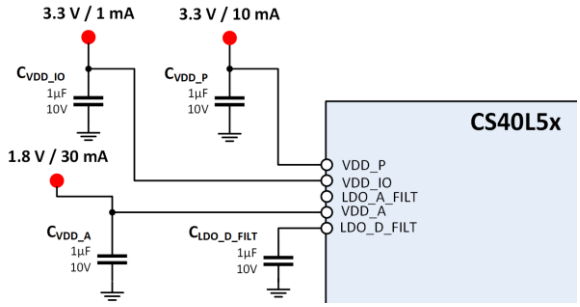
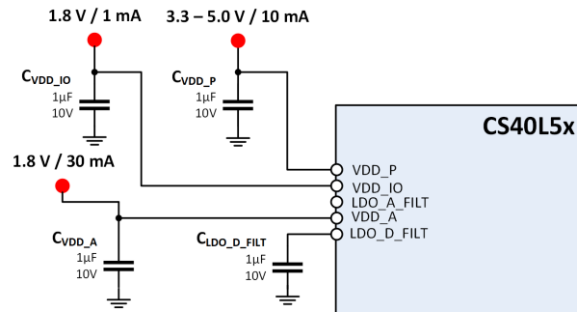
CS40L5x requires connections to one or two low-current supplies and one high-current supply. The low-current supplies are required for the system supply (VDD_P), digital input/output (VDD_IO), and analog (VDD_A) domains as described in the Low-Current Supply Connections section. The high-current supply is required for the boost converter and/or amplifier as described in the High-Current Supply Connections section.

### 2.2.1 Low-Current Supply Connections

CS40L5x requires one or two low-current supplies for the system supply (VDD_P), digital input/output (VDD_IO), and analog (VDD_A) domains. Three different configurations for the low-current supply connections provide support for different system topologies.

The system designer should select a power configuration from the table below, and verify the voltage and current requirements in the target application.

**Table 3 Low-Current Supply Requirements**

| Configuration | Power Supply Rail | Voltage | Maximum Current |
|---|---|---|---|
| **Single Supply, 3.3 V IOs**<br>  | **VDD_P** | 3.3 V (*typ*)<br>3.0 - 5.5 V | 40 mA |
| | **VDD_IO** | 3.3 V (*typ*)<br>1.71 - 3.6 V | 1 mA |
| | **VDD_A** | (Internal) | (Internal) |
| **Dual Supply, 3.3 V IOs**<br>  | **VDD_P** | 3.3 V (*typ*)<br>3.0 - 5.5 V | 10 mA |
| | **VDD_IO** | 3.3 V (*typ*)<br>1.71 - 3.6 V | 1 mA |
| | **VDD_A** | 1.8 V (*typ*)<br>1.71 - 1.89 V | 30 mA |
| **Dual Supply, 1.8 V IOs**<br>  | **VDD_P** | 3.3 V or 5.0 V (*typ*)<br>3.0 - 5.5 V | 10 mA |
| | **VDD_IO** | 1.8 V (*typ*)<br>1.71 - 3.6 V | 1 mA |
| | **VDD_A** | 1.8 V (*typ*)<br>1.71 - 1.89 V | 30 mA |
| **Note:** The maximum current shown represents typical test conditions. | | | |

The required decoupling capacitance on each low-power supply rail is 1 µF (typical), as described in the table below. Refer to the Recommended External Components section for part number recommendations.

**Table 4 Low-Current Supply Components**

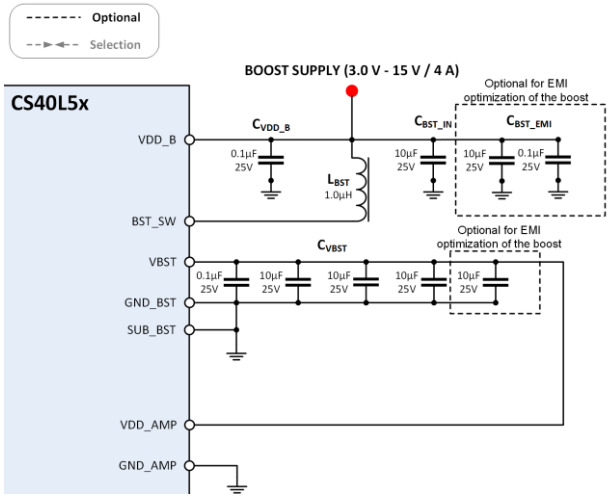
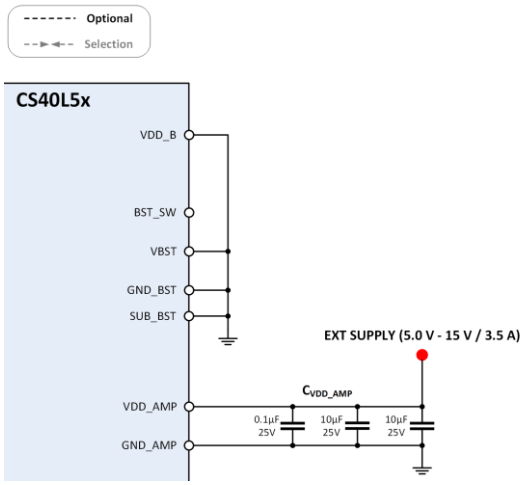
| Component | Min | Typ | Max | Units |
|---|---|---|---|---|
| $C_{VDD\_P}$ Decoupling Capacitance | — | 1.0 | — | µF |
| $C_{VDD\_IO}$ Decoupling Capacitance | — | 1.0 | — | µF |
| $C_{VDD\_A}$ Decoupling Capacitance | — | 1.0 | — | µF |
| $C_{LDO\_A\_FILT}$ Decoupling Capacitance at 1.8V | 0.50 | 1.0 | — | µF |
| $C_{LDO\_D\_FILT}$ Decoupling Capacitance at 1.25 V | 0.39 | 1.0 | — | µF |

## 2.2.2 High-Current Supply Connections

CS40L5x requires a high-current supply for the boost converter and/or amplifier. There are two possible configurations for the high-current supply, supporting different system topologies: *internal boost* and *external amplifier supply*.

The system designer should select a power configuration from table below, and verify the voltage and current requirements in the target application.

**Table 5 High-Current Supply Requirements**

| Configuration | Power Supply Rail | Voltage | Maximum Current |
|---|---|---|---|
| **Internal Boost** | **VDD_B** | 3.0 - 15 V | 20 mA |
|  | **BST_SW** | 3.0 - 15 V | 4 A |
| **External Amplifier Supply** | **VDD_AMP** | 5.0 - 15 V | 3.5 A |
|  | | | |

**Note:** The maximum current shown represents typical test conditions.

The component requirements for each configuration are described in the tables below. Refer to the Recommended External Components section for part number recommendations.

Note the CS40L5x boost converter requires a combined de-rated capacitance no less than 2 µF at 15 V from multiple capacitors ($C_{VBST}$). The $L_{BST}$ inductor must not de-rate to less than 0.5 µH during device operation in order to maintain proper loop stability. A $L_{BST}$ boost inductance of 1.0 µH is recommended.

**Table 6 High-Current Supply Components - Internal Boost Configuration**

| Component | Min | Typ | Max | Units |
|---|---|---|---|---|
| $C_{VBST}$ Decoupling Capacitance at 15V | 2 | — | — | µF |
| $L_{BST}$ Inductance | — | 1.0 | — | µH |
| Min $L_{BST}$ at peak inductor current | 0.5 | — | — | µH |

For the external amplifier supply configuration, the total $C_{VDD\_AMP}$ decoupling capacitance must not de-rate less than 2 µF at 15 V. Refer to the Recommended External Components section for part number recommendations.

**Table 7 High-Current Supply Components - External Amplifier Supply Configuration**

| Component | Min | Typ | Max | Units |
|---|---|---|---|---|
| $C_{VDD\_AMP}$ Decoupling Capacitance at 15V | 2 | — | — | µF |

### 2.2.3 Ground Connections

The following pins must be connected to ground in all configurations. Note that other pins may also be connected to ground, depending on the applicable power configuration - see High-Current Supply Connections. See also GPIO Connections for the required connection for unused GPIOs.

**Table 8 Ground Pins Summary**

| Pin Name | Pin Number | Description |
|---|---|---|
| GND | 17, 18, 25 | Low-power analog and digital ground return |
| PAD | PAD | Thermal pad ground |
| SUB_BST | 33 | Boost substrate ground |
| GND_BST | 1 | Boost converter ground reference |
| GND_AMP | 28 | Class D amplifier ground reference |
| GPIO1 / SYNC | 3 | Unused GPIO (see GPIO Connections) |
| GPIO9 / SPI1_SCK | 8 | Unused GPIO (see GPIO Connections) |

## 2.3 Control and Data Connections

The CS40L5x provides a hardware reset pin to turn the device on/off and an I²C interface (control port) to read and write the control registers. Furthermore, four pins are set as GPIs by default and four pins are set as an ASP interface by default (these pins can be reconfigured for GPI trigger purposes). One optional interrupt pin is provided for event notifications to a host. This section describes the requirements for these connections.

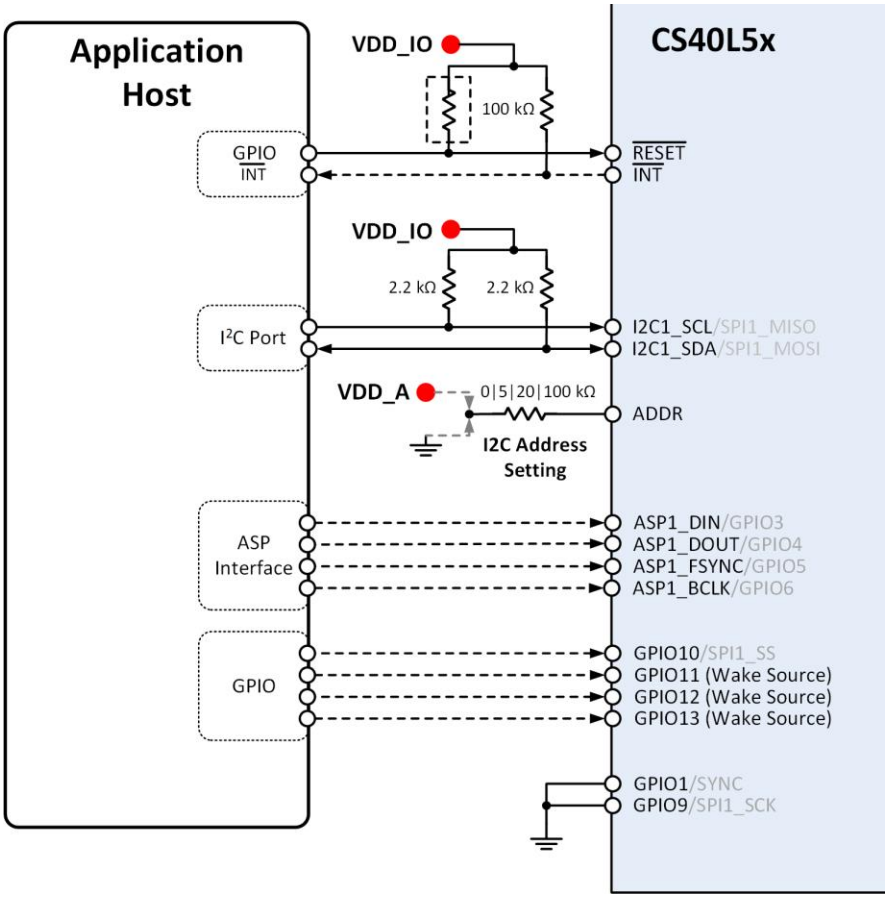



**Figure 4 CS40L5x Control and Data Connections Diagram**

### 2.3.1 Reset Connection

The hardware reset pin (RESET) allows turning on and off the CS40L5x device. This pin is connected to a host GPO output pin in a system. An external pull-up resistor to VDD_IO is only required if the host GPO is unable to drive it at all times while CS40L5x has power applied to it. The RESET pin is referenced to VDD_IO logic levels, but is also 5 V tolerant.

### 2.3.2 I²C Interface Connection

The CS40L5x control port uses an I²C interface to allow reading and writing to the device. The I²C interface is supported using the I2C1_SCL and I2C1_SDA pins; these pins use logic levels referenced to the VDD_IO supply. The CS40L5x is a target device on the I²C bus in a system. The I²C device address is configured using the ADDR pin which allows eight possible addresses.

#### 2.3.2.1 I²C Pull-Up Resistors

The I²C interface requires pull-up resistor to the VDD_IO supply. The pull-up resistor value is determined by the bus capacitance and the minimum drive strength of ICs on the I²C bus. Cirrus Logic recommends I²C pull-up resistors between 2.2 kΩ and 10 kΩ.

**Table 9 Recommended I2C Pull-Up Resistors**

| Component | Min | Typ | Max | Units |
|---|---|---|---|---|
| I²C pull-up resistors | — | 2.2 to 10 | — | kΩ |

#### 2.3.2.2 I²C Device Address

The CS40L5x supports eight I²C device address options; these are selected by connecting ADDR pin to GND or VDD_A through a 0 Ω, 5 kΩ, 20 kΩ, or 100 kΩ resistor as shown in the table below. The external resistance must be within 5% of the specified value.

Note that, in the table below, the specified I²C target device address is an 8-bit value, the LSB contains the R/W bit, e.g., Write address 0x60, Read address 0x61.

**Table 10 I2C Device Address Selection**

| External Resistance | Connection Type | I²C Target Device Address | |
|---|---|---|---|
| | | Write | Read |
| 0 Ω | Pull-Down to GND | 0x60 | 0x61 |
| | Pull-Up to VDD_A | 0x62 | 0x63 |
| 5 kΩ | Pull-Down to GND | 0x64 | 0x65 |
| | Pull-Up to VDD_A | 0x66 | 0x67 |
| 20 kΩ | Pull-Down to GND | 0x68 | 0x69 |
| | Pull-Up to VDD_A | 0x6A | 0x6B |
| 100 kΩ | Pull-Down to GND | 0x6C | 0x6D |
| | Pull-Up to VDD_A | 0x6E | 0x6F |

### 2.3.3 ASP Interface Connection

The CS40L5x has four pins configured for the ASP interface by default. These pins can be configured as GPIO pins if needed.

**Table 11 ASP Interface (GPIO) Pins Summary**

| Pin Name | Pin Number | Default State | System Connection | Unused Connection |
|---|---|---|---|---|
| ASP1_DIN/GPIO3 | 4 | Input, passive pull down | Connect to host GPO output pin (VDD_IO level) * | Not connected or connect to GND # |
| ASP1_DOUT/GPIO4 | 5 | Output, passive pull down | Connect to host GPO output pin (VDD_IO level) * | Not connected or connect to GND # |
| ASP1_FSYNC/GPIO5 | 6 | Input, passive pull down | Connect to host GPO output pin (VDD_IO level) * | Not connected or connect to GND # |
| ASP1_BCLK/GPIO6 | 7 | Input, passive pull down | Connect to host GPO output pin (VDD_IO level) * | Not connected or connect to GND # |

**Notes:**

* Non-wake up GPI trigger - Cannot wake device up from hibernate state

# A test point is recommended to enable ASP interface for tuning and debugging purposes

### 2.3.4 GPIO Connections

The CS40L5x has four default GPIs available to trigger haptic effects based on their rising / falling edge. These pins are connected to host GPO output pins at VDD_IO level for operation in a system. If these pins are not used, the "Unused Connection" recommendation must be followed.

**Table 12 GPIO Pins Summary**

| Pin Name | Pin Number | Default State | System Connection | Unused Connection |
|---|---|---|---|---|
| SPI1_SS/GPIO10 | 9 | Input, Hi-Z | Connect to host GPO output pin (VDD_IO level) * | Connect to VDD_IO |
| GPIO11 | 13 | Input, Hi-Z | Connect to host GPO output pin (VDD_IO level) ^ | Connect to GND |
| GPIO12 | 14 | Input, Hi-Z | Connect to host GPO output pin (VDD_IO level) ^ | Connect to GND |
| GPIO13 | 15 | Input, Hi-Z | Connect to host GPO output pin (VDD_IO level) ^ | Connect to GND |

**Notes:**

* Non-wake up GPI trigger - Cannot wake device up from hibernate state

^ Wake up GPI trigger - Can wake device up from hibernate state

### 2.3.5 Interrupt Connection

The CS40L5x provides an interrupt pin (INT) for event notifications to a host. This GPO pin is an open-drain output, and an external pull-up resistor is required. The INT pin is connected to a host GPI interrupt input pin at VDD_IO level for operation in a system.

**Table 13 Interrupt Pin Requirement**

| Pin Name | Pin Number | System Connection | Unused Connection |
|---|---|---|---|
| INT | 16 | Connect to host GPI interrupt input pin (VDD_IO level)<br>Connect to a 100 kΩ pull-up resistor to VDD_IO | Connect to a 100 kΩ pull-up resistor to VDD_IO |

## 2.4 Output and Monitoring Connections

The CS40L5x provides a high-performance Class D differential output for a direct connection to a haptic actuator. The CS40L5x contains dedicated voltage-monitor pins to track the voltage across the haptic actuator input.

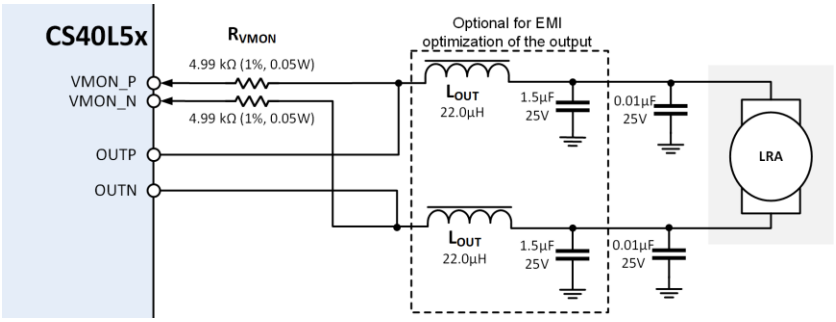



**Figure 5 CS40L5x Output and Monitoring Connections Diagram**

### 2.4.1 Output Connections

The CS40L5x output pins, OUTP and OUTN, are connected to Linear Resonant Actuator (LRA) or Voice Coil Motor (VCM) with an impedance as low as 4 Ω and a resonant frequency in the 50 Hz - 561 Hz range.

**Table 14 Haptic Output Characteristics - Supported Actuators**

| | Min | Typ | Max | Units |
|---|---|---|---|---|
| Load Resistance | 4 | 8 | — | Ω |
| Resonant Frequency | 50 | — | 561 | Hz |

### 2.4.2 Monitoring Connections

The CS40L5x voltage monitor pins, VMON_P and VMON_N, must be connected with series resistors to OUTP and OUTN respectively; these connections should be as close as possible to the haptic actuator (LRA/VCM). Both resistors must be 4.99 kΩ, 1/20 W power rating and 1% tolerance for optimal performance.

**Table 15 Monitoring Resistors**

| Component | Min | Typ | Max | Units |
|---|---|---|---|---|
| $R_{VMON}$ series resistors | — | 4.99 | — | kΩ |

## 2.5 EMI Filtering

Depending on the application, additional filters may be used to suppress EMI. These optional filters can be added on the input supply and to the output signals.

### 2.5.1 Input Supply Filter

A filter may be added to the input supply to provide additional EMI optimization.

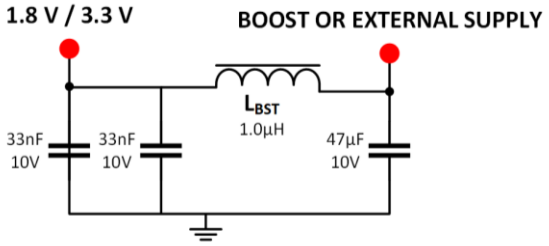



**Figure 6 Input Supply Filter Schematic**

### 2.5.2 Boost Supply Filter

For the internal-boost supply configuration, a filter can be added for EMI optimization.

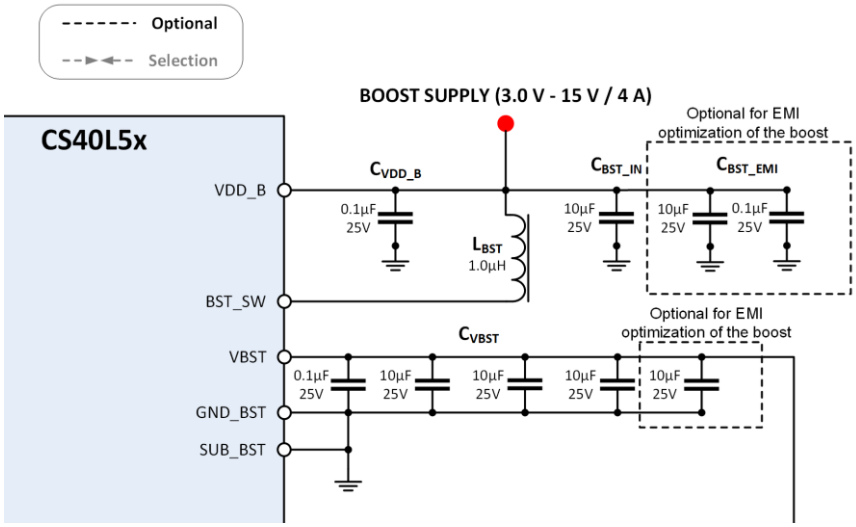



**Figure 7 Boost Supply Filter Schematic**

### 2.5.3 Output EMI Filter

The Class D amplifier switching causes radiated emissions on the output lines. The output connections can be optimized for EMI using an L-C filter circuit to reduce the switching noise. The optional filter circuit is shown below.

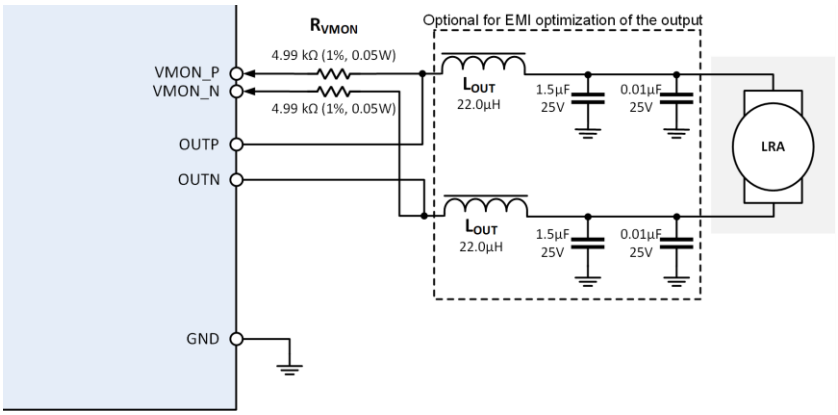



**Figure 8 Output Filter Schematic**

# 3 CS40L5x Layout Guidelines

This section describes the recommended routing for power supplies, data and control signals, and output and monitoring signals from a CS40L5x device. Component placement guidelines for the external BOM are also provided.

The following generic board layout guidelines are recommended.

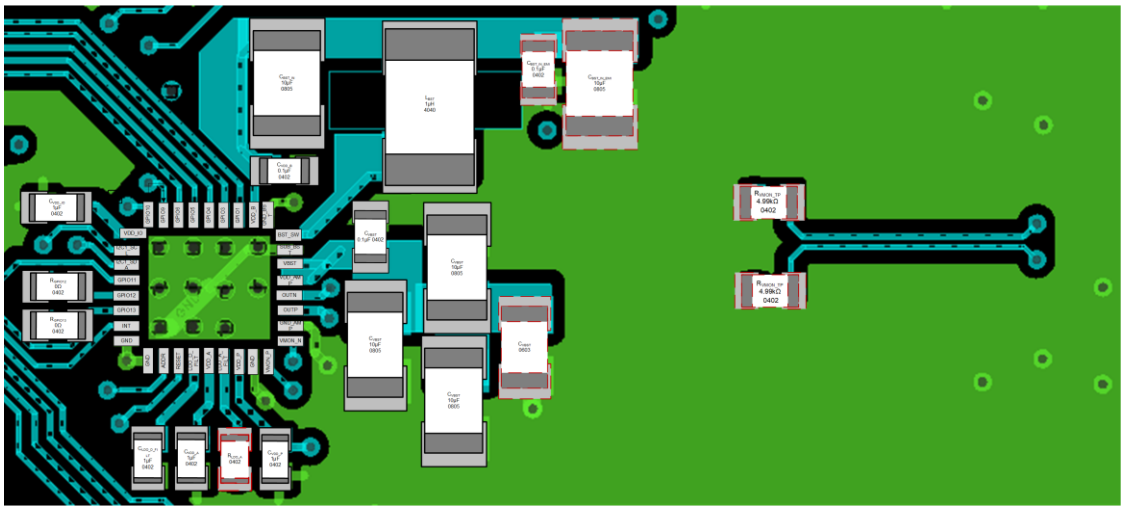
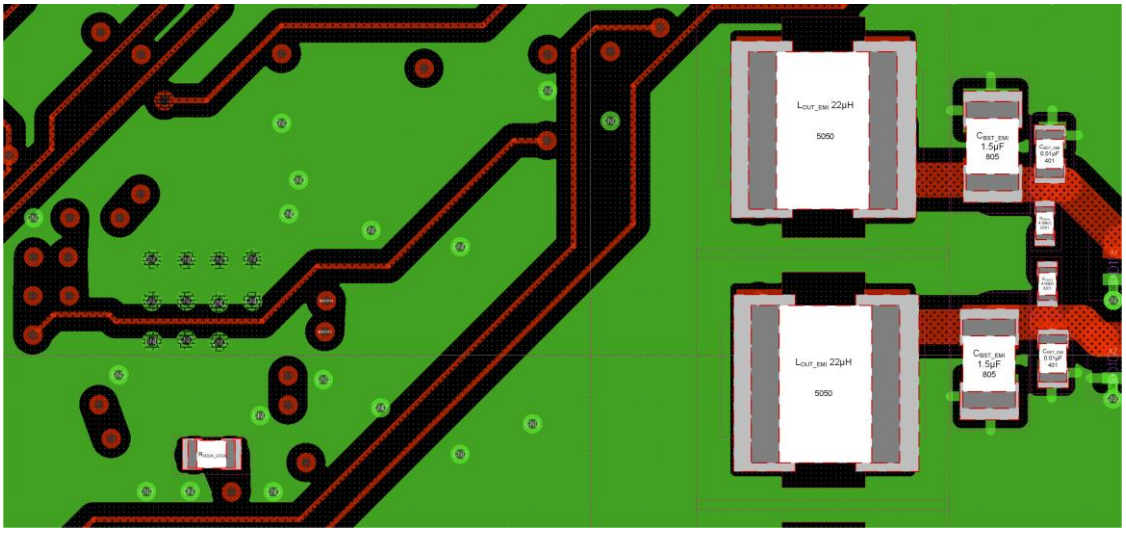
1. Four-layer PCB with the following stack up:
   – Layer 1 (top): Component placement and signal routing
   – Layer 2: Reference ground plane
   – Layer 3: Power planes
   – Layer 4 (bottom): Signal routing
2. Avoid routing digital signals between power planes on an adjacent layer
   – If signals have to cross on adjacent layers, it is recommended they should cross perpendicular in order to prevent coupling
3. Use controlled 50 Ω characteristic impedance for all digital signals
4. Avoid routing analog and digital signals next to each other

More layers may be required for a particular system. This would not impact the device as long as the recommendations above are followed. The second layer must be the reference ground plane.

## 3.1 Recommended Component Placement

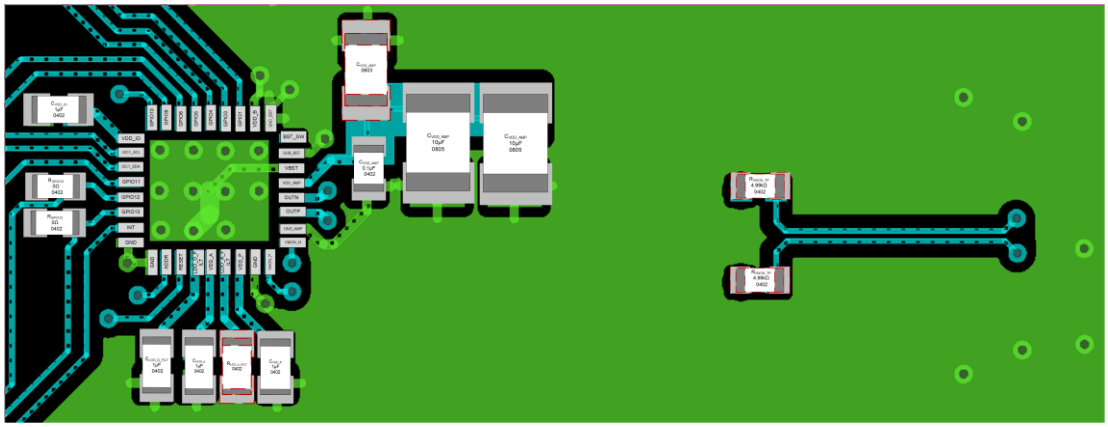
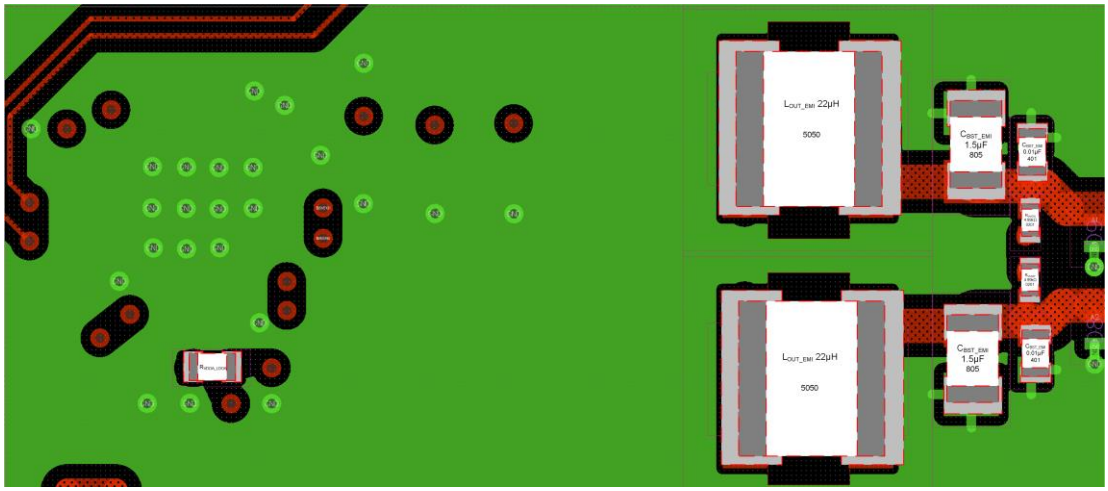
The recommended component placement for CS40L5x in *internal boost configuration* is shown in the following figure. Optional components are shown in red, dashed outlines.

**Table 16 Recommended Component Placement - Internal Boost**

| | |
|---|---|
| **Top Layer** |  |
| **Bottom Layer** |  |

The recommended component placement for CS40L5x in *external amplifier supply configuration* is shown in the following figure. Note this example shows the $R_{VMON}$ resistors on the bottom layer, but they can equally be placed on the top layer.

**Table 17 Recommended Component Placement - External Amplifier Supply**

| | |
|---|---|
| **Top Layer** |  |
| **Bottom Layer** |  |

## 3.2 Power Supply Routing

The routing and component placement for low-power supplies (VDD_P, VDD_IO, VDD_A) are described in the Low-Current Supply Routing section. The high-power supply routing and component placement guidelines are described in the High-Current Supply Routing section.

### 3.2.1 Low-Current Supply Routing

The following routing and component-placement guidelines are recommended for the low-current supplies (VDD_P, VDD_IO, VDD_A). The same guidelines are also applicable for the LDO_A FILT and LDO_D FILT pins.

1. Place decoupling capacitors on the same PCB side as the CS40L5x device, e.g. top layer.
2. Place decoupling capacitors as close as possible to the corresponding pin.
3. Use low-current power traces to the system power supply (1 mA - 40 mA) or a via to the corresponding power plane. Refer to the Low-Current Supply Connections section for maximum current consumption in each rail.
4. Add a via to reference ground plane close to each capacitor's ground pad.

A typical layout for the low-current supply components is shown in the figure below. Note that some vias are located within the pads of the passive components.

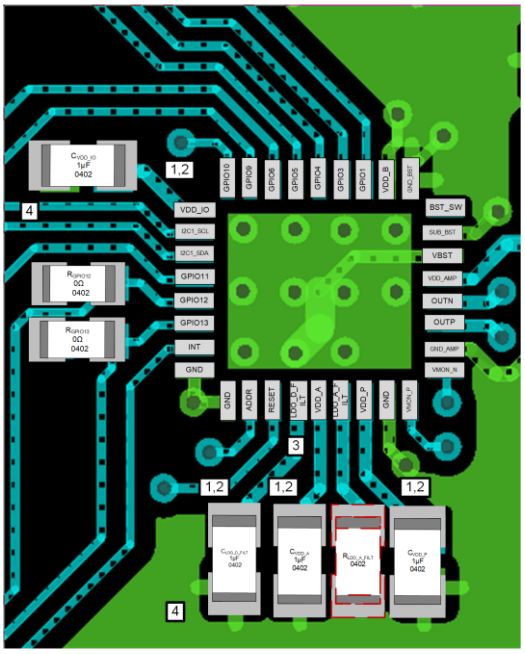



**Figure 9 Low-Current Supply Routing and Component Placement**

### 3.2.2 High-Current Supply Routing

#### 3.2.2.1 Internal Boost Configuration

If the CS40L5x is used in the *internal boost* configuration, the following routing and component placement guidelines are recommended for the high-power supplies (BST_SW, VBST, VDD_AMP, and VDD_B) and ground return paths (GND_BST and GND_AMP).

1. Place all the components on the same PCB side as the CS40L5x device (e.g. top layer).
2. Place **$L_{BST}$** inductor as close as possible to the BST_SW pin.
3. Use a very short and wide trace to connect inductor to BST_SW pin (4 A - high current path).
4. Place **$C_{VDD\_B}$** decoupling capacitor (0.1uF) as close as possible to VDD_B and GND_BST pins.
5. Add a via to reference ground plane close to **$C_{VDD\_B}$** capacitor's ground pad.
6. Place **$C_{BST\_IN}$** decoupling capacitor (10uF) as close as possible to inductor and GND_BST pin.
7. Add a via to reference ground plane close to **$C_{BST\_IN}$** capacitor's ground pad.
8. Use a short but wide local ground plane to connect GND_BST pin to **$C_{VDD\_B}$** and **$C_{BST\_IN}$** capacitors.
9. Place at least two vias to reference ground plane as close as possible to GND_BST pin. This is a high current ground return path for VBST (4 A).
   The distance between these vias and the **$C_{VBST}$** capacitors' ground vias must be minimized - See point 15 below.
10. Use a low-current trace (20 mA) to connect VDD_B to **$C_{VDD\_B}$** decoupling capacitor and power source.
11. Connect **$L_{BST}$** inductor to power source with a wide trace or plane (4 A - high current path). Use at least 4 vias if connecting to a power plane in a different layer.For optimum performance, the DC resistance of the trace or plane from the power source to the inductor should be as low as possible (20 mΩ).
12. Connect VBST and VDD_AMP together at the pins (3 A - high current path).
13. Place **$C_{VBST}$** decoupling capacitors as close as possible to VBST and VDD_AMP pins where:
    a. 0.1uF capacitor is the closest to VBST and GND_BST pins.
    b. One 10uF capacitor is close to VDD_AMP and GND_AMP.
14. Use a small local ground plane to connect **$C_{VBST}$** capacitors' ground pads.
15. Place two vias to reference ground plane close to the 0.1uF **$C_{VBST}$** capacitor's ground pad.
    The distance between these vias and the GND_BST pin's vias must be minimized - See point 9 above.
16. Add a via to reference ground plane close to each **$C_{VBST}$** capacitor’s ground pad.
17. Place one via close to GND_AMP pin to connect to reference ground plane.

A typical layout for the high-current supply components is shown in the figure below. Note that some vias are underneath the pads of the components.

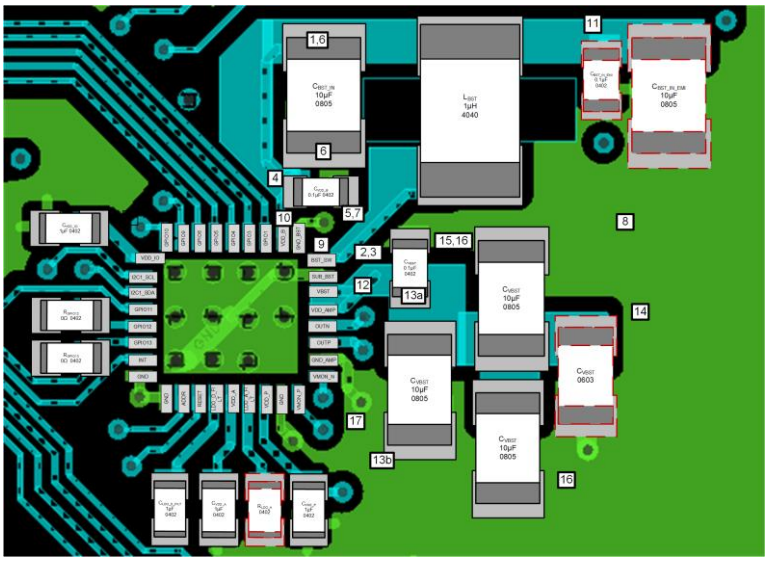



**Figure 10 High-Current Supply Routing and Component Placement - Internal Boost**

### 3.2.2.2 External Amplifier Supply Configuration

If the CS40L5x is used in the *external amplifier supply* configuration, the following routing and component placement guidelines are recommended for the high-power supply (VDD_AMP) and ground return path (GND_AMP). Guidelines are also provided for the unused pins (BST_SW, VBST, VDD_B, and GND_BST).

1. Place the **$C_{VDD\_AMP}$** decoupling capacitors on the same PCB side as the CS40L5x device, e.g. top layer.
2. Place the **$C_{VDD\_AMP}$** decoupling capacitors as close as possible to the VDD_AMP and GND_AMP pins. The 0.1uF capacitor should be closest to VDD_AMP and GND_AMP pins.
3. Connect VDD_AMP with a wide trace or plane to external connector or power source (3.5 A - high current path). Use at least three vias if connecting to a power plane in a different layer.
4. Connect GND_AMP with a wide trace to external connector or power source ground (3.5 A - high current path). Use at least three vias if connecting to a plane in a different layer.
5. Place one or two vias close to GND_AMP pin to connect to reference ground plane.
6. Add a via to reference ground plane close to each capacitor's ground pad.
7. Connect VBST and SUB_BST together at the pins.
8. Connect VDD_B and GND_BST to reference ground plane.

A typical layout for the high-current supply components is shown in the figure below.

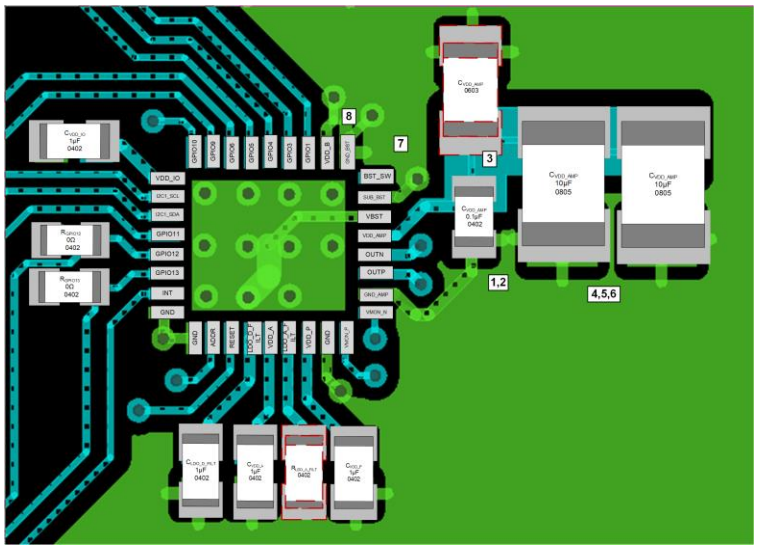



**Figure 11 High-Current Supply Routing and Component Placement - External VDD_AMP**

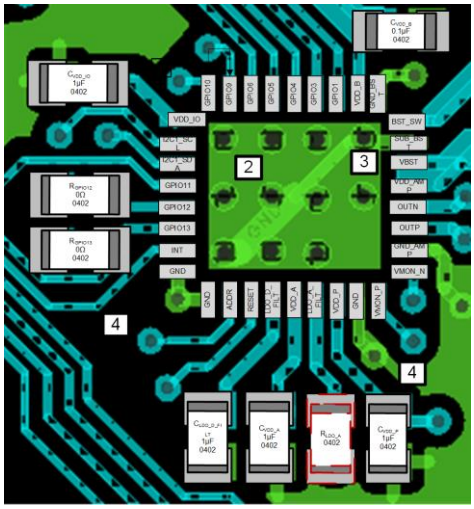
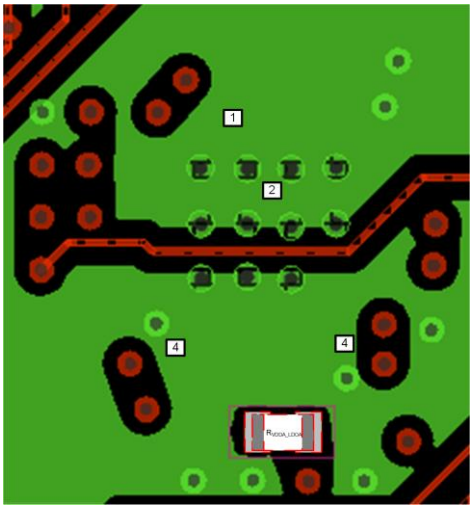
### 3.2.3 Ground Routing

The following routing and placement guidelines are recommended for a good ground reference for a CS40L5x device.

1. Use a solid reference ground plane on the layer underneath the device, e.g. CS40L5x is placed on layer 1 and solid ground plane is on layer 2.
2. Place 12 thermal vias on the thermal ground pad to reference ground plane.
3. Connect SUB_BST pin to the thermal ground pad directly on the same layer.
4. Place a via close to each ground pin (pins 17, 18, 25) to connect the low-power analog and digital grounds to reference ground plane.

A typical layout for the ground routing is shown in the figure below.

**Table 18 Ground Routing**

| Layer 1 (Top) | Layer 2 (Solid Ground) |
|---|---|
|  |  |

## 3.3 Control and Data Routing

### 3.3.1 Reset Routing

The RESET trace must be routed following standard layout practices for digital switching signals.

1. Use controlled 50 Ω characteristic impedance if possible.
2. Avoid routing the RESET trace between power planes on an adjacent layer. If signals have to cross on adjacent layers, it is recommended they should cross perpendicular in order to prevent coupling.
3. Avoid routing the RESET trace next to analog or digital switching signals.

A typical layout for the RESET pin routing is shown in the figure below.

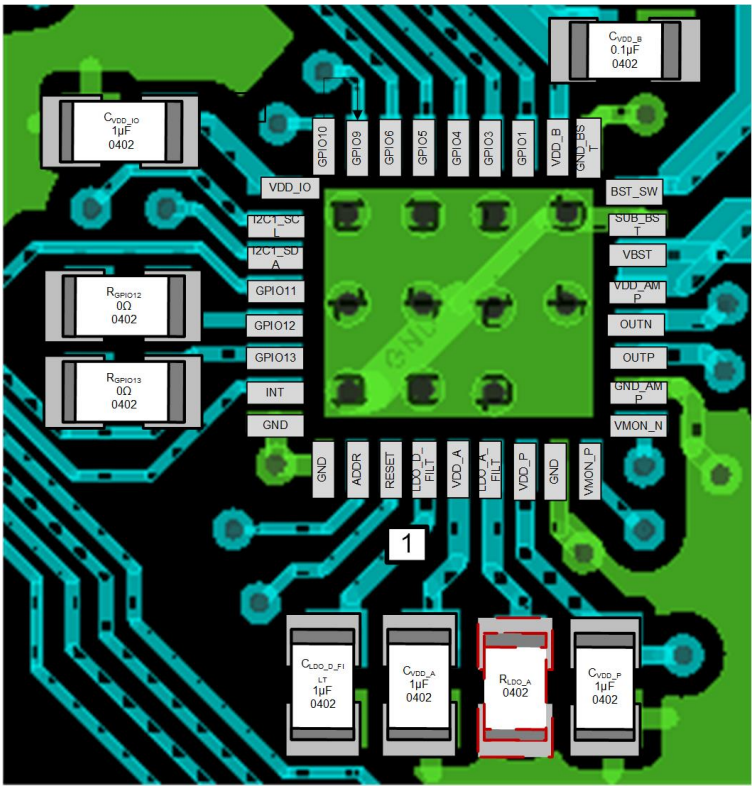



**Figure 12 Reset Signal Routing**

### 3.3.2 I²C Interface Routing

The I²C signals, I2C1_SCL and I2C1_SDA, must be routed following standard layout practices for digital switching signals.

1. Route the I2C1_SCL and I2C1_SDA traces as a pair over a reference ground plane. Each trace should have equal length to the signal source.
2. Use controlled 50 Ω characteristic impedance if possible.
3. Isolate the I2C1_SCL and I2C_SDA traces with ground planes if electrical noise sources are nearby.
4. Avoid routing the I²C traces between power planes on an adjacent layer. If signals have to cross on adjacent layers, it is recommended they should cross perpendicular in order to prevent coupling.
5. Avoid routing the I²C traces next to analog and other digital signals.
6. Place the ADDR pull up/down resistor close to the CS40L5x device.

A typical layout for the I²C signal routing is shown in the figure below.

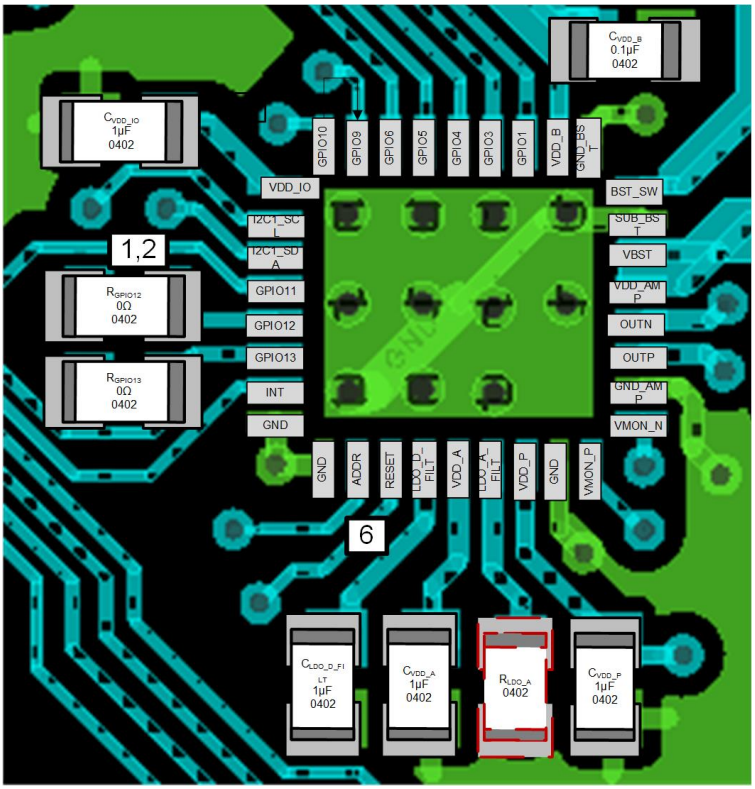



**Figure 13 I2C Signal Routing**

### 3.3.3 ASP Interface Routing

The ASP traces must be routed following standard layout practices for digital switching signals.

1. Use controlled 50 Ω characteristic impedance if possible.
2. Avoid routing these ASP traces between power planes on an adjacent layer. If signals have to cross on adjacent layers, it is recommended they should cross perpendicular in order to prevent coupling.
3. Avoid routing these ASP traces next to analog or digital switching signals.

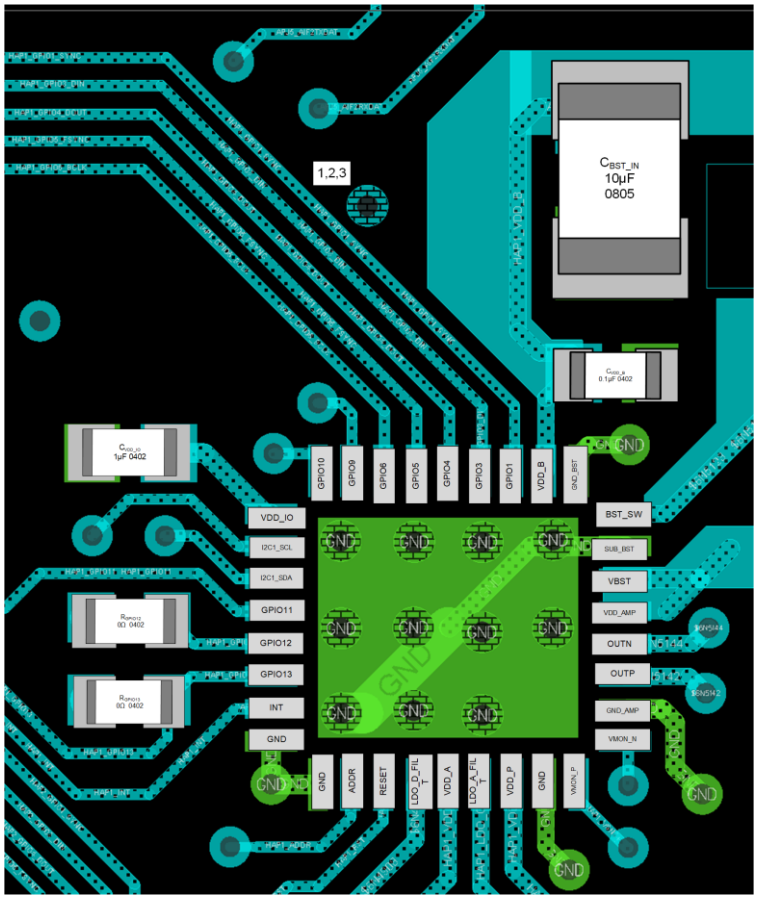



**Figure 14 ASP Routing**

### 3.3.4 GPIO Routing

The GPIO traces must be routed following standard layout practices for digital switching signals.

1. Use controlled 50 Ω characteristic impedance if possible.
2. Avoid routing these GPIO traces between power planes on an adjacent layer. If signals have to cross on adjacent layers, it is recommended they should cross perpendicular in order to prevent coupling.
3. Avoid routing these GPIOs traces next to analog or digital switching signals.

A typical layout for the GPIO signal routing is shown in the figure below.

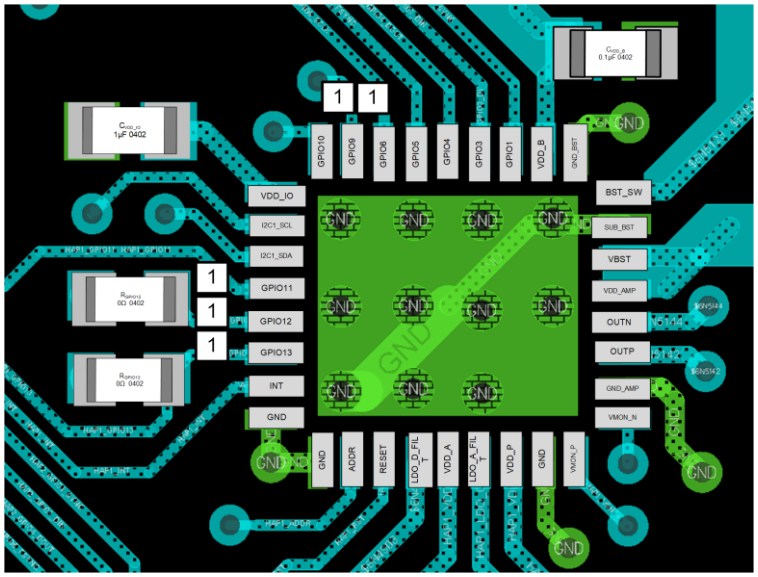



**Figure 15 GPIO Signal Routing**

### 3.3.5 Interrupt Routing

The INT trace must be routed following standard layout practices for digital switching signals.

1. Use controlled 50 Ω characteristic impedance if possible.
2. The pull up resistor can be placed either close to the CS40L5x device or the host.
3. Avoid routing the INT trace between power planes on an adjacent layer. If signals have to cross on adjacent layers, it is recommended they should cross perpendicular in order to prevent coupling.
4. Avoid routing the INT trace next to analog and digital switching signals.

A typical layout for the INT signal routing is shown in the figure below.

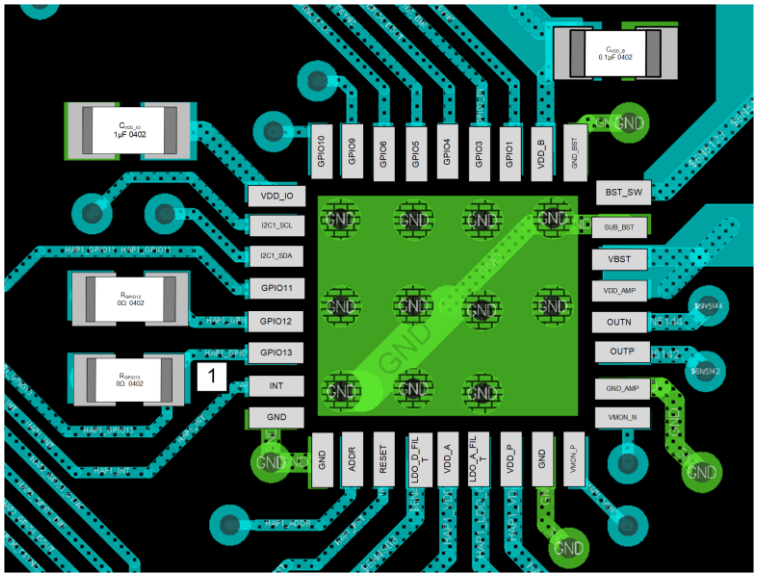



**Figure 16 Interrupt (INT) Signal Routing**

## 3.4 Output and Monitoring Routing

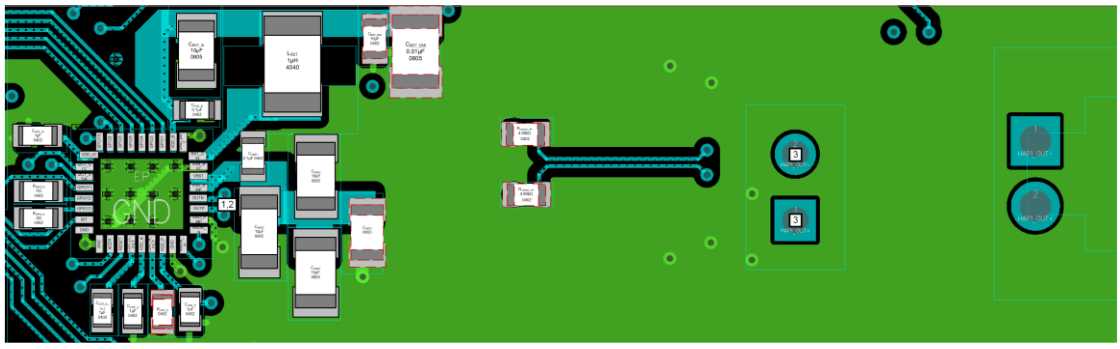
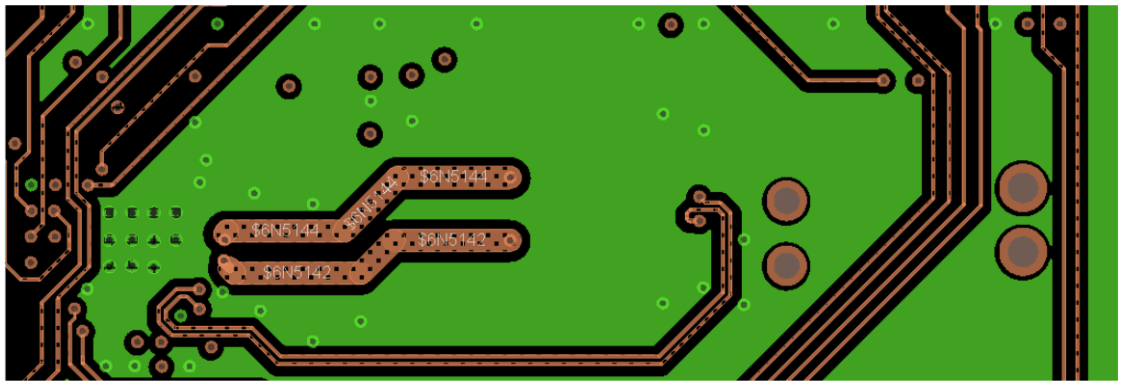
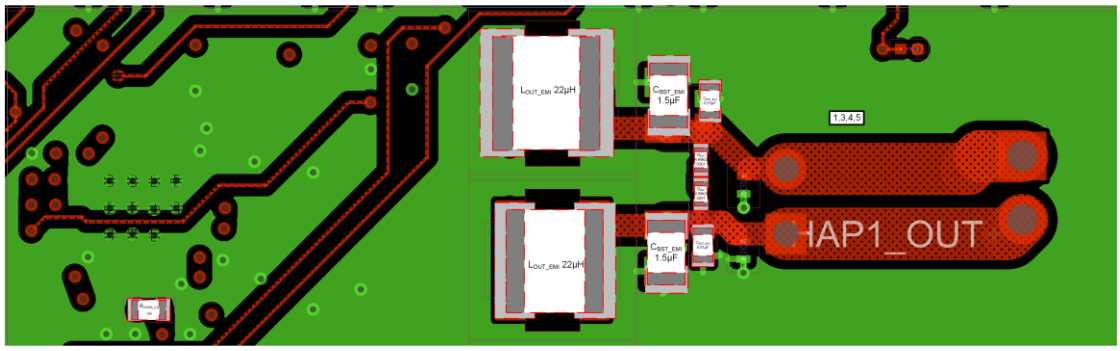
### 3.4.1 Output Routing

The following routing guidelines are recommended for the output signals (OUTP and OUTN).

1. Route OUTP and OUTN as a differential pair.
2. OUTP and OUTN traces can be escaped from the top layer using one or two high current vias per signal (3.5 A).
3. OUTP and OUTN must be routed with wide and short traces to haptic actuator (3.5 A).
4. The OUTP and OUTN signal traces must have low DC resistance. For best performance, the recommended DC resistance is 1% of minimum load, e.g. 0.06 Ω for 6 Ω load.
5. Avoid routing on same plane as power, and keep away from clock signals as far as possible.
6. Provide ground shielding around OUTP and OUTN.

A typical layout for the OUTP and OUTN signal routing is shown in the figure below.

**Table 19 Output Signal Routing**

| | |
|---|---|
| **Top Layer** |  |
| **Signal Layer** |  |
| **Bottom Layer** |  |

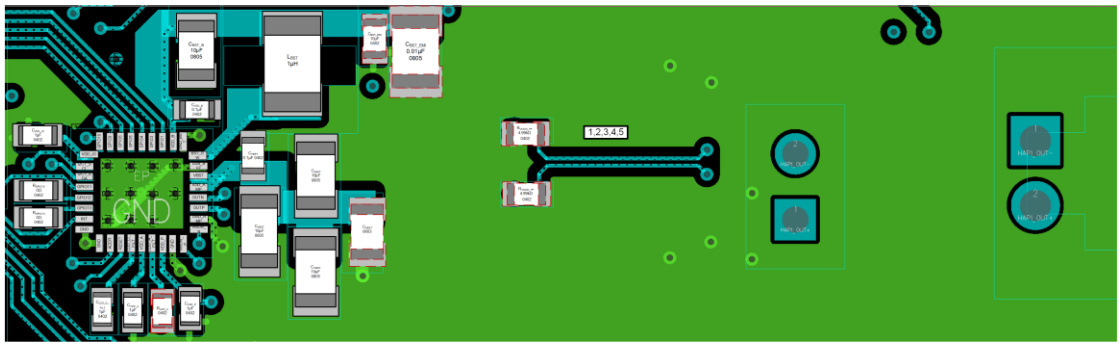
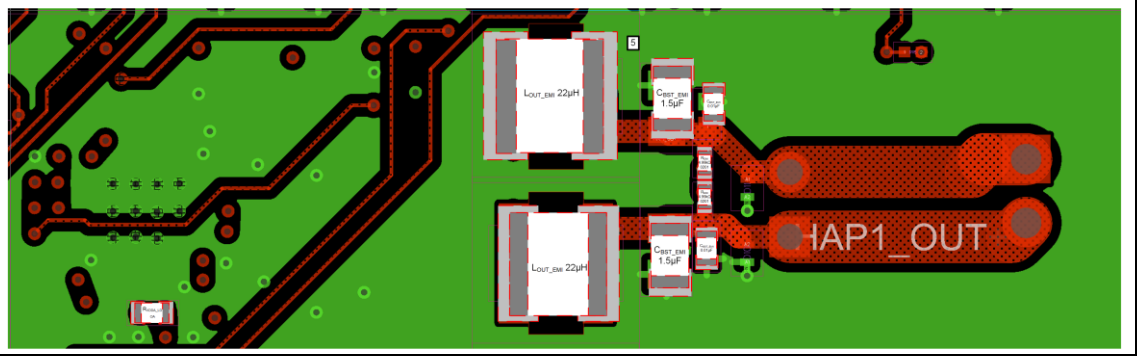
### 3.4.2 Monitoring Routing

The VMON_P and VMON_N pins are high impedance inputs dedicated to monitoring the voltage across the haptic actuator. The current flow in these pins is very small. The following routing and component placement guidelines are recommended for these signals.

1. Route VMON_P and VMON_N as low-current traces (10 mA).
2. Route VMON_P and VMON_N as a differential pair.
3. The VMON_P and VMON_N traces must connect to OUTP and OUTN (respectively) before the EMI filter. as close as possible to the actuator (LRA/VCM) in order to ensure an accurate reading of the actuator voltage.
4. Provide ground shielding around VMON_P and VMON_N, and keep away from power supplies and clock signals as far as possible.
5. The $\mathbf{R_{VMON}}$ series resistors must be placed before the EMI filter (if used).

A typical layout for the VMON_P and VMON_N signal routing is shown in the figure below.

**Table 20 Output Monitoring Signal Routing**

| | |
|---|---|
| **Top Layer** |  |
| **Bottom Layer** |  |

## 3.5 EMI Filter Routing

### 3.5.1 Input Supply Filter

If the input EMI filter is incorporated, it is recommended that the 33 nF capacitors are mirrored around the supply line.

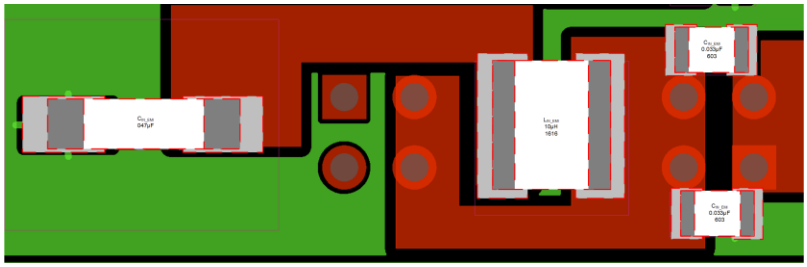


**Figure 17 Input EMI Filter**

### 3.5.2 Boost Supply Filter

The boost-supply EMI filter components should be placed as close as possible to the VDD_B pin. Additional 0.1 µF capacitors can be added to the VBST pin.

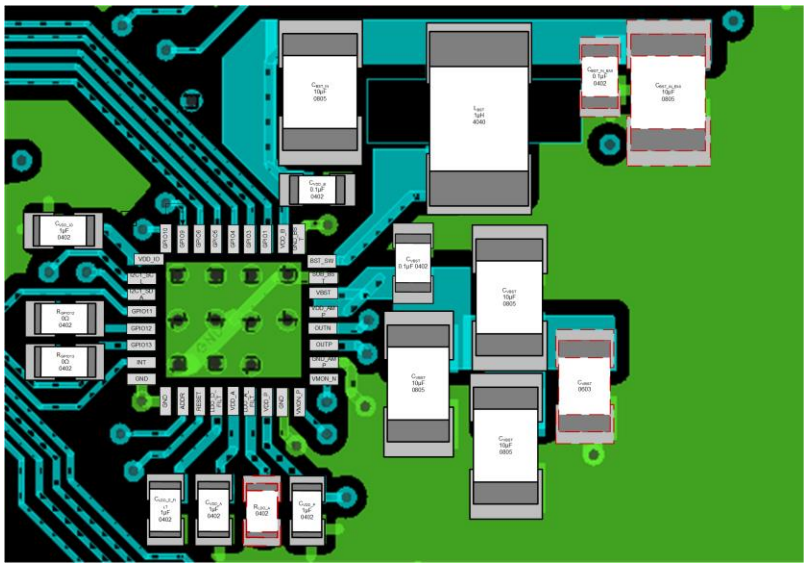
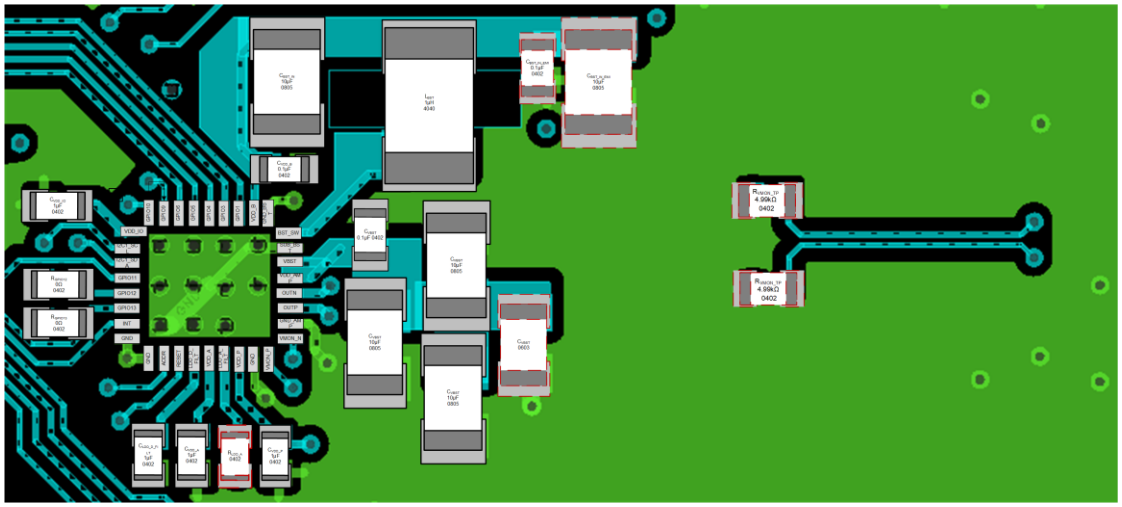
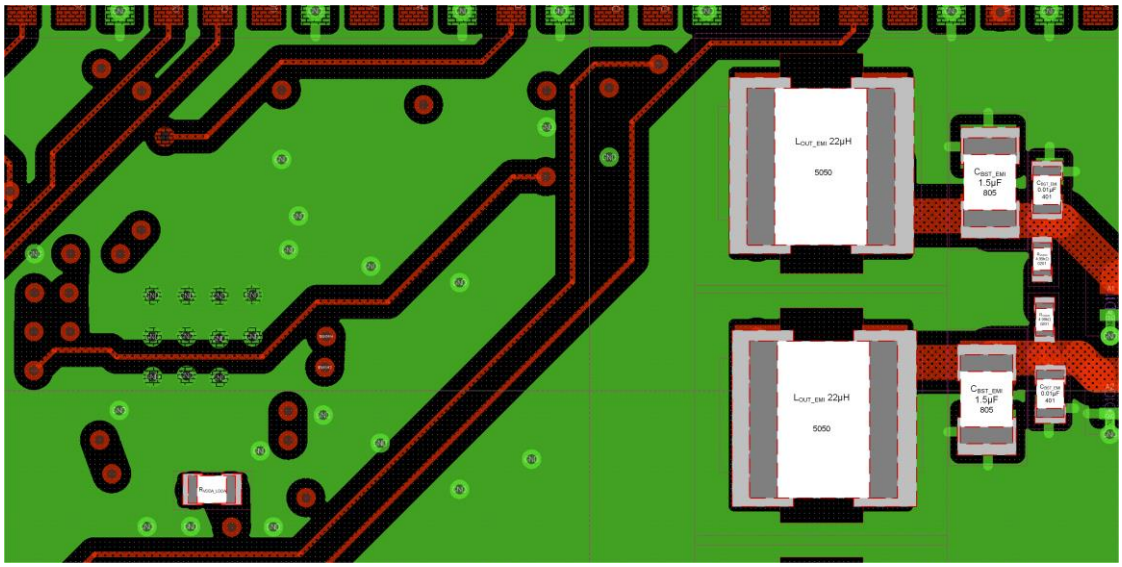


**Figure 18 Boost Supply EMI Filter**

### 3.5.3 Output EMI Filter

If the output EMI filter is incorporated, the components should be placed as close as possible to the CS40L5x. If possible, the output filter inductors should be placed on the bottom side of the board to reduce inductor-coupling interference.

**Table 21 Output EMI Filter**

| | |
|---|---|
| **Top Layer** |  |
| **Bottom Layer** |  |

## 4 Revision History

| Revision | Changes |
|---|---|
| R1<br>OCT 2025 | • Initial release |
| R2<br>NOV 2025 | • Added pinout illustration in Section 1 |
| R3<br>DEC 2025 | • Re-released without confidential restrictions |

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