

CS47L35 - Example Power Up Sequence

INTRODUCTION

The CS47L35 requires three power supplies at different voltage levels. It is designed to be as flexible as possible to support many different power up sequences, however, there are some restrictions on power supply voltage levels, the order in which the power supplies come up and the rate at which they rise.

This document provides an example power-up sequence and timing restrictions that could be used. For more complete information about power supply recommendations and power-up sequences, please refer to the datasheet.

POWER-UP EXAMPLE

Four power rails are provided to the chip as follows:

- SPKVDD = 2.4 to 5.5V (Can be left floating when speaker output not used)
- AVDD = CPVDD1 = DBVDD = 1.8V
- DCVDD = FLLVDD = CPVDD2 = 1.2V

The following diagram shows an example power-up sequence. This should be used in conjunction with Table 1, further below.

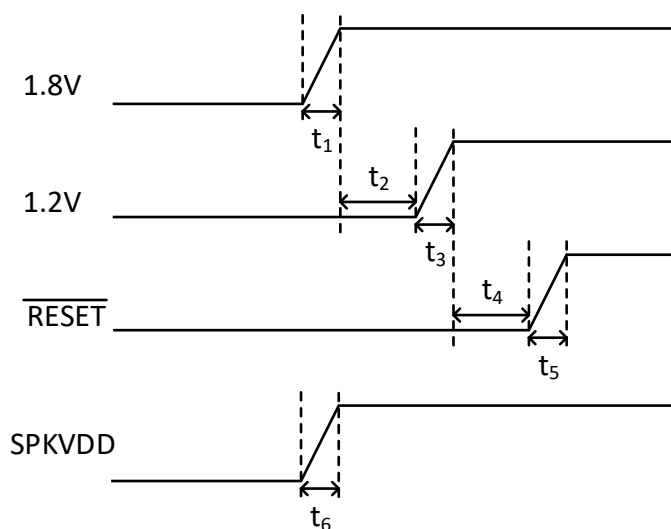


Figure 1 Example Power-up Sequence

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
1.8V supply ramp time	t_1	10			μs
1.8V high to 1.2V ramp delay	t_2	0			μs
1.2V supply ramp time	t_3	10		2000	μs
All supplies high to RESET delay	t_4	0			μs
RESET ramp time	t_5	0			μs
SPKVDD supply ramp time	t_6	10			μs

Table 1 Timing restrictions related to example sequence**Note:**

1. If the DCVDD rise time exceeds 2 ms, RESET must be asserted (low) during the rise and held asserted until after DCVDD is within the recommended operating limits.

TECHNICAL SUPPORT

If you require more information or require technical support, please contact one of the Cirrus Logic regional offices. To find one nearest you, go to www.cirrus.com.

REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
18/08/2017	1.0	Initial Release		CMcA

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find one nearest you, go to www.cirrus.com.

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