WM894x-6229-CS36-M-REV1
Example Configurations

DOC TYPE:	EXAMPLE CONFIGURATIONS
BOARD REFERENCE:	WM8944-6229-CS36-M-REV1, WM8945-6229-CS36-M-REV1, WM8946-6229-CS36-M-REV1, WM8948-6229-CS36-M-REV1
BOARD TYPE:	Customer Mini Board
WOLFSON DEVICE(S):	WM8944, WM8945, WM8946, WM8948
DATE:	August 2009
DOC REVISION:	Rev 1.0

INTRODUCTION

This is generic document that can be used for any of the available Customer Mini Boards for WM8944, WM8945, WM8946, WM8948 Wolfson CODECs referred to in this document as WM894x-6229-CS36-M-REV1. The WM894x-6229-CS36-M-REV1 Customer Mini Boards are compatible with the 6229-EV1 customer evaluation board and together provide a complete hardware platform for evaluation of the WM8944, WM8945, WM8946, WM8948 CODECs. The WM894x-6229-CS36-M-REV1 Customer Mini Board can also be used independently and connected directly to a processor board using flying wires or appropriate headers. This document will cover both options, but performance data will be based on the Wolfson system with 6229-EV1 motherboard. Configurations covered are listed below:

- DAC to LINEOUTL and LINEOUTR
- DAC to SPKOUT (8R BTL)
- IN1L, IN1R to ADC
- IN1L, IN2L, IN1R, IN2R to ADC (Diff)
- AUX1, AUX2 to ADC
- Video Buffer

This document should be used as a starting point for evaluation of WM8944, WM8945, WM8946, WM8948 CODECs but it will not cover every possible configuration. Different versions of the device may not support all of the configurations shown, e.g. WM8944 Mono version has only left channel MIC inputs and LINEOUT. This document relates to the WM8948 but shows the setup options for other devices where appropriate.

Assumptions:

1. The user is familiar with the 6229-EV1 main board and that the board is configured correctly for the path of interest (see related documents below).
2. The user has setup WISCE as per instruction and has control of the CODEC (register settings provided in this document).

Related documents:

1. WM8944-6229-CS36-M-REV1 Schematic and Layout.pdf, WM8945-6229-CS36-M-REV1 Schematic and Layout.pdf, WM8946-6229-CS36-M-REV1 Schematic and Layout.pdf, WM8948-6229-CS36-M-REV1 Schematic and Layout.pdf.
2. 6229-EV1-REV2 Schematic and Layout.pdf
3. WISCE Quick Start Guide.pdf

For the configurations in this document, the audio interface is connected to the main board through the S/PDIF ELECTRICAL IN and S/PDIF OPTICAL OUT connectors. All control signals for the device are using the 2-wire interface through the USB interface. All setup files are for 48kHz sample frequency using a reference MCLK frequency of 12.288MHz. The internal FLL is used to generate SYSCLK=512fs.

TABLE OF CONTENTS

BOARD CONFIGURATION STAND-ALONE

The WM894x-6229-CS36-M-REV1 can be used a stand-alone module for direct connection to a processor board via flying leads or dedicated headers. This section will detail important considerations and provide all information required to do this without risking damage to the device.

CONNECTION DIAGRAM

Figure 1 to 4 below shows the connections required to power-up and control the WM894x-6229-CS36-M-REV1 mini boards.

Please refer to the Table 1 for further detail on external I/O connections.

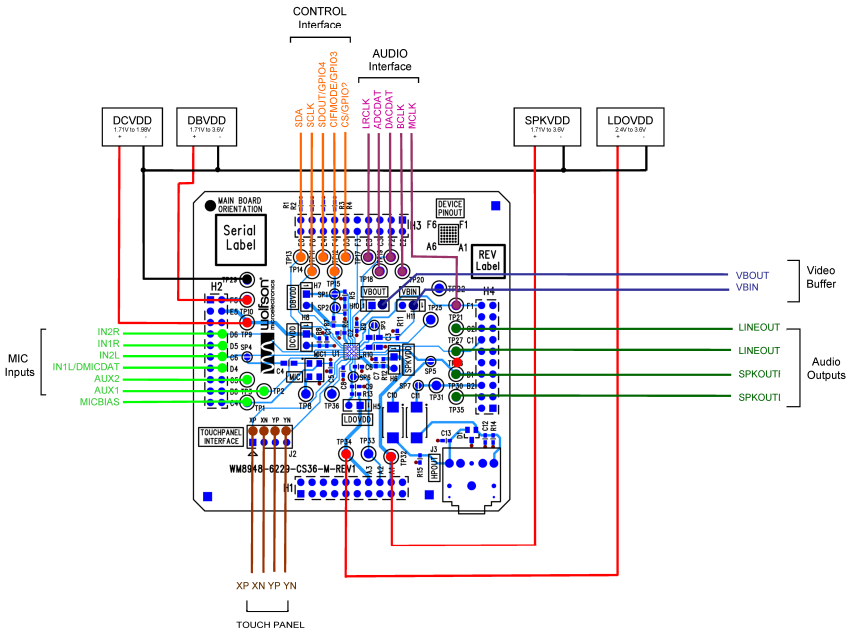


Figure 1 WM8948 Stand-Alone Board Configuration

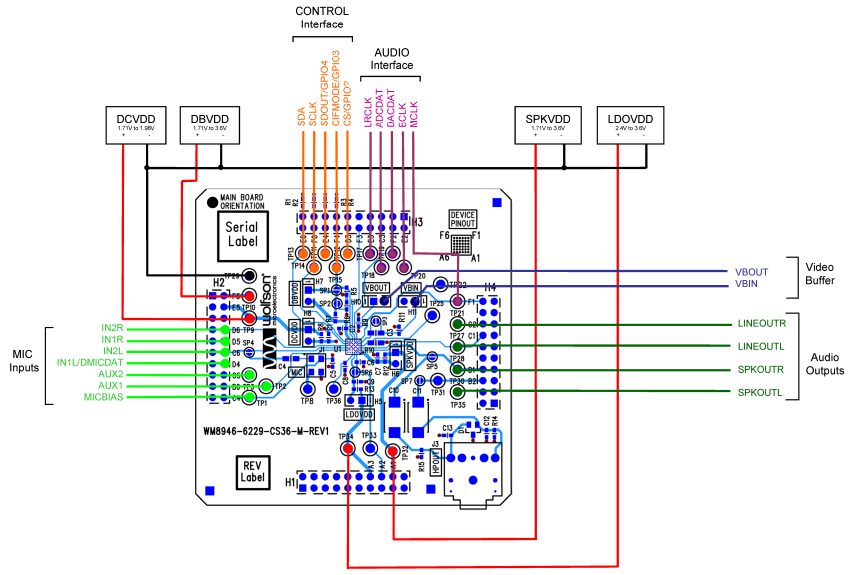


Figure 2 WM8946 Stand-Alone Board Configuration

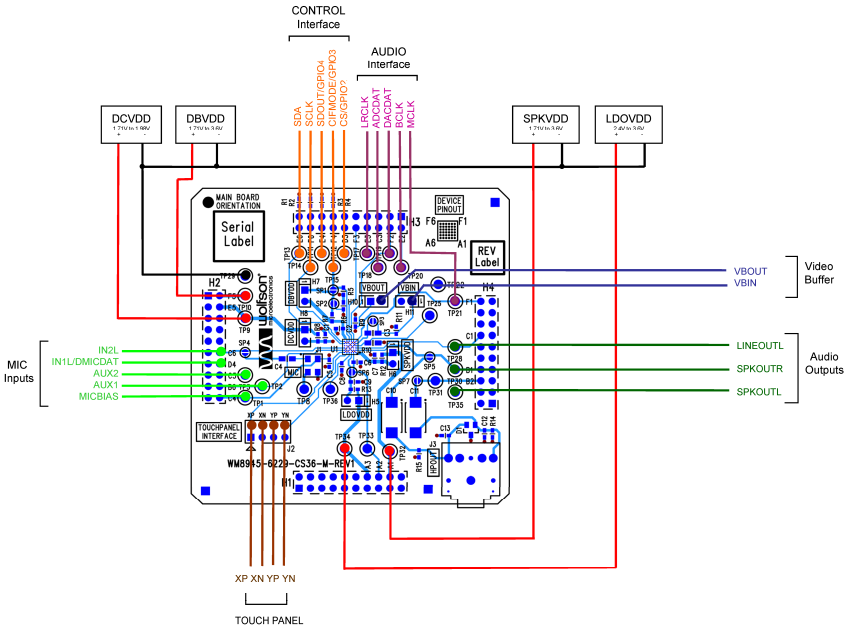


Figure 3 WM8945 Stand-Alone Board Configuration

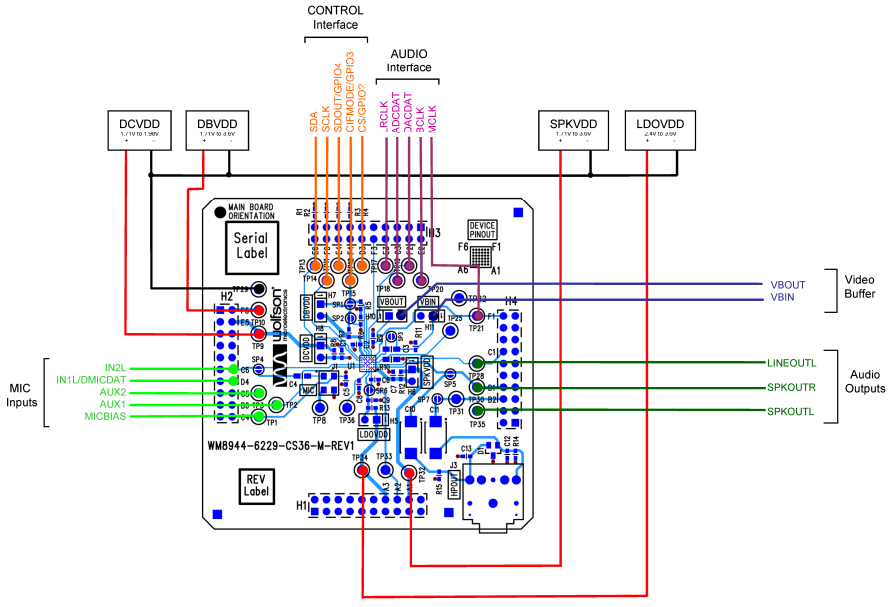


Figure 4 WM8944 Stand-Alone Board Configuration

I/O TABLE

SIGNAL	HEADER WM8948	HEADER WM8946	HEADER WM8945	HEADER WM8944	IMPORTANT NOTES
Voltage Supplies					
DBVDD	H2 pin 2				Digital buffer (I/O) supply
DCVDD	H2 pin 4				Digital core supply
LDOVDD	H1 pin 14				LDO supply input
SPKVDD	H1 pin 18				Supply for speaker driver
Ground					
GND	H1, H2, H4 odd numbered pins. H3 odd numbered pins from pin 1 to pin 11.				Analogue, Digital, Video Buffer, and Speaker GND
Control Interface					
SCLK	H3 pin 18				Control interface clock input
SDA	H3 pin 20				Control interface data input / output
SDOUT/GPIO4	H3 pin 16				Control interface data output / GPIO4
CS/GPIO2	H3 pin 12				Chip Select / GPIO2
CIFMODE/GPIO3	H3 pin 14				Control interface mode select / GPIO3
Master Clock					
MCLK	H4 pin 20				Master Clock
Audio Interface					
BCLK	H3 pin 2				Audio interface bit clock
LRCLK	H3 pin 8				Audio interface left / right clock
DACDAT	H3 pin 4				DAC digital audio data
ADCDAT	H3 pin 6				ADC / Digital Microphone digital audio data
Analogue Inputs					
IN1L/DMICDAT	H2 pin 14				Left input 1 / Digital Microphone data input
IN2L	H2 pin 12				Left input 2
IN1R	H2 pin 10	H2 pin 10	-	-	Right input 1
IN2R	H2 pin 8	H2 pin 8	-	-	Right input 2
AUX1	H2 pin 18				Aux input (audio or AUXADC input)
AUX2	H2 pin 16				Aux input (audio or AUXADC input)
XN	J5 pin 4	-	J5 pin 4	-	Touch Panel (left) connection
XP	J5 pin 2	-	J5 pin 2	-	Touch Panel (right) connection
YN	J5 pin 8	-	J5 pin 8	-	Touch Panel (bottom) connection
YP	J5 pin 6	-	J5 pin 6	-	Touch Panel (top) connection
VBIN	H11 pin 1				Video buffer input
Analogue Outputs					
LINEOUTL	H4 pin 14				Left line mixer output
LINEOUTR	H4 pin 16	H4 pin 16	-	-	Right line mixer output
SPKOUTL	H4 pin 6				Left speaker mixer output
SPKOUTR	H4 pin 8				Right speaker mixer output
LDOVOUT	H1 pin 16				LDO output
VBOUT	H10 pin 1				Video buffer output
MICBIAS	H2 pin 20				Microphone bias voltage
General Purpose Inputs/Outputs					
GPIO1	H3 pin 10				GPIO1

Table 1 I/O Configuration

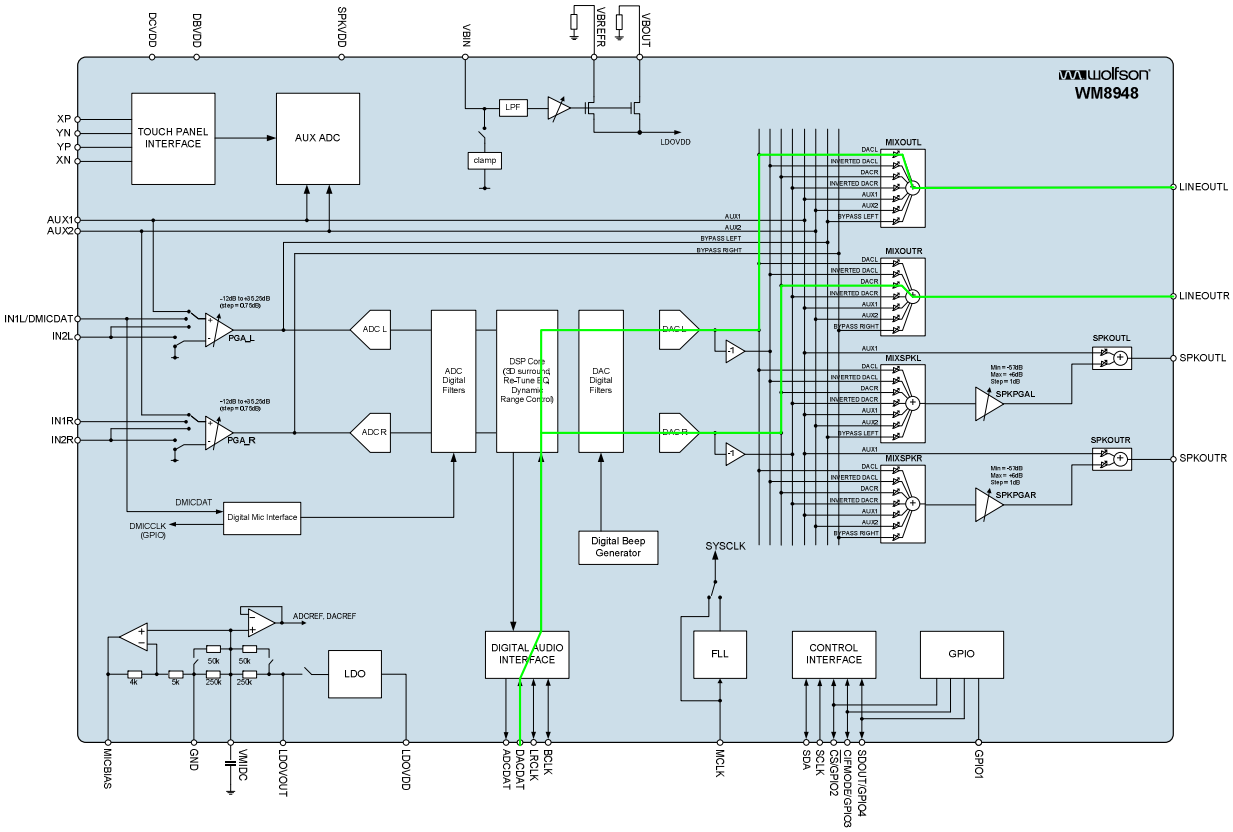
BOARD CONFIGURATION WITH 6229-EV1 MAIN BOARD

This section focuses on evaluation of the WM894x-6229-CS36-M-REV1 Customer Mini Board in combination with the 6229-EV1 main board. This system is the reference platform for measurement data contained in this document. Please note that only a limited number of usage modes will be covered.

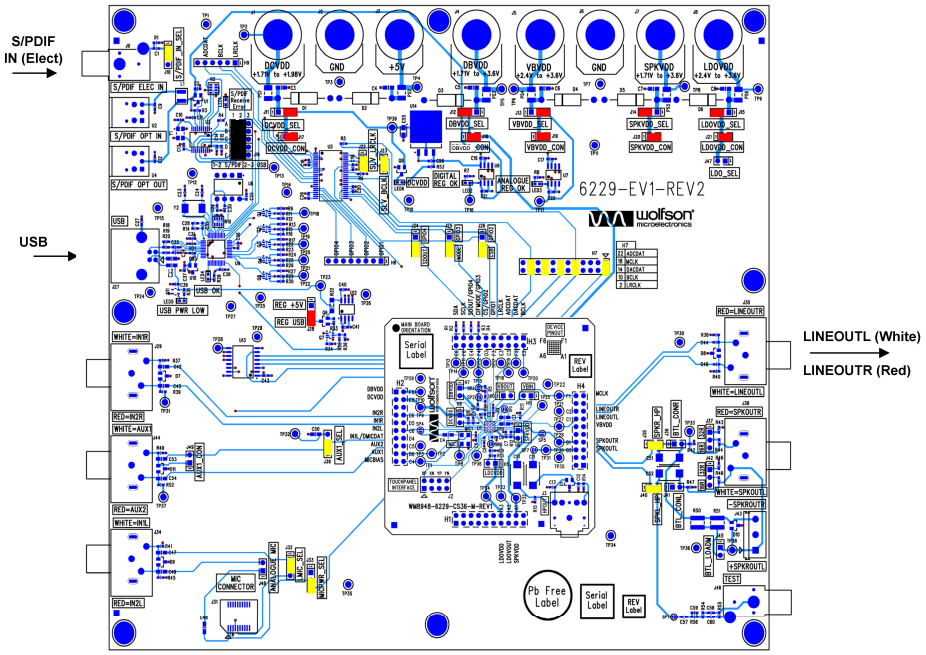
DAC TO LINEOUTL AND LINEOUTR

The following section details board configuration for DAC to LINEOUTL and LINEOUTR under no load conditions.

BLOCK DIAGRAM



BOARD CONFIGURATION



REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

WM8948 and WM8946 Devices

REG INDEX (HEX)	DATA VALUE (HEX)	COMMENT
0x00	0x0000	Reset
0x02	0x000D	Enable Master Bias and VMID buffer.
0x07	0x001D	Enable VMID, set sample rate to 48kHz.
0x35	0x8007	Enable LDO.
0x31	0x0008	LINEOUT L Mixer selects DACL to LINEOUTL.
0x32	0x0004	LINEOUT R Mixer selects DACR to LINEOUTR.
0x03	0xC333	Enable LINEOUT and DACs.
0x15	0x0010	Un-mute DACs
0x08	0x0101	MCLK=12.288MHz, SYSCLK=24.576MHz
0x2A	0x8C00	Enable VMID for LINEOUT output stage and un-mute LINEOUT.
0x40	0x0001	Select DSP Playback.
0x06	0x0306	FLL clock, enable SYSCLK.

WM8945 and WM8944 Devices

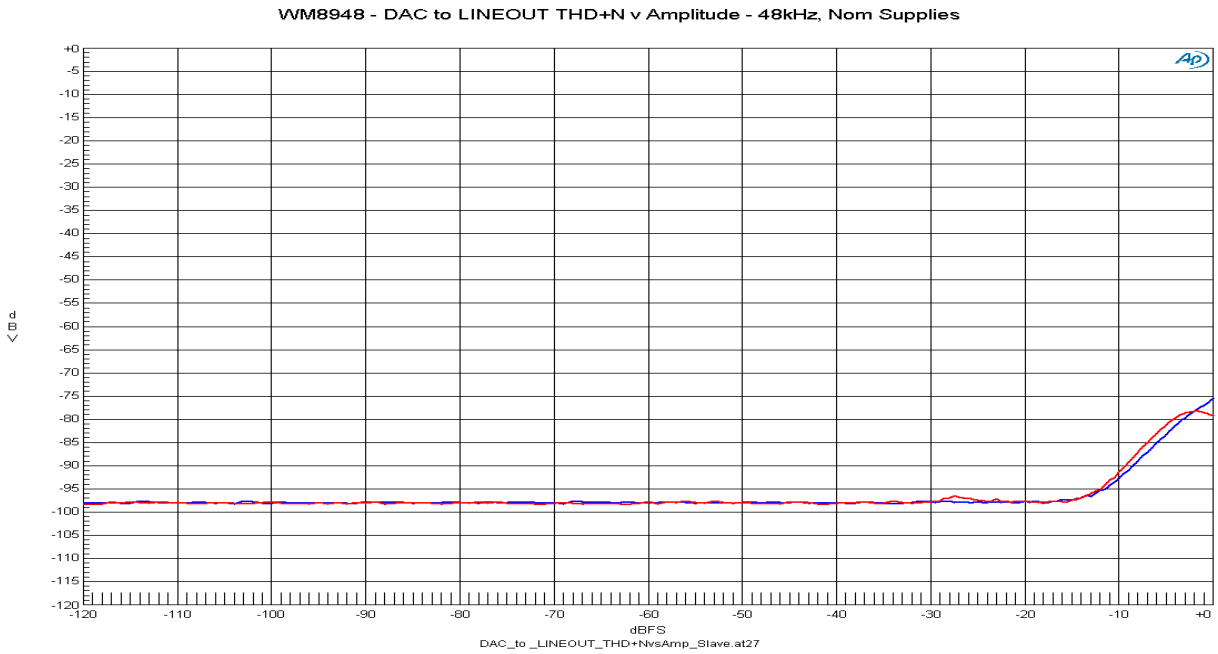
REG INDEX (HEX)	DATA VALUE (HEX)	COMMENT
0x00	0x0000	Reset
0x02	0x000D	Enable Master Bias and VMID buffer.
0x07	0x001D	Enable VMID, set sample rate to 48kHz.
0x35	0x8007	Enable LDO.
0x31	0x0008	LINEOUT L Mixer selects DACL to LINEOUTL.
0x03	0x4331	Enable LINEOUTL and Left DAC.
0x15	0x0010	Enable DAC Auto-mute
0x08	0x0101	MCLK=12.288MHz, SYSCLK=24.576MHz
0x2A	0x8400	Enable VMID for LINEOUT output stage and un-mute LINEOUT.
0x40	0x0001	Select DSP Playback.
0x06	0x0306	FLL clock, enable SYSCLK.

PERFORMANCE PLOT

DBVDD =LDOVDD=SPKVDD=3.3V; DCVDD=1.8V

Sample Frequency=48kHz

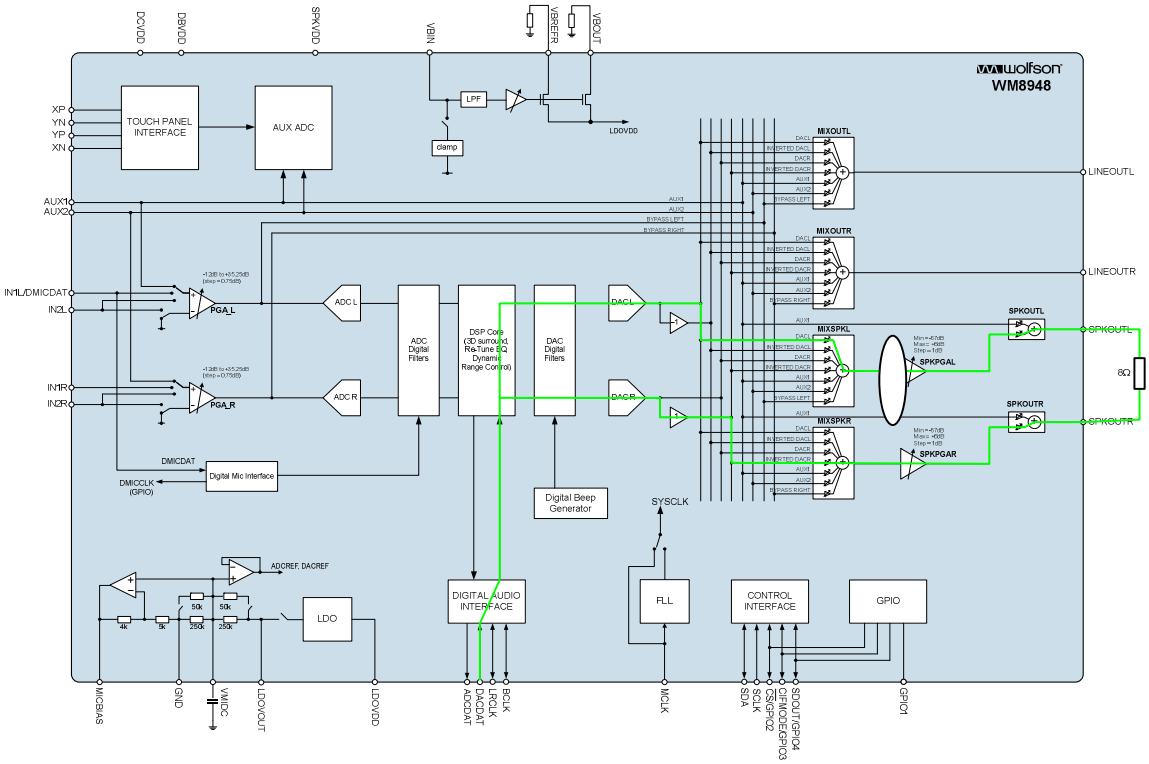
THD+N v Amplitude (A-weighted)



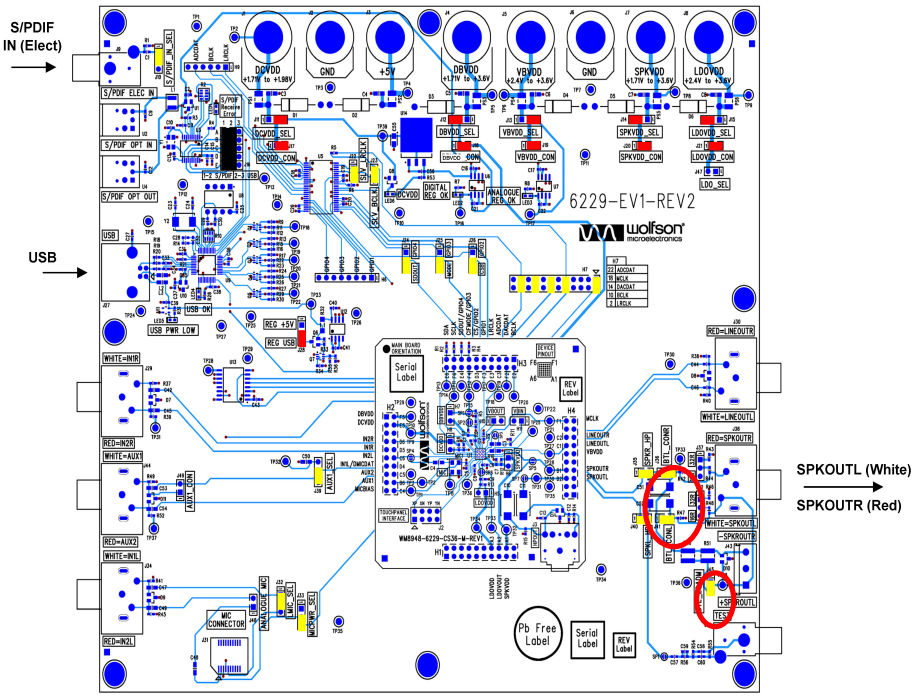
DAC TO SPKOUTR (8R BTL)

The following section details board configuration for DAC to SPKOUTL and SPKOUTR driving an 8Ω Bridge-tied-load (BTL).

BLOCK DIAGRAM



BOARD CONFIGURATION



Add shorting links to J36, J41 to bypass the output coupling capacitors and J45 connect an 8Ω load across the SPK outputs.

REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

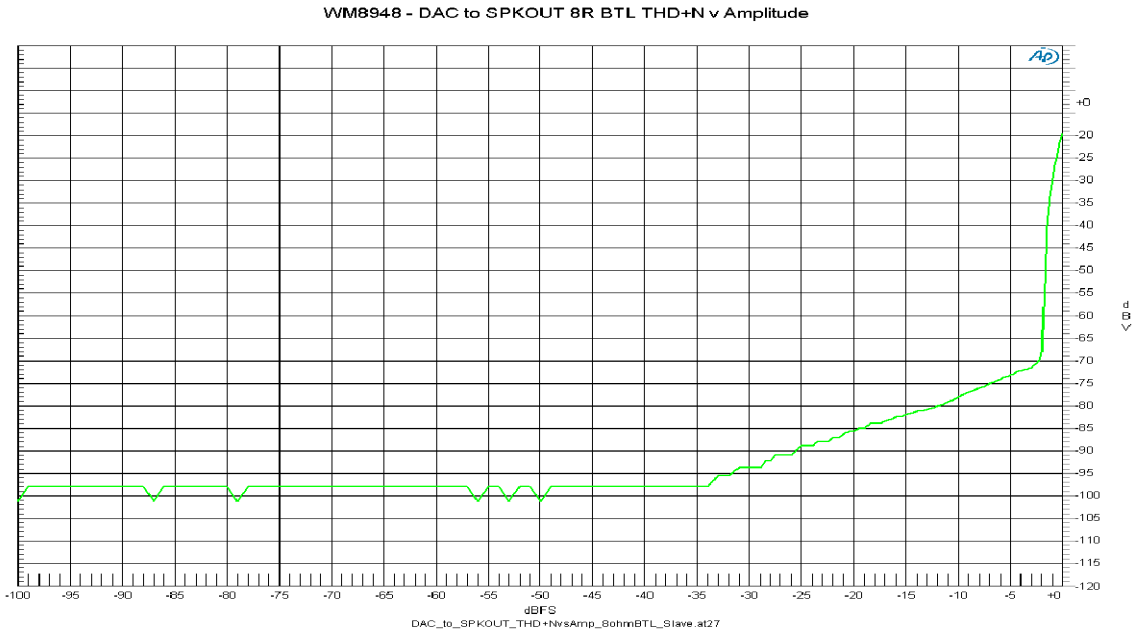
REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	Reset
0x02	0x000D	Enable Master Bias and VMID buffer.
0x07	0x001D	Enable VMID, set sample rate to 48kHz.
0x35	0x8007	Enable LDO.
0x2B	0x0088	SPKOUTL Mixer selects DACL to SPKOUTL, Output Mixer selects PGA to SPKL.
0x2C	0x00A0	SPKOUT R Mixer selects DACR to SPKOUTR, Output Mixer selects PGA to SPKR.
0x2F	0x0139	Unmute Left speaker PGA
0x30	0x0139	Unmute Right speaker PGA
0x03	0xFCCF	Enable SPKOUT, SPKOUT Mixers and DACs.
0x15	0x0010	Enable DAC Auto-mute
0x08	0x0101	MCLK=12.288MHz, SYSCLK=24.576MHz
0x2A	0xB000	Enable VMID for SPKOUT output stage.
0x40	0x0001	Select DSP Playback.
0x06	0x0306	FLL clock, enable SYSCLK.

PERFORMANCE PLOT

DBVDD =LDOVDD=SPKVDD=3.3V; DCVDD=1.8V

Sample Frequency=48kHz

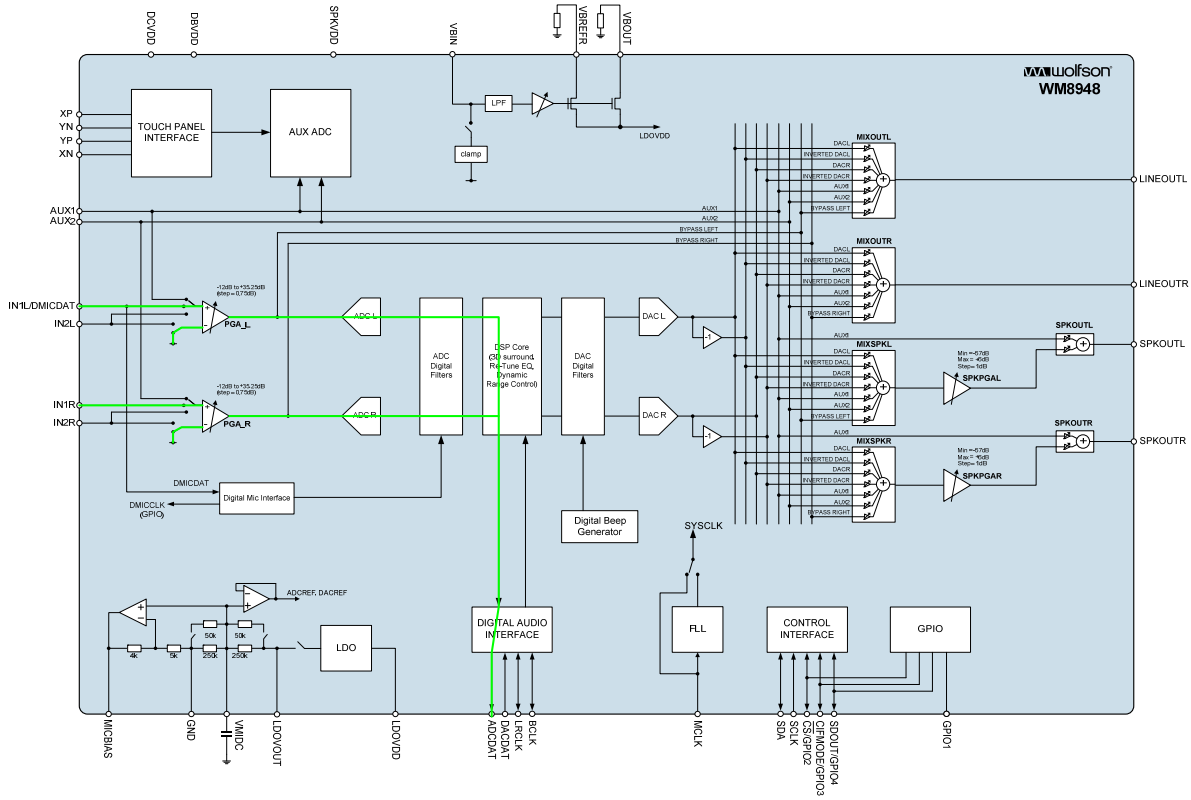
THD+N v Amplitude (A-weighted)



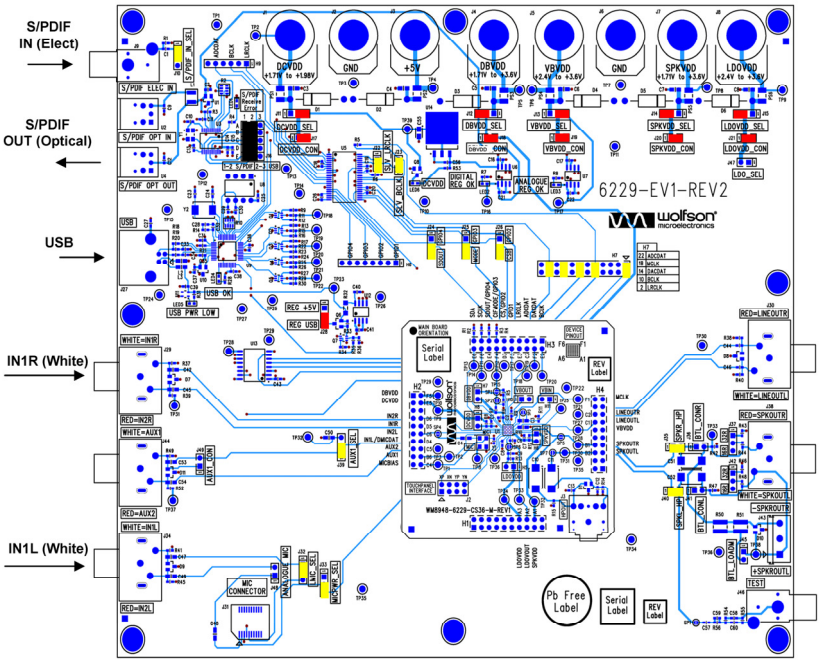
IN1L, IN1R TO ADC

The following section details board configuration for IN1L and IN1R inputs connected to the ADC.

BLOCK DIAGRAM



BOARD CONFIGURATION



REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

WM8948 and WM8946 Devices

REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	Reset
0x02	0x3C0D	Enable Input PGAs, ADCs, Master Bias and VMID buffer.
0x35	0x8007	Enable LDO.
0x27	0x0005	Configure PGA Source to select single-ended inputs.
0x28	0x0010	Un-mute PGAL.
0x29	0x0010	Un-mute PGAR.
0x19	0x0000	Un-mute ADCs.
0x08	0x0101	MCLK=12.288MHz, PLL set for 24.576MHz Output.
0x07	0x001D	Enable VMID, set sample rate to 48kHz.
0x06	0x0306	Enable SYSCLK, FLL clock, put digital audio Interface in slave mode.

WM8945 and WM8944 Devices

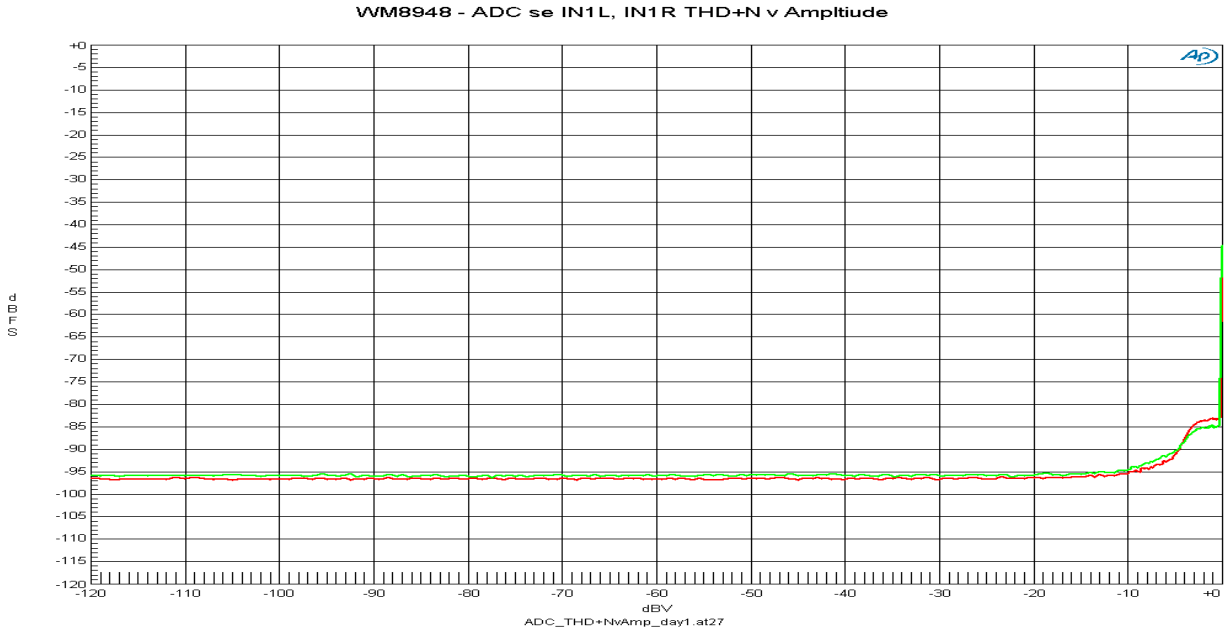
REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	Reset
0x02	0x140D	Enable Input PGAL, ADCL, Master Bias and VMID buffer.
0x35	0x8007	Enable LDO.
0x27	0x0005	Configure PGAL Source to select single-ended inputs.
0x28	0x0010	Un-mute PGAL.
0x19	0x0000	Un-mute ADCL.
0x08	0x0101	MCLK=12.288MHz, PLL set for 24.576MHz Output.
0x07	0x001D	Enable VMID, set sample rate to 48kHz.
0x06	0x0306	Enable SYSCLK, FLL clock, put digital audio Interface in slave mode.

PERFORMANCE PLOT

DBVDD =LDOVDD=SPKVDD=3.3V; DCVDD=1.8V

Sample Frequency=48kHz

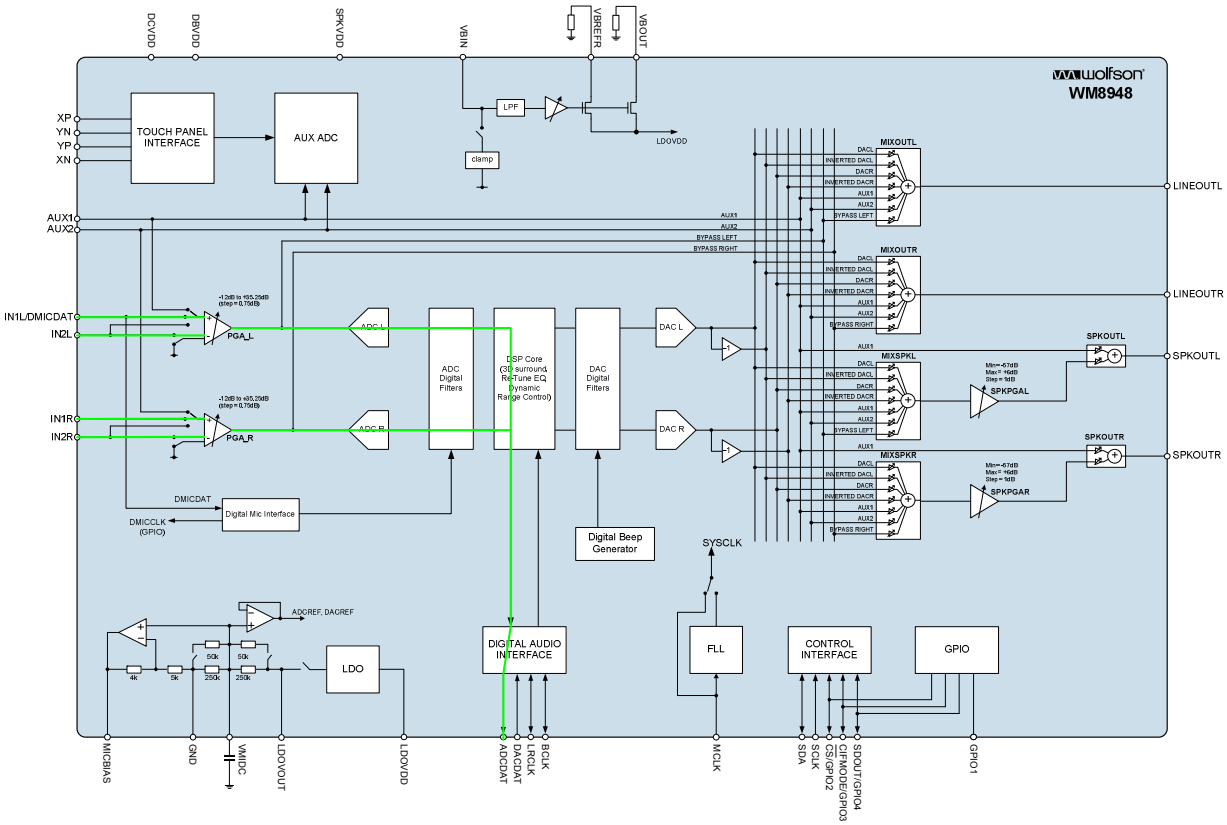
THD+N v Amplitude (A-weighted)



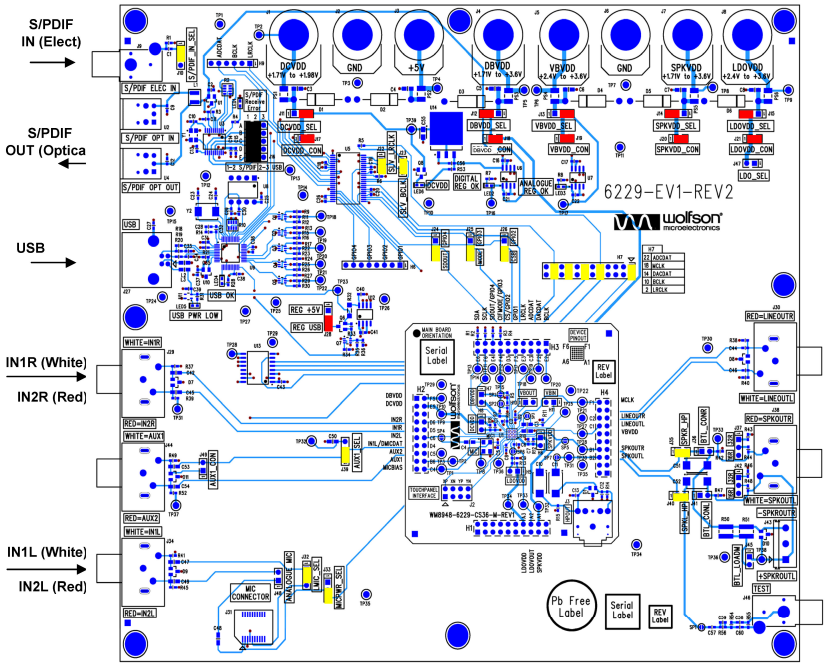
IN1L-IN2L, IN1R-IN2R TO ADC (DIFF)

The following section details board configuration for IN1L/DMICDAT-IN2L and IN1R-IN2R connected as differential signals to the ADC.

BLOCK DIAGRAM



BOARD CONFIGURATION



REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

WM8948 and WM8946 Devices

REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	Reset
0x02	0x3C0D	Enable Input PGAs, ADCs, Master Bias and VMID buffer.
0x35	0x8007	Enable LDO.
0x27	0x0035	Configure PGA Source to select differential inputs.
0x28	0x0010	Un-mute PGAL.
0x29	0x0010	Un-mute PGAR.
0x19	0x0000	Un-mute ADCs.
0x08	0x0101	MCLK=12.288MHz, PLL set for 24.576MHz Output.
0x07	0x001D	Enable VMID, set sample rate to 48kHz.
0x06	0x0306	Enable SYSCLK, FLL clock, put digital audio Interface in slave mode.

WM8945 and WM8944 Devices

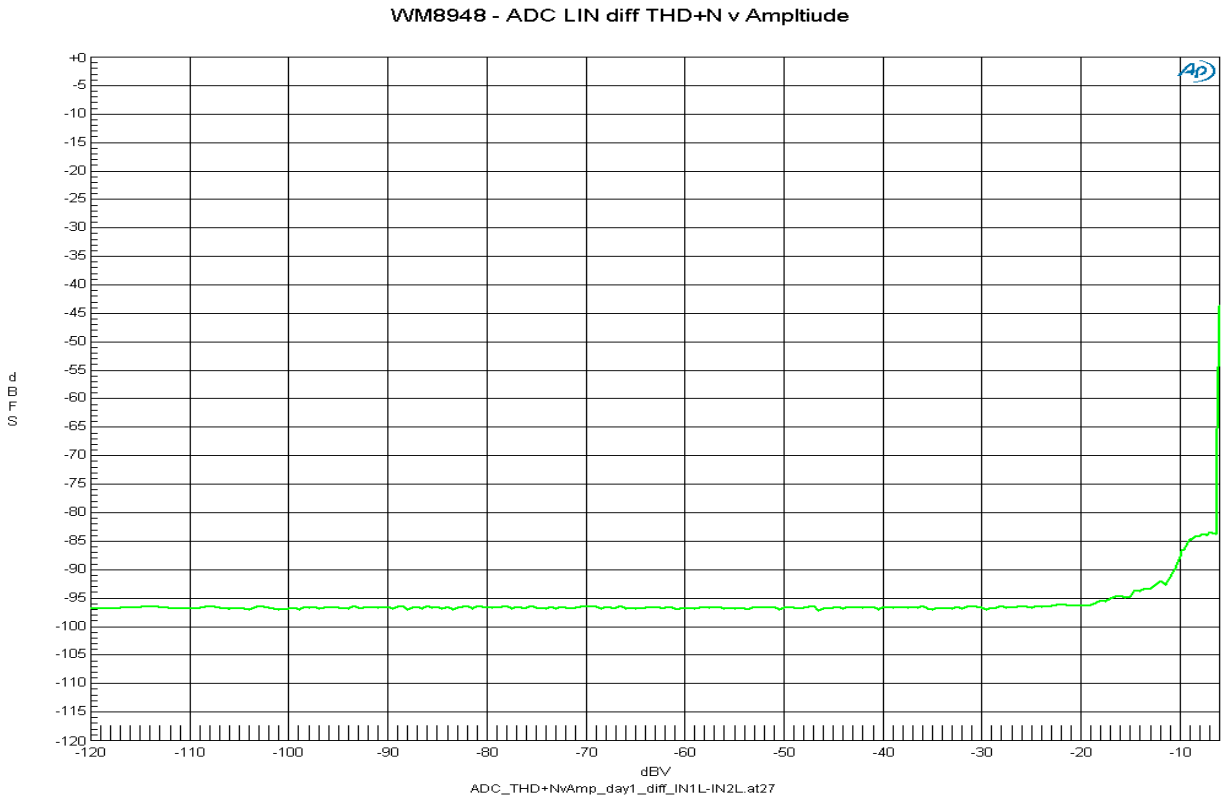
REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	Reset
0x02	0x140D	Enable Input PGAL, ADCL, Master Bias and VMID buffer.
0x35	0x8007	Enable LDO.
0x27	0x0035	Configure PGAL Source to select differential inputs.
0x28	0x0010	Un-mute PGAL.
0x19	0x0000	Un-mute ADCL.
0x08	0x0101	MCLK=12.288MHz, PLL set for 24.576MHz Output.
0x07	0x001D	Enable VMID, set sample rate to 48kHz.
0x06	0x0306	Enable SYSCLK, FLL clock, put digital audio Interface in slave mode.

PERFORMANCE PLOT

DBVDD =LDOVDD=SPKVDD=3.3V; DCVDD=1.8V

Sample Frequency=48kHz

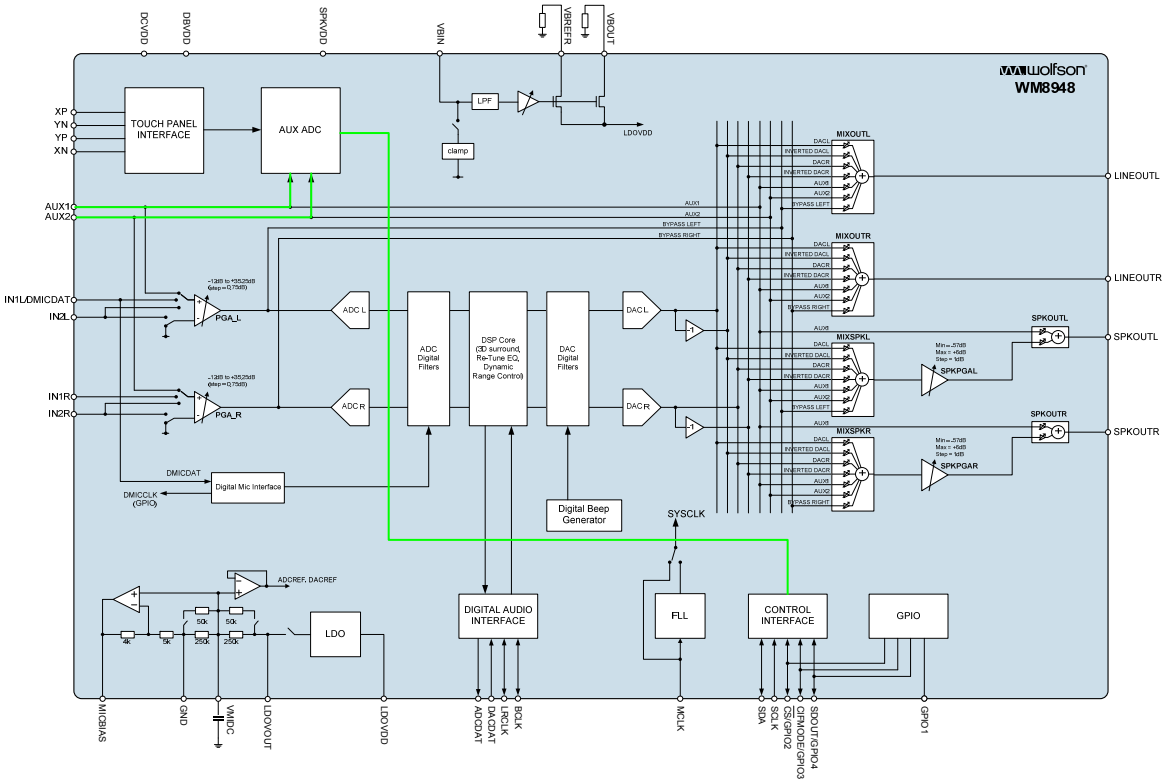
THD+N v Amplitude (A-weighted)



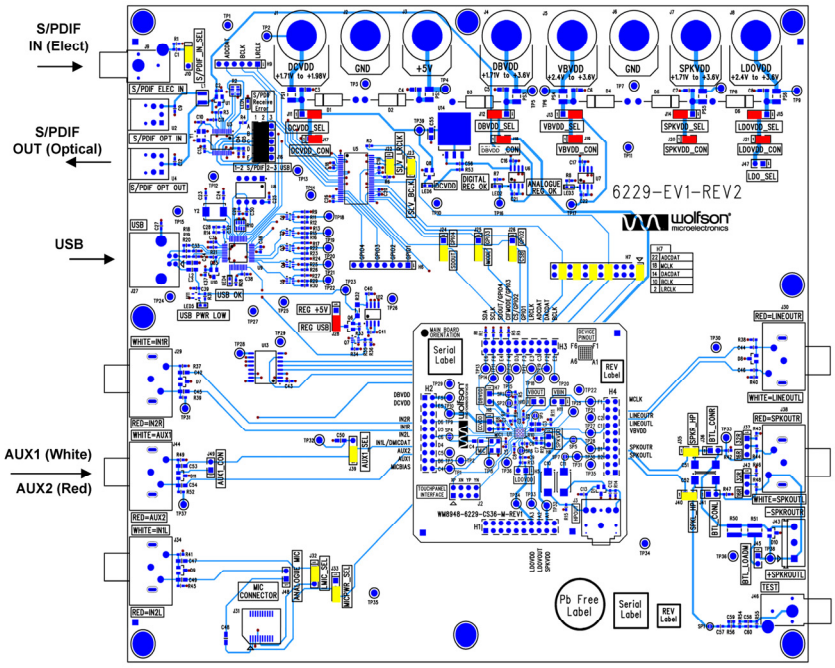
AUX1, AUX2 TO AUXADC

The following section details board configuration for AUX1 and AUX2 inputs to the AUXADC.

BLOCK DIAGRAM



BOARD CONFIGURATION



REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

WM8948 and WM8945 Devices

REG INDEX (HEX)	DATA VALUE (HEX)	COMMENT
0x00	0x0000	Reset
0x02	0x000D	Enable Master Bias and VMID buffer.
0x06	0x9106	Enable OSC_CLK.
0x07	0x001D	Enable VMID.
0x35	0x8007	Enable LDO.
0x0C	0x0006	Enable GPIO1 as an Output, Output AUX_DONE flag
0x3D	0x8000	Enable AUX ADC Measurement Manual.
0x3E	0x0001	Measure AUX1.

Example 1: Configure the AUX1 Measurement for Manual Polling

WM8946 and WM8944 Devices

REG INDEX (HEX)	DATA VALUE (HEX)	COMMENT
0x00	0x0000	Reset
0x02	0x000D	Enable Master Bias and VMID buffer.
0x06	0x9106	Enable OSC_CLK.
0x07	0x001D	Enable VMID.
0x35	0x8007	Enable LDO.
0x0C	0x0006	Enable GPIO1 as an Output, Output AUX_DONE flag
0x3D	0x8003	Enable AUX ADC Measurement, start conversions at 48kHz.
0x3E	0x0002	Measure AUX2.

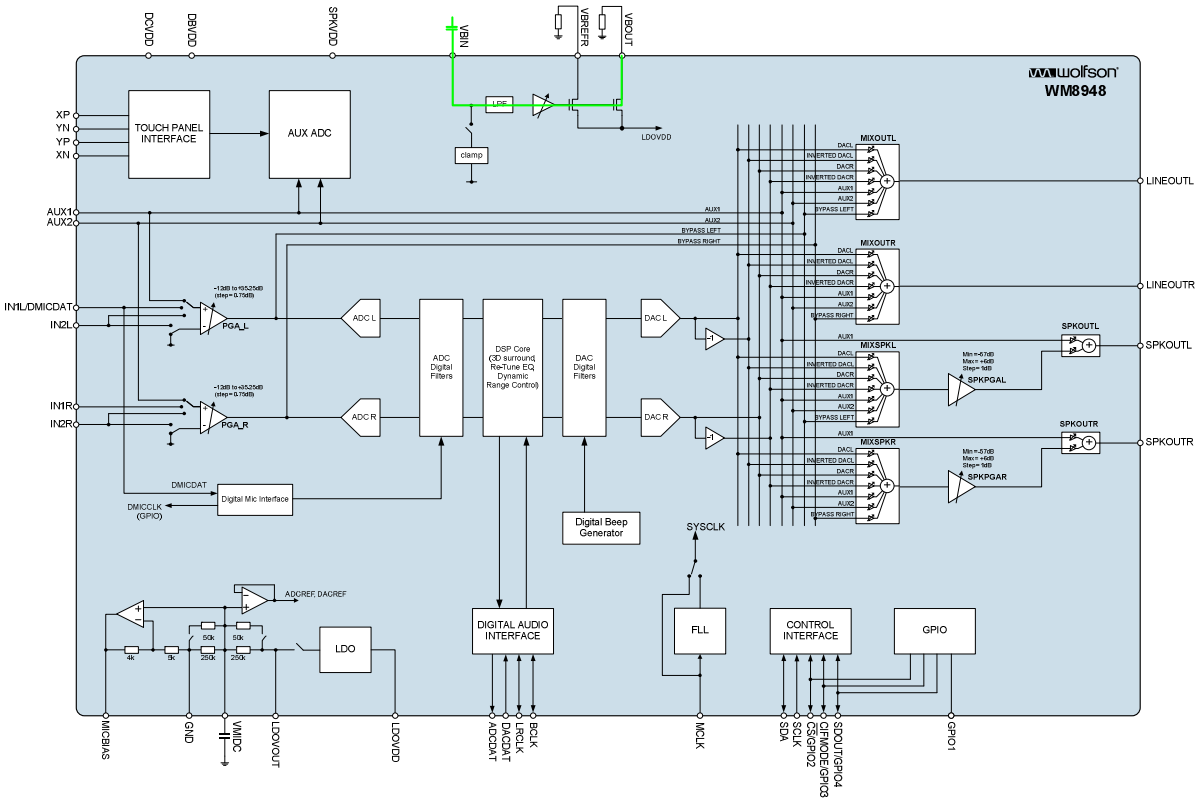
Example 2: Configure the AUX2 Measurement for 48kHz Conversions

To make a measurement using the AUXADC register 0x3D bit14 must be written with a 1 to start the conversion. Reading register 0x3C returns the data in bits [11:0]. Bits [13:12] indicate the source of the measured value, i.e. AUX1, AUX2 or SPKVDD.

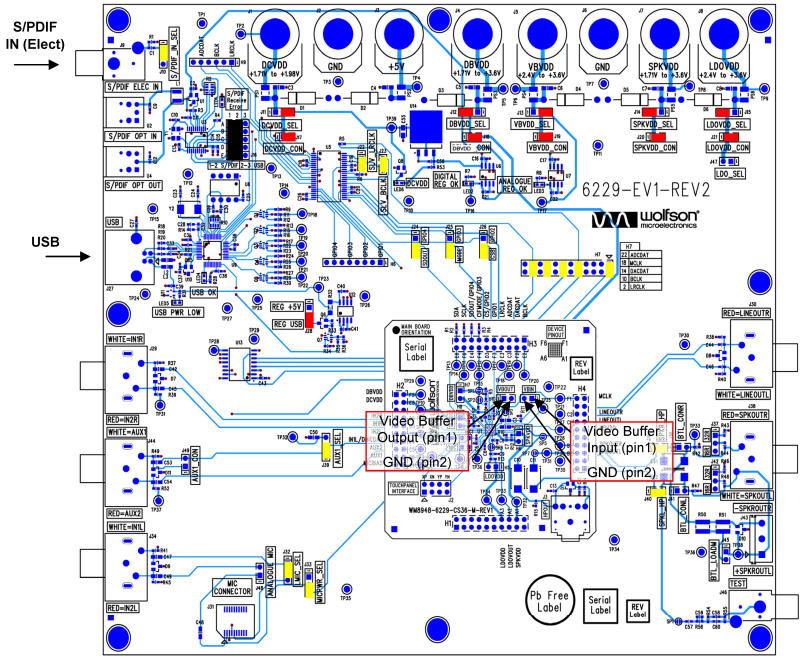
VIDEO BUFFER

The following section details board configuration of the Video Buffer.

BLOCK DIAGRAM



BOARD CONFIGURATION



REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not in any way been optimised.

REG INDEX (HEX)	DATA VALUE (HEX)	COMMENT
0x00	0x0000	Reset
0x02	0x000D	Enable Master Bias and VMID buffer.
0x07	0x001D	Enable VMID.
0x26	0x00A0	Enable Video Buffer with +6dB Gain and enable Clamp.

For ac coupled video signals, the signal is fed into the device on H11 pin1 with the GND connected to pin2. If the signal is dc coupled then the link SP7 should also be shorted to bypass the ac coupling capacitor.

APPLICATION SUPPORT

If you require more information or require technical support, please contact the Wolfson Microelectronics Applications group through the following channels:

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Fax: +44 (0) 131 272 7001
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