CDB47L90-M-1 Layout Guidelines

INTRODUCTION

This document describes the layout Guidelines for the CS47L90 customer board.

GENERAL BOARD CONSIDERATIONS

1. Avoid routing digital signals between power planes on an adjacent layer.

LAYOUT GUIDELINES

Note 1: **Analogue Inputs**

Route analogue inputs differentially

- Match impedance of input pairs and track together. **[Medium Priority]**
- Keep inputs away from High Speed signals. **[High Priority]**
- Mixed analogue/digital inputs are IN1AR, & IN2AL.
- Analogue only inputs are IN1AL, IN1B, IN2R, & IN2B.

Note 2: **HPOUT1**

- **Differential:** Route HPOUT3 Differentially. **[Medium Priority]**
- **Single Ended:** Route MICDET1/HPOUTFB1 & MICDET2/HPOUTFB2 between HPOUT1L and HPOUT1R. **[High Priority]**
- The HPOUT1 signal tracks should have low DC resistance tracks. Recommended DC resistance is 1% of Min load. (0.06 Ohms for 6 ohm load) **[Medium Priority]**

	Min	Typ	Max	Units
DC Resistance		< 0.06		**Ω**

Note 3: **HPOUT2**

- **Differential:** Route HPOUT3 Differentially. **[Medium Priority]**
- **Single Ended:** Route MICDET3/HPOUTFB3 & MICDET4/HPOUTFB4 between HPOUT2L and HPOUT2R. **[High Priority]**
- The HPOUT2 signal tracks should have low DC resistance tracks. Recommended DC resistance is 1% of Min load. (0.06 Ohms for 6 ohm load) **[Medium Priority]**

	Min	Typ	Max	Units
DC Resistance		< 0.06		**Ω**

Note 4: **HPOUT3**

- **Differential:** Route HPOUT3 Differentially. **[Medium Priority]**
- **Single Ended:** Route HPOUT3FB between HPOUT3L and HPOUT3R **[High Priority]**
- The HPOUT3 signal tracks should have low DC resistance tracks. Recommended DC resistance is 1% of Min load. (0.06 Ohms for 6 ohm load) **[Medium Priority]**

	Min	Typ	Max	Units
DC Resistance		< 0.06		**Ω**

Note 5: **Device Decoupling [Medium/High Priority]**

Place de-coupling capacitors close to device.

Note 6: **DCVDD Supply [Medium/High Priority]**

If the DCVDD track is routed through more than 1 layer. There should be 2-4 Via's for each layer transition to reduce the impedance between DCVDD and supply.

DCVDD Decoupling

- 1 x 1uF for DCVDD ball P16
- 1 x 1uF for DCVDD ball AA15 & AB12
- 1 x 1uF for DCVDD ball AB6 & AA3

Note 7: **1V2 Common Supply [Medium Priority]**

Star DCVDD. FLLVDD and CPVDD2 supplies separately to VDDCORE supply

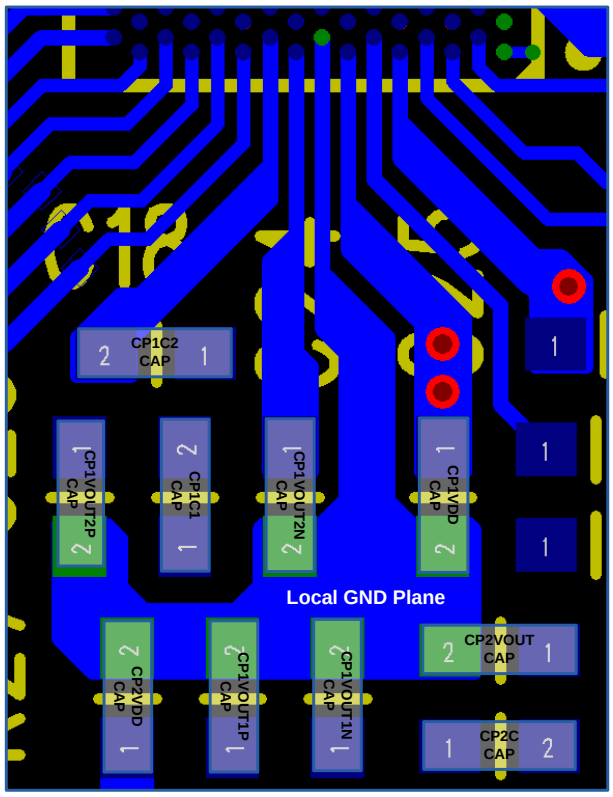
Note 8: **Charge Pump [High Priority]**

A local ground plane should be used for CPGND and the charge pump de-coupling. The local ground plane should be connected to the common ground plane close to the CPVDD de-coupling cap (C17).

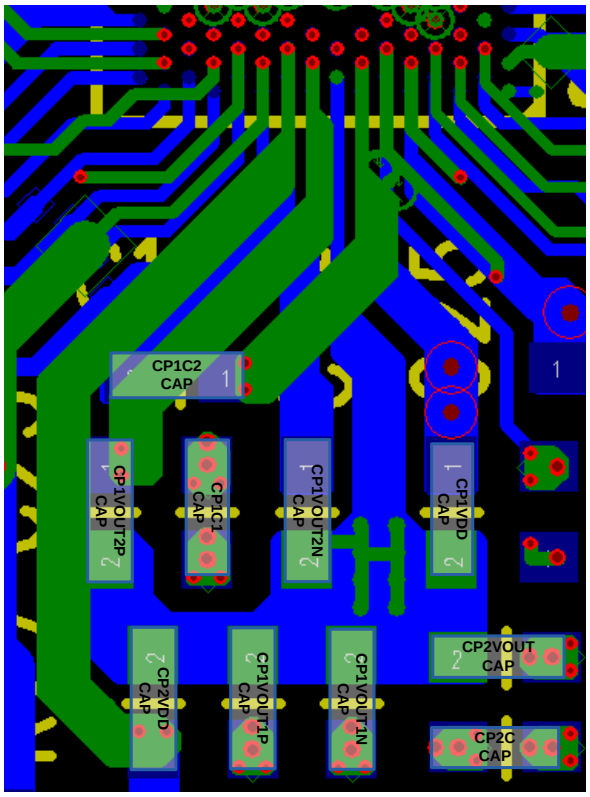
- VIAs to all GND planes should be placed under the local ground plane. (4 - 8 VIA's)
- Order of priority in relation to charge pump components.

Priority	
1	CP1VOUT2n CP1C2n
2	CP1VOUT1n CP1C1n
3	CP2VOUT CP2Cn

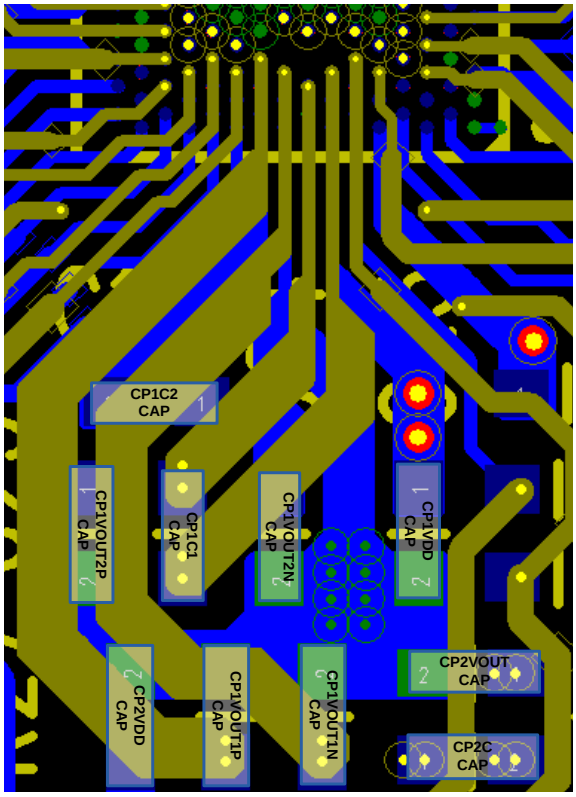
Charge Pump Layout – Top Layer



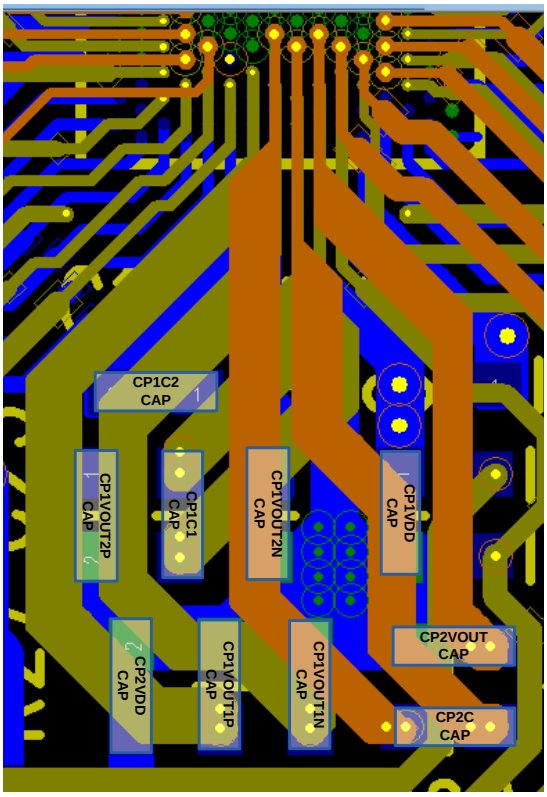
Charge Pump Layout – Layer 2



Charge Pump Layout – Layer 3

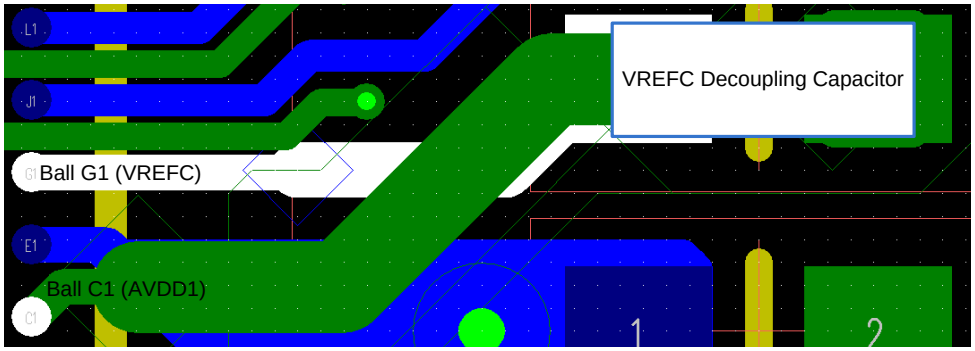


Charge Pump Layout – Layer 8



Note 9: **VREFC GND Return [High Priority]**

The VREFC cap current return path should be routed to AGND1 (Pin C1).



Note 10: **Digital Signals**

- Use controlled 50Ω characteristic impedance for digital signals. **[Low Priority]**
- Place series termination resistors close to DUT. **[Medium Priority]**

Note 11: **PDM Outputs [Low Priority]**

Route each set of speaker PDM outputs as a pair.

Note 12: **Slimbus Interface [Low Priority]**

Place SLIMCLK R-C network close to DUT.

Note 13: **Headset Connections [Medium/High Priority]**

Star connect IN1BRP, MICDET1/HPOUTFB1 and SP1 at J4:P1.

- Use a low impedance connection between J4:P1 and SP1.
- Use a low impedance connection between SP1 and the ground plane.
- Use a low impedance connection between U3:P1 and the ground plane
- Use a low impedance connection between J6:P1 and U3:P6&P8

Star connect IN1BN, HPOUTFB2/MICDET2 and SP2 at J4:P3.

- Use a low impedance connection between J4:P3 and SP2.
- Use a low impedance connection between SP2 and the ground plane.
- Use a low impedance connection between U3:P4 and the ground plane
- Use a low impedance connection between J6:P3 and U3:P3&P7

KEY TO LAYOUT ITEM PRIORITY

Priority	Description
High	Items of high priority must be followed by the customer. If not, this will affect the correct operation of the Cirrus device.
Medium	Items of Medium priority, if not followed may potentially affect the performance of the Cirrus device.
Low	Items of Low priority are listed as a 'good practice' measure.

SYSTEM ESD GUIDELINES FOR HEADSET

ESD PROTECTION DIODES

The customer should make sure the response time of any ESD protection Diodes used can protect the system for a broad spectrum of ESD transient pulses, from very fast, to extremely slow for large and small ESD voltages.

When testing ESD performance of a system, testing with different contact discharge waveforms from 500V to 8kV in incremental steps, helps verify the selected ESD protection devices can sufficiently protect the system.

BOARD SCHEMATIC OPTIMIZATION

Component placement and board layout are as important as selecting the most suitable ESD protection components. Figure 1 shows a typical combined ESD and EMI circuit protection for a headphone output.

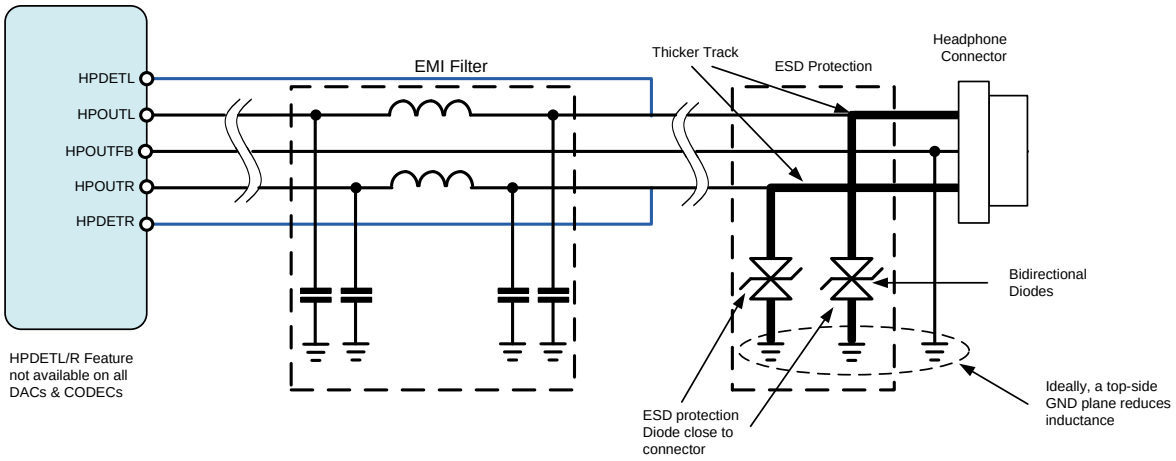


Figure 1 combined ESD and EMI protection

POSITION OF ESD PROTECTION COMPONENTS

PCB layout is critical when using ESD protection components. The ESD protection device should protect the whole PCB, not just the Cirrus Logic device, by diverting the discharge to ground and not letting it pass through the ICs. The following guidelines, as well as any stated on the ESD protection devices manufacturer's datasheet for ESD protection should be followed:

1. The ESD protection device should be placed as close to the connector as possible.
2. The ESD protection device should be placed on the line to be protected, *not* joined by a track stub, which adds inductance
3. The ESD protection device must have a short return path to ground to reduce inductance. A good way to achieve this is to place a pair of GND vias as close as possible to the GND pin of the ESD protection device and the GND pin of the connector, as shown in Figure 2. The double via technique reduces inductance. The best way to achieve it is a GND plane added to the top side of the PCB, to link the ESD diode and connector, as shown in Figure 3. This top side plane must have several vias to the main PCB GND plane in case the discharge path from the connector goes to another part of the end-product.
4. Don't share the GND return path between more than one ESD protection devices, unless it is via a low inductance GND plane.
5. Wide signal tracks from the connector to the protection device reduce the inductance for the ESD charge.
6. Figure 2 and Figure 3 below summaries the above suggestions

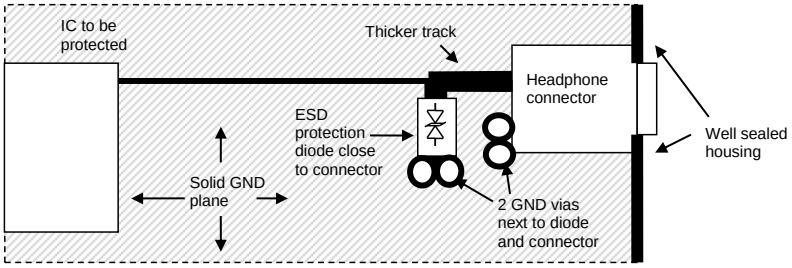


Figure 2 simplistic diagram showing placement of ESD protection diode

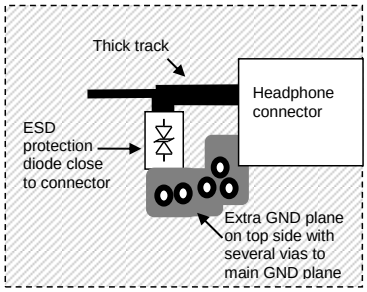


Figure 3 Best practice of top side GND plane between ESD diode and connector

Please consult the datasheet of the ESD protection diode for further advice.

TECHNICAL SUPPORT

If you require more information or require technical support, please contact one of the Cirrus Logic regional offices. To find one nearest you, go to www.cirrus.com.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.