

Fractional-N Clock Synthesizer and Clock Multiplier

Features

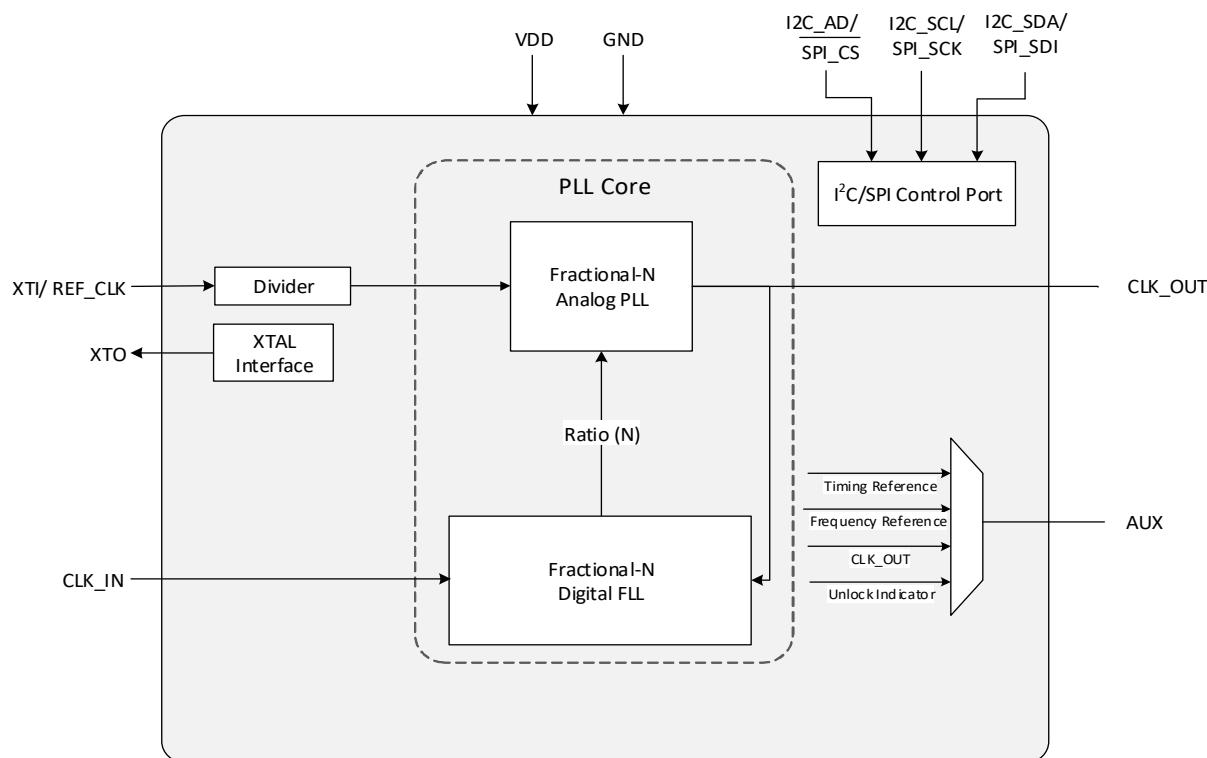
- Frequency synthesizer based on delta-sigma fractional-N analog PLL
 - Generates a low-jitter 6–75 MHz clock (CLK_OUT) from 8–75 MHz timing reference clock (REF_CLK)
- Clock multiplier and jitter reduction based on hybrid PLL
 - Generates a low-jitter 6–75 MHz clock (CLK_OUT) from a jittery or intermittent 50 Hz–30 MHz input clock source (CLK_IN)
- Highly accurate PLL multiplication factor
 - Less than 1 PPM
- I²C/SPI control port
- Configurable auxiliary output
- Flexible sourcing of timing reference clock
 - External clock and external crystal
- Period jitter of 40 ps_{RMS} for REF_CLK

- Minimal board space required
 - No external analog loop-filter components

- Glitchless clock outputs derived from an intermittent input clock

Applications

- Digital audio systems
- Network and USB audio interfaces
- IoT sensor and transducer systems
- Embedded systems
- Automotive audio systems



Target Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product.

General Description

The CS2500 is a system-clocking device that uses a programmable phase-locked loop (PLL). The hybrid analog/digital PLL architecture comprises a delta-sigma fractional-N analog PLL and a digital frequency-locked loop (FLL). The CS2500 enables frequency synthesis and clock generation from a stable timing reference clock. The device can generate low-jitter clocks from a noisy input clock source at frequencies as low as 50 Hz. The CS2500 can be configured using a control interface supporting I²C and SPI modes of operation.

The CS2500 can be powered from a single 1.8 V or 3.3 V supply. The device combines high performance with low power consumption.

The CS2500 is available in commercial-grade, 10-pin TSSOP package for operation from –40°C to +85°C. The device is also available in the AEC-Q100-qualified grade-2 package for operation from –40°C to +105°C.

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1 Pin Assignments and Descriptions

These sections show pin assignments and describe pin functions.

1.1 TSSOP Package Drawing (Top View, Through Package)

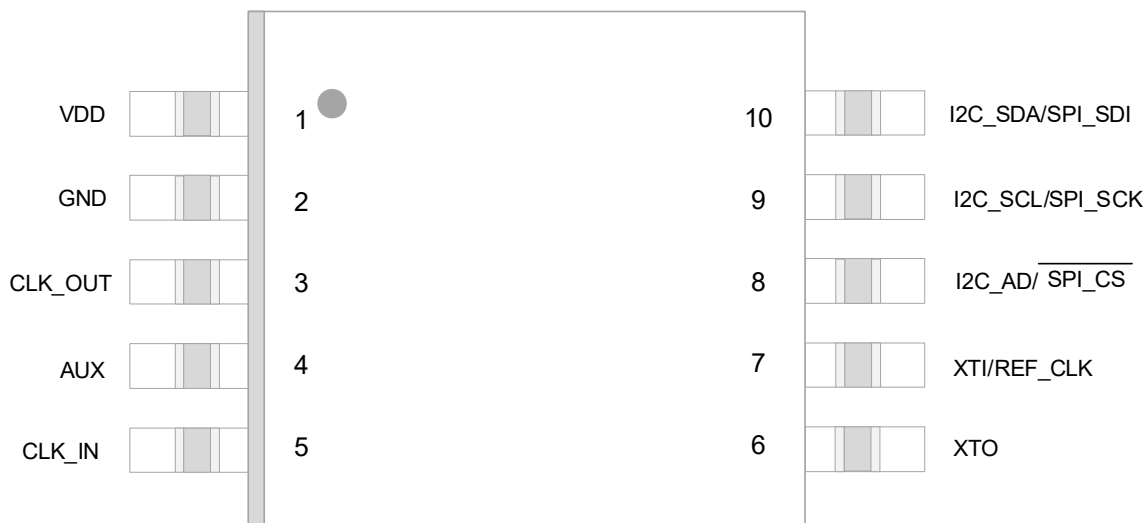


Figure 1-1. TSSOP 10-Pin Package Assignments (Top View, Through-Package)

1.2 Pin Descriptions

Table 1-1. Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description	Internal Connection	State at Reset
VDD	1	—	—	Power Supply. 3.3 V/1.8 V supply for the digital and analog blocks.	—	—
GND	2	—	—	Ground.	—	—
CLK_OUT	3	VDD	O	Clock Output. PLL clock output.	—	—
AUX	4	VDD	O	Auxiliary Output. Configurable input/output clock or status output.	—	—
CLK_IN	5	VDD	I	Clock Input. Frequency reference input for the digital PLL.	—	—
XTO	6	VDD	I/O	Crystal Connection. Output for an external crystal to generate the low-jitter PLL input clock.	—	—
XTI/REF_CLK	7	VDD	I	Crystal Connection. Input for an external crystal to generate the low-jitter PLL input clock. Reference Clock. External low-jitter timing reference input clock.	—	—
I2C_AD/SPI_CS	8	VDD	I	I2C Control-Port Address. Chip address input for the I2C interface. SPI Control-Port Chip Select. Active-low chip select input for the SPI interface.	—	—
I2C_SCL/SPI_SCK	9	VDD	I	I2C Control-Port Clock. Clock input for the I2C interface. SPI Control-Port Clock. Clock input for the SPI interface.	—	—
I2C_SDA/SPI_SDI	10	VDD	I/O	I2C Control-Port Data. Data input/output for the I2C interface. SPI Control-Port Serial Data In. SPI data input.	—	—

1.3 Electrostatic Discharge (ESD) Protection Circuitry



ESD-sensitive device. The CS2500 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is to be qualified to current JEDEC ESD standards.

2 Typical Connection Diagram

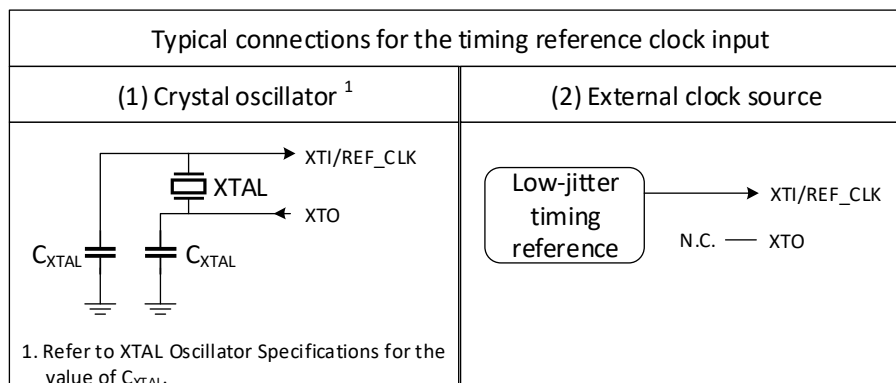
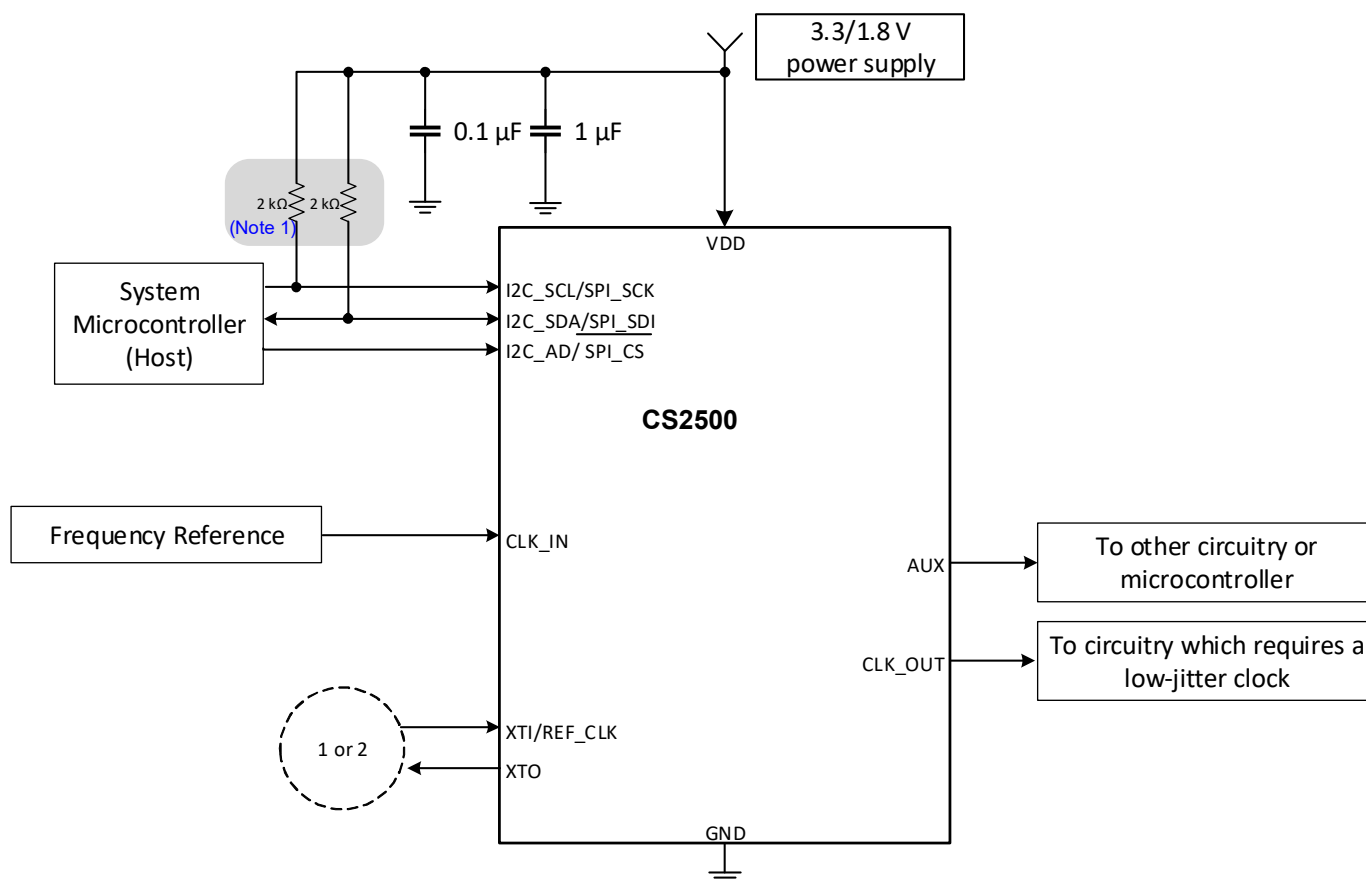


Figure 2-1. Typical Connection Diagram

Notes referenced in the typical connection diagrams:

1. The pull-up resistors are required only for I²C operation.

3 Characteristics and Specifications

Table 3-1. Recommended Operating Conditions

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters	Symbol	Min	Typ	Max	Units
DC power supply ¹	VDD	3.1	3.3	3.5	V
		1.77	1.8	1.89	V
Supply ramp up/down	t _{PWR-UD}	0.01	—	10	ms
Ambient temperature	T _A	Commercial Grade	—	85	°C
		AEC-Q100 Grade2	—	105	°C

1. The system can be either powered with a 3.3 V or a 1.8 V DC power supply.

Table 3-2. Absolute Maximum Ratings

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters	Symbol	Min	Max	Units
DC power supply	VDD	−0.3	4.32	V
External voltage applied to digital input/output	V _{INDI}	−0.3	VDD + 0.3	V
Input current	I _{IN}	—	±10	mA
Ambient temperature	T _A	−55	125	°C
Storage temperature	T _{STG}	−65	150	°C

Table 3-3. DC Electrical Characteristics

Test Conditions (unless specified otherwise): VDD = 3.3 V; T_A = 25°C; timing reference = external REF_CLK.

Parameters	Symbol	Min	Typ	Max	Units
Power supply current – unloaded ¹	I _{VDD}	—	3.94	TBD	mA
Power dissipation – unloaded	P _D	—	13	TBD	mW
Input leakage current (per pin)	I _{IN}	—	—	±10	μA
Input capacitance (per pin)	I _C	—	—	5	pF
High-level input voltage	V _{IH}	0.70 × VDD	—	—	V
Low-level input voltage	V _{IL}	—	—	0.30 × VDD	V
High-level output voltage	V _{OH}	0.90 × VDD	—	—	V
Low-level output voltage	V _{OL}	—	—	0.10 × VDD	V

1. To calculate the additional current consumption due to loading (per output pin), multiply clock output frequency by load capacitance (C_L) and power supply voltage (VDD).

Table 3-4. AC Electrical Characteristics

Test Conditions (unless specified otherwise): VDD = 3.3 V; T_A = −40°C to 85°C (commercial grade); T_A = −40°C to 105°C (AEC-Q100 grade-2); Load capacitance (C_L) = 15 pF.

Parameters		Symbol	Min	Typ	Max	Units
Crystal frequency Fundamental mode XTAL	RefClkDiv[1:0] = 10	f _{XTAL}	8	—	18.75	MHz
	RefClkDiv[1:0] = 01		16	—	37.50	MHz
	RefClkDiv[1:0] = 00		32	—	50	MHz
	Drive power		—	—	100	μW
	Negative resistance		500	—	—	Ω
	Maximum capacitance (C _{XTAL}) ¹		—	—	50	pF
Reference clock input frequency	RefClkDiv[1:0] = 10	f _{REF_CLK}	8	—	18.75	MHz
	RefClkDiv[1:0] = 01		16	—	37.50	MHz
	RefClkDiv[1:0] = 00		32	—	75	MHz
Reference clock input duty cycle		D _{REF_CLK}	45	—	55	%
Clock input frequency		f _{CLK_IN}	50	—	30 × 10 ⁶	Hz
Clock input pulse width ²	f _{CLK_IN} < f _{SYS_CLK} / 96	pw _{CLK_IN}	2	—	—	UI
	f _{CLK_IN} > f _{SYS_CLK} / 96		10	—	—	ns
PLL clock output frequency ³		f _{CLK_OUT}	6	—	75	MHz
PLL clock output duty cycle	Measured at VDD / 2	t _{OD}	45	50	55	%
Clock output rise time	20% to 80% of VDD	t _{OR}	—	1.7	3.0	ns
Clock output fall time	80% to 20% of VDD	t _{OF}	—	1.7	3.0	ns
Period jitter ⁴	REF_CLK	t _{JIT}	—	40	—	ps _{RMS}

Table 3-4. AC Electrical Characteristics (Cont.)

Test Conditions (unless specified otherwise): VDD = 3.3 V; T_A = –40°C to 85°C (commercial grade); T_A = –40°C to 105°C (AEC-Q100 grade-2); Load capacitance (C_L) = 15 pF.

Parameters	Symbol	Min	Typ	Max	Units
Baseband TIE jitter (100 Hz to 40 kHz) ^{4, 5}	REF_CLK	—	50	—	ps _{RMS}
Wideband TIE jitter (100 Hz Corner) ^{4, 6}	REF_CLK	—	165	—	ps _{RMS}
PLL lock time – CLK_IN ⁷	f _{CLK_IN} < 200 kHz	—	100	200	UI
	f _{CLK_IN} > 200 kHz	—	1	3	ms
PLL lock time – REF_CLK	f _{REF_CLK} = 8 to 75 MHz	—	1	3	ms
Output frequency resolution ^{4, 8}	High resolution	0	—	±0.50	ppm
	High multiplication	0	—	±112	ppm
Time to first locked clock output ⁹	After boot-up	—	—	20	ms
Maximum output frequency deviation ¹⁰	—	—	—	TBD	%

1. Refer to XTAL oscillator specifications for the value of C_{XTAL}.

2. UI (unit interval) corresponds to t_{SYS_CLK} or 1 / f_{SYS_CLK}.

3. f_{CLK_OUT} = 75 MHz is ratio-limited when f_{CLK_IN} is below 72 Hz (high multiplication) or 18.3 kHz (high precision).

4. REF_CLK is a 12 MHz timing reference clock. If the phase noise of REF_CLK is 20 dB lower than the output clock's noise across the bandwidth spectrum, the clock is considered jitter-free. The clock output frequency (f_{CLK_OUT}) is 24.576 MHz and sample size is 10000.

5. 3rd order 100 Hz – 40 kHz bandpass filtered according to AES-12id-2020 section 3.4.2.

6. 3rd order 100 Hz high pass filtered according to AES-12id-2020 section 3.4.1.

7. UI corresponds to t_{CLK_IN} or 1 / f_{CLK_IN}.

8. The frequency accuracy of the PLL clock output is directly proportional to the accuracy of the input clocks.

9. The time to first locked clock o/p is calculated for f_{CLK_IN} = 48 kHz and lock time = 100 UI.

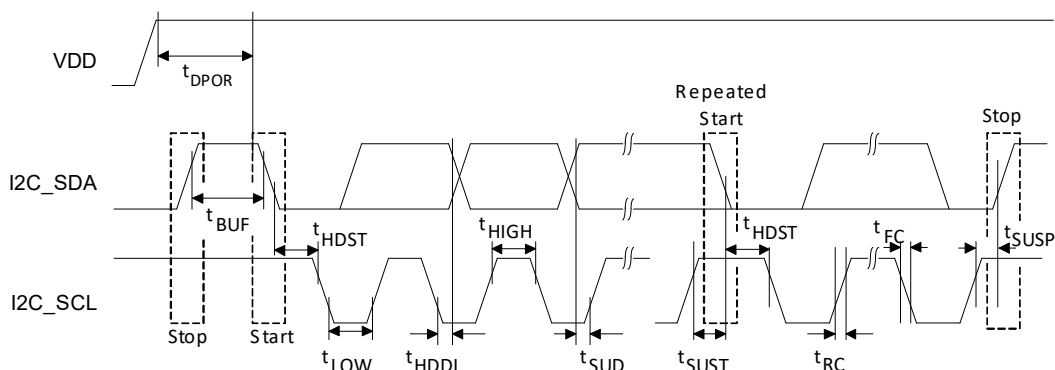
10. This parameter refers to the maximum frequency deviation in the Multiplier mode after the CLK_IN signal is lost and before the dynamic ratio is fixed.

Table 3-5. Switching Specifications—I2C Control Port

Test conditions (unless specified otherwise): VDD = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds; T_A = 25°C.

Parameters ¹	Symbol	Min	Max	Units
SCL clock frequency	f _{SCL}	—	100	kHz
Clock low time	t _{LOW}	4.7	—	μs
Clock high time	t _{HIGH}	4.0	—	μs
Start condition hold time (before first pulse clock)	t _{HDST}	4.0	—	μs
Setup time for repeated start	t _{SUST}	4.7	—	μs
Rise time of SCL and SDA	t _{RC}	—	1	μs
Fall time SCL and SDA	t _{FC}	—	300	ns
Setup time for stop condition	t _{SUSP}	4.7	—	μs
SDA setup time to SCL rising	t _{SUD}	250	—	ns
SDA input hold time from SCL falling ²	t _{HDDI}	0	—	ns
Bus free time between transmissions	t _{BUF}	4.7	—	μs
Acknowledge delay from SCL falling	t _{ACK}	300	1000	ns
Delay from supply voltage stable to control port ready	t _{DPOR}	—	200	μs

1. I2C control-port timing. {150}



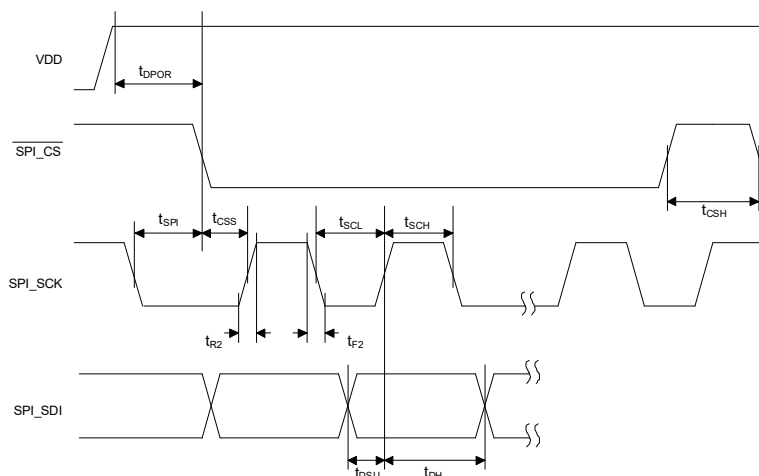
2. Data must be held long enough to bridge the transition time (t_{FC}) of SCL.

Table 3-6. Switching Specifications—SPI Control Port

Test conditions (unless specified otherwise): VDD = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds; T_A = 25°C.

Parameters ¹	Symbol	Min	Max	Units
SCK clock frequency	f _{SCL}	—	6	MHz
SCK edge to $\overline{\text{CS}}$ falling ²	t _{SP1}	500	—	ns
$\overline{\text{CS}}$ high time between transmissions	t _{CSH}	1	—	μs
$\overline{\text{CS}}$ falling to SCK rising edge	t _{CSS}	20	—	ns
SCK pulse width low	t _{SCL}	66	—	ns
SCK pulse width high	t _{SCH}	66	—	ns
SDI to SCK rising setup time	t _{DSU}	40	—	ns
SCK rising to SDI hold time ³	t _{DH}	15	—	ns
Rise time of SCK and SDI ⁴	t _{R2}	—	100	ns
Fall time of SCK and SDI ⁴	t _{F2}	—	100	ns
Delay from supply voltage stable to control port ready ⁵	t _{DPOR}	—	200	μs

1. SPI control-port timing. {172}



2. t_{SP1} is only needed before first falling edge of $\overline{\text{CS}}$ after power is applied; t_{SP1} is 0 all other times.

3. Data must be held for sufficient time to bridge the transition time of SCK.

4. For f_{SCK} < 1 MHz.

5. The supply voltage is considered stable after VDD is within the specified operating conditions (see Table 3-4).

4 Revision History

Table 4-1. Revision History

Revision	Change
R2 JUL 2023	• Initial revision

Important:

Please check to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

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