CS2600

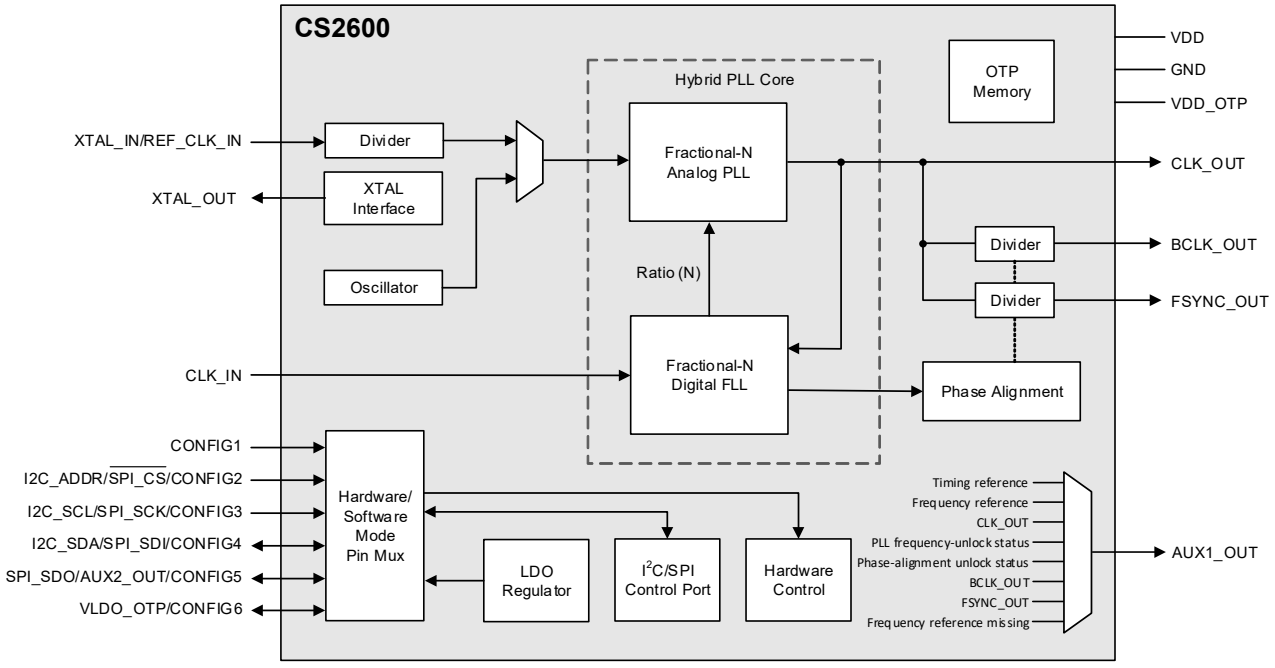
Fractional-N Clock Synthesizer and Multiplier

Features

- Clock frequency synthesizer incorporating delta-sigma fractional-N analog PLL
  - Generates low-jitter 6–75 MHz clock (CLK_OUT) from 8–75 MHz timing reference (REF_CLK_IN)
- Fractional clock multiplier and jitter reduction using hybrid analog/digital PLL
  - Generates low-jitter 6–75 MHz clock (CLK_OUT), synchronized to a 50 Hz–30 MHz low-quality or intermittent frequency reference (CLK_IN)
- Flexible timing reference source
  - External clock, external crystal, or built-in oscillator
- High resolution PLL ratio (1 PPM)
- 40 ps_{RMS} period jitter (external timing reference), 35 ps_{RMS} period jitter (oscillator reference)
- Glitchless clock output generated from intermittent input
- BCLK and FSYNC outputs (derived from CLK_OUT) for digital audio applications
  - Phase alignment with CLK_IN frequency reference
- Automatic rate control (ARC) for digital audio applications
  - Seamless transitions through changes in CLK_IN frequency reference
- Customer-programmable startup configuration, using integrated one-time programmable (OTP) memory
- Hardware and software control modes
  - I²C/SPI control port
  - Hardware control with no host processor required
- Configurable auxiliary clock/status output
- Minimal board space required
  - No external analog loop-filter components
- Single-supply operation at 1.8 V or 3.3 V

Applications

- Automotive audio systems
- Digital audio systems
- Network and USB audio interfaces
- IoT sensor and transducer systems
- Embedded systems



Advanced Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product.

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General Description

The CS2600 is a system-clocking device incorporating a programmable phase-locked loop (PLL). The hybrid analog/digital PLL architecture comprises a delta-sigma fractional-N analog PLL and a digital frequency-locked loop (FLL). The CS2600 enables frequency synthesis and clock generation from a stable timing reference clock. The device can generate low-jitter clocks from a noisy clock reference at frequencies as low as 50 Hz. An internal oscillator can provide the timing reference clock, enabling a reduction in external component requirements. The CS2600 can be configured using a control interface supporting I²C and SPI modes of operation. The device can also be configured in Hardware Control Mode using pull-up/pull-down resistors, reducing system software overhead.

The CS2600 supports BCLK and FSYNC outputs, derived from the PLL output signal. All of the clock outputs can be phase-aligned with the clock input source. The automatic rate control (ARC) function detects the clock input frequency and configures the PLL ratio for the required output. The ARC supports seamless transitions through changes in the reference frequency; the BCLK and FSYNC outputs are automatically adjusted to maintain the applicable ratios.

The CS2600 provides a built-in OTP memory to configure the default operating settings, loaded at boot-up. The OTP memory is optimized and managed to support multiple programming cycles.

The CS2600 can be powered from a single 1.8 V or 3.3 V supply. The device combines high performance with low power consumption.

The CS2600 is available in commercial-grade 16-pin QFN package for operation from –40°C to +85°C. The device is also available in the AEC-Q100-qualified grade-2 package for operation from –40°C to +105°C.

Table of Contents

1 Pin Assignments and Descriptions

These sections show pin assignments and describe pin functions.

1.1 QFN Pin Assignments (Top View, Through Package)

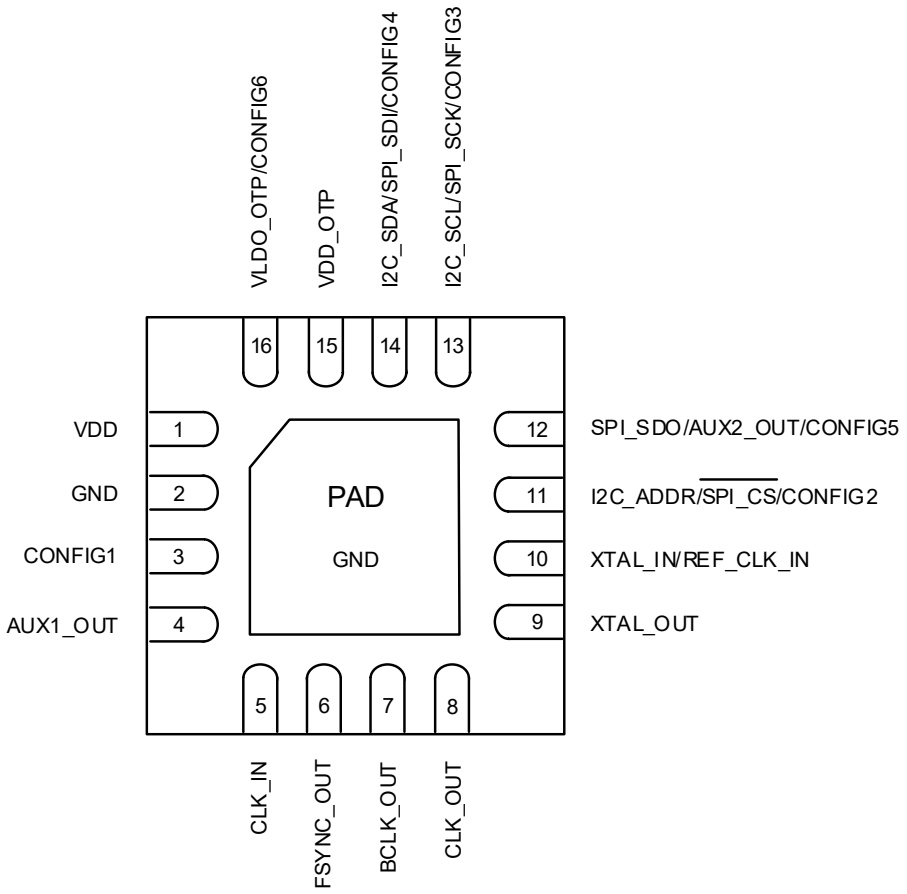


Figure 1-1. QFN 16-Pin Diagram (Top View, Through-Package)

1.2 Pin Descriptions

Table 1-1. Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description
VDD	1	—	—	**Power Supply.** 3.3 V/1.8 V supply for the digital and analog blocks.
GND	2, PAD	—	—	**Ground and Pad.** The paddle must be connected to ground plane directly underneath the CS2600.
CONFIG1	3	VDD	I	**Hardware Configuration 1.** Hardware Control Mode configuration connection. Connect to GND for Software Control Mode.
AUX1_OUT	4	VDD	O	**Auxiliary Output.** Configurable clock output or status output.
CLK_IN	5	VDD	I	**Clock Input.** Frequency reference input for the digital FLL.
FSYNC_OUT	6	VDD	O	**FSYNC Output.** PLL frame sync clock output (CLK_OUT derived), which can be phase-aligned with CLK_IN.
BCLK_OUT	7	VDD	O	**BCLK Output.** PLL bit clock output (CLK_OUT derived), which can be phase-aligned with CLK_IN.
CLK_OUT	8	VDD	O	**Clock Output.** PLL clock output.

Table 1-1. Pin Descriptions *(Cont.)*

Pin Name	Pin #	Power Supply	I/O	Description
XTAL_OUT	9	VDD	O	**Crystal Connection.** Output for an external crystal. Connect to GND for internal oscillator reference clock.
XTAL_IN/REF_CLK_IN	10	VDD	I	**Crystal Connection.** Input for an external crystal. **Reference Clock.** External low-jitter timing reference clock input. Connect to GND for internal oscillator reference clock.
I2C_ADDR/$\overline{\text{SPI\_CS}}$/CONFIG2	11	VDD	I	**I²C Control-Port Address.** Chip address input for the I²C interface. **SPI Control-Port Chip Select.** Active-low chip select input for the SPI interface. **Hardware Configuration 2.** Hardware Control Mode configuration connection.
SPI_SDO/AUX2_OUT/CONFIG5	12	VDD	I/O	**SPI Control-Port Serial Data Out.** SPI data output. **Auxiliary Output 2.** Configurable status output. **Hardware Configuration 5.** Hardware Control Mode configuration connection.
I2C_SCL/SPI_SCK/CONFIG3	13	VDD	I	**I²C Control-Port Clock.** Clock input for the I²C interface. **SPI Control-Port Clock.** Clock input for the SPI interface. **Hardware Configuration 3.** Hardware Control Mode configuration connection.
I2C_SDA/SPI_SDI/CONFIG4	14	VDD	I/O	**I²C Control-Port Data.** Data input/output for the I²C interface. **SPI Control-Port Serial Data In.** SPI data input. **Hardware Configuration 4.** Hardware Control Mode configuration connection.
VDD_OTP	15	—	—	**OTP Programming Supply (Input).** If VDD = 1.8 V, an external programming supply is required when writing to the OTP memory. This supply can be generated internally if VDD = 3.3 V.
VLDO_OTP/CONFIG6	16	VDD	I/O	**OTP Programming Supply (Output).** OTP programming regulator output (VDD = 3.3 V). **Hardware Configuration 6.** Hardware Control Mode configuration connection.

1.3 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS2600 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

2 Typical Connections

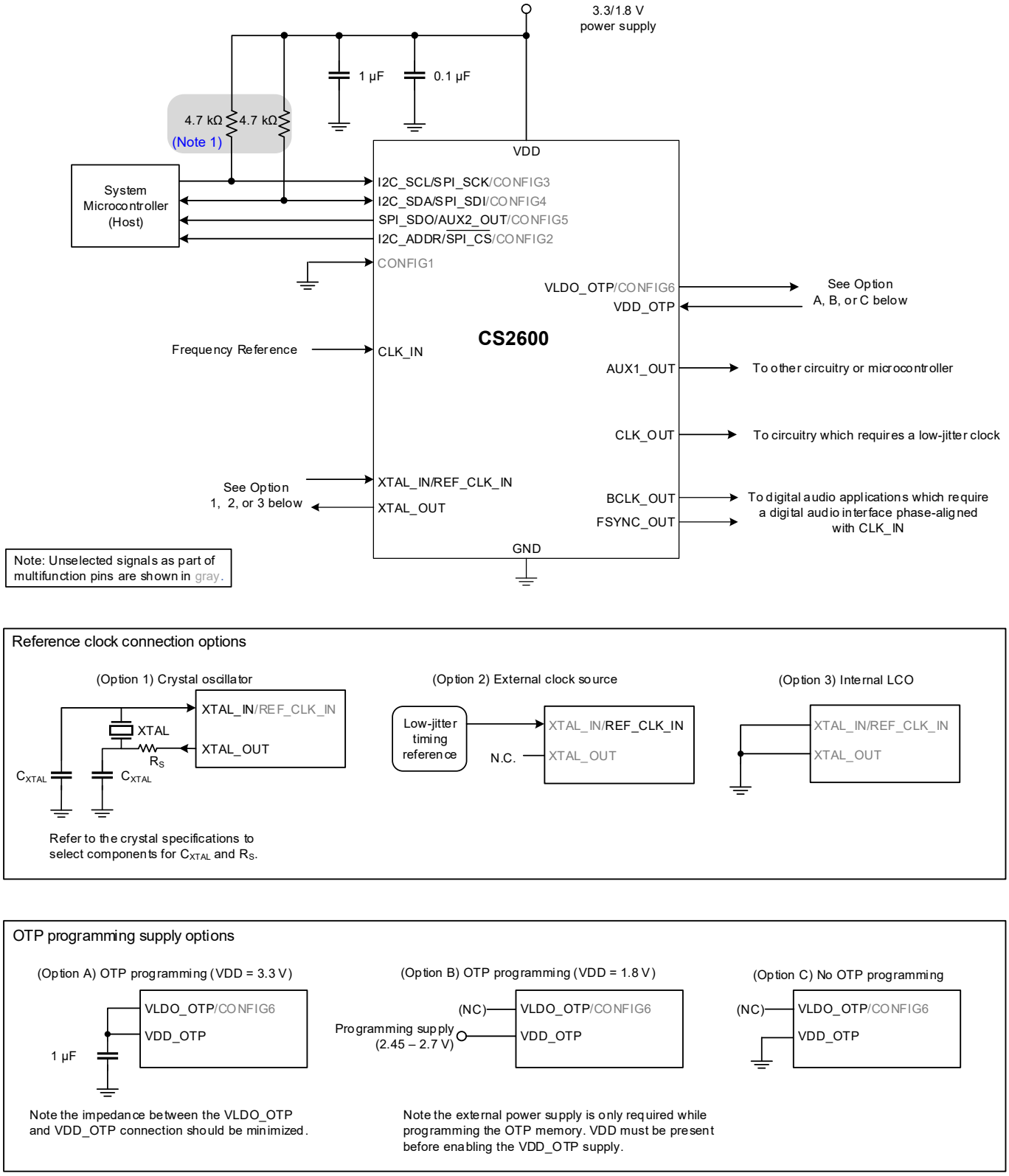


Figure 2-1. Typical Connection Diagram—Software Control Mode

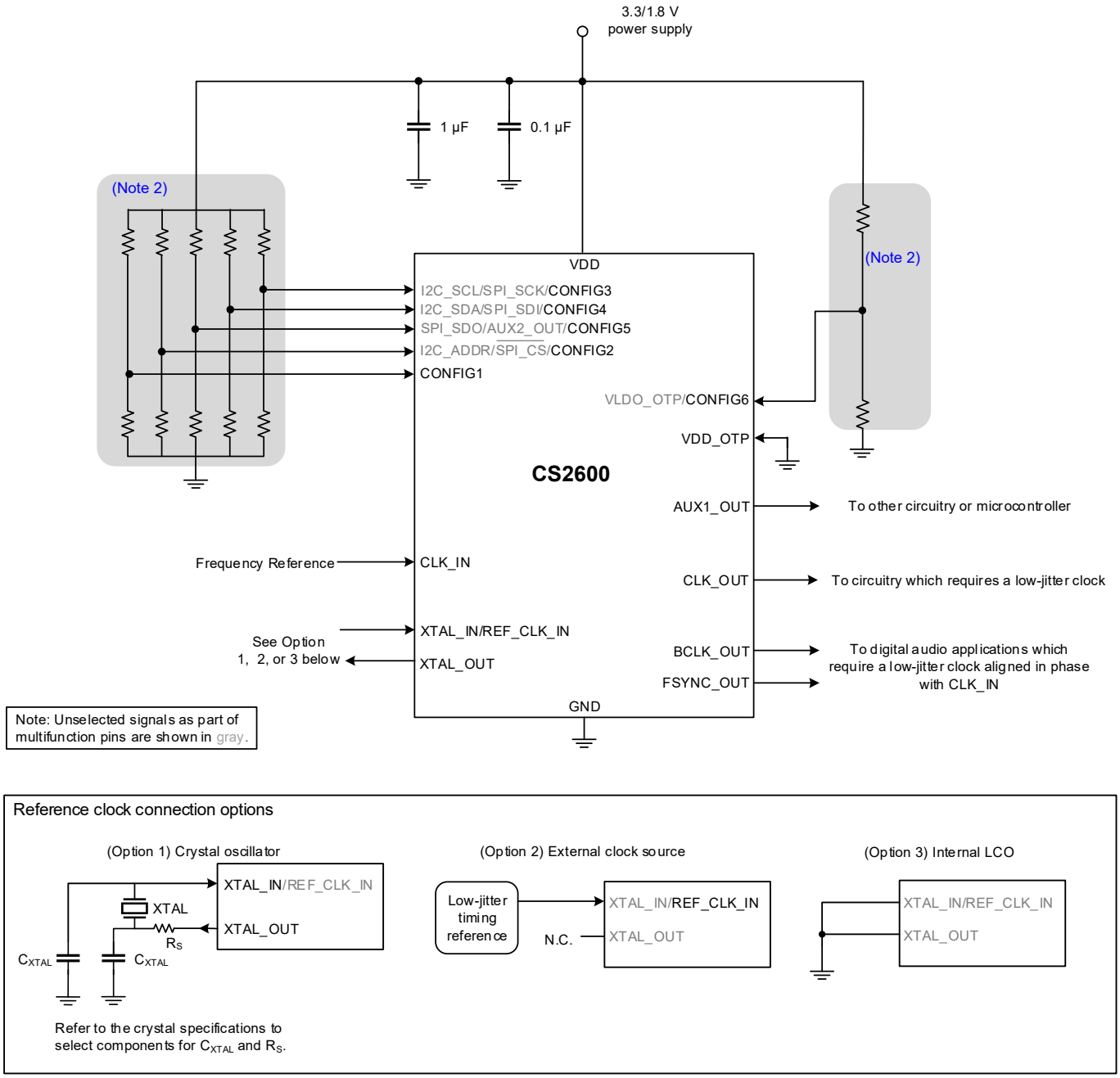


Figure 2-2. Typical Connection Diagram—Hardware Control Mode

Notes referenced in the typical connection diagrams:

1. The pull-up resistors are required only for I²C operation. The diagram shows 4.7 kΩ pull-up, but higher impedance can be supported depending on clock speed and bus capacitance.
2. Each hardware pin is configured using a pull-up to VDD or pull-down to GND, supporting up to eight configuration options per pin.

3 Characteristics and Specifications

Table 3-1. Recommended Operating Conditions

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters	Symbol	Min	Typ	Max	Units
DC power supply	VDD	3.1	3.3	3.5	V
		1.71	1.8	1.89	V
OTP programming supply [1,2]	VDD_OTP	2.45	—	2.7	V
Supply ramp up/down (all supplies)	t_{PWR_UD}	0.01	—	10	ms
Ambient temperature — Commercial Grade	T_A	–40	—	85	°C
Ambient temperature — AEC-Q100 Grade 2		–40	—	105	°C

1. The OTP programming supply can be generated by an internal LDO, or else powered externally. To use the internal LDO, the VDD_OTP pin must be connected to VLDO_OTP. If VDD < 3.1 V, the OTP programming supply must be powered externally. If OTP programming is not required, VDD_OTP should be connected to GND.
2. VDD must be present before enabling the VDD_OTP supply. VDD_OTP must be removed before powering down VDD.

Table 3-2. Absolute Maximum Ratings

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters	Symbol	Min	Max	Units
DC power supply	VDD	–0.3	4.32	V
OTP programming supply	VDD_OTP	–0.3	2.75	V
External voltage applied to digital input/output	V_{INDI}	–0.3	VDD + 0.3	V
Input current	I_{in}	—	±10	mA
Ambient temperature	T_A	–55	125	°C
Storage temperature	T_{STG}	–65	150	°C

Table 3-3. DC Electrical Characteristics

Test Conditions (unless specified otherwise): T_A = 25°C; timing reference = 12 MHz (external clock or crystal).

Parameters	Symbol	Min	Typ	Max	Units
Power supply current—unloaded [1]	I_{VDD}	—	4	—	mA
OTP programming supply current	I_{VDD_OTP}	—	—	25	mA
Input leakage current (per pin)	I_{IN}	—	—	±10	µA
Input capacitance (per pin)	I_C	—	—	5	pF
High-level input voltage	V_{IH}	0.70 × VDD	—	—	V
Low-level input voltage	V_{IL}	—	—	0.30 × VDD	V
High-level output voltage	V_{OH}	0.90 × VDD	—	—	V
Low-level output voltage	V_{OL}	—	—	0.10 × VDD	V

1. To calculate the additional current consumption due to loading (per output pin), multiply clock output frequency by load capacitance (C_L) and power supply voltage (VDD).

Table 3-4. AC Electrical Characteristics

Test Conditions (unless specified otherwise): T_A = –40°C to 85°C (commercial grade); T_A = –40°C to 105°C (AEC-Q100 grade-2); Load capacitance (C_L) = 15 pF.

Parameters		Symbol	Min	Typ	Max	Units
Crystal frequency	REF_CLK_IN_DIV = 10 REF_CLK_IN_DIV = 01 REF_CLK_IN_DIV = 00	f_{XTAL}	8 16 32	— — —	18.75 37.50 50	MHz MHz MHz
Reference clock input frequency	REF_CLK_IN_DIV = 10 REF_CLK_IN_DIV = 01 REF_CLK_IN_DIV = 00	$f_{REF\_CLK\_IN}$	8 16 32	— — —	18.75 37.50 75	MHz MHz MHz
Reference clock input duty cycle		$D_{REF\_CLK\_IN}$	45	—	55	%
Clock input frequency		f_{CLK_IN}	50	—	30×10^6	Hz
Clock input pulse width	$f_{CLK\_IN} < f_{SYSCLK} / 96$ [1] $f_{CLK\_IN} > f_{SYSCLK} / 96$ [1]	pw_{CLK_IN}	2 10	— —	— —	UI [2] ns
CLK_OUT frequency range		f_{CLK_OUT}	6	—	75	MHz
BCLK frequency range		f_{BCLK_OUT}	$f_{CLK\_OUT} / 48$	—	f_{CLK_OUT}	MHz
FSYNC frequency range		f_{FSYNC_OUT}	$f_{CLK\_OUT} / 1536$	—	$f_{CLK\_OUT} / 16$	MHz
Clock output duty cycle	measured at VDD / 2	t_{OD}	45	50	55	%
Clock output rise time	10% to 90% of VDD	t_{OR}	—	2.5	—	ns
Clock output fall time	90% to 10% of VDD	t_{OF}	—	2.5	—	ns
CLK_OUT period jitter [3,4]	external timing reference internal oscillator reference	t_{JIT}	— —	40 35	TBD TBD	ps_{RMS} ps_{RMS}
CLK_OUT baseband TIE jitter [3,5]	external timing reference internal oscillator reference	—	— —	50 300	TBD TBD	ps_{RMS} ps_{RMS}
CLK_OUT wideband TIE jitter [3,6]	external timing reference internal oscillator reference	—	— —	165 300	TBD TBD	ps_{RMS} ps_{RMS}
PLL lock time—Multiplier Mode	f_{CLK_IN} < 200 kHz f_{CLK_IN} > 200 kHz	t_{LC}	— —	100 1	200 3	UI [7] ms
PLL lock time—Synthesizer Mode	$f_{REF\_CLK\_IN}$ = 8 to 75 MHz	t_{LR}	—	1	3	ms
CLK_OUT frequency resolution [3,8]	high resolution high multiplication	—	— —	1 224	— —	ppm ppm
Oscillator frequency	at 25°C	—	11.76	12.0	12.24	MHz
Oscillator frequency thermal sensitivity	at 25°C	—	—	50	—	ppm/°C
Oscillator frequency stability (relative to 25°C)	–40 to 85°C –40 to 105°C	—	–0.2 –0.2	— —	0.4 0.6	% %
Phase alignment error	CLK_IN to FSYNC	—	—	±0.5	—	UI [9]
Clock output skew	CLK_OUT, BCLK, and FSYNC	—	—	—	±0.5	ns
Clock output frequency deviation	CLK_IN stopped, holdover enabled	—	—	—	0.1	%
Start-up time [10]	from VDD applied	—	—	—	20	ms

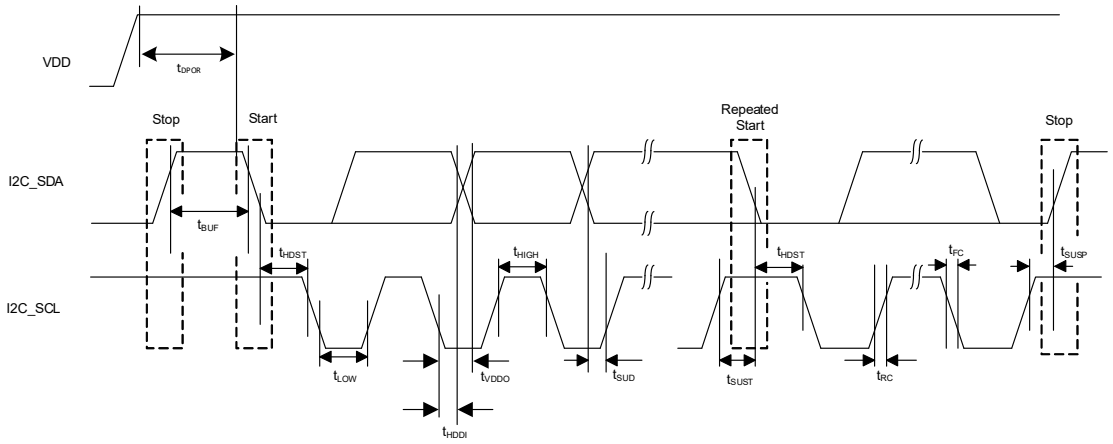
1. The internal timing reference clock (SYSCLK) is derived from REF_CLK_IN.
2. UI (unit interval) corresponds to t_{SYSCLK} or 1 / f_{SYSCLK}.
3. REF_CLK_IN is a 12 MHz timing reference clock, with phase noise 20 dB lower than the output clock noise. The clock output frequency (f_{CLK_OUT}) is 24.576 MHz.
4. Sample size is 10000.
5. Using 3rd order 100 Hz–40 kHz bandpass filter as defined in AES-12id-2020 Section 3.4.2.
6. Using 3rd order 100 Hz high pass filter as defined in AES-12id-2020 Section 3.4.1.
7. UI (unit interval) corresponds to t_{CLK_IN} or 1 / f_{CLK_IN}.
8. The frequency accuracy of the PLL clock output is directly proportional to the accuracy of the clock input.
9. UI (unit interval) corresponds to t_{CLK_OUT} or 1 / f_{CLK_OUT}.
10. The time to first locked clock output, assuming OTP configuration for f_{CLK_IN} = 48 kHz.

Table 3-5. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds; T_A = 25°C.

Parameters [1,2]		Symbol	Min	Max	Units
SCL clock frequency		f_{SCL}	—	1000	kHz
Clock low time		t_{LOW}	500	—	ns
Clock high time		t_{HIGH}	260	—	ns
Start condition hold time (before first pulse clock)		t_{HDST}	260	—	ns
Setup time for repeated start		t_{SUST}	260	—	ns
Rise time of SCL and SDA	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{RC}	600 180 72	1000 300 120	ns ns ns
Fall time SCL and SDA	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{FC}	6.5 6.5 6.5	300 300 120	ns ns ns
Rise time variation between SDA and SCL		—	—	1.67	x
Fall time variation between SDA and SCL	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	—	— — —	100 100 75	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
SDA setup time to SCL rising		t_{SUD}	50	—	ns
SDA input hold time from SCL falling		t_{HDDI}	0	—	ns
Output data valid (Data/ACK)	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
SDA bus capacitance		C_B	—	400	pF
SCL/SDA pull-up resistance		R_P	500	—	Ω
Pulse width of spikes to be suppressed		t_{ps}	0	50	ns
Start-up time from power-up/software reset to control port ready [3]		t_{DPOR}	—	5	ms

1. The I²C control port uses a 16-bit register address and 16-bit data words.
2. I²C control-port timing.



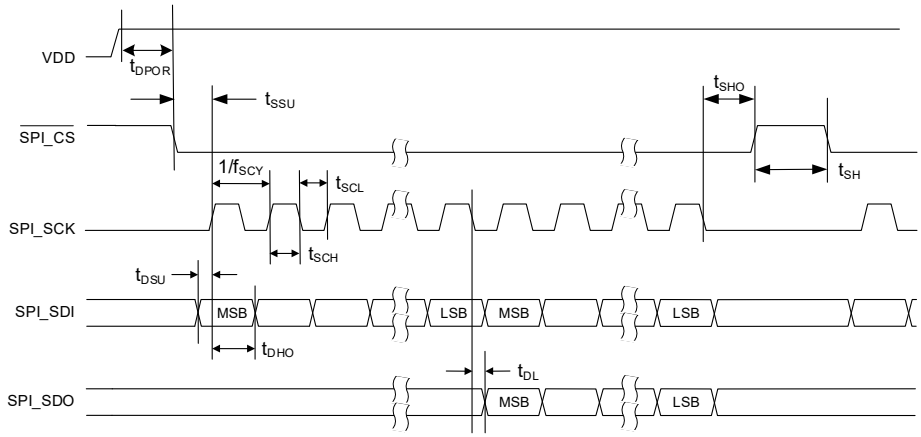
3. Time from power-up measured from when VDD is within the recommended operating conditions (see Table 3-1).

Table 3-6. Switching Specifications—SPI Control Port

Test conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds; T_A = 25°C.

Parameters [1,2]	Symbol	Min	Max	Units
SCK clock frequency — Access to OTP registers (0x2300–0x232F)	f_{SCL}	—	4.5	MHz
SCK clock frequency — Access to all other registers	f_{SCL}	—	17.5	MHz
$\overline{CS}$ falling edge to SCK rising edge	t_{SSU}	5	—	ns
SCK falling edge to $\overline{CS}$ rising edge	t_{SHO}	0.5	—	ns
SCK pulse width low	t_{SCL}	18.5	—	ns
SCK pulse width high	t_{SCH}	18.5	—	ns
SDI to SCK rising setup time	t_{DSU}	5	—	ns
SDI to SCK hold time	t_{DHO}	2.5	—	ns
SCK falling edge to SDO transition	t_{DL}	0	15	ns
$\overline{CS}$ rising edge to SDO output high-Z	—	0	20	ns
Bus free time between active $\overline{CS}$	t_{SH}	110	—	ns
Delay from supply voltage stable to control port ready [3]	t_{DPOR}	—	5	ms

1. The SPI control port uses a 15-bit register address and 16-bit data words.
2. SPI control-port timing.



3. The supply voltage is considered stable when VDD is within the recommended operating conditions (see Table 3-1).

Contacting Cirrus Logic Support

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