CS42L43

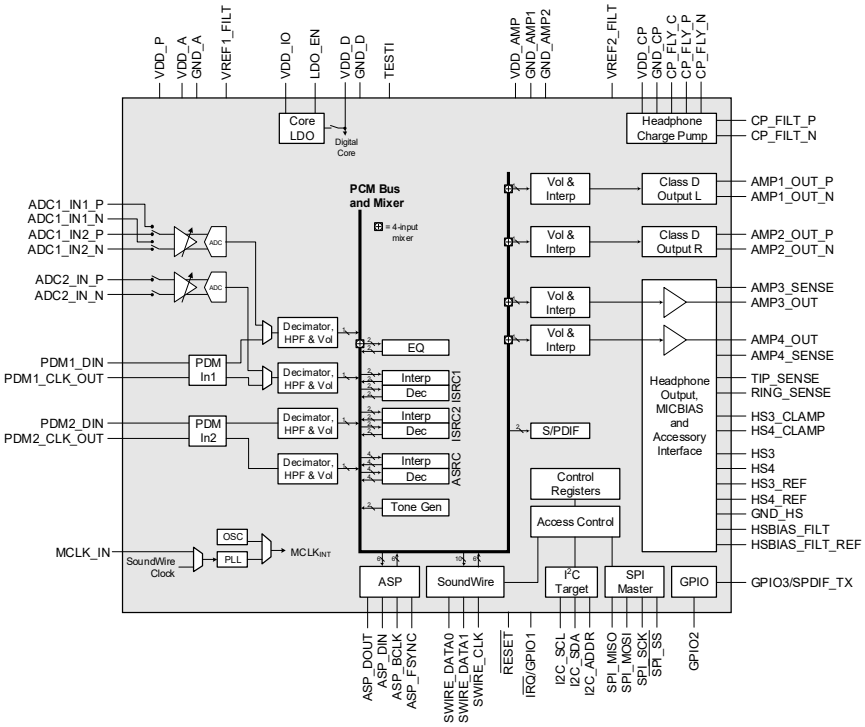
PC Codec with Headphone, MIC Interface and Class D Speaker Drivers

System Features

- Stereo headphone (HP) output with 114 dB dynamic range
  - Class H headphone amplifier with automatic or manual supply adjust
  - 2 × 33.7 mW power output at –85 dB THD+N into 30 Ω
  - 1 V_{RMS} output swing into 30 Ω loads
  - Load detection
- Mono mic/stereo line input with 94 dB dynamic range
  - Headset bias with integrated bias resistor
  - 1 V_{RMS} input voltage
  - Programmable analog front end (AFE) gain from –6 to +18 dB in 6 dB steps
- Integrated detect features
  - OMTP (Open Mobile Terminal Platform) and CTIA headset-type detection and configuration with low-impedance internal switches
  - Mic button press detect with ADC automute
  - Mic button detection compatible with Android Wired Headset Specification (Version 1.1)
  - Automatic Hi-Z of headset bias output on headset bias current drop or HP/headset unplug
- Stereo Class D Bridge-tied load (BTL) speaker driver
  - 2 W @ 1% THD+N into 4 Ω load
  - 102 dB dynamic range
- System wake from headset/headphone plug/unplug or mic button press
- Stereo three-band parametric equalizers
- I²C control supporting rates up to Fast Mode Plus
- MIPI® SoundWire® v1.2.1 interface with SDCA support
- S/PDIF transmit (Sony/Philips digital interface format)
- Integrated fractional-N PLL
  - Allows multiple clock input rates
  - Reference clock sourced from either SoundWire clock or external MCLK_IN source
- PDM input for digital microphones
- Audio serial port (ASP)
  - I²S (two channels) or TDM (up to six channels)
  - Master or Slave Mode
  - Sample rate support for 8 to 192 kHz
- Integrated power management
  - Digital core can be supplied externally, or by an internal LDO from the VDD_IO supply
  - Step-up/down charge pump improves HP efficiency
  - VDD_P monitor to detect and report brownout conditions

Applications

- Laptops, desktops, ultrabooks, and Chromebooks



PB1018R5
SEP 2025

General Description

The CS42L43 is an audio codec with integrated MIPI SoundWire interface (Version 1.2.1 compliant), I²C, SPI, and I²S/TDM interfaces designed for portable applications. It provides a high dynamic range, stereo DAC for headphone output, two integrated Class D amplifiers for loudspeakers, and two ADCs for wired headset microphone input or stereo line input. PDM inputs are provided for digital microphones.

The CS42L43 provides high performance audio capture from the ADC and PDM inputs and audio playback to the headphone DACs, Class D speaker drivers, and an IEC-60958-3-compatible S/PDIF transmitter. The CS42L43 includes assignable SRCs and an assignable stereo, three-band, 32-bit, parametric equalizer.

Digital mixers are available with independent attenuation on each mixer input.

Digital volume/mute control is available on all capture and playback paths and selectable high-pass filters are available on the capture paths for removal of DC offsets or wind noise suppression.

A headset mic bias with an integrated pull-up resistor is provided for use with the headset interface. Other headset features include automatic headset type detection (OMTP/CTIA-compliant), mic-bias/ground switching, and headset-button detection including Android Wired Headset Specification v1.1. Other features include insert/removal detection, headphone load impedance detection, and stereo line-in support.

The CS42L43 can be configured to provide a bridge between a SoundWire host and the SPI master and ASP ports. This enables non-SoundWire audio peripherals such as additional speaker amplifiers or a companion DSP to be integrated alongside a SoundWire host system.

A high performance fractional PLL is available for generating internal audio sample clocks.

The CS42L43 is available in a commercial-grade, 70-ball WLCSP (wafer-level chip scale package) and a commercial-grade, 88-pin QFN package for operation between –40°C to +85°C. Note that the WLCSP package can be routed using standard PCB with vias in many applications.

See Section 7 for ordering information.

1 Pin Assignments and Descriptions

This section shows pin assignments and describes pin functions.

1.1 WLCSP Pin Out (Through-Package, Top View)

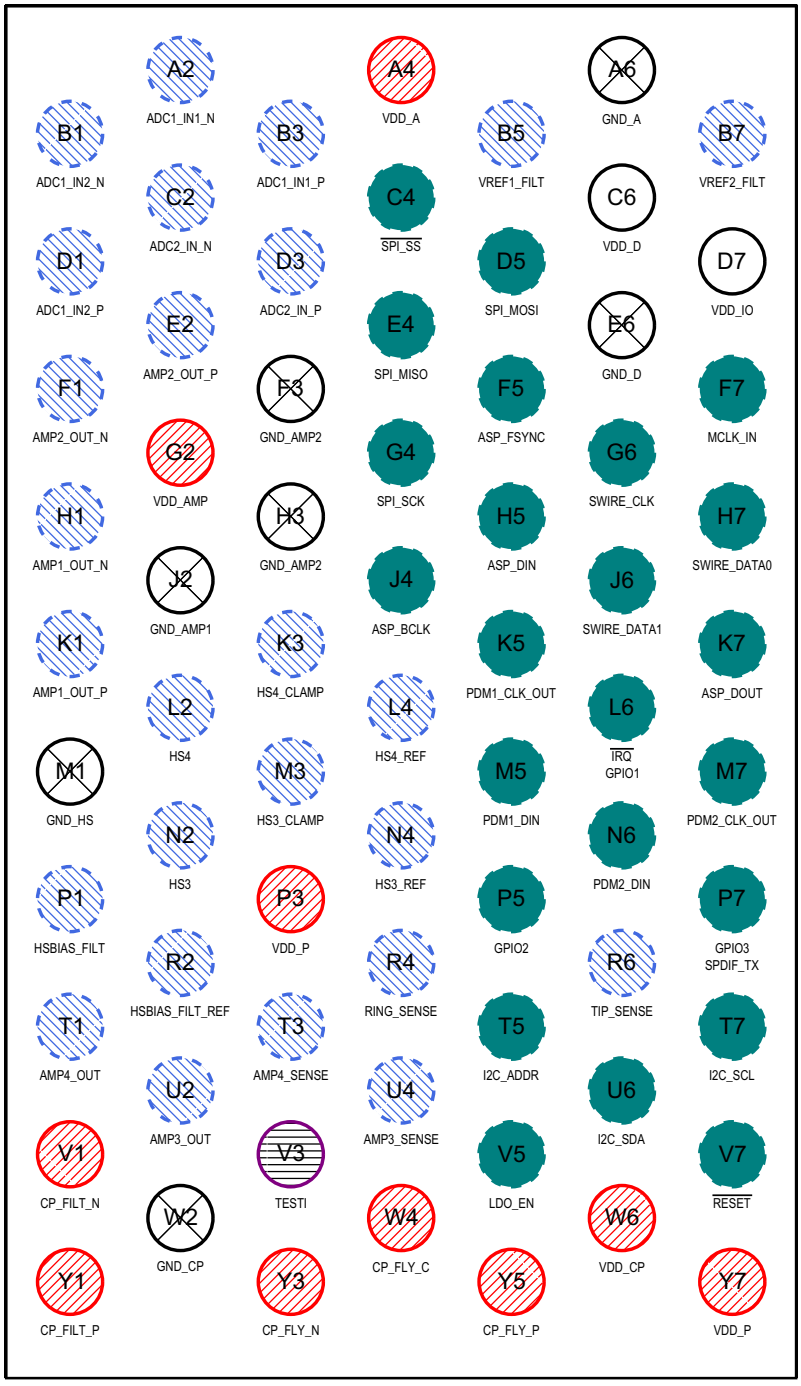


Figure 1-1. WLCSP Pin Diagram (Through-Package, Top View)

1.2 WLCSP Pin Descriptions

Table 1-1. WLCSP Pin Descriptions

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
ADC1_IN1_N	A2	VDD_P	I	**Inverting analog input for ADC 1 mux input 1**.	—	—
ADC1_IN1_P	B3	VDD_P	I	**Non-inverting analog input for ADC 1 mux input 1**.	—	—
ADC1_IN2_N	B1	VDD_P	I	**Inverting analog input for ADC 1 mux input 2**.	—	—
ADC1_IN2_P	D1	VDD_P	I	**Non-inverting analog input for ADC 1 mux input 2**.	—	—
ADC2_IN_N	C2	VDD_P	I	**Inverting analog input for ADC2**.	—	—
ADC2_IN_P	D3	VDD_P	I	**Non-inverting analog input for ADC 2**.	—	—
AMP1_OUT_N	H1	VDD_AMP	O	**Amplifier 1 Negative Output.** This amplifier is typically used to drive the negative-side of a differentially connected low impedance speaker.	—	—
AMP1_OUT_P	K1	VDD_AMP	O	**Amplifier 1 Positive Output.** This amplifier is typically used to drive the positive-side of a differentially connected low impedance speaker.	—	—
AMP2_OUT_N	F1	VDD_AMP	O	**Amplifier 2 Negative Output.** This amplifier is typically used to drive the negative-side of a differentially connected low impedance speaker.	—	—
AMP2_OUT_P	E2	VDD_AMP	O	**Amplifier 2 Positive Output.** This amplifier is typically used to drive the positive-side of a differentially connected low impedance speaker.	—	—
AMP3_OUT	U2	CP_FILT_P/N	O	**Amplifier 3 Output.** Ground-centered audio output typically used for headphone speakers and connects to TIP (HS1).	—	—
AMP3_SENSE	U4	CP_FILT_P/N	I	**Amplifier 3 Feedback Sense Input**.	—	—
AMP4_OUT	T1	CP_FILT_P/N	O	**Amplifier 4 Output.** Ground-centered audio output typically used for headphone speakers and connects to RING1 (HS2).	—	—
AMP4_SENSE	T3	CP_FILT_P/N	I	**Amplifier 4 Feedback Sense Input**.	—	—
ASP_BCLK	J4	VDD_IO	I/O	**ASP Bit Clock.** Serial shift clock for the interface.	Weak pull down	Weak pull down
ASP_DIN	H5	VDD_IO	I	**ASP Data Input.** Input for two's complement serial PCM audio data.	Weak pull down	Weak pull down
ASP_DOUT	K7	VDD_IO	O	**ASP Data Output.** Output for two's complement serial PCM audio data.	Weak pull down	Weak pull down
ASP_FSYNC	F5	VDD_IO	I/O	**ASP Frame Sync Clock.** Identifies the start of each serialized PCM data word and indicates which channel, left or right, is active on the serial PCM audio data lines or indicates the start of each TDM frame.	Weak pull down	Weak pull down
CP_FILT_N	V1	Power	O	**Inverting Charge Pump Filter Connection.** Power supply for the inverting charge pump that provides the negative rail for amplifiers 3 and 4.	—	—
CP_FILT_P	Y1	Power	O	**Step-Up/Down Charge Pump Filter Connection.** Power supply for the step-up/down charge pump that provides the positive rail for amplifiers 3 and 4.	—	—
CP_FLY_C	W4	VDD_P	O	**Charge Pump Cap Common Node.** Common positive node for amplifiers 3 and 4 step-down and inverting charge pumps' flying capacitors.	—	—
CP_FLY_N	Y3	CP_FILT_P	O	**Charge Pump Cap Negative Node.** Negative node for amplifiers 3 and 4 step-up/down charge-pump flying capacitor.	—	—
CP_FLY_P	Y5	VDD_P	O	**Charge Pump Cap Positive Node.** Positive node for amplifiers 3 and 4 step-up/down charge-pump flying capacitor.	—	—
GND_A	A6	Power	I	**Analog Ground.** Ground reference for the internal analog circuits.	—	—
GND_AMP1	J2	Power	I	**Amplifier 1 Output Ground.** This amplifier is typically used to drive a low impedance speaker.	—	—
GND_AMP2	F3, H3	Power	I	**Amplifier 2 Output Ground.** This amplifier is typically used to drive a low impedance speaker.	—	—

Table 1-1. WLCSP Pin Descriptions *(Cont.)*

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
GND_CP	W2	Power	I	**Charge Pump Ground.** Ground reference for amplifiers 3 and 4 charge pump.	—	—
GND_D	E6	Power	I	**Digital Ground.** Ground reference for the internal digital circuits.	—	—
GND_HS	M1	Power	I	**Headset Ground.** Ground reference for the internal headset analog circuits.	—	—
GPIO2	P5	VDD_IO	I/O	**General Purpose Input/Output 2**.	Weak pull up	Weak pull up
GPIO3/ SPDIF_TX	P7	VDD_IO	I/O	**General Purpose Input/Output 3**. **S/PDIF Audio Serial Data Output.** Serial data output for S/PDIF interface.	Weak pull down	Weak pull down
HS3	N2	VDD_P	I	**Headset Connection.** Input to headset and mic-button detection functions.	—	—
HS3_CLAMP	M3	VDD_P	I	**Headset Depletion FET Connections.** Input to drain of integrated depletion FET for ground-noise rejection.	—	—
HS3_REF	N4	VDD_P	I	**Headset Connection Reference.** Input to pseudodifferential amplifier 3 and 4 output reference.	—	—
HS4	L2	VDD_P	I	**Headset Connection.** Input to headset and mic-button detection functions.	—	—
HS4_CLAMP	K3	VDD_P	I	**Headset Depletion FET Connections.** Input to drain of integrated depletion FET for ground-noise rejection.	—	—
HS4_REF	L4	VDD_P	I	**Headset Connection Reference.** Input to pseudodifferential amplifier 3 and 4 output reference.	—	—
HSBIAS_FILT	P1	VDD_P	I	**Headset Bias Source Voltage Filter.** Filter connection for the internal bias voltage used for headset bias.	—	—
HSBIAS_FILT_ REF	R2	VDD_P	I	**Headset Bias Source Voltage Filter Reference.** Input of filter connection for the internal headset bias voltage.	—	—
I2C_ADDR	T5	VDD_IO	I	**I²C Address Input.** Address pin for the I²C target address and the SoundWire Unique ID. Latched on POR, hard, or soft reset. Connect this pin to VDD_IO or GND.	Weak pull down	Weak pull down
I2C_SCL	T7	VDD_IO	I	**I²C Clock.** Clock input for the I²C interface.	—	—
I2C_SDA	U6	VDD_IO	I/O	**I²C Input/Output.** Data input/output for the I²C interface.	—	—
$\overline{\text{IRQ}}$/GPIO1	L6	VDD_IO	I/O	**Interrupt output.** Programmable, open-drain, active-low programmable interrupt output. **General Purpose Input/Output 1**.	Weak pull up	Weak pull up
LDO_EN	V5	VDD_P	I	**LDO Enable.** Digital core logic LDO enable.	Weak pull down	Weak pull down
MCLK_IN	F7	VDD_IO	I	**Main Clock Input.** Clock source for the device core, serial port mastering, and converters.	Weak pull down	Weak pull down
PDM1_CLK_OUT	K5	VDD_IO	O	**PDM 1 Bit Clock Output**.	Weak pull down	Weak pull down
PDM1_DIN	M5	VDD_IO	I	**PDM 1 Data Input**.	Weak pull down	Weak pull down
PDM2_CLK_OUT	M7	VDD_IO	O	**PDM 2 Bit Clock Output**.	Weak pull down	Weak pull down
PDM2_DIN	N6	VDD_IO	I	**PDM 2 Data Input**.	Weak pull down	Weak pull down
$\overline{\text{RESET}}$	V7	VDD_P	I	**Reset.** The device enters a low power mode when this pin is driven low.	Weak pull down	Weak pull down
RING_SENSE	R4	VDD_P	I	**Ring Sense Input.** Sense pin to detect headphone plug. Can be configured to be debounced on plug and unplug events independently.	—	—
SPI_MISO	E4	VDD_IO	I	**SPI Slave Out Master In.** SPI serial data where the slave device is the transmitter and the master device is the receiver.	Weak pull down	Weak pull down

Table 1-1. WLCSP Pin Descriptions *(Cont.)*

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
SPI_MOSI	D5	VDD_IO	O	**SPI Master Out Slave In.** SPI serial data where the master device is the transmitter and the slave device is the receiver.	Weak pull down	Weak pull down
SPI_SCK	G4	VDD_IO	O	**SPI Serial Data Clock.** The bit clock for the data on the SPI_MOSI and SPI_MISO pins.	Weak pull down	Weak pull down
$\overline{\text{SPI\_SS}}$	C4	VDD_IO	O	**SPI Slave Select.** SPI slave device select.	Weak pull up	Weak pull up
SWIRE_CLK	G6	VDD_IO	I	**SoundWire Serial Clock Input.** Clock input to the SoundWire peripheral interface.	—	—
SWIRE_DATA0	H7	VDD_IO	I/O	**SoundWire Serial Data Input and Output 0.** Primary serial data input and output of the SoundWire peripheral interface.	—	—
SWIRE_DATA1	J6	VDD_IO	I/O	**SoundWire Serial Data Input and Output 1.** Serial data input and output of the SoundWire peripheral interface.	—	—
TESTI	V3	—	I	**Test Input Pin.** Must be connected to ground.	—	—
TIP_SENSE	R6	VDD_P	I	**Tip Sense.** Sense pin to detect headphone plug. Can be set to wake the system. Independently configurable to be debounced on plug and unplug events.	—	—
VDD_A	A4	Power	I	**Analog Power Supply.** Power supply for internal analog circuits.	—	—
VDD_AMP	G2	Power	I	**Amplifiers 1 and 2 Power Supply**.	—	—
VDD_CP	W6	Power	I	**Charge Pump Power.** Power supply for amplifiers 3 and 4 charge pump.	—	—
VDD_D	C6	Power	I	**Digital Core Power Supply.** Power supply for internal digital circuits.	—	—
VDD_IO	D7	Power	I	**I/O Power Supply.** Power supply for external interface and internal digital logic.	—	—
VDD_P	P3, Y7	Power	I	**High Voltage Supply.** Power supply for the high voltage interface.	—	—
VREF1_FILT	B5	VDD_A	I	**Voltage Reference.** Reference voltage for internal ADCs and amplifiers 3 and 4.	—	—
VREF2_FILT	B7	VDD_A	I	**Voltage Reference.** Reference voltage for internal amplifiers 1 and 2.	—	—

1.3 QFN Pin Out (Through-Package, Top View)

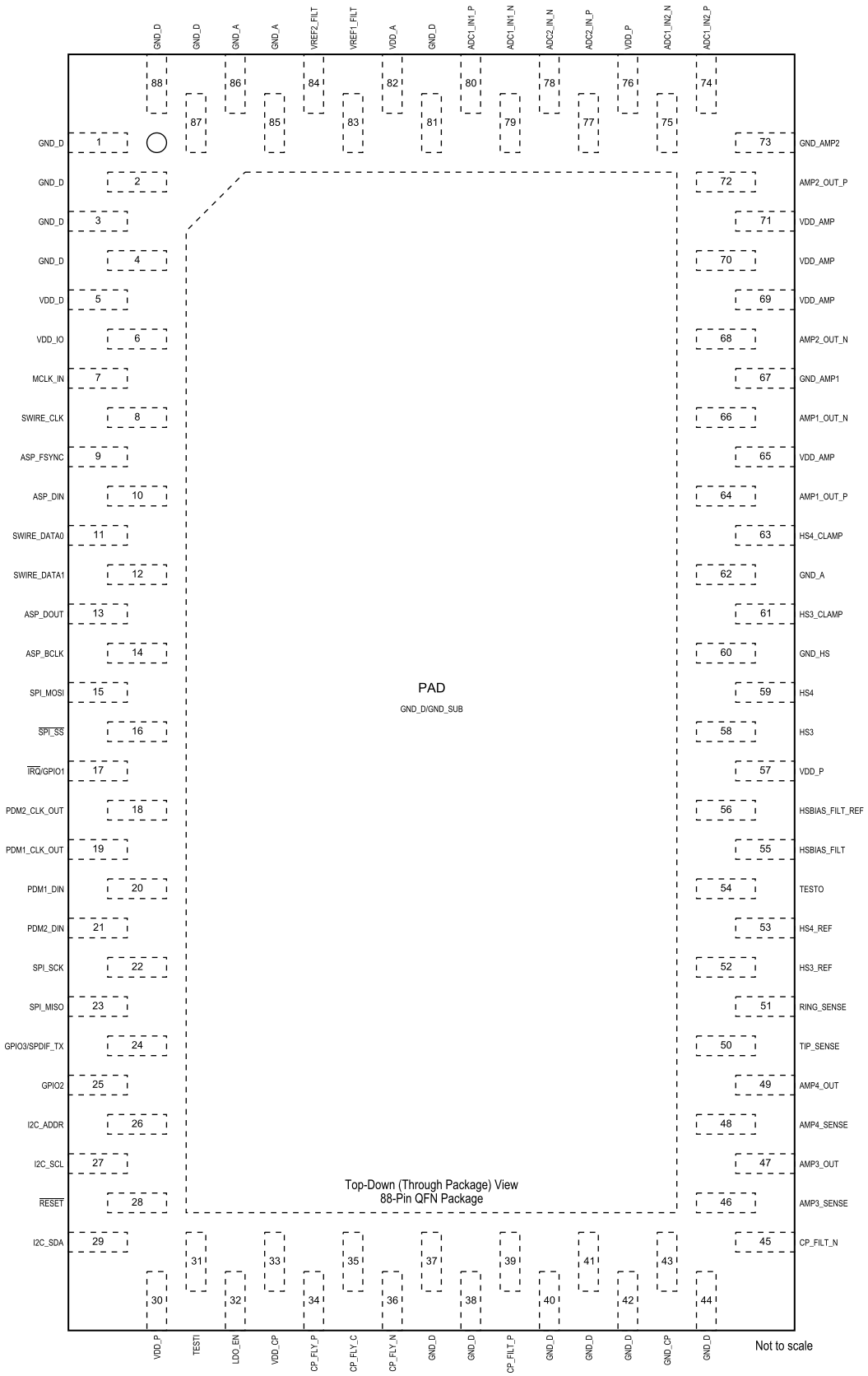


Figure 1-2. QFN Pin Diagram (Through-Package, Top View)

1.4 QFN Pin Descriptions

Table 1-2. QFN Pin Descriptions

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
ADC1_IN1_N	79	VDD_P	I	**Inverting analog input for ADC 1 mux input 1**.	—	—
ADC1_IN1_P	80	VDD_P	I	**Non-inverting analog input for ADC 1 mux input 1**.	—	—
ADC1_IN2_N	75	VDD_P	I	**Inverting analog input for ADC 1 mux input 2**.	—	—
ADC1_IN2_P	74	VDD_P	I	**Non-inverting analog input for ADC 1 mux input 2**.	—	—
ADC2_IN_N	78	VDD_P	I	**Inverting analog input for ADC 2**.	—	—
ADC2_IN_P	77	VDD_P	I	**Non-inverting analog input for ADC 2**.	—	—
AMP1_OUT_N	66	VDD_AMP	O	**Amplifier 1 Negative Output.** This amplifier is typically used to drive the negative-side of a differentially connected low impedance speaker.	—	—
AMP1_OUT_P	64	VDD_AMP	O	**Amplifier 1 Positive Output.** This amplifier is typically used to drive the positive-side of a differentially connected low impedance speaker.	—	—
AMP2_OUT_N	68	VDD_AMP	O	**Amplifier 2 Negative Output.** This amplifier is typically used to drive the negative-side of a differentially connected low impedance speaker.	—	—
AMP2_OUT_P	72	VDD_AMP	O	**Amplifier 2 Positive Output.** This amplifier is typically used to drive the positive-side of a differentially connected low impedance speaker.	—	—
AMP3_OUT	47	CP_FILT_P/N	O	**Amplifier 3 Output.** Ground-centered audio output typically used for headphone speakers and connects to TIP (HS1).	—	—
AMP3_SENSE	46	CP_FILT_P/N	I	**Amplifier 3 Feedback Sense Input**.	—	—
AMP4_OUT	49	CP_FILT_P/N	O	**Amplifier 4 Output.** Ground-centered audio output typically used for headphone speakers and connects to RING1 (HS2).	—	—
AMP4_SENSE	48	CP_FILT_P/N	I	**Amplifier 4 Feedback Sense Input**.	—	—
ASP_BCLK	14	VDD_IO	I/O	**ASP Bit Clock.** Serial shift clock for the interface.	Weak pull down	Weak pull down
ASP_DIN	10	VDD_IO	I	**ASP Data Input.** Input for two's complement serial PCM audio data.	Weak pull down	Weak pull down
ASP_DOUT	13	VDD_IO	O	**ASP Data Output.** Output for two's complement serial PCM audio data.	Weak pull down	Weak pull down
ASP_FSYNC	9	VDD_IO	I/O	**ASP Frame Sync Clock.** Identifies the start of each serialized PCM data word and indicates which channel, left or right, is active on the serial PCM audio data lines or indicates the start of each TDM frame.	Weak pull down	Weak pull down
CP_FILT_N	45	Power	O	**Inverting Charge Pump Filter Connection.** Power supply for the inverting charge pump that provides the negative rail for amplifiers 3 and 4.	—	—
CP_FILT_P	39	Power	O	**Step-Up/Down Charge Pump Filter Connection.** Power supply for the step-up/down charge pump that provides the positive rail for amplifiers 3 and 4.	—	—
CP_FLY_C	35	VDD_P	O	**Charge Pump Cap Common Node.** Common positive node for amplifiers 3 and 4 step-down and inverting charge pumps' flying capacitors.	—	—
CP_FLY_N	36	CP_FILT_P	O	**Charge Pump Cap Negative Node.** Negative node for amplifiers 3 and 4 step-up/down charge-pump flying capacitor.	—	—
CP_FLY_P	34	VDD_P	O	**Charge Pump Cap Positive Node.** Positive node for amplifiers 3 and 4 step-up/down charge-pump flying capacitor.	—	—
GND_A	62, 85, 86	Power	I	**Analog Ground.** Ground reference for the internal analog circuits.	—	—
GND_AMP1	67	Power	I	**Amplifier 1 Output Ground.** This amplifier is typically used to drive a low impedance speaker.	—	—

Table 1-2. QFN Pin Descriptions *(Cont.)*

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
GND_AMP2	73	Power	I	**Amplifier 2 Output Ground.** This amplifier is typically used to drive a low impedance speaker.	—	—
GND_CP	43	Power	I	**Charge Pump Ground.** Ground reference for amplifiers 3 and 4 charge pump.	—	—
GND_D	1, 2, 3, 4, 37, 38, 40, 41, 42, 44, 81, 87, 88	Power	I	**Digital Ground.** Ground reference for the internal digital circuits.	—	—
GND_D/ GND_SUB	PAD	Power	I	**Digital Ground.** Ground reference for the internal digital circuits. **Substrate Ground**.	—	—
GND_HS	60	Power	I	**Headset Ground.** Ground reference for the internal headset analog circuits.	—	—
GPIO2	25	VDD_IO	I/O	**General Purpose Input/Output 2**.	Weak pull up	Weak pull up
GPIO3/ SPDIF_TX	24	VDD_IO	I/O	**General Purpose Input/Output 3**. **S/PDIF Audio Serial Data Output.** Serial data output for S/PDIF interface.	Weak pull down	Weak pull down
HS3	58	VDD_P	I	**Headset Connection.** Input to headset and mic-button detection functions.	—	—
HS3_CLAMP	61	VDD_P	I	**Headset Depletion FET Connections.** Input to drain of integrated depletion FET for ground-noise rejection.	—	—
HS3_REF	52	VDD_P	I	**Headset Connection Reference.** Input to pseudodifferential amplifier 3 and 4 output reference.	—	—
HS4	59	VDD_P	I	**Headset Connection.** Input to headset and mic-button detection functions.	—	—
HS4_CLAMP	63	VDD_P	I	**Headset Depletion FET Connections.** Input to drain of integrated depletion FET for ground-noise rejection.	—	—
HS4_REF	53	VDD_P	I	**Headset Connection Reference.** Input to pseudodifferential amplifier 3 and 4 output reference.	—	—
HSBIAS_FILT	55	VDD_P	I	**Headset Bias Source Voltage Filter.** Filter connection for the internal bias voltage used for headset bias.	—	—
HSBIAS_FILT_ REF	56	VDD_P	I	**Headset Bias Source Voltage Filter Reference.** Input of filter connection for the internal headset bias voltage.	—	—
I2C_ADDR	26	VDD_IO	I	**I²C Address Input.** Address pin for the I²C target address and the SoundWire Unique ID. Latched on POR, hard, or soft reset. Connect this pin to VDD_IO or GND.	Weak pull down	Weak pull down
I2C_SCL	27	VDD_IO	I	**I²C Clock.** Clock input for the I²C interface.	—	—
I2C_SDA	29	VDD_IO	I/O	**I²C Input/Output.** Data input/output for the I²C interface.	—	—
$\overline{\text{IRQ}}$/GPIO1	17	VDD_IO	I/O	**Interrupt output.** Programmable, open-drain, active-low programmable interrupt output. **General Purpose Input/Output 1**.	Weak pull up	Weak pull up
LDO_EN	32	VDD_P	I	**LDO Enable.** Digital core logic LDO enable.	Weak pull down	Weak pull down
MCLK_IN	7	VDD_IO	I	**Main Clock Input.** Clock source for the device core, serial port mastering, and converters.	Weak pull down	Weak pull down
PDM1_CLK_OUT	19	VDD_IO	O	**PDM 1 Bit Clock Output**.	Weak pull down	Weak pull down
PDM1_DIN	20	VDD_IO	I	**PDM 1 Data Input**.	Weak pull down	Weak pull down
PDM2_CLK_OUT	18	VDD_IO	O	**PDM 2 Bit Clock Output**.	Weak pull down	Weak pull down
PDM2_DIN	21	VDD_IO	I	**PDM 2 Data Input**.	Weak pull down	Weak pull down

Table 1-2. QFN Pin Descriptions *(Cont.)*

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
$\overline{\text{RESET}}$	28	VDD_P	I	**Reset.** The device enters a low power mode when this pin is driven low.	Weak pull down	Weak pull down
RING_SENSE	51	VDD_P	I	**Ring Sense Input.** Sense pin to detect headphone plug. Can be configured to be debounced on plug and unplug events independently.	—	—
SPI_MISO	23	VDD_IO	I	**SPI Slave Out Master In.** SPI serial data where the slave device is the transmitter and the master device is the receiver.	Weak pull down	Weak pull down
SPI_MOSI	15	VDD_IO	O	**SPI Master Out Slave In.** SPI serial data where the master device is the transmitter and the slave device is the receiver.	Weak pull down	Weak pull down
SPI_SCK	22	VDD_IO	O	**SPI Serial Data Clock.** The bit clock for the data on the SPI_MOSI and SPI_MISO pins.	Weak pull down	Weak pull down
$\overline{\text{SPI\_SS}}$	16	VDD_IO	O	**SPI Slave Select.** SPI slave device select.	Weak pull up	Weak pull up
SWIRE_CLK	8	VDD_IO	I	**SoundWire Serial Clock Input.** Clock input to the SoundWire peripheral interface.	—	—
SWIRE_DATA0	11	VDD_IO	I/O	**SoundWire Serial Data Input and Output 0.** Primary serial data input and output of the SoundWire peripheral interface.	—	—
SWIRE_DATA1	12	VDD_IO	I/O	**SoundWire Serial Data Input and Output 1.** Serial data input and output of the SoundWire peripheral interface.	—	—
TESTI	31	—	I	**Test Input Pin.** Must be connected to ground.	—	—
TESTO	54	—	O	**Test Output Pin.** Must be left floating.	—	—
TIP_SENSE	50	VDD_P	I	**Tip Sense.** Sense pin to detect headphone plug. Can be set to wake the system. Independently configurable to be debounced on plug and unplug events.	—	—
VDD_A	82	Power	I	**Analog Power Supply.** Power supply for internal analog circuits.	—	—
VDD_AMP	65, 69, 70, 71	Power	I	**Amplifiers 1 and 2 Power Supply**.	—	—
VDD_CP	33	Power	I	**Charge Pump Power.** Charge pump power supply for amplifiers 3 and 4.	—	—
VDD_D	5	Power	I	**Digital Core Power Supply.** Power supply for internal digital circuits.	—	—
VDD_IO	6	Power	I	**I/O Power Supply.** Power supply for external interface and internal digital logic.	—	—
VDD_P	30, 57, 76	Power	I	**High Voltage Supply.** Power supply for the high voltage interface.	—	—
VREF1_FILT	83	VDD_A	I	**Voltage Reference.** Reference voltage for internal ADCs and amplifiers 3 and 4.	—	—
VREF2_FILT	84	VDD_A	I	**Voltage Reference.** Reference voltage for internal amplifiers 1 and 2.	—	—

1.5 Termination of Unused Pins

Some systems may not need to connect to all of the device pins. Table 1-3 shows the recommended termination for any permanently unused pins. A pin that is connected to other circuits but is only occasionally active is not required to follow the terminations shown.

Table 1-3. Recommended Termination of Unused Pins

Pin Name	Termination
$\overline{\text{IRQ}}$/GPIO1 GPIO3/SPDIF_TX	Float
AMP1_OUT_P/N AMP2_OUT_P/N AMP3_OUT AMP4_OUT	
ASP_BCLK ASP_FSYNC ASP_DOUT ASP_DIN	
HSBIAS_FILT	
PDM1_CLK_OUT PDM2_CLK_OUT PDM1_DIN PDM2_DIN	
SPI_MOSI SPI_SCK $\overline{\text{SPI_SS}}$	
TESTO [1]	
ADC1_IN1_P/N ADC1_IN2_P/N ADC2_IN_P/N	Grounded
AMP3_SENSE [2] AMP4_SENSE [3]	
HS3 HS3_CLAMP HS3_REF HS4 HS4_CLAMP HS4_REF HSBIAS_FILT_REF	
I2C_ADDR I2C_SCL I2C_SDA	
MCLK_IN	
TIP_SENSE RING_SENSE	
TESTI	
SPI_MISO	
SWIRE_CLK SWIRE_DATAx	
NC [4]	
VDD_AMP [5]	
$\overline{\text{RESET}}$	Pulled high
GPIO2	Float or Tie to VDD_IO

1. TESTO is only available in the QFN package.
2. AMP3_SENSE must not be grounded if AMP3_OUT is used.
3. AMP4_SENSE must not be grounded if AMP4_OUT is used.
4. While the no connect (NC) pins on the QFN package have no internal connection to circuitry, it is recommended to connect them to GND_D.
5. VDD_AMP must be grounded for configurations that do not require speakers.

1.6 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS42L43 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to JEDEC ESD protection standards JS-001-2017 and JS-001-2018.

2 Typical Connections

2.1 Typical Connection Diagrams

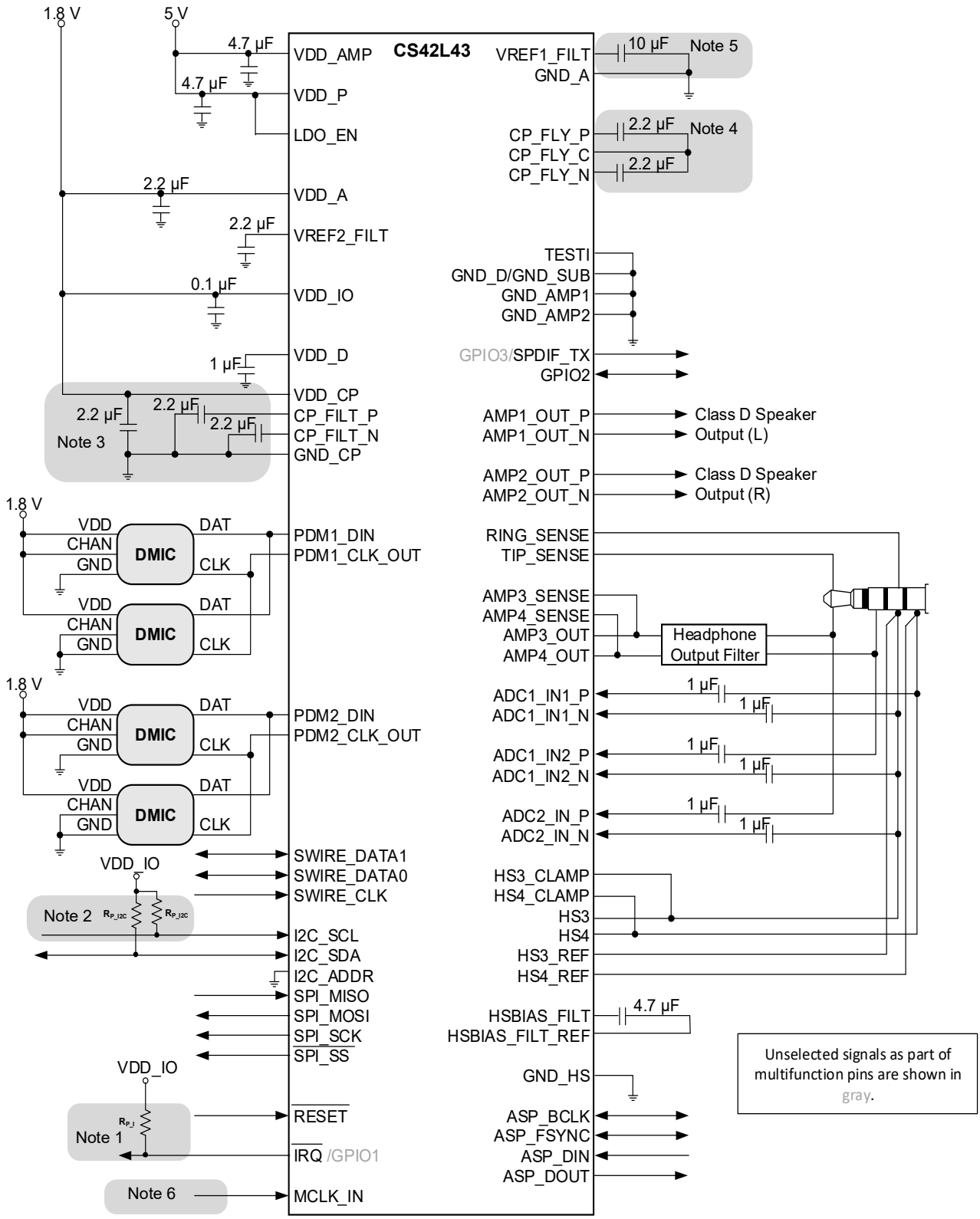


Figure 2-1. Typical Connection Diagram—Non-DSP Use Case, Separate ADC1 Ground

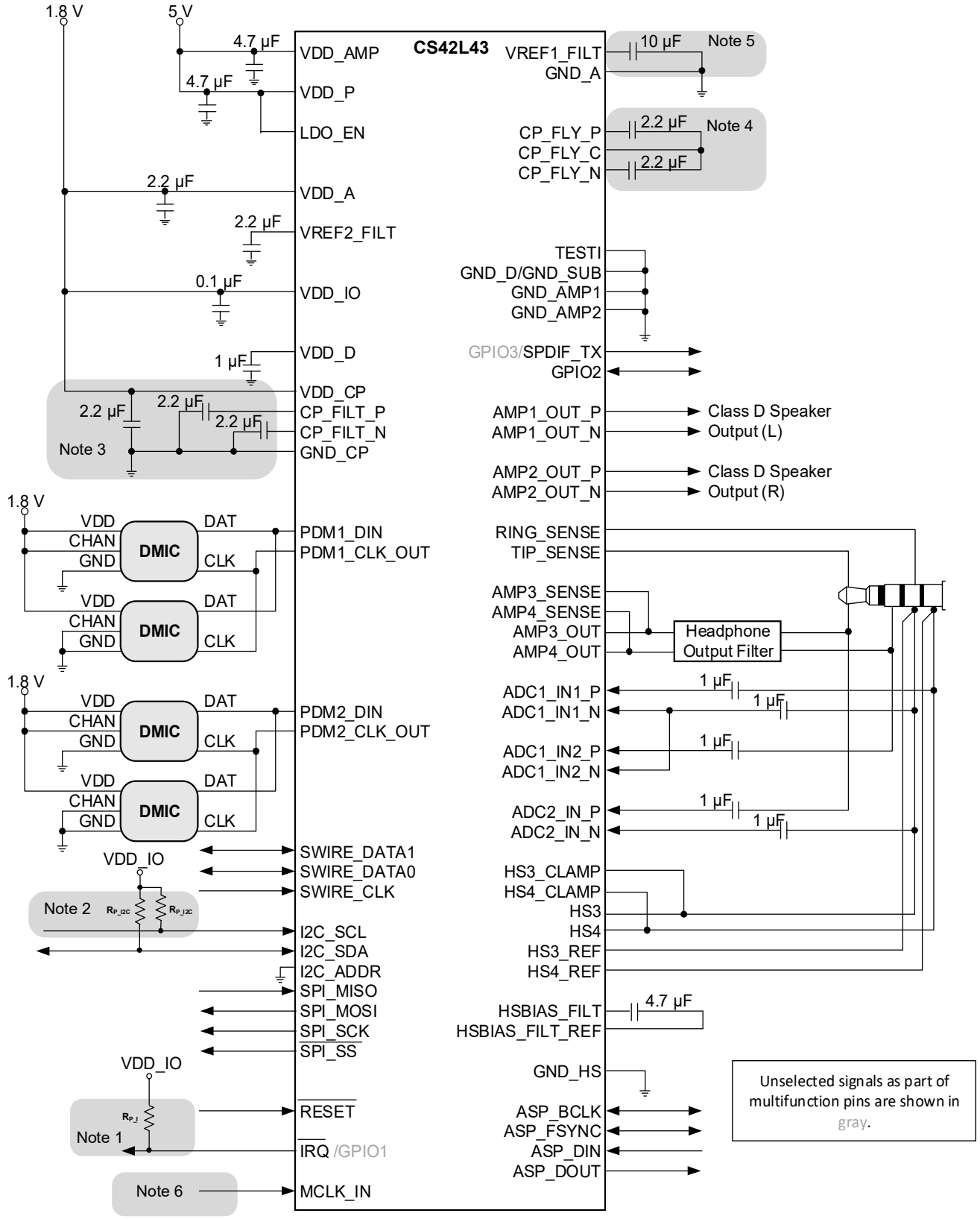


Figure 2-2. Typical Connection Diagram—Non-DSP Use Case, Shared ADC1 Ground

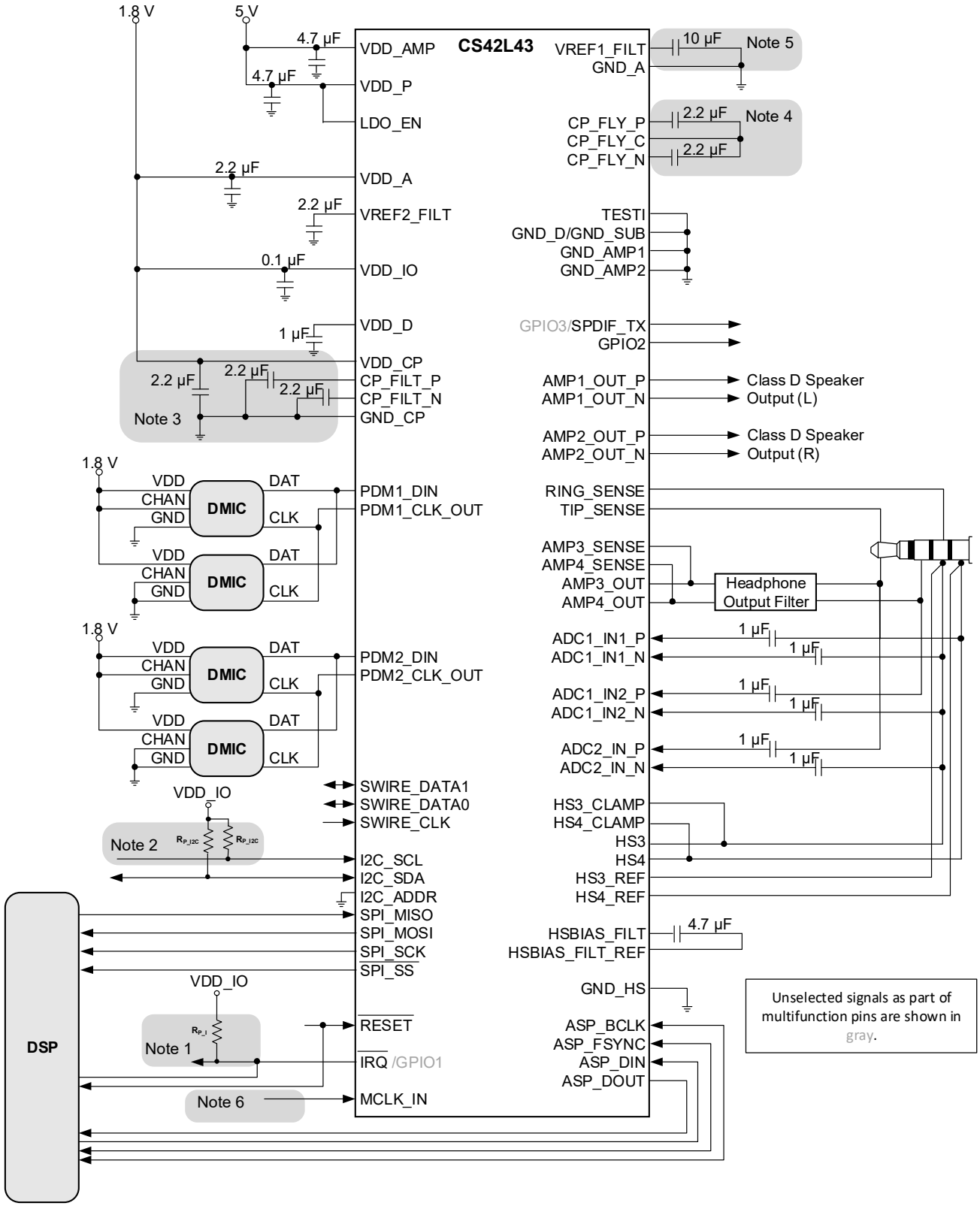


Figure 2-3. Typical Connection Diagram—DSP Use Case

Notes:
1. A pull-up resistance of 10 kΩ or greater is recommended. R_{P_I} value can be determined by the $\overline{IRQ}$ pin specification in Table 3-30.
2. R_{P_I2C} values can be determined by the I²C pull-up resistance specification in Table 3-25.
3. The headphone amplifier's output power and distortion ratings use the nominal capacitances shown. Larger capacitance reduces ripple on the internal amplifiers' supplies and, in turn, reduces distortion at high-output power levels. Smaller capacitance may not reduce ripple enough to achieve output power and distortion ratings. Because actual values of typical X7R/X5R ceramic capacitors deviate from nominal

values by a percentage specified in the manufacturer's data sheet, capacitors must be selected for maximum output power and minimum distortion required. Higher value capacitors than those shown may be used, however lower value capacitors must not (values can vary from the nominal by ±20%). A 0402-size or larger package is recommended.

4. Series resistance in the path of the power supplies must be avoided. Any voltage drop on charge pump fly nodes directly affects the charge-pump supplies and clips the audio output.
5. Lowering capacitance below the value shown affects PSRR, THD+N performance, ADC-DAC isolation and intermodulation, and interchannel isolation and intermodulation.
6. Connect to ground or a reference clock source.

3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

Table 3-1. Parameter Definitions

Parameter	Definition
Channel separation	Left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
Common-mode rejection ratio (CMRR)	The ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
Dynamic range	The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. A signal-to-noise ratio measurement over the specified bandwidth made with a –60 dB signal; 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17–1991, and the Electronic Industries Association of Japan, EIAJ CP–307. Dynamic range is expressed in decibel units.
Signal-to-noise-floor ratio (SNR)	The ratio of the rms value of all the spectral components of the muted output over the specified measurement bandwidth relative to a full-scale output signal.
Gain drift	The change in gain value with temperature, expressed in ppm/°C units.
Gain accuracy	The difference between the actual gain and the nominal gain.
Idle channel noise	The rms value of the signal with no input applied (properly back-terminated analog input, digital zero, or zero modulation input). Measured over the specified bandwidth.
Interchannel gain mismatch	The gain difference between left and right channel pairs. Interchannel gain mismatch is expressed in dB.
Interchannel isolation	A measure of cross talk between the left and right channel pairs. Interchannel isolation is measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Interchannel isolation is expressed in decibel units.
Load resistance and capacitance	The recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. The load capacitance effectively moves the band-limiting pole of the amp in the output stage. Increasing load capacitance beyond the recommended value can cause the internal op-amp to become unstable.
Offset error	The deviation of the midscale transition (111…111 to 000…000) from the ideal.
Output offset voltage	The DC offset voltage present at the amplifier's output when its input signal is in a mute state. The offset exists due to CMOS process limitations and is proportional to analog volume settings. When measuring the offset out the headphone amplifier, the headphone amplifier is ON.
Total harmonic distortion (THD)	The ratio of the RMS sum of the harmonic distortion products in the specified bandwidth [1] relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
Total harmonic distortion + noise (THD+N)	The ratio of the rms sum of distortion and noise spectral components across the specified bandwidth (typically 20 Hz–20 kHz or 20 Hz–80 kHz) relative to the rms value of the signal. THD+N is measured at –1 dBFS for the analog input and at 0 dB (or as otherwise specified in the table) for the analog output, as suggested in AES17–1991 Annex A. THD+N is expressed in decibel units.

1.All performance measurements are specified with a 20 kHz low-pass brick-wall filter and, where noted, an A-weighted filter. The low-pass filter removes out-of-band noise.

Table 3-2. Recommended Operating Conditions

Test conditions: Ground = GND_A = GND_D = GND_CP = GND_AMP1/2 = 0 V; voltages are with respect to ground.

Parameter			Symbol	Minimum	Maximum	Unit
DC power supply	Charge pump		VDD_CP	1.66	1.94	V
	LDO regulator for digital [1]	LDO_EN = 0	VDD_D	1.10	1.30	V
	Serial interface control port	1.8 V nominal	VDD_IO	1.66	1.94	V
	Analog		VDD_A	1.66	1.94	V
	Main power supply	Functional range [2,3]	VDD_P	2.50	5.25	V
		Parametric performance range [4]		3.20	5.25	V
		Parametric performance with stereo HS MIC support [5]		3.30	5.25	V
	Class D supplies		VDD_AMP	4.75	5.25	V
External voltage applied to pin [6,7]		TIP_SENSE pin	$V_{TIPSENSE}$	CP_FILT_N	VDD_P	V
		CP_FILT_P/N domain pins [8]	V_{CP_FILT}	CP_FILT_N	VDD_P	V
		VDD_IO domain pins	V_{VDD_IO}	0	VDD_IO	V
		VDD_A domain pins	V_{VDD_A}	0	VDD_A	V
		VDD_P domain pins	V_{VDD_P}	0	VDD_P	V
		RING_SENSE pin	$V_{RINGSENSE}$	0	VDD_P	V

Table 3-2. Recommended Operating Conditions *(Cont.)*

Test conditions: Ground = GND_A = GND_D = GND_CP = GND_AMP1/2 = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
Ambient temperature	Functional range [2]	T_A	–40	+85	°C
	Parametric performance range [4]		–10	+70	°C
VDD_AMP supply ramp rate		—	0.0017	0.1	V/µs

Note: The device is fully functional and meets all parametric specifications in this section if operated within the specified conditions. Functionality and/or parametric performance are not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

1. If LDO_EN is asserted, no external voltage must be applied to VDD_D and VDD_IO must be within the recommended operating range specified in Table 3-2. When LDO_EN is asserted, the VDD_D pin outputs 1.2 V. The minimum high input for LDO_EN is 1.2 V. It can be connected to 1.2 V, 1.8 V, 3.3 V, or 5 V supplies to enable the LDO.
2. Defined as the range that the CS42L43 is capable of operating functionally, but may not meet all parametric specifications.
3. The following are affected when VDD_P < 3.0 V: HSBIAS, charge pump LDO, TIP_SENSE threshold, and RING_SENSE threshold.
4. Defined as the range that the CS42L43 is capable of operating functionally, and meets all parametric specifications.
5. To support unplug detection of a stereo MIC jack if MICBIAS is set to 2.75 V, VDD_P must be at least 3.3 V.
6. The maximum over/undervoltage is limited by the input current.
7. Section 1.2 and Section 1.4 list the power supply domain in which each CS42L43 pin resides.
8. CP_FILT_P/N is specified in Table 3-16.

Table 3-3. Absolute Maximum Ratings

Test conditions: Ground = GND_A = GND_D = GND_CP = GND_AMP1/2 = 0 V; voltages are with respect to ground.

Parameter		Symbol	Min	Max	Unit
DC power supply	Charge pump, LDO, serial/control, analog	VDD_IO, VDD_A, VDD_CP	–0.3	2.33	V
	Digital core	VDD_D	–0.3	1.55	V
	Main power	VDD_P	–0.3	6.3	V
	Class D	VDD_AMP	–0.3	6.3	V
Input current [1]		I_{in}	—	±10	mA
Ambient operating temperature (power applied)		T_A	–50	+115	°C
Storage temperature		T_{stg}	–65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2, “Recommended Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Any pin except supply pins. Transient currents of up to ±100 mA on analog input pins do not cause SCR latch-up.

Table 3-4. Combined ADC On-Chip Analog and Digital Filter Characteristics

Test conditions (unless specified otherwise): Signal inputs AC-coupled with 1 µF; GND_A = GND_CP = 0 V; voltages are with respect to ground; typical performance data taken with VDD_IO = VDD_A = 1.8 V, VDD_P = 3.3 V, T_A = +25°C; min/max performance data taken with VDD_A = 1.66–1.94 V; VDD_IO = 1.8 V, VDD_P = 3.2–5.25 V, T_A = +25°C; DECIMn_WNF_EN = 0 and DECIMn_HPF_EN = 0; entire path characteristics including AFE + ADC + serial port.

Parameter [1]			Minimum	Typical	Maximum	Unit
LPF passband (normalized to 28.33×10^{-3} •Fs)	Fs ≤ 48 kHz	–0.17 dB corner	0.417	—	—	Fs
		–3 dB corner	—	0.428	—	Fs
	Fs = 96 kHz	–0.38 dB corner	0.417	—	—	Fs
		–3 dB corner	—	0.428	—	Fs
Passband ripple (DC to LPF passband corner; normalized to 28.33×10^{-3} • Fs)		Fs ≤ 48 kHz	–0.17	—	0.11	dB
		Fs = 96 kHz	–0.38	—	0.2	dB
Transition band (0.5•Fs to 0.55•Fs)			50	—	—	dB
Stopband attenuation 1 (0.55•Fs to 3•Fs)[2]			80	—	—	dB
Stopband attenuation 2 (3•Fs to 10•Fs) [2]			120	—	—	dB
ADCn_INy_x-to-ASP_DOUT group delay @1 kHz (ASP output)		Fs = 48 kHz	—	—	10/Fs	s
		Fs = 96 kHz	—	—	10/Fs	s
ADCn_INy_x-to-SWIRE_DATAn group delay @1 kHz (SoundWire output)		Fs = 48 kHz	—	—	11/Fs	s
		Fs = 96 kHz	—	—	11/Fs	s

1. Response scales with Fs (internal sample rate, based on MCLK_IN). Specifications are normalized to Fs and are denormalized by multiplying by Fs.
2. Measurement is with high frequency out of band tone amplitude set to –24 dBFS with PGA setting = 0 dB and Fs = 48 kHz. Additionally, measurement may be limited by measuring equipment and/or noise floor.

Table 3-5. Combined PDM Input and On-Chip Digital Filter Characteristics

Test conditions (unless specified otherwise): GND_A = GND_CP = 0 V; voltages are with respect to ground; typical performance data taken with VDD_IO = VDD_A = 1.8 V, VDD_P = 3.3 V, T_A = +25°C; min/max performance data taken with VDD_A = 1.66–1.94 V; VDD_IO = 1.8 V, VDD_P = 3.2–5.25 V, T_A = +25°C; DECIMn_WNF_EN = 0 and DECIMn_HPF_EN = 0; entire path characteristics including decimators and serial port.

Parameter [1]			Minimum	Typical	Maximum	Unit
LPF passband (normalized to 28.33×10^{-3} •Fs)	Fs ≤ 48 kHz	–0.17 dB corner	0.417	—	—	Fs
		–3 dB corner	—	0.428	—	Fs
	Fs = 96 kHz	–0.38 dB corner	0.417	—	—	Fs
		–3 dB corner	—	0.428	—	Fs
Passband ripple (DC to LPF passband corner; normalized to 28.33×10^{-3} • Fs)		Fs ≤ 48 kHz	–0.17	—	0.11	dB
		Fs = 96 kHz	–0.38	—	0.2	dB
Transition band (0.5•Fs to 0.55•Fs)			50	—	—	dB
Stopband attenuation 1 (0.55•Fs to 3•Fs)[2]			80	—	—	dB
Stopband attenuation 2 (3•Fs to 10•Fs) [2]		except f_{PDM} = 1.536 MHz with Fs = 32 kHz and f_{PDM} = 768 kHz with Fs = 16 kHz	120	—	—	dB
		f_{PDM} = 1.536 MHz with Fs = 32 kHz or f_{PDM} = 768 kHz with Fs = 16 kHz	100	—	—	dB
PDMn_DIN-to-ASP_DOUT group delay for Fs ≤ 48 kHz (ASP output)		–0.1 dB HPF corner to 0.333•Fs	—	—	10/Fs	s
PDMn_DIN-to-ASP_DOUT group delay for Fs = 96 kHz (ASP output)		–0.1 dB HPF corner to 0.333•Fs	—	—	11/Fs	s
PDMn_DIN-to-SWIRE_DATAn group delay for Fs ≤ 48 kHz (SoundWire output)		–0.1 dB HPF corner to 0.333•Fs	—	—	13/Fs	s
PDMn_DIN-to-SWIRE_DATAn group delay for Fs =96 kHz (SoundWire output)		–0.1 dB HPF corner to 0.333•Fs	—	—	14/Fs	s
Offset error		DECIMn_HPF_EN = 1	120	—	132	LSB
Turn-on time			—	—	10	ms
Volume control range			–64	—	31.5	dB
THD+N, –1 dBFS input		Tone < $Fs_{(OUT)}$/2	—	–75	—	dB

1.Response scales with Fs (internal sample rate, based on MCLK_IN). Specifications are normalized to Fs and are denormalized by multiplying by Fs.
2.Measurement is with high frequency out of band tone amplitude set to –10 dBFS with PGA setting = 0 dB and Fs = 48 kHz. Additionally, measurement may be limited by measuring equipment and/or noise floor.

Table 3-6. ADC Digital High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise): Specifications represent the frequency response of the entire path with DECIMn_WNF_EN = 0, and DECIMn_HPF_EN = 1.

Parameter			Minimum	Typical	Maximum	Unit
Passband	–0.1 dB corner	DECIMn_HPF_CF = 00	—	—	9	Hz
		DECIMn_HPF_CF = 01	—	—	36	Hz
		DECIMn_HPF_CF = 10	—	—	144	Hz
		DECIMn_HPF_CF = 11	—	—	288	Hz
	–3 dB corner	DECIMn_HPF_CF = 00	—	3	—	Hz
		DECIMn_HPF_CF = 01	—	12	—	Hz
		DECIMn_HPF_CF = 10	—	48	—	Hz
		DECIMn_HPF_CF = 11	—	96	—	Hz
Passband ripple (–0.05 dB corner to 0.417•Fs; normalized to 0.417•Fs) [1]			–0.05	—	0.05	dB

1.Response scales with Fs (based on $MCLK_{INT}$). Specifications are normalized to Fs and are denormalized by multiplying by Fs.

Table 3-7. Wind-Noise Digital Filter Characteristics

Test conditions (unless specified otherwise): Fs = 16/24/32/48/96 kHz; ADC HPF disabled (DECIMn_HPF_EN = 0).

Parameter [1,2]			Minimum	Typical	Maximum	Unit
Passband	–3.0 dB corner	DECIMn_WNF_CF = 000	—	160	—	Hz
		DECIMn_WNF_CF = 001	—	180	—	Hz
		DECIMn_WNF_CF = 010	—	200	—	Hz
		DECIMn_WNF_CF = 011	—	220	—	Hz
		DECIMn_WNF_CF = 100	—	240	—	Hz
		DECIMn_WNF_CF = 101	—	260	—	Hz
		DECIMn_WNF_CF = 110	—	280	—	Hz
		DECIMn_WNF_CF = 111	—	300	—	Hz
	–0.05 dB corner	DECIMn_WNF_CF = 000	—	280	—	Hz
		DECIMn_WNF_CF = 001	—	315	—	Hz
		DECIMn_WNF_CF = 010	—	350	—	Hz
		DECIMn_WNF_CF = 011	—	385	—	Hz
		DECIMn_WNF_CF = 100	—	420	—	Hz
		DECIMn_WNF_CF = 101	—	455	—	Hz
		DECIMn_WNF_CF = 110	—	490	—	Hz
		DECIMn_WNF_CF = 111	—	525	—	Hz
Passband ripple (–0.05 dB corner to 0.417•Fs; normalized to 0.417•Fs)			–0.15	—	0.15	dB
Filter settling time		DECIMn_WNF_CF = 000	7.7	8.0	8.3	ms
		DECIMn_WNF_CF = 001	6.7	7.0	7.3	ms
		DECIMn_WNF_CF = 010	5.9	6.2	6.5	ms
		DECIMn_WNF_CF = 011	5.5	5.8	6.1	ms
		DECIMn_WNF_CF = 100	5.0	5.3	5.6	ms
		DECIMn_WNF_CF = 101	4.6	4.9	5.2	ms
		DECIMn_WNF_CF = 110	4.2	4.5	4.8	ms
		DECIMn_WNF_CF = 111	4.0	4.3	4.6	ms

1. Responses are clock dependent and scale with Fs.
2. Wind-noise HPF characteristics apply only if the given filter is enabled (DECIMn_WNF_EN = 1). Otherwise, the signal is unaffected by this block.

Table 3-8. Combined DAC Digital, On-Chip Analog, and AMP3/4_OUT (Headphone Output) Filter Characteristics

Test conditions (unless specified otherwise): T_A = +25°C; MCLK_IN = 12 MHz, MCLK_SRC_SEL = 0, Fs = 48 kHz; path is internal routing engine to AMP3/4_OUT, analog and digital gains are all set to 0 dB; HPF disabled.

Parameter [1]		Minimum	Typical	Maximum	Unit
Passband (normalized to 0.417× 10^{-3} Fs)	–0.05 dB corner	—	0.48	—	Fs
	–3.0 dB corner	—	0.50	—	Fs
Passband ripple (0.417 ×10^{-3} Fs to 0.417 Fs; normalized to 0.417 × 10^{-3} Fs)		–0.04	—	0.063	dB
Stopband attenuation (0.545 Fs to Fs)		60	—	—	dB
Total group delay [2] (ASP input)		—	9.35/Fs	—	s
Total group delay [2] (SoundWire input)		—	10.35/Fs	—	s

1. Response scales with Fs (based on internal MCLK_IN). Specifications are normalized to Fs and denormalized by multiplying by Fs.
2. Informational only; group delay cannot be measured for this block by itself. An additional 5.5/Fs group delay may be present through the serial ports and internal audio bus.

Table 3-9. AMP3/4_OUT (Headphone Output) High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise) Analog and digital gains are all set to 0 dB; T_A = +25°C.

Parameter [1]		Minimum	Typical	Maximum	Unit
Passband (normalized to 0.417 Fs)	–0.05 dB corner	—	0.180×10^{-3}	—	Fs
	–3.0 dB corner	—	19.5×10^{-6}	—	Fs
Passband ripple (0.417 × 10^{-3} Fs to 0.417 Fs; normalized to 0.417 Fs)		—	—	0.015	dB
Phase deviation @ 0.453 × 10^{-3} Fs		—	2.45	—	°
Filter settling time [2]		—	24.5×10^{3}/Fs	—	s

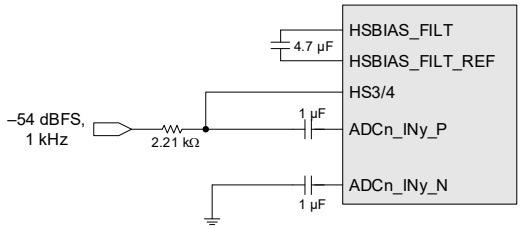
1. Response scales with Fs (internal sample rate, based on MCLK_IN). Specifications are normalized to Fs and are denormalized by multiplying by Fs.
2. Required time for the magnitude of the DC component present at the output of the HPF to reach 5% of the applied DC signal.

Table 3-10. ADCn_INy_x-to-Serial Data Out Characteristics (0.5 V_{RMS} Maximum Input Voltage)

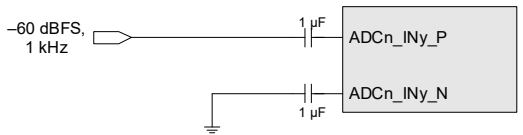
Test conditions (unless specified otherwise): Path is ADCn_INx to decimator to SoundWire Data Port output or ASP_DOUT; Input is a full-scale 1 kHz sine wave; voltages are with respect to ground; typical performance data taken with VDD_A = VDD_IO = 1.8 V, VDD_D = 1.2 V, VDD_P = 3.3 V; min/max performance data taken with VDD_A = 1.66–1.94 V, VDD_IO = 1.8 V, VDD_D = 1.2 V, VDD_P = 3.3 V; TA = +25°C; measurement bandwidth is 20 Hz–20 kHz; Fs = 48 kHz; Internal MCLK = $MCLK_{INT}$ = 12.288 MHz or 24.576 MHz; PGAn_WIDESWING_MODE_EN = 0; Specifications valid for AC-coupled, pseudo-differential inputs except where noted.

Parameter			Minimum	Typical	Maximum	Unit
Dynamic range [1, 2] (see definition in Table 3-1), input = fully-/pseudo-differential	PGA setting: –6 dB	A-weighted	84	90	—	dB
		Unweighted	81	87	—	dB
	PGA setting: 0 dB	A-weighted	88	94	—	dB
		Unweighted	85	91	—	dB
	PGA setting: +6 dB	A-weighted	86	92	—	dB
		Unweighted	83	89	—	dB
	PGA setting: +12 dB	A-weighted	82	88	—	dB
		Unweighted	79	85	—	dB
	PGA setting: +18 dB	A-weighted	77	80	—	dB
		Unweighted	74	77	—	dB
Input-referred, idle-channel integrated noise		PGA setting = –6 dB	—	24	48	µVrms
		PGA setting = 0 dB	—	15	30	µVrms
		PGA setting = +18 dB	—	9.5	14	µVrms
Total harmonic distortion + noise (see definition in Table 3-1)	PGA setting: –6 dB	–1 dBFS	—	–81	–76	dB
	PGA setting: 0 dB	–1 dBFS	—	–86	–76	dB
	PGA setting: +18 dB	–1 dBFS	—	–70	–64	dB
Common-mode rejection [3]			55	73	—	dB
Accuracy	Interchannel gain mismatch (see definition in Table 3-1) [4]		–0.2	—	0.2	dB
	Gain drift (defined in Table 3-1) [5]		–175	—	175	ppm/°C
	PGA gain accuracy (see definition in Table 3-1)		–0.25	—	0.25	dB
	Offset error [5]	DECIMn_HPF_EN = 1	120	127	132	LSB
		DECIMn_HPF_EN = 0	–35,000	–1,500	35,000	LSB
Input	AMP3/4 (HP) amplifier-to-ADC isolation [6]	HP load = 5 kΩ	84	90	—	dB
		HP load = 30 Ω	77	83	—	dB
	AMP1/2 (Speaker) amplifier-to-ADC isolation [7]	Speaker load = 8 Ω	75	80	—	dB
	Interchannel isolation [8]	20 Hz–20 kHz	80	90	—	dB
	Full-scale signal input voltage [9,10], Pseudo-differential input	PGA setting: –6 dB	0.40•VDD_A	0.415•VDD_A	0.43•VDD_A	Vpk
		PGA setting: 0 dB	0.40•VDD_A	0.415•VDD_A	0.43•VDD_A	Vpk
		PGA setting: +6 dB	—	0.207•VDD_A	—	Vpk
		PGA setting: +12 dB	—	0.104•VDD_A	—	Vpk
		PGA setting: +18 dB	—	0.052•VDD_A	—	Vpk
	Input impedance	ADCn_EN = 1	40	50	—	kΩ
		ADCn_EN = 0	500	—	—	kΩ
	Input common-mode voltage		0	—	0.87•VDD_A	V
Turn-on time [11]			—	—	10	ms

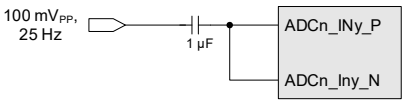
1. ADCn_INy_x dynamic range test configuration is shown here for the mic-bias use case. Due to the voltage divider formed between the internal 2.21 kΩ resistor and the external 2.21 kΩ resistor, a –54 dBFS signal is applied to achieve a –60 dBFS signal at ADCn_INy_P pin.



2. ADCn_INy_x dynamic range test configuration is shown here for the line-in use case.



3. ADCn_INy_x CMRR test configuration.



4. Measurements taken at all defined full-scale signal input voltages.
5. ASP_DOUT code with DECIMn_HPF_EN = 1

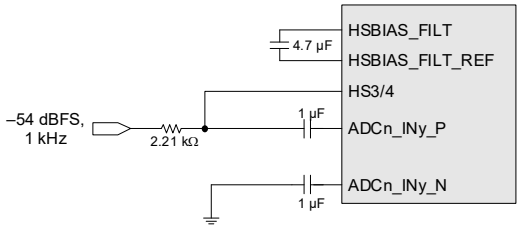
6. Measured with the following settings: ADCn_PGA_GAIN = +18 dB, HPx_PATH_VOL = 0 dB for 30 Ω and 5 kΩ load. Measured without external connections associated with the headset.
7. Measured with the following settings: ADCn_PGA_GAIN = +18 dB, SPKRx_PATH_VOL = 0 dB for 8 Ω load. Measured without external connections associated with the speaker.
8. Measured between both input pairs (ADCn_INy_P to ADCn_INy_N) with 0 dB PGA gain.
9. ADC full-scale input voltage is measured between ADCn_INy_P to ADCn_INy_N.
10. If a differential common-mode input voltage is applied to the ADCn_INy_x pins, the digital domain's overflow interrupt (DECIM_CHn_OVF_INT may not trigger even if the analog front-end exceeds the full-scale signal input voltage specification.
11. Turn-on time is measured from the ADCn_EN = 1 ACK signal to when data comes through an ASP port, with DC-coupled inputs and ADCn_QUICKCHG_EN = 0.

Table 3-11. ADCn_INy_x-to-Serial Data Out Characteristics (1 V_{RMS} Maximum Input Voltage)

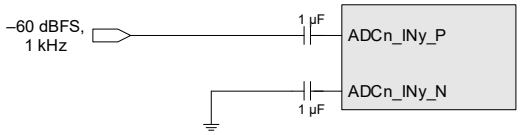
Test conditions (unless specified otherwise): Path is ADCn_INx to decimator to SoundWire Data Port output or ASP_DOUT; Input is a full-scale 1 kHz sine wave; voltages are with respect to ground; typical performance data taken with VDD_A = VDD_IO = 1.8 V, VDD_D = 1.2 V, VDD_P = 3.3 V; min/max performance data taken with VDD_A = 1.66–1.94 V, VDD_IO = 1.8 V, VDD_D = 1.2 V, VDD_P = 3.3 V; TA = +25°C; measurement bandwidth is 20 Hz–20 kHz; Fs = 48 kHz; Internal MCLK = $MCLK_{INT}$ = 12.288 MHz or 24.576 MHz; PGAn_WIDESWING_MODE_EN = 1; Specifications valid for AC-coupled, pseudo-differential inputs except where noted.

Parameter			Minimum	Typical	Maximum	Unit
Dynamic range [1, 2] (see definition in Table 3-1), input = fully-/pseudo-differential	PGA setting: –6 dB	A-weighted	90	93	—	dB
		Unweighted	84	90	—	dB
	PGA setting: 0 dB	A-weighted	85	91	—	dB
		Unweighted	82	88	—	dB
	PGA setting: +6 dB	A-weighted	83	89	—	dB
		Unweighted	80	86	—	dB
	PGA setting: +12 dB	A-weighted	80	86	—	dB
		Unweighted	77	83	—	dB
	PGA setting: +18 dB	A-weighted	75	81	—	dB
		Unweighted	72	78	—	dB
Input-referred, idle-channel integrated noise		PGA setting = –6 dB	—	65	130	µVrms
		PGA setting = 0 dB	—	41	82	µVrms
		PGA setting = +18 dB	—	16	32	µVrms
Total harmonic distortion + noise (see definition in Table 3-1)	PGA setting: –6 dB	–1 dBFS	—	–80	–75	dB
	PGA setting: 0 dB	–1 dBFS	—	–82	–75	dB
	PGA setting: +18 dB	–1 dBFS	—	–70	–64	dB
Common-mode rejection [3]			55	73	—	dB
Accuracy	Interchannel gain mismatch [4]		–0.2	—	0.2	dB
	Gain drift [5]		–175	—	175	ppm/°C
	PGA gain accuracy (see definition in Table 3-1)		–0.25	—	0.25	dB
	Offset error [5]	DECIMn_HPF_EN = 1	120	127	132	LSB
		DECIMn_HPF_EN = 0	–35,000	–1,500	35,000	LSB
Input	AMP3/4 (HP) amplifier-to-ADC isolation [6]	HP load = 5 kΩ	84	90	—	dB
		HP load = 30 Ω	77	83	—	dB
	AMP1/2 (Speaker) amplifier-to-ADC isolation [7]	Speaker load = 8 Ω	75	80	—	dB
	Interchannel isolation [8]	20 Hz–20 kHz	80	90	—	dB
	Full-scale signal input voltage [9,10], Pseudo-differential input	PGA setting: –6 dB	0.80•VDD_A	0.83•VDD_A	0.86•VDD_A	Vpk
		PGA setting: 0 dB	0.40•VDD_A	0.415•VDD_A	0.43•VDD_A	Vpk
		PGA setting: +6 dB	—	0.207•VDD_A	—	Vpk
		PGA setting: +12 dB	—	0.104•VDD_A	—	Vpk
		PGA setting: +18 dB	—	0.052•VDD_A	—	Vpk
	Input impedance	ADCn_EN = 1	40	50	—	kΩ
		ADCn_EN = 0	500	—	—	kΩ
	Input common-mode voltage		0	—	0.87•VDD_A	V
Turn-on time [11]			—	—	10	ms

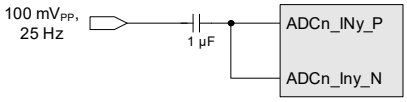
1. ADCn_INy_x dynamic range test configuration is shown here for the mic-bias use case. Due to the voltage divider formed between the internal 2.21 kΩ resistor and the external 2.21 kΩ resistor, a –54 dBFS signal is applied to achieve a –60 dBFS signal at ADCn_INy_P pin.



2.ADCn_INy_x dynamic range test configuration is shown here for the line-in use case.



3.ADCn_INy_x CMRR test configuration.



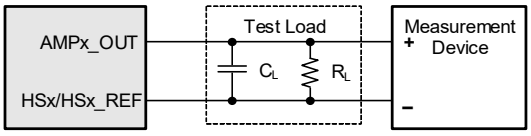
4.Measurements taken at all defined full-scale signal input voltages.
5.ASP_DOUT code with DECIMn_HPF_EN = 1
6.Measured with the following settings: ADCn_PGA_GAIN = +18 dB, HPx_PATH_VOL = 0 dB for 30 Ω and 5 kΩ load. Measured without external connections associated with the headset.
7.Measured with the following settings: ADCn_PGA_GAIN = +18 dB, SPKRx_PATH_VOL = 0 dB for 8 Ω load. Measured without external connections associated with the speaker.
8.Measured between both input pairs (ADCn_INy_P to ADCn_INy_N) with 0 dB PGA gain.
9.ADC full-scale input voltage is measured between ADCn_INy_P to ADCn_INy_N.
10.If a differential common-mode input voltage is applied to the ADCn_INy_x pins, the digital domain's overflow interrupt (DECIM_CHn_OVF_INT may not trigger even if the analog front-end exceeds the full-scale signal input voltage specification.
11.Turn-on time is measured from the ADCn_EN = 1 ACK signal to when data comes through an ASP port, with DC-coupled inputs and ADCn_QUICKCHG_EN = 0.

Table 3-12. Serial Data In-to-AMP3/4_OUT (Headphone Output) Characteristics

Test conditions (unless specified otherwise): Section 2 shows CS42L43 connections; input test signal is a 24-bit full-scale 997 Hz sine wave with 1 LSB of triangular PDF dither applied; GND_A = GND_CP = 0 V; voltages are with respect to ground; typical performance data taken with VDD_CP = VDD_A = VDD_IO = 1.8 V, VDD_P =3.3 V, T_A = +25°C; ADPTPWR_MODE = 111 (adapt to signal); min/max performance data taken with VDD_CP = VDD_A = 1.66–1.94 V, VDD_IO = 1.8 V, VDD_P = 3.3 V, T_A = +25°C; for 48 kHz Fs (default condition) measurement bandwidth is 20 Hz–20 kHz; MCLK_IN input = Internal MCLK = $MCLK_{INT}$ = 24.576 MHz, PLL disabled; mixer attenuation and digital volume = 0 dB.

Parameter [1]				Minimum	Typical	Maximum	Unit
R_L = 3 kΩ VDD_P Mode	Dynamic range	24 bit	A-weighted	108	114	—	dB
			unweighted	105	111	—	dB
	THD+N [2]	24 bit	0 dB	—	–90	–81	dB
			–20 dB	—	–83	—	dB
			–60 dB	—	–51	–46	dB
		16 bit	0 dB	—	–88	–80	dB
			–20 dB	—	–73	—	dB
			–60 dB	—	–33	–27	dB
	Idle channel noise (A-weighted)			—	2.0	—	µV
	Full-scale output voltage [3]			1.50•VDD_A	1.58•VDD_A	1.66•VDD_A	V_{PP}
R_L = 30 Ω VDD_P Mode	Dynamic range	24 bit	A-weighted	108	114	—	dB
			unweighted	105	111	—	dB
	THD+N [2]		Pout = 10 mW	—	–93	—	dB
			Pout = 33.7 mW	—	–85	–79	dB
	Full-scale output voltage [3]			1.50•VDD_A	1.58•VDD_A	1.66•VDD_A	V_{PP}
	Output power [2]			—	33.7	—	mW
R_L = 15 Ω VDD_CP Mode (DACx_PATH_VOL = –6 dB)	Dynamic range	24 bit	A-weighted	102	108	—	dB
			unweighted	99	105	—	dB
	THD+N [2]		Pout = 16.8 mW	—	–85	–79	dB
	Full-scale output voltage [3]			0.71•VDD_A	0.79•VDD_A	0.86•VDD_A	V_{PP}
	Output power [2]			—	16.8	—	mW
R_L = 15 Ω VDD_P Mode	Dynamic range	24 bit	A-weighted	102	108	—	dB
			unweighted	99	105	—	dB
Other characteristics (Table 3-1 gives parameter definitions)	Interchannel isolation [3] (5 kΩ)		217 Hz	—	90	—	dB
			1 kHz	—	90	—	dB
			20 kHz	—	80	—	dB
	Interchannel isolation [3] (30 Ω)		217 Hz	—	90	—	dB
			1 kHz	—	90	—	dB
			20 kHz	—	70	—	dB
	Output offset voltage: mute [3,4] (ANA_MUTE_x = 1)			—	±0.5	±1.0	mV
	Output offset voltage [3,4]			—	±0.5	±2.5	mV
	Load resistance (R_L)		Normal operation [3]	15	—	—	Ω
	Load capacitance (C_L) [3,5]			—	—	10	nF
	Turn-on time [6]			—	—	35	ms

1. One LSB of triangular PDF dither is added to data.
2. Because VDD_CP settings lower than VDD_A reduce the HP amplifier headroom, the specified THD+N performance at full-scale output voltage and power may not be achieved.
3. HP output test configuration. Symbolized component values are specified in the test conditions above.



4. Assumes no external impedance on HSx/HSx_REF. External impedance on HSx/HSx_REF affects the offset and step deviation.
5. Amplifier is guaranteed to be stable with either headphone load setting.
6. Turn-on time is measured from when the HP_EN = 1 ACK signal is received to when the signal appears on the HP output. In most cases, enabling the SRC increases the turn-on time and may exceed the maximum specified value.

Table 3-13. Serial Data In-to-AMP1/2_OUT (Speaker Output) Characteristics

Test conditions (unless specified otherwise): VDD_IO = VDD_CP = VDD_A = 1.8 V, VDD_D = 1.2 V; VDD_AMP = VDD_P = 5.0 V; T_A = +25ºC; 1 kHz sinusoid signal; Fs = 48 kHz; 24-bit audio data.

Parameter			Minimum	Typical	Maximum	Units
Speaker output driver (AMP1/2_OUT_P + AMP1/2_OUT_N)	DC offset at Load		—	300	—	µV
	VDD_AMP leakage current		—	1	—	µA
	Load resistance	Normal operation	4	—	—	Ω
	Load capacitance		—	—	200	pF
DAC to speaker output (AMP1/2_OUT_P + AMP1/2_OUT_N, Load = 8 Ω, 22 µH, BTL)	Maximum output power [1]	VDD_AMP = 5.0 V, 1% THD+N	—	1.3	—	W
	SNR	A-weighted, output signal = 2.83 V_{RMS}	—	123	—	dB
	Dynamic range	A-weighted, –60 dBFS input	92	102	—	dB
	THD	P_O = 1.0 W	—	–60	—	dB
	THD+N	P_O = 1.0 W	—	–60	—	dB
	THD	P_O = 0.5 W	—	–70	—	dB
	THD+N	P_O = 0.5 W	—	–70	–60	dB
	Output noise floor	A-weighted	—	1.3	—	μV_{RMS}
DAC to speaker output (AMP1/2_OUT_P + AMP1/2_OUT_N, Load = 4 Ω, 15 µH, BTL)	Maximum output power [1]	VDD_AMP = 5.0 V, 1% THD+N (QFN)	—	2	—	W
		VDD_AMP = 5.0 V, 1% THD+N (CSP)	—	2.2	—	W
	SNR	A-weighted, output signal = 2.83 V_{RMS}	—	123	—	dB
	Dynamic range	A-weighted, –60 dBFS input	—	102	—	dB
	THD	P_O = 1.0 W	—	–71	—	dB
	THD+N	P_O = 1.0 W	—	–70	—	dB
	THD	P_O = 0.5 W	—	–71	—	dB
	THD+N	P_O = 0.5 W	—	–70	—	dB
	Output noise floor	A-weighted	—	1.3	—	μV_{RMS}

1. This specification defines the capability of the device to deliver the specified power level at the conditions indicated for measurement purposes, using continuous sine waves. It is not intended to imply continuous sine-wave operation indefinitely at those power levels in a real application.

Table 3-14. HSBIAS/MICBIAS Characteristics

Test conditions (unless specified otherwise): Section 2 shows CS42L43 connections; voltages are with respect to ground; parameters can vary with VDD_A and VDD_P; typical performance data taken with VDD_IO = VDD_A = 1.8 V, VDD_P = 3.6 V; min/max performance data taken with VDD_A = 1.66–1.94 V, VDD_IO = 1.8 V, VDD_P = 3.2–5.25; I_{OUT} = 500 µA; T_A = +25°C; HSBIAS_MODE = 2.7 V Mode.

Parameter [1]			Minimum	Typical	Maximum	Unit
Output voltage [2]	BUTTON_DETECT_MODE	HSBIAS_MODE				
	0x (inactive/short detect only)	10 (2.0 V Mode)	1.40	1.86	2.15	V
	01 (short detect only)	11 (2.7 V Mode)	1.75	2.30	2.70	V
	11 (normal mode)	10 (2.0 V Mode) [3]	1.80	2.00	2.10	V
	00/11 (inactive/normal mode)	11 (2.7 V Mode)	2.61	2.75	2.86	V
DC output current, I_{OUT} [4]		HSBIAS_MODE = 10 (2.0 V Mode)	—	0.91	—	mA
		HSBIAS_MODE = 11 (2.7 V Mode)	—	1.2	—	mA
Integrated output noise, 2.7 V Mode (measured at HSx)		f = 100 Hz–20 kHz, T_A = 25°C	—	—	4	μV_{RMS}
Output resistance, R_{OUT} [2]			2.18	2.21	2.24	kΩ

Table 3-14. HSBIAS/MICBIAS Characteristics *(Cont.)*

Test conditions (unless specified otherwise): Section 2 shows CS42L43 connections; voltages are with respect to ground; parameters can vary with VDD_A and VDD_P; typical performance data taken with VDD_IO = VDD_A = 1.8 V, VDD_P = 3.6 V; min/max performance data taken with VDD_A = 1.66–1.94 V, VDD_IO = 1.8 V, VDD_P = 3.2–5.25; I_{OUT} = 500 µA; T_A = +25°C; HSBIAS_MODE = 2.7 V Mode.

Parameter [1]		Minimum	Typical	Maximum	Unit
Output resistance temperature variation	T_A = –40°C to +85°C	—	±3	—	%
Current-sense trip point (mono MIC on HS3/HS4)	HSBIAS_SENSE_TRIP = 000	—	14	—	µA
	HSBIAS_SENSE_TRIP = 001	—	24	—	µA
	HSBIAS_SENSE_TRIP = 010	—	43	—	µA
	HSBIAS_SENSE_TRIP = 011	—	52	—	µA
	HSBIAS_SENSE_TRIP = 100	—	61	—	µA
	HSBIAS_SENSE_TRIP = 101	—	71	—	µA
	HSBIAS_SENSE_TRIP = 110	—	90	—	µA
	HSBIAS_SENSE_TRIP = 111	—	99	—	µA
Current-sense trip point (stereo MIC on HS1 and HS2)	HS1_BIAS_SENSE_TRIP_THRESH/HS2_BIAS_SENSE_TRIP_THRESH = 000	—	26	—	µA
	HS1_BIAS_SENSE_TRIP_THRESH/HS2_BIAS_SENSE_TRIP_THRESH = 001	—	35	—	µA
	HS1_BIAS_SENSE_TRIP_THRESH/HS2_BIAS_SENSE_TRIP_THRESH = 010	—	52	—	µA
	HS1_BIAS_SENSE_TRIP_THRESH/HS2_BIAS_SENSE_TRIP_THRESH = 011	—	62	—	µA
	HS1_BIAS_SENSE_TRIP_THRESH/HS2_BIAS_SENSE_TRIP_THRESH = 100	—	70	—	µA
	HS1_BIAS_SENSE_TRIP_THRESH/HS2_BIAS_SENSE_TRIP_THRESH = 101	—	79	—	µA
	HS1_BIAS_SENSE_TRIP_THRESH/HS2_BIAS_SENSE_TRIP_THRESH = 110	—	97	—	µA
	HS1_BIAS_SENSE_TRIP_THRESH/HS2_BIAS_SENSE_TRIP_THRESH = 111	—	106	—	µA

1. If HSBIAS_MODE = 01, or given combinations that are not shown above, the internal HSBIAS node is to be shorted to ground. Output from HSBIAS to HS3/HS4 or AMP3_OUT/AMP4_OUT can be controlled independently. When output pins are connected to the HSBIAS under this internally shorted to ground mode (e.g., HSBIAS_MODE = 01), the output is pulled down to ground via an internal resistance of R_{OUT} to the HS3/HS4 or AMP3_OUT/AMP4_OUT pins, which is, in turn, connected internally or externally to ground (per Section 2).
2. The output voltage is the unloaded, open-circuit voltage present at the HSx pin selected as HSBIAS output. AMP3_SENSE and AMP4_SENSE should be disconnected from AMP3 and AMP4 for HS1 and HS2.
3. To avoid ADC performance degradation, do not use ADCn_INy_x/HSx if BUTTON_DETECT_MODE = 11 and HSBIAS_MODE = 10.
4. Specifies use limits for the normal operation and IN short conditions.

Table 3-15. Switching Specifications—HSBIAS/MICBIAS

Test conditions (unless specified otherwise): Section 2 shows CS42L43 connections; voltages are with respect to ground; parameters can vary with VDD_A and VDD_P; typical performance data taken with VDD_IO = VDD_A = VDD_CP = 1.8 V, VDD_P = 3.6 V; min/max performance data taken with VDD_A = 1.66–1.94 V; VDD_IO = VDD_CP = 1.8 V; VDD_P = 3.2–5.25; I_{OUT} = 500 µA (not valid for fall time); T_A = +25°C; AMP3_SENSE and AMP4_SENSE not connected.

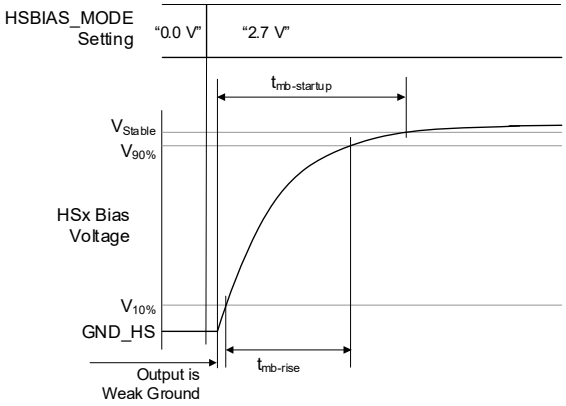
Parameter [1]		Symbol	Minimum	Typical	Maximum	Unit
Bias rise time [2, 3]	HSBIAS_RAMP = 00	$t_{mb-rise}$	—	0.005	—	ms
	HSBIAS_RAMP = 01		—	9	—	ms
	HSBIAS_RAMP = 10		—	22	—	ms
	HSBIAS_RAMP = 11		—	43	—	ms
Bias fall time [4]	HSBIAS_RAMP = 00	$t_{mb-fall}$	—	3	—	ms
	HSBIAS_RAMP = 01		—	15	—	ms
	HSBIAS_RAMP = 10		—	35	—	ms
	HSBIAS_RAMP = 11		—	72	—	ms

Table 3-15. Switching Specifications—HSBIAS/MICBIAS *(Cont.)*

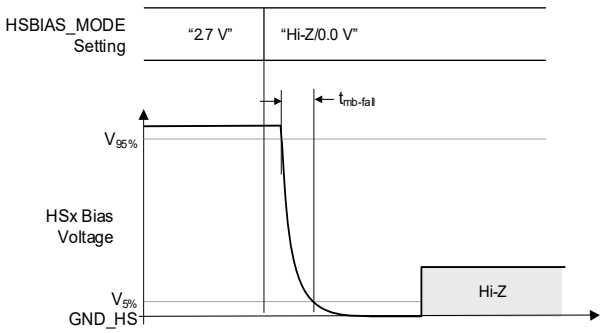
Test conditions (unless specified otherwise): Section 2 shows CS42L43 connections; voltages are with respect to ground; parameters can vary with VDD_A and VDD_P; typical performance data taken with VDD_IO = VDD_A = VDD_CP = 1.8 V, VDD_P = 3.6 V; min/max performance data taken with VDD_A = 1.66–1.94 V; VDD_IO = VDD_CP = 1.8 V; VDD_P = 3.2–5.25; I_{OUT} = 500 µA (not valid for fall time); T_A = +25°C; AMP3_SENSE and AMP4_SENSE not connected.

Parameter [1]			Symbol	Minimum	Typical	Maximum	Unit
Bias transition time [5, 6]	Condition 1 [7]	1.8 V → Hi-Z	$t_{mb-tran}$	—	92	—	µs
		2.0 V → Hi-Z		—	92	—	µs
		2.3 V → Hi-Z		—	93	—	µs
	Condition 2 [8]	2.7 V → 2.3 V	$t_{mb-tran}$	—	43	—	µs
		1.8 V → 2.3 V		—	34	—	µs
		2.0 V → 2.3 V		—	32	—	µs
		2.0 V → 2.7 V		—	21	—	µs
		2.3 V → 1.8 V		—	40	—	µs
		2.0 V → 1.8 V		—	20	—	µs
		1.8 V → 2.0 V		—	10000	—	µs
		1.8 V → 2.7 V		—	10000	—	µs
	Condition 3 [9]	Hi-Z → 1.8 V	$t_{mb-tran}$	—	96	—	µs
		Hi-Z → 2.3 V		—	96	—	µs
	Condition 4 [9,10]	2.7 V → 2.0 V	$t_{mb-tran}$	—	0.02	—	ms
		2.7 V → 1.8 V		—	0.03	—	ms
		2.3 V → 2.0 V		—	10	—	ms
		2.3 V → 2.7 V		—	10	—	ms
	Condition 5 [11]	Hi-Z → 2.7 V, HSBIAS_RAMP = 01	$t_{mb-tran}$	—	183	—	µs
		Hi-Z → 2.7 V, HSBIAS_RAMP = 10		—	198	—	µs
		Hi-Z → 2.7 V, HSBIAS_RAMP = 11		—	220	—	µs
Bias droop [12]		Condition 2 [8]	$V_{mb-droop}$	—	—	650	mV
Bias startup-to-stable time [13]		HSBIAS_RAMP = 00	$t_{mb-startup}$	—	0.01	—	ms
		HSBIAS_RAMP = 01		—	14	—	ms
		HSBIAS_RAMP = 10		—	36	—	ms
		HSBIAS_RAMP = 11		—	65	—	ms

1. HSBIAS/MICBIAS startup timing example

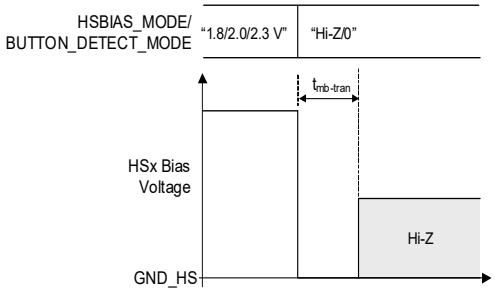


2. HSBIAS/MICBIAS rise time is measured from 10% to 90% of the final output voltage. Transitions are specified with an HSBIAS_FILT capacitance of 4.7 µF.
3. Under the specified configuration, the HSBIAS/MICBIAS transitions with an exponential rise time.
4. HSBIAS/MICBIAS fall time is the time associated with the bias output voltage falling from 95% to 5% of the programmed typical output voltage. If transitioning to Hi-Z, the output does not enter Hi-Z state until the internal digital counter completes, as determined by the HSBIAS_RAMP setting.

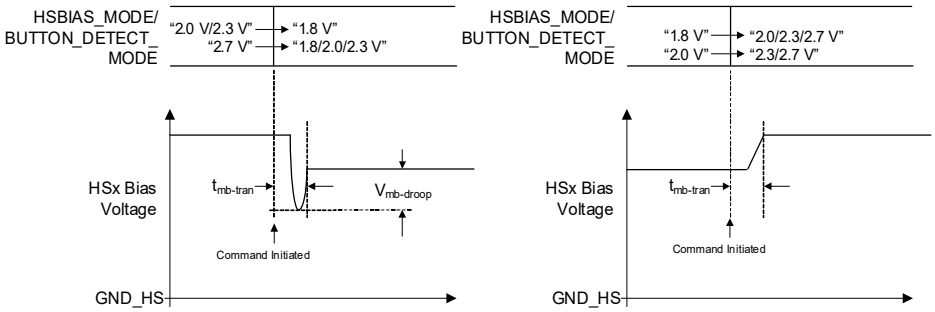


5. HSBIAS/MICBIAS transitions between the Ground Mode and on modes occur with no transition state.
6. External loads are removed for all transitions to or from Hi-Z.

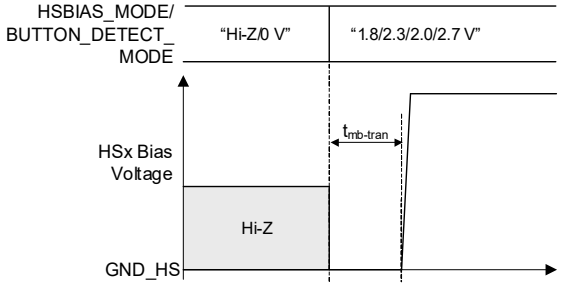
7. Condition 1 transition timing.



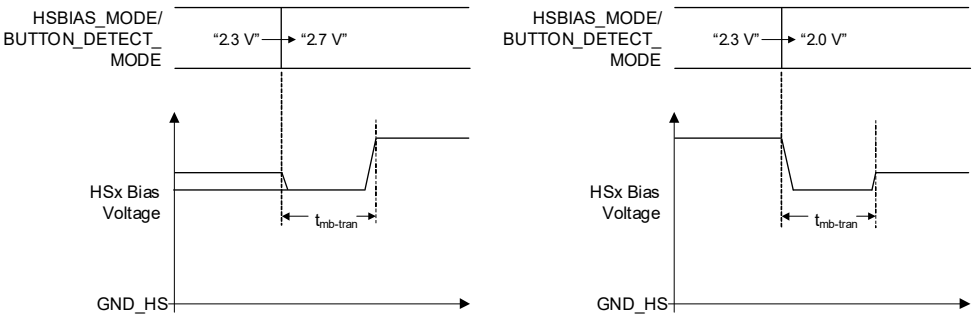
8. Condition 2 transition timing.



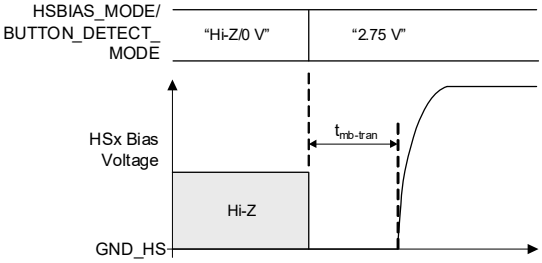
9. Due to isolation between HSBIAS/MICBIAS internal node and HSx pins, the following is informational only and cannot be measured externally. Condition 3 applies when transitioning from Hi-Z or 0 V Mode to 1.8 or 2.3 V Mode.
Condition 4 applies when transitioning from Hi-Z or 0 V Mode to 2.0 or 2.7 V Mode with HSBIAS_RAMP = 00.



10. Condition 4 also applies when transitioning from 2.3 V Mode to 2.0 or 2.75 V Mode.



11. Condition 5 applies when transitioning from Hi-Z or 0 V Mode to 2.75 V Mode with HSBIAS_RAMP = 01/10/11.



12. The bias droop specification is the HSx bias voltage at the pin when an external microphone load of 2.3 kΩ is applied.
13. HSBIAS/MICBIAS startup to stable time period begins when the bias output voltage starts to be applied. The period ends when the output voltage is stable (output voltage is at 95% of its programmed typical value).

Table 3-16. DC Characteristics

Test conditions (unless specified otherwise): Section 2 shows CS42L43 connections; voltages are with respect to ground; VDD_IO = VDD_CP = VDD_A = 1.8 V, VDD_P = 3.3 V; T_A = +25°C.

Parameter			Minimum	Typical	Maximum	Unit
CP_FILT_x (No load connected to AMP3/4_OUT)	VDD_P Mode (ADPTPWR_MODE = 001)	CP_FILT_P	—	2.6	—	V
		CP_FILT_N	—	–2.6	—	V
	VDD_CP Mode (ADPTPWR_MODE = 010)	CP_FILT_P	—	VDD_CP	—	V
		CP_FILT_N	—	–VDD_CP	—	V
	VDD_CP/2 Mode (ADPTPWR_MODE = 011)	CP_FILT_P	—	VDD_CP/2	—	V
		CP_FILT_N	—	–VDD_CP/2	—	V
	VDD_CP/3 Mode (ADPTPWR_MODE = 100)	CP_FILT_P	—	VDD_CP/3	—	V
		CP_FILT_N	—	–VDD_CP/3	—	V
HS3/HS4 ground switch resistance			—	0.4	0.65	Ω
HSn_CLAMP depletion FET ground switch resistance			—	1	—	Ω
Other DC filter	VREF1_FILT voltage		—	VDD_A	—	V
	VREF2_FILT voltage		0.87	0.90	0.93	V
	HP output current limiter on threshold [1]		50	120	190	mA
	VDD_D power-on reset threshold (V_{POR})	Up	—	0.78	—	V
		Down	—	0.67	—	V
	VDD_IO power-on reset threshold (V_{POR})	Up	—	1.13	—	V
		Down	—	0.98	—	V
AMP3/4_OUT (headphone out) pull-down resistance [2,3]		HP_PULLDOWN_SEL = 1001	—	9.3	—	kΩ
		HP_PULLDOWN_SEL = 1010	—	5.8	—	kΩ
		HP_PULLDOWN_SEL = 1100	—	0.9	—	kΩ
Headset Type Detect Comparator 1 level			—	0.79	—	V
Headset Type Detect Comparator 2 level			—	1.31	—	V
Headset Type Detect Comparator 3 level			—	1.76	—	V
Charge pump disable time			—	—	30	ms

1. The HP output current limiter threshold spec is valid only while the Class H rails are in 1.8 V Mode.
2. Typical values have ±20% tolerance.
3. Clamp is disabled (HP_AUTO_CLAMP_DISABLE = 1) and DAC is powered down (HP_EN = 0).

Table 3-17. Power-Supply Rejection Ratio (PSRR) Characteristics

Test conditions (unless specified otherwise): Section 2 shows CS42L43 connections; input test signal held low (all zero data); voltages are with respect to ground; VDD_IO = VDD_A = 1.8 V, VDD_P = 5.0 V; T_A = +25°C.

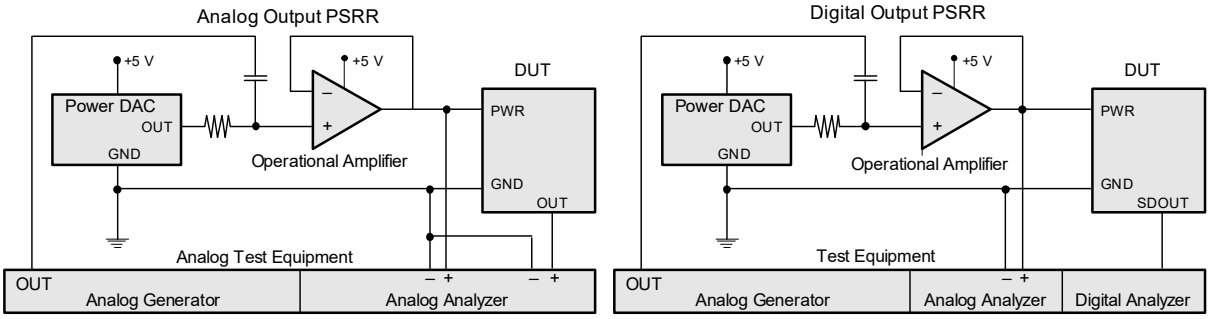
Parameter [1]		Minimum	Typical	Maximum	Unit
ADCn_INy_x PSRR with 1 Vpp signal and +12 dB analog gain, differential input, AC-coupled to VDD_P supply	217 Hz	—	110	—	dB
	1 kHz	—	105	—	dB
	20 kHz	—	100	—	dB
ADCn_INy_x PSRR with 100 mVpp signal and +12 dB analog gain, differential input, AC-coupled to VDD_A supply	217 Hz	—	80	—	dB
	1 kHz	—	80	—	dB
	20 kHz	—	75	—	dB
AMP3/4_OUT (headphone out) (–6 dB analog gain) PSRR with 100 mVpp signal AC coupled to VDD_A supply [2]	217 Hz	—	75	—	dB
	1 kHz	—	75	—	dB
	20 kHz	—	70	—	dB
AMP3/4_OUT (headphone out) (–6 dB analog gain) PSRR with 100 mVpp signal AC-coupled to VDD_CP supply [2]	217 Hz	—	85	—	dB
	1 kHz	—	85	—	dB
	20 kHz	—	65	—	dB
AMP3/4_OUT (headphone out) (0 dB analog gain) PSRR with 100 mVpp signal AC coupled to VDD_P supply	217 Hz	—	80	—	dB
	1 kHz	—	80	—	dB
	20 kHz	—	60	—	dB
HSBIAS (HSBIAS = 2.7 V mode, I_{OUT} = 500 µA) PSRR with 100 mVpp signal AC coupled to VDD_A supply	217 Hz	90	105	—	dB
	1 kHz	85	100	—	dB
	20 kHz	60	83	—	dB
HSBIAS (HSBIAS = 2.7 V mode, I_{OUT} = 500 µA) PSRR with 100 mVpp signal AC coupled to VDD_P supply [3,4]	217 Hz	90	108	—	dB
	1 kHz	80	95	—	dB
	20 kHz	60	70	—	dB
HSBIAS (HSBIAS = 2.0 V mode, I_{OUT} = 500 µA) PSRR with 100 mVpp signal AC coupled to VDD_A supply [3,4]	217 Hz	65	75	—	dB
	1 kHz	60	70	—	dB
	20 kHz	48	55	—	dB
HSBIAS (HSBIAS = 2.0 V mode, I_{OUT} = 500 µA) PSRR with 100 mVpp signal AC coupled to VDD_P supply [3,4]	217 Hz	65	75	—	dB
	1 kHz	60	70	—	dB
	20 kHz	48	55	—	dB

Table 3-17. Power-Supply Rejection Ratio (PSRR) Characteristics *(Cont.)*

Test conditions (unless specified otherwise): Section 2 shows CS42L43 connections; input test signal held low (all zero data); voltages are with respect to ground; VDD_IO = VDD_A = 1.8 V, VDD_P = 5.0 V; T_A = +25°C.

Parameter [1]		Minimum	Typical	Maximum	Unit
DAC to speaker output (AMP1/2_OUT_P + AMP1/2_OUT_N, Load = 8 Ω, 22 µH, BTL) PSRR with 100 mVpp signal AC coupled to VDD_A supply	217 Hz	—	125	—	dB
	10 kHz	—	90	—	dB
DAC to speaker output (AMP1/2_OUT_P + AMP1/2_OUT_N, Load = 8 Ω, 22 µH, BTL) PSRR with 100 mVpp signal AC coupled to VDD_AMP supply	217 Hz	—	120	—	dB
	10 kHz	—	90	—	dB
DAC to speaker output (AMP1/2_OUT_P + AMP1/2_OUT_N, Load = 4 Ω, 15 µH, BTL) PSRR with 100 mVpp signal AC coupled to VDD_A supply	217 Hz	—	125	—	dB
	10 kHz	—	90	—	dB
DAC to speaker output (AMP1/2_OUT_P + AMP1/2_OUT_N, Load = 4 Ω, 15 µH, BTL) PSRR with 100 mVpp signal AC coupled to VDD_AMP supply	217 Hz	—	120	—	dB
	10 kHz	—	90	—	dB

1. PSRR test configuration: Typical PSRR can vary by approximately 6 dB below the indicated values.



2. No load connected to any analog outputs.
3. The accurate reference, which sets the HSBIAS output voltage, is powered from VDD_A.
4. If HS3/4_CLAMP are connected to HS3/4, PSRR is reduced by 6 dB.

Table 3-18. Typical Power Consumption

Test conditions (unless specified otherwise): GND_A = GND_CP = GND_D = GND_HS = 0 V; voltages are with respect to ground; LDO_EN = VDD_P; typical performance data taken with VDD_A = VDD_CP = VDD_IO = 1.8 V, VDD_P = 3.3 V, VDD_AMP = 5.0 V, T_A = +25°C; 1 kHz sinusoidal test tone; ASP_FSYNC = 48 kHz; Fs = 48 kHz; ASP_BCLK = 12.288 MHz; mixer attenuation = 0 dB; JACKDET_MODE = 11, BUTTON_DETECT_MODE = 01 (short detect only), all other fields are set to defaults; control port inactive; input clock/data are held low when not required; test load is R_L = 30 Ω and C_L = 1 nF and Class H Mode = Adapt-to-Output Signal (ADPTPWR_MODE = 111) for AMP3/4_OUT (headphone output); speaker load = 8 Ω + 22 µH; measured values include currents consumed by the codec and do not include current delivered to external loads unless specified otherwise (e.g., AMP3/4_OUT).

Use Case					Typical Current (µA)					Total Typical Power (µW)
					i_{VDD_A}	i_{VDD_CP}	i_{VDD_IO}	i_{VDD_P}	i_{VDD_AMP}	
1	A	Off [1]			0	0	0	3.5	0.1	12
2	A	Standby [2]		Depletion FETs on [3]	0.2	3	862	33	0.1	1667
	B			Mic button press detect and tip sense active, Depletion FETs off [4]	0.2	3	862	42	0.1	1696
	C			Mic button press detect	0.2	3	862	35	0.1	1673
	D			Tip sense	0.2	3	862	38	0.1	1683
3	A	Mono ADC Record		Fs = 48 kHz @ 24-bit, C_{load} = 60 pF; ASP Slave Mode	450	3	1800	350	0.1	5211
4	A	Stereo Record		Fs = 48 kHz @ 24-bit, C_{load} = 60 pF; ASP Slave Mode	600	3	2000	470	0.1	6237
5	A	2-channel DMIC record		PDM clock = 3.072 MHz, Fs = 48 kHz @ 24-bit	60	3	3300	58	0.1	6245
6	A	Stereo Headphone Amp Playback	No signal	Class H mode = VDD_CP/3	1450	1000	2300	95	0.1	8864
	B			Class H mode = VDD_CP/2	1450	1300	2300	95	0.1	9404
	C			Class H mode = VDD_CP	1450	2600	2300	95	0.1	11744
	D			Class H mode = 2.6 V	1450	580	2300	3500	0.1	19345
	E		0.1 mW	Class H mode = VDD_CP/3	1450	2100	2350	95	0.1	10934
	F			Class H mode = VDD_CP/2	1450	2800	2350	95	0.1	12194
	G			Class H mode = VDD_CP	1450	5600	2350	95	0.1	17234
	H			Class H mode = 2.6 V	1450	580	2350	6600	0.1	29665
	I		2.0 mW	Class H mode = VDD_CP/2	1450	9600	2350	95	0.1	24434
	J			Class H mode = VDD_CP	1450	18550	2350	95	0.1	40544
	K			Class H mode = 2.6 V	1450	1050	2350	18451	0.1	69619

Table 3-18. Typical Power Consumption *(Cont.)*

Test conditions (unless specified otherwise): GND_A = GND_CP = GND_D = GND_HS = 0 V; voltages are with respect to ground; LDO_EN = VDD_P; typical performance data taken with VDD_A = VDD_CP = VDD_IO = 1.8 V, VDD_P = 3.3 V, VDD_AMP = 5.0 V, T_A = +25°C; 1 kHz sinusoidal test tone; ASP_FSYNC = 48 kHz; Fs = 48 kHz; ASP_BCLK = 12.288 MHz; mixer attenuation = 0 dB; JACKDET_MODE = 11, BUTTON_DETECT_MODE = 01 (short detect only), all other fields are set to defaults; control port inactive; input clock/data are held low when not required; test load is R_L = 30 Ω and C_L = 1 nF and Class H Mode = Adapt-to-Output Signal (ADPTPWR_MODE = 111) for AMP3/4_OUT (headphone output); speaker load = 8 Ω + 22 µH; measured values include currents consumed by the codec and do not include current delivered to external loads unless specified otherwise (e.g., AMP3/4_OUT).

Use Case				Typical Current (µA)					Total Typical Power (µW)
				i_{VDD_A}	i_{VDD_CP}	i_{VDD_IO}	i_{VDD_P}	i_{VDD_AMP}	
7	A	Class D Speaker Playback per channel	ASP to DAC to AMP1/2_OUT_x — Quiescent	1250	3	2350	68	7	6745
8	A	Voice call (ASP, Stereo Headphone and Mono ADC)	Headset (HSIN, HSBIAS_MODE = 10)	1800	1000	2450	170	0.1	10012
	B	Voice call (SoundWire, Stereo Headphone and Mono ADC)	Headset (HSIN, HSBIAS_MODE = 10)	1800	1000	2000	170	0.1	9202
9	A	Block adders [5]	PLL: MCLK_IN = 6.144 MHz, PLL_{OUT} = 196.608 MHz	165	0	157	0	0	580
	B		HSBIAS, 2.0 V Mode	0	0	0	15	0	50
	C		HSBIAS, 2.7 V Mode	58	0	0	210	0	797
	D		2-ch crude LDO wide swing protection for inactive input paths	0	0	2	36	0	122

1. Off configuration: Clock/data lines held low; $\overline{\text{RESET}}$ = LOW; VDD_A = VDD_IO = VDD_CP = VDD_AMP = 0 V; VDD_P = 3.3 V.
2. Standby configuration: Clock/data lines held low; VDD_A = VDD_CP = VDD_IO = 1.8 V; VDD_P = 3.3 V; VDD_AMP = 5 V; $\overline{\text{RESET}}$ = 1; AFE weak bias disabled.
3. To turn on the depletion FETs, clear HS_CLAMP_DISABLE.
4. To turn off the depletion FETs, set HS_CLAMP_DISABLE.
5. The values in these rows specify only the power consumption of the specified feature and do not include any power used by the rest of the device.

Table 3-19. Maximum Power Consumption

Test conditions (unless specified otherwise): GND_A = GND_CP = GND_D = GND_HS = 0 V; voltages are with respect to ground; LDO_EN = VDD_P; typical performance data taken with VDD_A = VDD_CP = VDD_IO = 1.8 V, VDD_P = 3.3 V, VDD_AMP = 5.0 V, T_A = +25°C; 1 kHz sinusoidal test tone; ASP_FSYNC = 48 kHz; Fs = 48 kHz; ASP_BCLK = 12.288 MHz; mixer attenuation = 0 dB; JACKDET_MODE = 11, BUTTON_DETECT_MODE = 01 (short detect only), all other fields are set to defaults; control port inactive; input clock/data are held low when not required; test load is R_L = 30 Ω and C_L = 1 nF and Class H Mode = Adapt-to-Output Signal (ADPTPWR_MODE = 111) for AMP3/4_OUT (headphone output); speaker load = 8 Ω + 22 µH; measured values include currents consumed by the codec and do not include current delivered to external loads unless specified otherwise (e.g., AMP3/4_OUT).

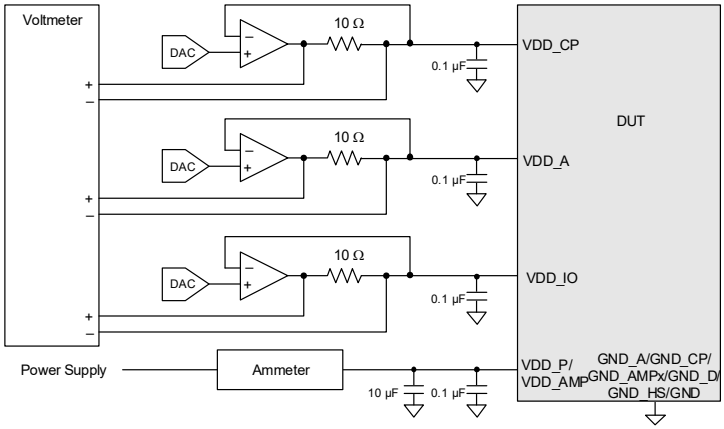
Use Case					Maximum Current (µA)					Total Maximum Power (µW)
					i_{VDD_A}	i_{VDD_CP}	i_{VDD_IO}	i_{VDD_P}	i_{VDD_AMP}	
1	A	Off [1]			0.5	0.5	0.5	6	0.5	37
2	A	Standby [2]		Depletion FETs on [3]	9	9	1300	42	1	2783
	B			Mic button press detect and tip sense active, Depletion FETs off [4]	9	9	1300	52	1	2835
	C			Mic button press detect	9	9	1300	44	1	2793
	D			Tip sense	9	9	1300	48	1	2814
3	A	Mono ADC Record	Fs = 48 kHz @ 24-bit, Cload = 60 pF; ASP Slave Mode		600	9	3200	460	1	9810
4	A	Stereo Record	Fs = 48 kHz @ 24-bit, Cload = 60 pF; ASP Slave Mode		1000	9	3600	620	1	12202
5	A	2-channel DMIC record		PDM clock = 3.072 MHz, Fs = 48 kHz @ 24-bit	100	9	4500	82	1	9377
6	A	Stereo Headphone Amp Playback	No signal	Class H mode = VDD_CP/3	2000	1500	3600	118	1	14399
	B			Class H mode = VDD_CP/2	2000	1800	3600	118	1	14981
	C			Class H mode = VDD_CP	2000	3600	3600	118	1	18473
	D			Class H mode = 2.6 V	2000	800	3600	4500	1	36046
	E		0.1 mW	Class H mode = VDD_CP/3	2000	2600	3800	118	1	16921
	F			Class H mode = VDD_CP/2	2000	3400	3800	118	1	18473
	G			Class H mode = VDD_CP	2000	6800	3800	118	1	25069
	H			Class H mode = 2.6 V	2000	800	3800	7800	1	53759
	I		2.0 mW	Class H mode = VDD_CP/2	2000	11000	3800	118	1	33217
	J			Class H mode = VDD_CP	2000	21200	3800	118	1	53005
	K			Class H mode = 2.6 V	2000	1350	3800	22000	1	129376

Table 3-19. Maximum Power Consumption *(Cont.)*

Test conditions (unless specified otherwise): GND_A = GND_CP = GND_D = GND_HS = 0 V; voltages are with respect to ground; LDO_EN = VDD_P; typical performance data taken with VDD_A = VDD_CP = VDD_IO = 1.8 V, VDD_P = 3.3 V, VDD_AMP = 5.0 V, T_A = +25°C; 1 kHz sinusoidal test tone; ASP_FSYNC = 48 kHz; Fs = 48 kHz; ASP_BCLK = 12.288 MHz; mixer attenuation = 0 dB; JACKDET_MODE = 11, BUTTON_DETECT_MODE = 01 (short detect only), all other fields are set to defaults; control port inactive; input clock/data are held low when not required; test load is R_L = 30 Ω and C_L = 1 nF and Class H Mode = Adapt-to-Output Signal (ADPTPWR_MODE = 111) for AMP3/4_OUT (headphone output); speaker load = 8 Ω + 22 µH; measured values include currents consumed by the codec and do not include current delivered to external loads unless specified otherwise (e.g., AMP3/4_OUT).

Use Case				Maximum Current (µA)					Total Maximum Power (µW)
				i_{VDD_A}	i_{VDD_CP}	i_{VDD_IO}	i_{VDD_P}	i_{VDD_AMP}	
7	A	Class D Speaker Playback per channel	ASP to DAC to AMP1/2_OUT_x Quiescent	1600	9	3800	85	1	10945
8	A	Voice call (ASP, Stereo Headphone and Mono ADC)	Headset (HSIN, HSBIAS_MODE = 10)	2400	1500	3800	240	1	16203
	B	Voice call (SoundWire, Stereo Headphone and Mono ADC)	Headset (HSIN, HSBIAS_MODE = 10)	2400	1500	3200	240	1	15039
9	A	Block adders [5]	PLL: MCLK_IN = 6.144 MHz, PLL_{OUT} = 196.608 MHz	200	0	180	0	0	737
	B		HSBIAS, 2.0 V Mode	0	0	8	19	0	114
	C		HSBIAS, 2.7 V Mode	80	0	8	250	0	1483
	D		2-ch crude LDO wide swing protection for inactive input paths	0	0	8	44	0	247

1. Off configuration: Clock/data lines held low; $\overline{\text{RESET}}$ = LOW; VDD_A = VDD_IO = VDD_CP = VDD_AMP = 0 V; VDD_P = 3.3 V.
2. Standby configuration: Clock/data lines held low; VDD_A = VDD_CP = VDD_IO = 1.8 V; VDD_P = 3.3 V; VDD_AMP = 5 V; $\overline{\text{RESET}}$ = 1.
3. To turn on the depletion FETs, clear HS_CLAMP_DISABLE.
4. To turn off the depletion FETs, set HS_CLAMP_DISABLE.
5. The values in these rows specify only the power consumption of the specified feature and do not include any power used by the rest of the device.



The current draw on the VDD_A, VDD_CP, and VDD_IO power supply pins is derived from the measured voltage drop across a 10 Ω series resistor between the associated supply source and each voltage supply pin. Given the larger currents that are possible on the VDD_P supply, an ammeter is used for the measurement.

Table 3-20. Main Clock (MCLK_IN) Input Specifications

Test conditions (unless specified otherwise): Section 2 shows CS42L43 connections; voltages are with respect to ground; parameters can vary with VDD_IO; min/max performance data taken with VDD_IO = 1.66–1.94 VVDD_A = 1.8 V, VDD_D = 1.2 V, VDD_P = 3.6 V; T_A = +25°C; logic 0 = ground, logic 1 = VDD_IO.

Parameter [1]		Symbol	Minimum	Maximum	Unit
MCLK_IN frequency [2, 3]		f_{MCLK}	0.973	25.81	MHz
MCLK_IN duty cycle		—	45	55	%
MCLK_IN rise time (10% to 90% of VDD_IO)		t_r	—	3	ns
MCLK_IN fall time (90% to 10% of VDD_IO)		t_f	—	3	ns
MCLK_IN TIE jitter (100 Hz to 6 MHz)	Parametric performance Functional performance [4]	j_{TIE}	— —	100 70	ps_{RMS} ns_{RMS}
500-cycle jitter	Functional performance [4]	j_{500}	—	74	ns_{PP}

1. MCLK_IN in this table refers to the external clock supplied to an external MCLK_IN pin.
2. Clock generation and output timing specifications are a function of the MCLK_IN input.
3. Operation with MCLK_IN below 2.8224 MHz may result in degraded performance.
4. Defined as the range that the CS42L43 is capable of operating functionally, but may not meet all parametric specifications.

Table 3-21. Analog Headset Interface Characteristics

Test conditions (unless specified otherwise): Section 2 shows CS42L43 connections; GND_D = GND_CP = GND_A = GND_HS = 0 V; VDD_A = VDD_CP = VDD_IO = 1.8 V; VDD_D = 1.2 V; VDD_P = VDD_AMP =5.0 V; voltages are with respect to ground; parameters can vary with VDD_A and VDD_AMP; T_A = +25°C.

Parameter			Minimum	Typical	Maximum	Unit
HS DC-detection parameters[1]	Function A impedance		—	—	70	Ω
	Function D impedance		110	—	180	Ω
	Function B impedance		210	—	290	Ω
	Function C impedance		360	—	680	Ω
	Headphone accessory (tip-ring-sleeve, TRS) [2]		—	—	100	Ω
	Headset accessory (four-pole tip-ring-ring-sleeve, TRRS) [2]		100	—	—	Ω
	Headphone load [3]		—	—	1	kΩ
	Line load [3]		5	—	—	kΩ
	Mic button press detect threshold	HSBIAS = 1.8 V	440	500	560	mV
		HSBIAS = 2.0 V	480	550	620	mV
		HSBIAS = 2.3 V	550	625	700	mV
		HSBIAS = 2.75 V	670	750	830	mV
	HS DC detect threshold [4]		—	(M+1) x 100 / (128 x 2^N)	—	%
	HS DC detect ADC resolution		—	8	—	bits
	HS DC detect filtered sample rate		—	187	—	Hz
	DC level detect power-up time [5]		—	11	—	ms

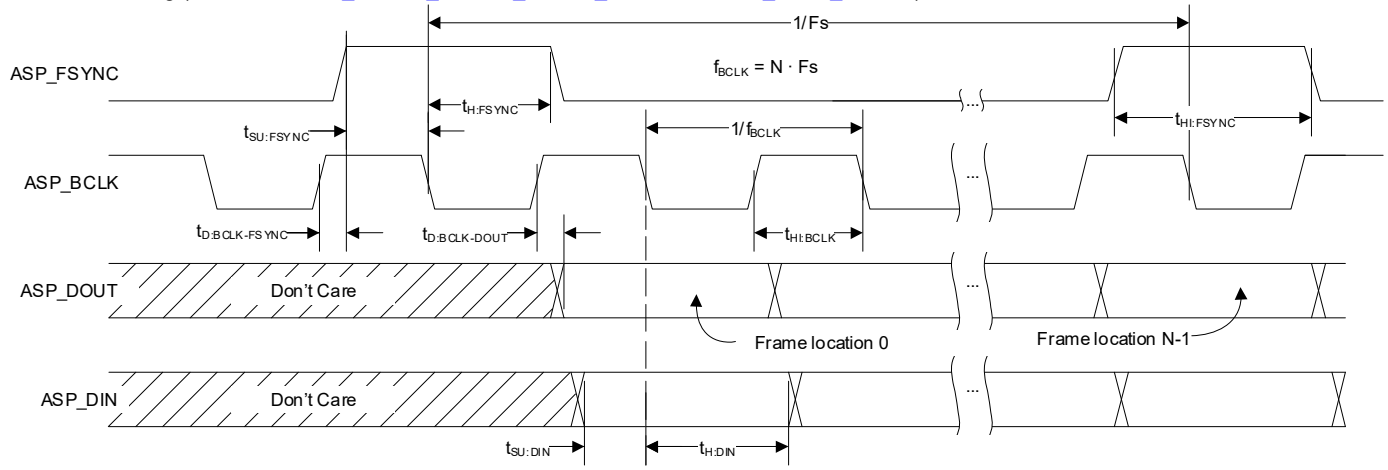
1. Compatible with *Android Wired Headset Specification (V1.1)*.
2. Measured between HS3 and HS4.
3. Measured from AMP3/4_OUT to GND_HS.
4. M is the decimal representation of the HSDET_LVL1_THRESH setting and N = HSDET_LVL_COMBWIDTH field setting.
5. Time for the DC level detector circuits to completely power up/settle after MIC_LVL_DET_DISABLE is cleared and while input signal is greater than 0.75×1.5625×MICBIAS of the threshold set point.

Table 3-22. PCM Audio Serial Port Interface Characteristics—8 mA Drive Strength, 60 pF Load

Test conditions (unless specified otherwise): Typical performance data taken with VDD_A = 1.8 V, VDD_D = 1.2 V, LDO_EN = 0 V (LDO disabled), VDD_IO = 1.8 V; min/max performance data taken with VDD_A = 1.8 V, VDD_D = 1.2 V; LDO_EN = 0 V (LDO disabled), VDD_IO = 1.66 to 1.94 V; Ground = GND_A = GND_D = 0 V, all voltages with respect to ground; T_A = 25°C; I/O drive strengths = 8 mA (default); input transition time = 3 ns; C_L = 60 pF.

Parameter [1,2,3]	Symbol	Minimum	Typical	Maximum	Unit
ASP_FSYNC input sample/frame rate	Fs	8	—	192	kHz
ASP_BCLK frequency C_L = 60 pF	f_{BCLK}	32•Fs	—	12.288	MHz
ASP_BCLK high period	$t_{HI:BCLK}$	0.45/f_{BCLK}	—	0.55/f_{BCLK}	s
ASP_FSYNC setup time before ASP_BCLK latching edge (Slave Mode) [4]	$t_{SU:FSYNC}$	5	—	—	ns
ASP_FSYNC hold time after ASP_BCLK latching edge (Slave Mode) [4]	$t_{H:FSYNC}$	3	—	—	ns
ASP_FSYNC high period–TDM	$t_{HI:FSYNC}$	1/f_{BCLK}	—	(n-1)/f_{BCLK}	s
ASP_FSYNC delay time after BCLK launching edge (Master Mode) [3]	$t_{D:BCLK-FSYNC}$	3	—	20	ns
ASP_DIN setup time before ASP_BCLK latching edge [4]	$t_{SU:DIN}$	5	—	—	ns
ASP_DIN hold time after ASP_BCLK latching edge [4]	$t_{H:DIN}$	3	—	—	ns
ASP_DOUT delay time after ASP_BCLK latching edge [4]	$t_{D:BCLK-DOUT}$	3	—	20	ns
ASP_DOUT Hi-Z delay time after ASP_BCLK latching edge [4,5]	$t_{DLY:Hi-Z}$	2	—	20	ns

1. In ASP Master Mode, output clock frequencies follow the SYS_CLK frequency proportionally. Any deviation of the clock source from the nominal supported rates are directly imparted to the output clock rate by the same factor (e.g., +100 ppm offset in the frequency of SYS_CLK becomes a +100 ppm offset in ASP_FSYNC, and ASP_BCLK).
2. ASP TDM Timing (shown with ASP_FSYNC_FRAME_START_DLY = 010, ASP_BCLK_INV = 0):



3. All timing is relative to 50% of the VDD_IO supply level.
4. FSYNC and Data may be latched/launched on either the rising or falling edge of ASP_BCLK as determined by ASP_BCLK_INV.
5. TDM interface Hi-Z timing. The launching edge in this case is the edge opposite that which launches data.

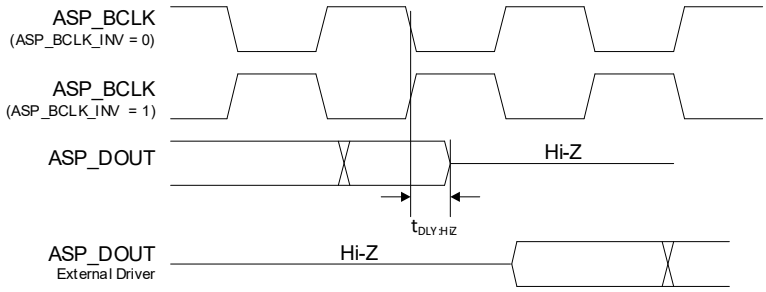
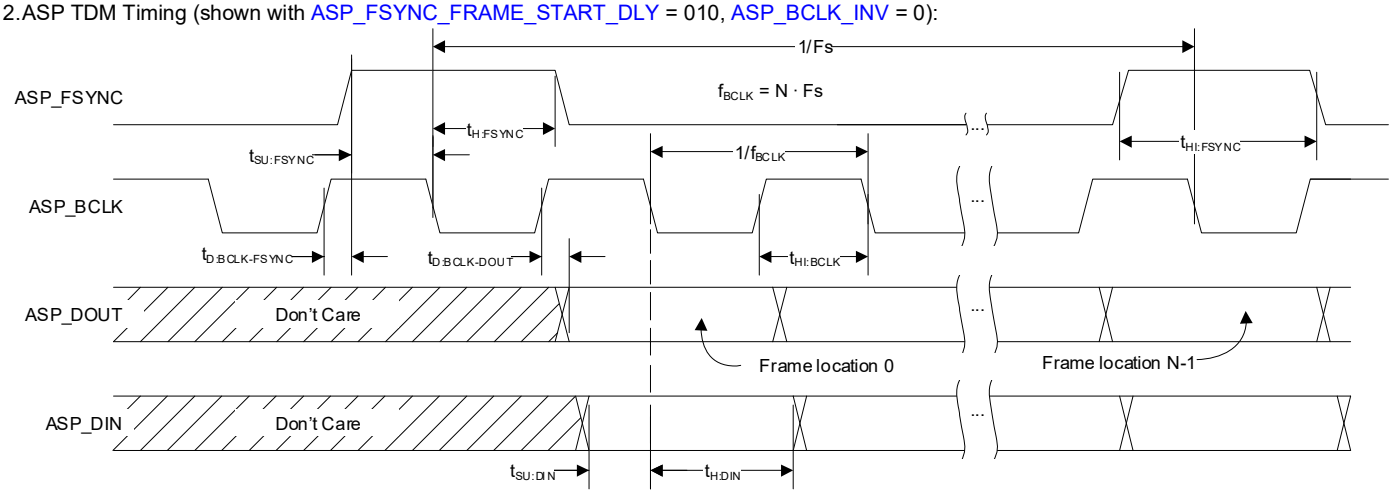


Table 3-23. PCM Audio Serial Port Interface Characteristics—16 mA Drive Strength, 30 pF Load

Test conditions (unless specified otherwise): Typical performance data taken with VDD_A = 1.8 V, VDD_D = 1.2 V, LDO_EN = 0 V (LDO disabled), VDD_IO = 1.8 V; min/max performance data taken with VDD_A = 1.8 V, VDD_D = 1.2 V; LDO_EN = 0 V (LDO disabled), VDD_IO = 1.66 to 1.94 V; Ground = GND_A = GND_D = 0 V, all voltages with respect to ground; T_A = 25°C; I/O drive strengths = 16 mA; input transition time = 3 ns; C_L = 30 pF.

Parameter [1,2,3]	Symbol	Minimum	Typical	Maximum	Unit
ASP_FSYNC input sample/frame rate	Fs	8	—	192	kHz
ASP_BCLK frequency C_L = 30 pF	f_{BCLK}	32•Fs	—	24.576	MHz
ASP_BCLK high period	$t_{HI:BCLK}$	0.45/f_{BCLK}	—	0.55/f_{BCLK}	s
ASP_FSYNC setup time before ASP_BCLK latching edge (Slave Mode) [4]	$t_{SU:FSYNC}$	5	—	—	ns
ASP_FSYNC hold time after ASP_BCLK latching edge (Slave Mode) [4]	$t_{H:FSYNC}$	3	—	—	ns
ASP_FSYNC high period–TDM	$t_{HI:FSYNC}$	1/f_{BCLK}	—	(n-1)/f_{BCLK}	s
ASP_FSYNC delay time after BCLK launching edge (Master Mode) [3]	$t_{D:BCLK-FSYNC}$	3	—	12	ns
ASP_DIN setup time before ASP_BCLK latching edge [4]	$t_{SU:DIN}$	5	—	—	ns
ASP_DIN hold time after ASP_BCLK latching edge [4]	$t_{H:DIN}$	3	—	—	ns
ASP_DOUT delay time after ASP_BCLK latching edge [4]	$t_{D:BCLK-DOUT}$	3	—	12	ns
ASP_DOUT Hi-Z delay time after ASP_BCLK latching edge [4,5]	$t_{DLY:Hi-Z}$	2	—	12	ns

1. In ASP Master Mode, output clock frequencies follow the SYS_CLK frequency proportionally. Any deviation of the clock source from the nominal supported rates are directly imparted to the output clock rate by the same factor (e.g., +100 ppm offset in the frequency of SYS_CLK becomes a +100 ppm offset in ASP_FSYNC, and ASP_BCLK).
2. ASP TDM Timing (shown with ASP_FSYNC_FRAME_START_DLY = 010, ASP_BCLK_INV = 0):



3. All timing is relative to 50% of the VDD_IO supply level.
4. FSYNC and Data may be latched/launched on either the rising or falling edge of ASP_BCLK as determined by ASP_BCLK_INV.
5. TDM interface Hi-Z timing. The launching edge in this case is the edge opposite that which launches data.

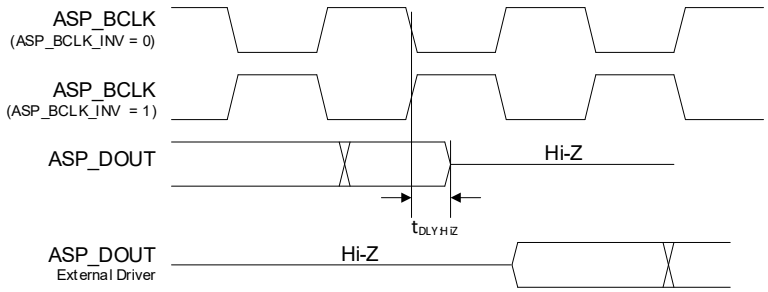


Table 3-24. Switching Characteristics—S/PDIF Transmitter

Test conditions (unless specified otherwise): Outputs: Logic 0 = 0 V, Logic 1 = VL = 1.8 V; C_L = 60 pF.

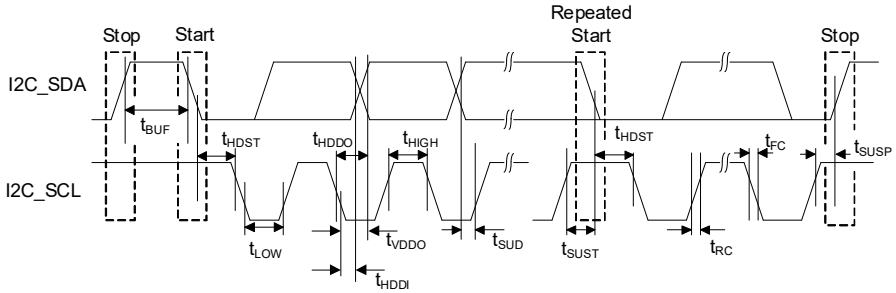
Parameter	Minimum	Typical	Maximum	Unit
Frame rate	8	—	192	kHz
S/PDIF transmitter output time-interval error (TIE) jitter	—	500	—	ps RMS

Table 3-25. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise): Section 2 shows connections to, and passive components used with, the CS42L43; all voltages are with respect to ground; parameters can vary with VDD_IO; min/max performance data taken with VDD_IO = 1.66–1.94 V, VDD_A = 1.8 V, VDD_D = 1.2 V, VDD_P = 3.3 V; logic 0 = ground, logic 1 = VDD_IO; T_A = +25°C; I2C_SDA_DRV = 10 (4 mA, default); input and output timings are measured with respect to V_{IH}/V_{IL}; I2C_SDA C_{LOAD} = 400 pF; R_P calculated according to footnote 4.

Parameter [1]		Symbol [2]	Minimum	Maximum	Unit
I2C_SCL clock frequency		f_{SCL}	—	1000	kHz
Clock low time		t_{LOW}	500	—	ns
Clock high time		t_{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)		t_{HDST}	260	—	ns
Setup time for repeated start		t_{SUST}	260	—	ns
Rise time of I2C_SCL and I2C_SDA	Standard Mode Fast Mode Fast Mode Plus	t_{RC}	— — —	1000 300 120	ns ns ns
Fall time of I2C_SCL and I2C_SDA	Standard Mode Fast Mode Fast Mode Plus	t_{FC}	6.5 6.5 6.5	106.5 106.5 81.5	ns ns ns
Fall time variation between I2C_SDA and I2C_SCL (relative to V_{IH}/V_{IL})	Standard Mode Fast Mode Fast Mode Plus	t_{FC_VAR}	100 100 75	— — —	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
I2C_SDA setup time to I2C_SCL rising		t_{SUD}	50	—	ns
I2C_SDA input hold time from I2C_SCL falling		t_{HDDI}	0	—	ns
I2C_SDA output hold time from I2C_SCL falling		t_{HDDO}	50	—	ns
Output data valid (Data/Ack) [3]	Standard Mode Fast Mode Fast Mode Plus	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
I2C_SDA bus capacitance		C_B	—	400	pF
I2C_SCL/I2C_SDA pull-up resistance [4]		R_P	500	—	Ω
Input spike pulse suppression	I2C_SCL, I2C_SDA	t_{ps}	0	50	ns
Time from power-up to control port ready (after VDD_P, VDD_D, VDD_CP, and VDD_IO exceed the minimum operating voltage)		—	—	1	ms
SFT_RESET assertion to control port active		—	—	1000	µs

1. All timing is relative to thresholds specified in Table 3-30.
2. I²C control-port timing.



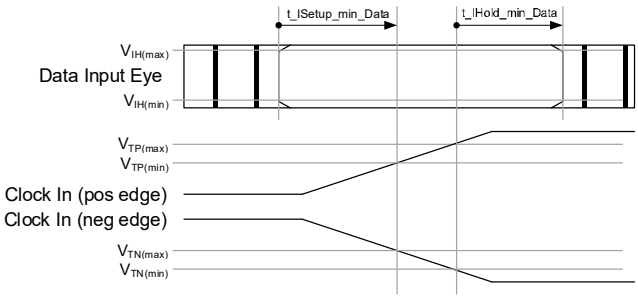
3. Time from falling edge of I2C_SCL until data output is valid.
4. The minimum R_P value (resistor shown in Section 2) is determined by using the maximum level of VDD_IO, the minimum sink current strength of its respective output, and the maximum low-level output voltage V_{OL}. The maximum R_P value may be determined by how fast its associated signal must transition (e.g., the lower the value of R_P, the faster the I²C bus is able to operate for a given bus load capacitance). See I²C bus specification referenced in Section 8.

Table 3-26. SoundWire Interface Specifications

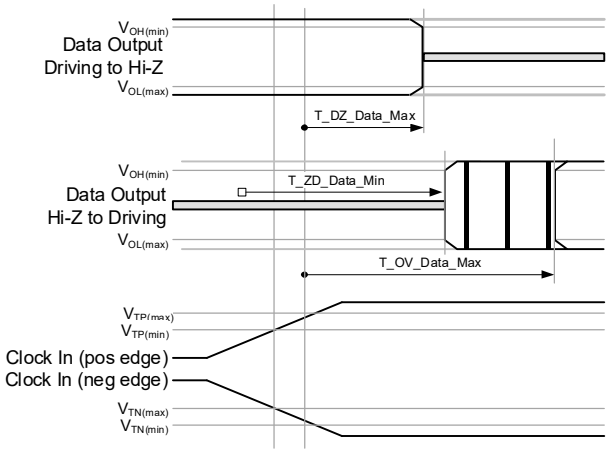
Test conditions (unless specified otherwise): Section 2 shows connections to, and passive components used with, the CS42L43; all voltages are with respect to ground; parameters can vary with VDD_IO; min/max performance data taken with VDD_IO = 1.66–1.94 V, VDD_A = 1.8 V, VDD_D = 1.2 V, VDD_P = 3.3 V; logic 0 = ground, logic 1 = VDD_IO; TA = +25°C; SCP_PhyOutCtrl registers set to 0x02 for small data bus and 0x04 for large data bus; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds for VIO_SWIRE logic (as shown in Table 3-30).

Parameter		Symbol	Minimum	Maximum	Unit
SWIRE_CLK input frequency [1]	Small data bus (10 to 60 pF capacitance) Large data bus (10 to 100 pF capacitance)	F_{SWSCLK}	2.4 2.4	12.7 10.1	MHz MHz
Input clock slew time	Small data bus Large data bus	— —	2.0 2.0	5.4 9.0	ns ns
Data output slew time [2]		T_{SLEW}	2.0	—	ns
Data driver disable time [3]		T_{DZ}	—	4.0	ns
Delay from clock to Active State		T_{ZD}	7.9	—	ns
Time for data output valid	Small data bus (10 to 60 pF capacitance) Large data bus (10 to 100 pF capacitance)	T_{OV_DATA}	— —	27.6 31.6	ns ns
Data output hold time		T_{OH_DATA}	6.7	—	ns
Data input minimum setup time [3]		$T_{ISETUP\_MIN\_DATA}$	—	0.0	ns
Data input minimum hold time		$T_{IHOLD\_MIN\_DATA}$	—	4.0	ns
Clock input duty cycle		—	45	55	%
VDD_IO logic (SWIRE_CLK and SWIRE_DATAx pins)	High-level output voltage Low-level output voltage High-level input voltage Low-level input voltage Input voltage threshold (rising edge) Input voltage threshold (falling edge)	V_{OH} V_{OL} V_{IH} V_{IL} V_{TP} V_{TN}	0.8•VDD_IO — 0.65•VDD_IO — 0.5•VDD_IO 0.35•VDD_IO	— 0.2•VDD_IO — 0.33•VDD_IO 0.65•VDD_IO 0.5•VDD_IO	V V V V V V

1. If the SWIRE_CLK is used as the source for the PLL, then the minimum active-mode operation is 3 MHz.
2. Slew time for positive or negative clock/data edge on clock/data output between 0.2 and 0.8•VDD_IO.
3. SoundWire data timing.



Data Input Timing



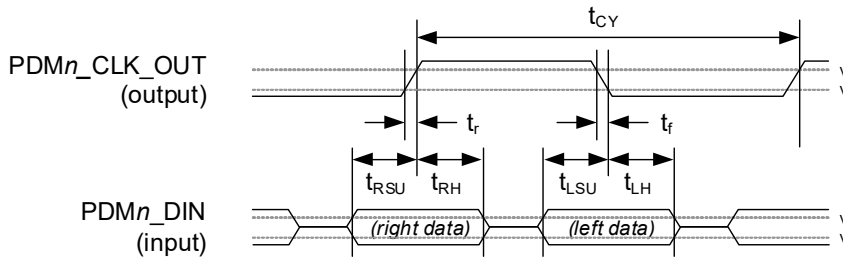
Data Output Timing

Table 3-27. Digital Input (PDM/DMIC) Interface Specifications

Test conditions (unless specified otherwise): Typical performance data taken with VDD_A = 1.8 V, VDD_D = 1.2 V, LDO_EN = 0 V (LDO disabled), VDD_IO = 1.8 V; min/max performance data taken with VDD_A = 1.8 V, VDD_D = 1.2 V, VDD_IO = 1.66 to 1.94 V; LDO_EN = 0 V (LDO disabled), Ground = GND_A = GND_D = 0 V, all voltages with respect to ground; TA = +25°C; default I/O drive strengths.

Parameter [1]	Symbol	Minimum	Typical	Maximum	Unit
PDM*n*_CLK_OUT cycle time	t_{CY}	320	326	1302	ns
PDM*n*_CLK_OUT duty cycle	—	45	—	55	%
PDM*n*_CLK_OUT rise/fall time (60 pF load)	t_r, t_f	1.5	—	30	ns
PDM*n*_DIN (left) setup time to falling PDM*n*_CLK_OUT edge	t_{LSU}	22	—	—	ns
PDM*n*_DIN(left) hold time from falling PDM*n*_CLK_OUT edge	t_{LH}	0.5	—	—	ns
PDM*n*_DIN (right) setup time to rising PDM*n*_CLK_OUT edge	t_{RSU}	22	—	—	ns
PDM*n*_DIN (right) hold time from rising PDM*n*_CLK_OUT edge	t_{RH}	0.5	—	—	ns
Informative:					
Full-scale input level [2] 0 dBFS digital core input, 0 dB gain	—	—	–6	—	dBFS

1.PDM/DMIC interface timing



2.The digital input signal level is measured in dBFS, where 0 dBFS is the signal level equal to the full-scale range of the PDM input. The full-scale range is defined as the amplitude of a 1 kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1 kHz sine wave that can fit in the digital output range without clipping.

Table 3-28. Master Interface Timing (SPI Master)—12 MHz

Test conditions (unless specified otherwise): Min/max performance data taken with VDD_A = 1.8 V, VDD_D = 1.2 V, VDD_IO = 1.66 to 1.94 V; LDO_EN = 0 V (LDO disabled), Ground = GND_A = GND_D = 0 V, all voltages with respect to ground; TA = +25°C; default I/O drive strengths.

Parameter [1]		Symbol	Minimum	Maximum	Unit
$\overline{SS}$ falling edge to SCK rising edge		t_{SSU}	30	—	ns
SCK falling edge to $\overline{SS}$ rising edge		t_{SHO}	0	—	ns
SCK pulse cycle time		t_{SCY}	80	—	ns
SCK pulse width low		t_{SCL}	38.4	—	ns
SCK pulse width high		t_{SCH}	38.4	—	ns
MISO (input) to SCK setup time		t_{DSU}	10	—	ns
MISO (input) to SCK hold time		t_{DHO}	0	—	ns
MOSI (output) valid from falling SCK edge	SCLK slew (90%–10%) = 5 ns, C_{LOAD} (SIO*n*) = 60 pF	t_{DV}	—	15	ns
MOSI (output) hold from falling SCK edge	SCLK slew (90%–10%) = 5 ns, C_{LOAD} (SIO*n*) = 60 pF	t_{HO}	0	—	ns

1.Master interface (SPI) timing

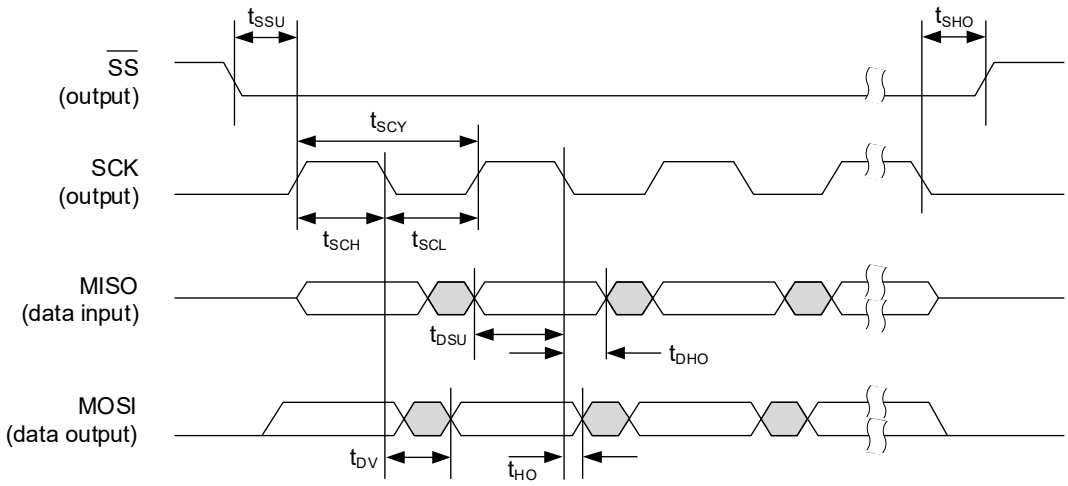


Table 3-29. Master Interface Timing (SPI Master)—24 MHz

Test conditions (unless specified otherwise): Min/max performance data taken with VDD_A = 1.8 V, VDD_D = 1.2 V, VDD_IO = 1.66 to 1.94 V; LDO_EN = 0 V (LDO disabled), Ground = GND_A = GND_D = 0 V, all voltages with respect to ground; TA = +25°C; default I/O drive strengths.

Parameter [1]		Symbol	Minimum	Maximum	Unit
$\overline{SS}$ falling edge to SCK rising edge		t_{SSU}	10	—	ns
SCK falling edge to $\overline{SS}$ rising edge		t_{SHO}	0	—	ns
SCK pulse cycle time		t_{SCY}	40	—	ns
SCK pulse width low		t_{SCL}	19.2	—	ns
SCK pulse width high		t_{SCH}	19.2	—	ns
MISO (input) to SCK setup time		t_{DSU}	6	—	ns
MISO (input) to SCK hold time		t_{DHO}	0	—	ns
MOSI (output) valid from falling SCK edge	SCLK slew (90%–10%) = 5 ns, C_{LOAD} (SIO*n*) = 30 pF	t_{DV}	—	12	ns
MOSI (output) hold from falling SCK edge	SCLK slew (90%–10%) = 5 ns, C_{LOAD} (SIO*n*) = 30 pF	t_{HO}	0	—	ns

1.Master interface (SPI) timing

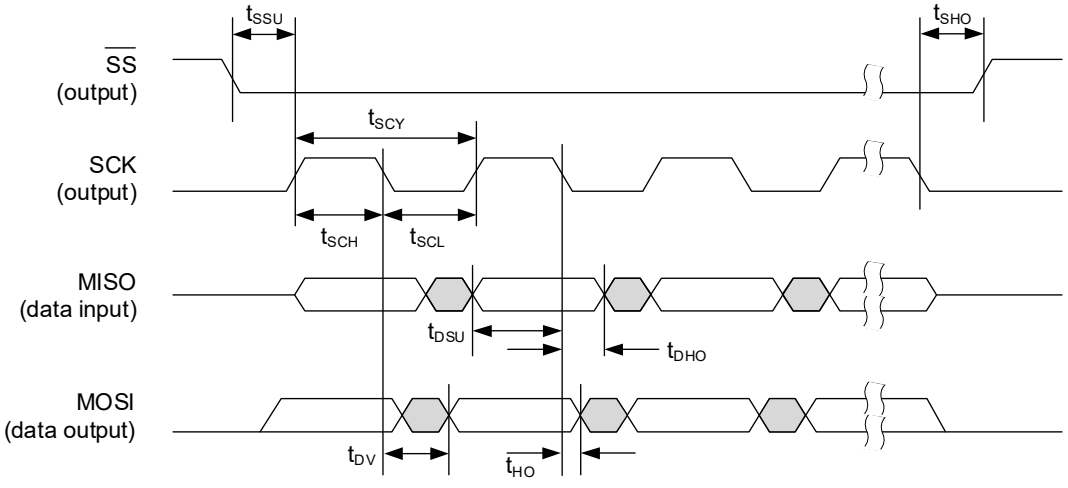


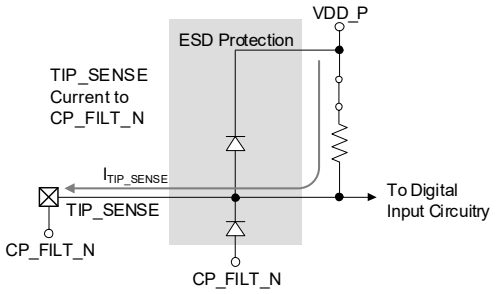
Table 3-30. Pad and Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise): Section 2 shows CS42L43 connections; voltages are with respect to ground; parameters can vary with VDD_IO and VDD_P; typical performance data taken with VDD_P = 3.3 V, VDD_IO = VDD_CP = VDD_A = 1.8 V, VDD_D = 1.2 V, T_A = +25°C; min/max performance data taken with VDD_CP = VDD_A = 1.8 V, VDD_D = 1.2 V; VDD_P = 3.2–5.25 V; VDD_IO = 1.66–1.94 VT_A = +25°C; C_L = 60 pF.

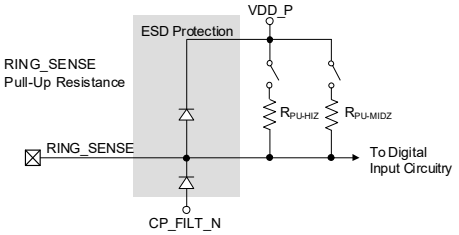
Parameter [1]			Symbol	Min	Typ	Max	Unit
Input leakage current [2,3]		ASP_x	I_{in}	—	—	±4	µA
		RING_SENSE, TIP_SENSE		—	—	±500	nA
		I2C_SDA, I2C_SCL		—	—	±1	µA
		$\overline{IRQ}$		—	—	±100	nA
		$\overline{RESET}$, LDO_EN		—	—	±10	µA
		SWIRE_CLK, SWIRE_DATAx		—	—	±4	µA
Internal weak pull-up or pull-down			—	550	—	3500	kΩ
Digital I/O hysteresis (I²C only)			—	0.065•VDD_IO	—	—	V
Input capacitance [2]			—	—	—	10	pF
$\overline{IRQ}$ current sink (V_{OL} = 0.3 V maximum)			—	825	—	—	µA
$\overline{RESET}$ assertion time			—	1.8	—	—	µs
VDD_IO Logic [4]	Non-I²C	High-level output voltage [5]	V_{OH}	VDD_IO – 0.2	—	—	V
		Low-level output voltage [6]	V_{OL}	—	—	0.2	V
		High-level input voltage	V_{IH}	0.7•VDD_IO	—	—	V
		Low-level input voltage	V_{IL}	—	—	0.3•VDD_IO	V
	I²C only	Low-level output voltage [7]	V_{OL}	—	—	0.2•VDD_IO	V
		High-level input voltage	V_{IH}	0.7•VDD_IO	—	—	V
		Low-level input voltage	V_{IL}	—	—	0.3•VDD_IO	V
VDD_P Logic (excluding TIP_SENSE and RING_SENSE)		High-level input voltage	V_{IH}	1.0	—	—	V
		Low-level input voltage	V_{IL}	—	—	0.2	V
I2C_SDA output drive strength [8]		I2C_SDA_DRV = 00	—	0.5	1	1.5	mA
		I2C_SDA_DRV = 01		1	2	3	mA
		I2C_SDA_DRV = 10		2	4	6	mA
		I2C_SDA_DRV = 11		4	8	12	mA
ASP, SPI, PDM*n*_CLK_OUT output drive strength [9]		x_DRV = 001	—	1	2	3	mA
		x_DRV = 010		2	4	6	mA
		x_DRV = 011		4	8	12	mA
		x_DRV = 111		8	16	24	mA
TIP_SENSE [10]		High-level input voltage	V_{IH}	0.89•VDD_P	—	—	V
		Low-level input voltage	V_{IL}	—	—	2	V
RING_SENSE [11]	RINGSENSE_TRIM = 0x0	High-level input voltage	V_{IH}	0.15•VDD_P	—	—	V
		Low-level input voltage	V_{IL}	—	—	0.03•VDD_P	V
	RINGSENSE_TRIM = 0x2	High-level input voltage	V_{IH}	0.40•VDD_P	—	—	V
		Low-level input voltage	V_{IL}	—	—	0.28•VDD_P	V
TIP_SENSE pull-up resistance			—	0.9	1.2	1.5	MΩ
RING_SENSE pull-up resistance	RINGSENSE_PULLUP_HIZ = 1	RINGSENSE_TRIM = 0x0; R_{PU} to Hi-Z	R_{PU-Hi}	1.7	—	2.9	MΩ
		RINGSENSE_TRIM = 0x1; R_{PU} to Hi-Z	$R_{PU-Hi-Z}$	0.8	—	1.4	MΩ
	RINGSENSE_PULLUP_HIZ = 0	R_{PU} to Mid-Z	$R_{PU-MIDZ}$	12.15	—	20.25	kΩ
TIP_SENSE current to CP_FILT_N [10]		JACKDET_MODE = 11 (Short-Detect Mode)	I_{TIP_SENSE}	1	—	2.9	µA
RING_SENSE current to GND_CP [11]		RINGSENSE_TRIM = 0x0 (Hi-Z Mode)	I_{RING_SENSE}	1.0	—	3.2	µA

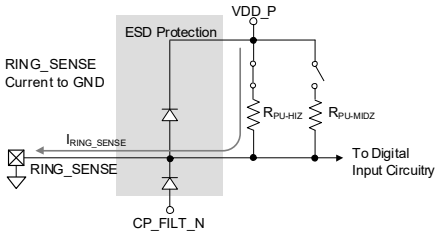
1. See Section 1.2 and Section 1.4 for serial and control-port power rails.
2. Specification is per pin.
3. Includes current through internal pull-up or pull-down resistors on pin.
4. Current measured with V_{OL} = 0.4 V and V_{OH} = VDD_IO - 0.4 V levels.
5. I_{OH} = –100 µA for x_DRV = 10 (8 mA, default).
6. I_{OL} = 100 µA for x_DRV = 10 (8 mA, default).
7. Minimum R_P values (shown in Section 2) are determined from the maximum VDD_IO level, the minimum sink current strength of their respective output, and the maximum low-level output voltage (V_{OL}). Maximum R_P values may be determined by how fast their associated signals must transition (e.g., the lower the R_P value, the faster the I²C bus can operate for a given bus load capacitance).
8. Current measured with V_{OL} = 0.4 V.
9. Current measured with V_{OL} = 0.4 V and V_{OH} = VDD_IO – 0.4 V.

10.TIP_SENSE input circuit. This circuit allows the TIP_SENSE signal to go as low as CP_FILT_N and as high as VDD_P.



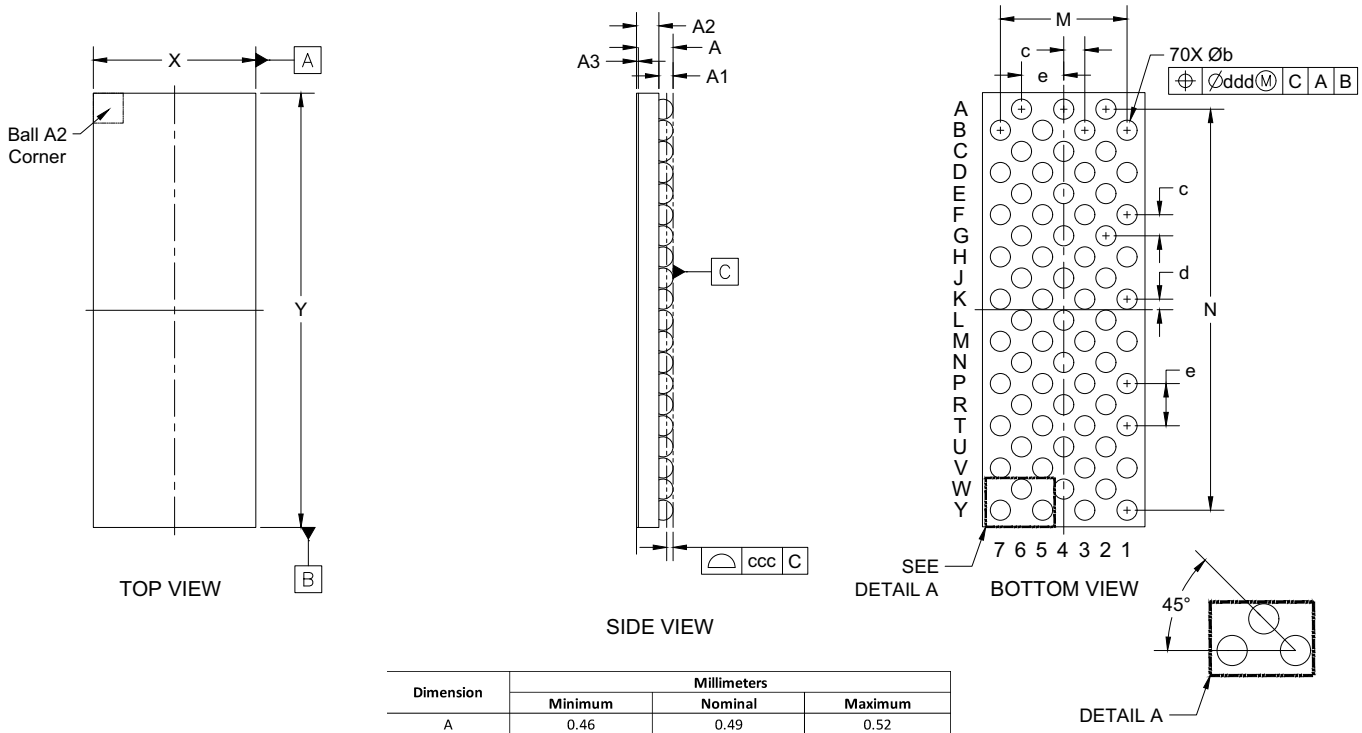
11.RING_SENSE input circuit. This circuit allows the RING_SENSE signal to range between CP_FILT_N and VDD_P, although in practice RING_SENSE is recommended to stay above ground (per Table 3-2).





4 Package Dimensions

4.1 WLCSP Package Dimensions

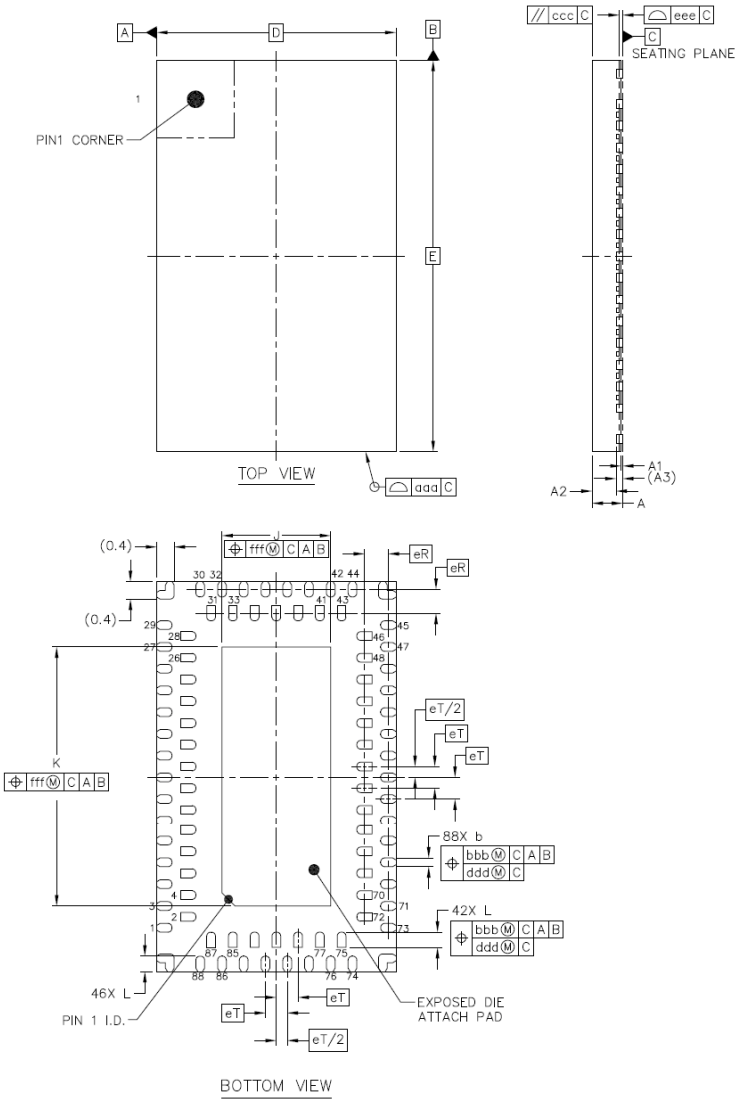


Dimension	Millimeters		
	Minimum	Nominal	Maximum
A	0.46	0.49	0.52
A1	0.175	0.19	0.205
A2	0.285	0.3	0.315
A3	REF	0.025	REF
b	0.24	0.27	0.3
c	REF	0.2828	REF
d	REF	0.1414	REF
e	BSC	0.5657	BSC
M	BSC	1.6971	BSC
N	BSC	5.3741	BSC
X	2.1528	2.1778	2.2028
Y	5.7942	5.8192	5.8442
ccc=0.03			
ddd=0.015			

Notes: Controlling dimension is millimeters.
Dimensioning and tolerances per ASME Y 14.5-2009. The Ball A1 position indicator is for illustration purposes only. Dimension "b" applies to the solder sphere diameter and is measured at the maximum solder sphere diameter, parallel to primary Datum C.
X/Y Tolerances can apply to an individual edge increasing or decreasing by 25um.

Figure 4-1. WLCSP Package Dimensions

4.2 QFN Package Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.65	0.7	0.75
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.152		REF
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	5.5		BSC
	Y	E	9		BSC
LEAD PITCH		eT	0.5		BSC
		eR	0.55		BSC
EP SIZE	X	J	2.4	2.5	2.6
	Y	K	5.9	6	6.1
LEAD LENGTH		L	0.25	0.35	0.45
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD OFFSET		bbb	0.1		
		ddd	0.05		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
EXPOSED PAD OFFSET		fff	0.1		

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
2.0 TOTAL THICKNESS NOT INCLUDE SAW BURR.

Figure 4-2. QFN Package Dimensions

5 Thermal Characteristics

5.1 Typical Thermal Characteristics—JEDEC Four-layer 2s2p Board

Table 5-1. Typical JEDEC Four-layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	WLCSP	QFN	Unit
Junction-to-ambient thermal resistance	θ_{JA}	36.34	30.84	°C/W
Junction-to-board thermal resistance	θ_{JB}	16.24	20.84	°C/W
Junction-to-case thermal resistance	θ_{JC}	1.54	22.63	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	16.06	18.69	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	1.29	1.15	°C/W

Notes:
- Natural convection at the maximum recommended operating temperature T_A (see Table 3-2)
- Four-layer, 2s2p PCB as specified by JESD51-9, and JESD51-11; dimensions: 101.5 × 114.5 × 1.6 mm
- Thermal parameters as defined by JESD51-12

6 Package Marking

Top Side Brand
Line 1: Customer-designated part number
Line 2: Package mark
Line 3: Country of origin (CO)
Line 4: Encoded Wafer/Device ID

Package Mark Fields
C1 = Cirrus Logic Index code 1
C2 = Cirrus Logic Index code 2
RR = Device revision code
LL = Lot sequence code
YY = Year of manufacture
WW = Work week of manufacture

Figure 6-1. WLCSP Package Marking

Top Side Brand
Line 1: Customer-designated part number
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C1 = Cirrus Logic Index code 1
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RR = Device revision code
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Figure 6-2. QFN Package Marking

7 Ordering Information

Table 7-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number
CS42L43	PC Codec with Headphone, MIC Interface and Class D Speaker Drivers	70-ball WLCSP	Yes	Commercial	–40°C to +85°C	Tape and Reel	CS42L43-CWR
		88-pin QFN	Yes	Commercial	–40°C to +85°C	Tape and Reel	CS42L43-CNR

8 References

- Google, *Android Wired Headset Specification, V.1.1,* http://source.android.com/devices/accessories/headset/specification.html
- NXP Semiconductors, *The I2C-Bus Specification and User Manual (UM10204)*, http://ww.nxp.com/
- MIPI Alliance, *MIPI SoundWire Specification, Version 1.2.1* (2022), http://www.mipi.org/
- MIPI Alliance, *MIPI Discovery and Configuration (DisCoSM) Specification, Version 1.0* (2016), http://www.mipi.org/

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.