Technical Bulletin: CS5461A
Functional & Performance Improvements in Revision C

Reference CS5461A Data Sheet revision DS661F2 dated April 2008.

Determining the Silicon Revision of the Integrated Circuit

On the top of the integrated circuit, directly under the part number, is an alpha-numeric line. Characters 3 and 4 in this line represent the silicon revision of the chip. For example, this line indicates that the chip is a "CX" revision chip:

NA**CX****YYWW

This Errata is applicable only to the C revision of the chip.

Dynamic Range of Pulse Outputs (E1, E2, E3)

Revision C

The dynamic range of the pulse outputs has been improved in revision C. When using the pulse outputs to verify the energy measurement accuracy, the device now meets all specified typical accuracy levels listed in the Characteristics and Specifications section of the data sheet.

Programmable Pulse Widths

Revision B

Revision B of the CS5461A had only one fixed pulse width.

Revision C

A register named *PulseWidth* (Address 22) has been added that defines the width of pulse outputs in units of 1/OWR sample. The range is from 1 to 838607. The default value is 0 which enables the hardware pulse width generation to be compatible with the earlier revisions.

$$T_{PW} = PulseWidth \times \frac{1}{(MCLK / K) / 1024}$$

Power Consumption

Revision B

Typical power consumption specification: I_{A+} = 1.3 mA

Revision C

Typical power consumption specification: I_{A+} = 1.1 mA

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Temperature Sensor

Revision B

In revision B of the CS5461A, the temperature sensor has a potential for failure in the low-temperature ranges. Additionally it showed linearity problems and chip-to-chip variations.

Revision C

In revision C of the CS5461A, the temperature gain (T_{Gain}) and temperature offset (T_{Off}) register default values have been updated to the following values to improve the dynamic range and accuracy of the temperature sensor.

T_{Gain} (Address 29) = 0x2F02C3

T_{Off} (Address 30) = 0xF3D35A

All Pass Filter (APF) Function

Revision B

In Revision B of the CS5461A, a phase shift is introduced when the HPF is enabled in only one channel, causing a phase matching issue.

Revision C

In Revision C of the CS5461A, a new Conversion command (0xEC) has been added. In the case that the HPF is enabled in only one channel, using this command will enable the APF function on the other channel, which corrects the phase matching issue.

No Load Threshold

Revision B

Revision B of the CS5461A does not offer no load threshold functionality.

Revision C

Revision C of the CS5461A has been modified to include the LoadIntv register and the LoadMin register. When the accumulated energy within the time defined by the LoadIntv register does not reach the value in the LoadMin register, the pulse outputs will be disabled.

LoadIntv register - Address 25

Determines the duration or interval of the no load detection window in units of 1/OWR. The range is from 1 to 16777215. The default value is 0 which disables this no load threshold feature.

LoadMin register - Address 27

Set the no load threshold. LoadMin is a two's complement value in the range of -1.0 < LoadMin < 1.0, with the binary point to the right of the MSB. Negative values are not allowed. The default value is 0 which disables the no load threshold feature.

DRDY (Data Ready) Delay After Conversion Start

Revision B

The DRDY bit in the Status register is set T seconds after the start of the conversion, where T equals:

$$T = N \times \frac{1}{(MCLK/K)/1024}$$

N equals the value loaded in the Cycle Count register.

Revision C

In revision C of the CS5461A, the HPF settling time is increased to 3000 / OWR seconds. The DRDY delay is increased by 3000 cycles or 750 ms (OWR = 4000) if any HPF is enabled. Or the time between the start of a conversion and the setting of the DRDY bit is T seconds if any HPF is enabled, where T equals:

$$T = N \times \frac{1}{(MCLK/K)/1024} + \frac{3000}{(MCLK/K)/1024}$$

N equals the value loaded in the Cycle Count register.

AC Offset Calibration

Revision B

In revision B of the CS5461A, AC offset calibration would result in the I_{ACOFF} and V_{ACOFF} values being twice as large as necessary.

Revision C

In revision C of the CS5461A, this problem has been corrected.

Maximum Pulse Rate

Revision B

In revision B of the CS5461A, the pulse rate is limited to a maximum of 256 kHz.

Revision C

In revision C of the CS5461A, this problem has been corrected. The maximum pulse rate for revision C is 512 kHz.