WM8325

Processor Power Management Subsystem

DESCRIPTION

The WM8325 is an integrated power-management subsystem which provides a cost-effective, flexible, single-chip solution for power management. It is specifically targeted at the requirements of a range of low-power portable consumer products, but is suitable to any application with a multimedia processor. The WM8325 is designed to operate as a system PMIC supporting the ARM9™, ARM11™ and ARM Cortex-A™ processors, but is also capable of supporting the majority of application and mobile processors at the heart of a wide range of low-power consumer multimedia applications.

The start-up behaviour and configuration is fully programmable in an integrated OTP non-volatile memory. This highly flexible solution helps reduce time-to-market, as changing application requirements can be very easily accommodated in the OTP. The InstantConfig™ interface enables an external EEPROM to configure the WM8325.

The WM8325 power management subsystem comprises four programmable DC-DC converters and eleven LDO regulators (four of which are low-noise for supplying sensitive analogue subsystems). The integrated OTP bootstrap circuitry controls the start-up sequencing and voltages of the converters and regulators as well as the sequencing of system clocks.

The DC-DC converters deliver high performance and high efficiency across a wide range of operating conditions. They are optimised to support the high load current transients seen in modern processor core domains. DC-DC3 / DC-DC4 can be connected together and operated in 'dual' mode to support an increased current load of up to 1.6A.

An on-chip regulator provides power for always-on PMIC functions such as register map and the RTC. The device provides autonomous backup battery switchover. A low-power LDO is included to support 'Alive' processor power domains external to the WM8325.

A 12-bit Auxiliary ADC supports a wide range of applications for internal as well as external analogue sampling, such as voltage detection and temperature measurement.

WM8325 includes a crystal oscillator and an internal RC oscillator to generate all clock signals for autonomous system start-up and processor clocking. A Secure Real-time Clock (S-RTC) and alarm function is included, capable of waking up the system from low-power modes. A watchdog function is provided to ensure system integrity.

To maximise battery life, highly-granular power management enables each function in the WM8325 subsystem to be independently powered down through a control interface or alternatively through register and OTP-configurable GPIOs. The device offers a standby power consumption of <7uA, making it particularly suitable for portable applications.

The WM8325 is supplied in an 8x8mm 81-lead QFN package, ideal for use in portable systems. The WM8325 forms part of the Wolfson series of audio and power management solutions, and is widely register compatible with the WM831X family of PMIC devices.

FEATURES

Power Management

- 1 x DC-DC synchronous buck converter (0.6V - 1.8V, 2.5A, DVS)
- 1 x DC-DC synchronous buck converter (0.6V - 1.8V, 1.25A, DVS)
- 2 x DC-DC synchronous buck converters (0.85V - 3.4V, 1A)
- 1 x LDO regulator (0.9V - 3.3V, 300mA, 1Ω)
- 2 x LDO regulators (0.9V - 3.3V, 200mA, 1Ω)
- 3 x LDO regulators (0.9V - 3.3V, 100mA, 2Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 200mA, 1Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 150mA, 2Ω)
- 1 x 'Alive' regulator (0.8V – 1.55V, up to 25mA)

System Control

- I^2C or SPI compatible primary control interface
- Comprehensive interrupt scheme
- Watchdog timer and system reset control
- Autonomous power sequencing and fault detection
- OTP memory bootstrap configuration function

Additional Features

- Auxiliary ADC for multi-function analogue measurement
- 128-bit pseudo-random unique ID
- Secure Real-Time Clock with wake-up alarm
- 12 x configurable multi-function (GPIO) pins
- Comprehensive clocking scheme: low-power 32kHz RTC crystal oscillator, GPIO clock output and 4MHz RC clock for power management
- System LED outputs indicating device power state, and fault status

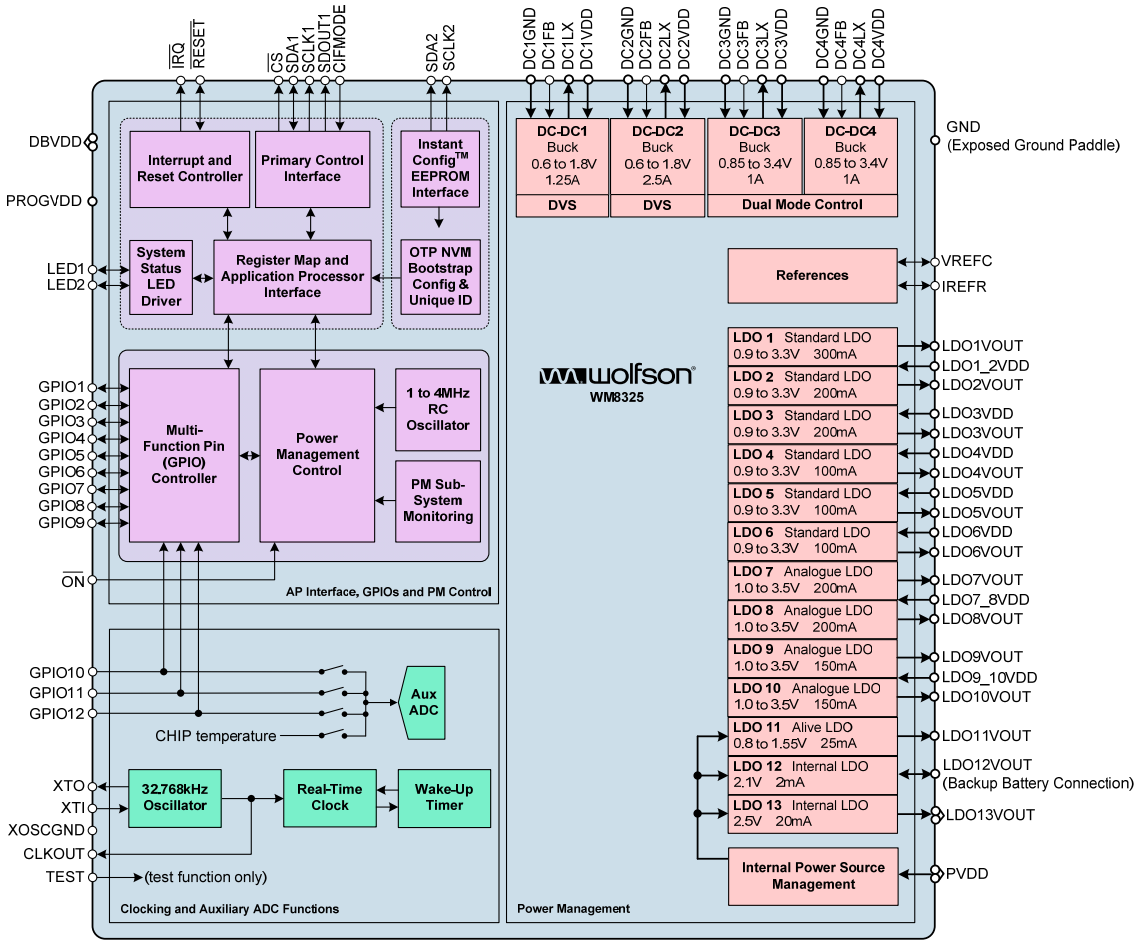
Package Options

- 8 x 8 x 0.85mm, 81-lead QFN package

APPLICATIONS

- Cellular Handsets
- Smartphones
- Electronic Books
- Portable Media Players
- Mobile Internet Devices
- Electronic Gaming Devices
- Netbooks
- Smartbooks
- Set Top Box
- Digital Picture Frames

BLOCK DIAGRAM



TYPICAL APPLICATIONS

The WM8325 is designed as a system PMIC device that generates configurable DC supplies to power processors and associated peripherals within a system. The WM8325 provides four DC-DC synchronous buck (step-down) converters. Two of these can operate in dual mode, providing an increased current capability. Eleven LDO regulators provide a high degree of flexibility to provide power to multiple devices, with the capability to power-up and power-down different circuits independently.

Two of the DC-DC step-down converters incorporate Wolfson's BuckWise™ technology specifically designed to handle rapid changes in load current; programmable slew rate DVS is also provided, as required by modern application processors. Selectable operating modes on all of the DC-DC converters allow each converter to be optimally configured for light, heavy or transient load conditions. Flexible operating configurations allow the converters to be tailored for minimum PCB area, maximum performance, or for maximum efficiency. The analogue LDOs provide low-noise outputs suitable for powering sensitive circuits such as RF / Wi-Fi / cellular handset applications.

The WM8325 powers up the converters and LDOs according to a programmable sequence. A configurable 'SLEEP' state is also available, providing support for an alternate configuration, typically for low-power / standby operation. The power control sequences and many other parameters can be stored in an integrated user-configurable OTP (One-Time Programmable) memory or may be loaded from an external memory. The WM8325 supports the programming and verification of the integrated OTP memory.

A backup battery supply can be connected to the WM8325 in order to maintain the Real Time Clock (RTC) in the absence of the primary supply.

Programmable GPIO pins may be configured as hardware inputs for general use or for selecting different power management configurations. As outputs, the GPIOs can provide indications of the device status, or may be used as control signals for other power management circuits. The WM8325 also provides two LED drivers, which can be controlled manually or configured as status indicators for the OTP memory programmer or operating power state.

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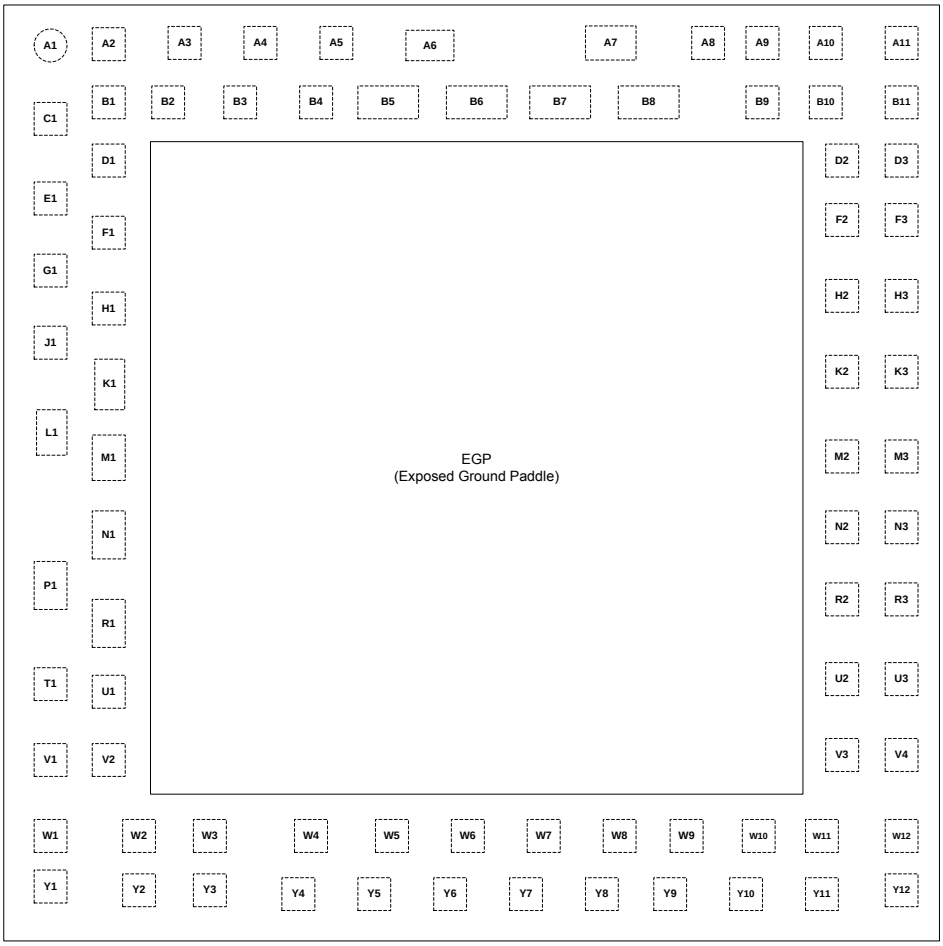
PIN CONFIGURATION



Top View – WM8325

ORDERING INFORMATION

ORDER CODE	OTP	TEMPERATURE RANGE (T_A)	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8325GEFL/V	Unprogrammed	-40°C to +85°C	81-lead QFN (8 x 8mm) (Pb-free)	MSL3	260°C
WM8325GEFL/RV	Unprogrammed	-40°C to +85°C	81-lead QFN (8 x 8mm) (Pb-free, tape and reel)	MSL3	260°C
WM8325GEFLxxx/RV*	Custom	-40°C to +85°C	81-lead QFN (8 x 8mm) (Pb-free, tape and reel) **	MSL3	260°C

Note:

Reel quantity = 2200

* xxx = Unique OTP part number

** Custom OTP minimum order quantity 22,000.

PIN DESCRIPTION

Notes:

1. Pins are sorted by functional groups.
2. The power domain associated with each pin is noted; VPMIC is the domain powered by LDO12 for the 'always-on' functions internal to the WM8325.

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION	
Clocking and Real Time Clock					
Y12	XTO	Analogue Output	VPMIC	Crystal Drive Output	
Y11	XTI	Analogue Input		Crystal Drive Input or 32.768kHz CMOS Clock Input	
W11	XOSCGND	Supply		Crystal Oscillator Ground	
H1	CLKOUT	Digital Output	DBVDD	CMOS Clock Output	
General Purpose Input / Output and Auxiliary ADC					
D3	GPIO1	Digital I/O	DBVDD or VPMIC	GPIO Pin 1	
F2	GPIO2	Digital I/O		GPIO Pin 2	
F3	GPIO3	Digital I/O		GPIO Pin 3	
W4	GPIO4	Digital I/O	DBVDD or PVDD	GPIO Pin 4	
Y4	GPIO5	Digital I/O		GPIO Pin 5	
W5	GPIO6	Digital I/O		GPIO Pin 6	
H2	GPIO7	Digital I/O	DBVDD or VPMIC	GPIO Pin 7	
H3	GPIO8	Digital I/O		GPIO Pin 8	
K3	GPIO9	Digital I/O		GPIO Pin 9	
Y5	GPIO10	Digital I/O	DBVDD or PVDD	GPIO Pin 10 / Auxiliary ADC input	
Y6	GPIO11	Digital I/O		GPIO Pin 11 / Auxiliary ADC input	
W6	GPIO12	Digital I/O		GPIO Pin 12 / Auxiliary ADC input	
Processor Interface and IC Control					
W9	$\overline{ON}$	Digital Input	VPMIC	ON Request Pin (Internal pull-up)	
B10	$\overline{RESET}$	Digital I/O	DBVDD	System Reset Input and Open Drain Output. (Internal pull-up)	
A11	$\overline{IRQ}$	Digital Output	DBVDD	PMIC Interrupt Flag Output. Configurable Open Drain / CMOS mode. (Internal pull-up in Open Drain mode.)	
E1	CIFMODE	Digital Input	DBVDD	Primary Control Interface Mode Select: 0 = I^2C Compatible Control Interface Mode 1 = SPI Compatible Control Interface Mode	
				SPI Compatible Control Interface Mode	*I^2C Compatible Control Interface Mode*
D2	SDOUT1	Digital Output	DBVDD	Control Interface Serial Data Out	No Function
B9	SCLK1	Digital Input		Control Interface Serial Clock	Control Interface Serial Clock
A9	SDA1	Digital I/O		Control Interface Serial Data In	Control Interface Serial Data Input and Open Drain Output. (Output can extend above DBVDD domain.)
A10	$\overline{CS}$	Digital Input		Control Interface Chip Select	I^2C Address Select: 0 = 68h 1 = 6Ch

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
Y10	SCLK2	Digital I/O	VPMIC	Control Interface Serial Clock for external InstantConfig™ EEPROM (ICE) (Internal pull-down)
W10	SDA2	Digital I/O		Control Interface Serial Data to/from external InstantConfig™ EEPROM (ICE) (Internal pull-down)
B11	DBVDD1	Supply		Digital Buffer Supply
F1	DBVDD2	Supply		Digital Buffer Supply
OTP Memory				
Y3	PROGVDD	Supply		High-voltage input for OTP programming.
DC-DC Converters and LDO Regulators				
B7	DC1GND	Supply		DC-DC1 Power Ground
A8	DC1FB	Analogue Input	DC1VDD	DC-DC1 Feedback Pin
A7	DC1LX	Analogue I/O		DC-DC1 Inductor Connection
B8	DC1VDD	Supply		DC-DC1 Power Input (connect to PVDD system supply)
B6	DC2GND	Supply		DC-DC2 Power Ground
A5	DC2FB	Analogue Input	DC2VDD	DC-DC2 Feedback Pin
A6	DC2LX	Analogue I/O		DC-DC2 Inductor Connection
B5	DC2VDD	Supply		DC-DC2 Power Input (connect to PVDD system supply)
M1	DC3GND	Supply		DC-DC3 Power Ground
J1	DC3FB	Analogue Input	DC3VDD	DC-DC3 Feedback Pin
L1	DC3LX	Analogue I/O		DC-DC3 Inductor Connection
K1	DC3VDD	Supply		DC-DC3 Power Input (connect to PVDD system supply)
N1	DC4GND	Supply		DC-DC4 Power Ground
T1	DC4FB	Analogue Input	DC4VDD	DC-DC4 Feedback Pin
P1	DC4LX	Analogue I/O		DC-DC4 Inductor Connection
R1	DC4VDD	Supply		DC-DC4 Power Input (connect to PVDD system supply)
A3	LDO1_2VDD	Supply		LDO1 & LDO2 Power Input
B2	LDO1VOUT	Analogue Output	LDO1VDD	LDO1 Power Output
B3	LDO2VOUT	Analogue Output	LDO2VDD	LDO2 Power Output
B4	LDO3VDD	Supply		LDO3 Power Input
A4	LDO3VOUT	Analogue Output	LDO3VDD	LDO3 Power Output
W3	LDO4VDD	Supply		LDO4 Power Input
Y2	LDO4VOUT	Analogue Output	LDO4VDD	LDO4 Power Output
Y1	LDO5VDD	Supply		LDO5 Power Input
W2	LDO5VOUT	Analogue Output	LDO5VDD	LDO5 Power Output
W1	LDO6VDD	Supply		LDO6 Power Input
V1	LDO6VOUT	Analogue Output	LDO6VDD	LDO6 Power Output
R3	LDO7_8VDD	Supply		LDO7 & LDO8 Power Input
N2	LDO7VOUT	Analogue Output	LDO7VDD	LDO7 Power Output
R2	LDO8VOUT	Analogue Output	LDO8VDD	LDO8 Power Output
M2	LDO9_10VDD	Supply		LDO9 Power Input
M3	LDO9VOUT	Analogue Output	LDO9VDD	LDO9 Power Output
N3	LDO10VOUT	Analogue Output	LDO10VDD	LDO10 Power Output
V3	LDO11VOUT	Analogue Output	PVDD	LDO11 (Alive) Power Output
Y8	LDO12VOUT	Analogue I/O	PVDD	LDO12 (Internal VPMIC) Output; Backup battery supply input / output
W7	LDO13VOUT1	Analogue I/O	PVDD	LDO13 (Internal INTVDD) Output; not for general use
K2	LDO13VOUT2	Analogue I/O	PVDD	LDO13 - Connect to LDO13VOUT1 (W7)

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
Voltage and Current References				
W8	VREFC	Analogue I/O	VPMIC	Voltage Reference capacitor connection point
Y9	IREFR	Analogue I/O		Current Reference resistor connection point
System LED Drivers				
U3	LED1	Digital Output	PVDD	Status LED Driver 1. Open Drain Output
U2	LED2	Digital Output		Status LED Driver 2. Open Drain Output
System Power				
U1	PVDD1	Supply		System VDD Supply
Y7	PVDD2	Supply		System VDD Supply
V4	PVDD3	Supply		System VDD Supply
EGP	Exposed Ground Paddle	Analogue Ground		Ground
Miscellaneous				
A1, A2, B1, C1, D1, V2	DNC			Do Not Connect
G1, W12	TEST			Test function (connect to GND)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The WM8325 has been classified as MSL3.

CONDITION	MIN	MAX
OTP Programming Supply (PROGVDD)	-0.3V	7.0V
System supply (PVDD1, PVDD2, PVDD3)	-0.3V	7.0V
Input voltage for LDO regulators	-0.3V	7.0V
Input voltage for DC-DC converters	-0.3V	7.0V
Digital buffer supply (DBVDD1, DBVDD2)	-0.3V	4.5V
Voltage range for digital inputs	-0.3V	DBVDD + 0.3V
Operating Temperature Range, T_A	-40°C	+85°C
Junction Temperature, T_J	-40°C	+125°C
Thermal Impedance Junction to Ambient, θ_{JA}		24°C/W
Storage temperature prior to soldering	30°C max / 60% RH max	
Storage temperature after soldering	-65°C	+150°C
Soldering temperature (10 seconds)		+260°C
Note: These ratings assume that all ground pins are at 0V.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
System power source	PVDD1, PVDD2, PVDD3	2.7		5.5	V
Digital buffer supply	DBVDD1, DBVDD2	1.71		3.6	V
OTP Programming Supply (see note)	PROGVDD	6.25	6.5	6.75	V
	LDO12VOUT		3.3		V
Ground	Exposed Ground Paddle (EGP), DC1GND, DC2GND, DC3GND, DC4GND, XOSCGND		0		V

Note:

The OTP Programming Supply PROGVDD should only be present when programming the OTP. At other times, this pin should be left unconnected. The LDO12VOUT must be overdriven by an external supply when programming the OTP. At other times, the voltage at this pin is driven by the internal circuits of the WM8325.

FEATURES OVERVIEW

POWER MANAGEMENT FUNCTIONS

DESCRIPTION	INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT CURRENT	EXTERNAL COMPONENTS	FEATURES
DC-DC1, DC-DC2 (BuckWise™ Step-down converters)	PVDD	0.6V to 1.8V (12.5mV steps)	Up to 1.25A (DC-DC1) Up to 2.5A (DC-DC2)	4.7µF - 47µF C_{OUT}, 0.5µH - 2.2µH L_{OUT}	Best-in-class transient performance. Dynamic Voltage Scaling (DVS). Up to 93% efficiency. Selectable 2/4MHz switching frequency. FCCM, Auto and Hysteretic switching modes. Low I_Q LDO mode.
DC-DC3, DC-DC4 (Step-down converters)	PVDD	0.85V to 3.4V (25mV steps)	Up to 1.0A	10µF to 47µF C_{OUT}, 2.2µH L_{OUT}	Up to 95% efficiency. 2MHz switching frequency. FCCM, Auto, Hysteretic switching modes. Low I_Q LDO mode.
LDO1	1.5V to PVDD	0.9V to 3.3V (50/100mV steps)	Up to 300mA	2.2µF C_{OUT}	5µA low I_Q mode. Current limited switch mode.
LDO2, LDO3	1.5V to PVDD	0.9V to 3.3V (50/100mV steps)	Up to 200mA	2.2µF C_{OUT}	5µA low I_Q mode. Current limited switch mode.
LDO4, LDO5, LDO6	1.5V to PVDD	0.9V to 3.3V (50/100mV steps)	Up to 100mA	2.2µF C_{OUT}	5µA low I_Q mode. Current limited switch mode.
LDO7, LDO8 (Analogue, low noise regulators)	1.71V to PVDD	1V to 3.5V (50/100mV steps)	Up to 200mA	1µF C_{OUT}	0.003%/mA load regulation. 0.025%/V line regulation. 30µV output noise from 10Hz to 100kHz. 85dB PSRR.
LDO9, LDO10 (Analogue, low noise regulators)	1.71V to PVDD	1V to 3.5V (50/100mV steps)	Up to 150mA	1µF C_{OUT}	0.004%/mA load regulation. 0.025%/V line regulation. 30µV output noise from 10Hz to 100kHz. 85dB PSRR.
LDO11	PVDD: 1.8V to 3.1V	0.8 to 1.55 (50/100mV steps)	Up to 10mA		Stable with or without output capacitor. 2µA quiescent current. Can be enabled in OFF power state. Option to track DC-DC1 output voltage.
	PVDD: 3.1V to 5.5V		Up to 25mA		
EPE1, EPE2 (Sequenced control outputs)	n/a	n/a	n/a	n/a	Digital outputs for external regulators etc. Controlled as part of the programmable power-up/power-down sequences.
LDO12 (VPMIC)	n/a	2.1V	Internal only	0.1µF C_{OUT}	Internal Supply (always ON). Constant voltage output for charging backup power source.
LDO13 (INTVDD)	n/a	2.5V	Internal only	1µF C_{OUT}	Internal supply when ON Used for Touch Panel (TPVDD)

Table 1 Power Management Feature Summary

Note: PVDD range is 2.7V to 5.5V

The WM8325 provides 4 DC-DC Converters and 11 LDO Regulators. The DC-DC Converters include 2 BuckWise™ valley-mode converters. The Regulators comprise general purpose LDOs (LDO1 - LDO6) and low-noise analogue LDOs (LDO7 - LDO10). The analogue LDOs offer superior PSRR, noise and load-transient performance. LDO11 is a low power LDO intended for powering “always on” circuits connected to the WM8325; this LDO can be configured to remain enabled in the OFF state.

These power management components are designed to support application processors and associated peripherals. DC-DC1 and DC-DC2 are intended to provide power to the processor voltage domains; DC-DC3 is suitable for powering memory circuits or for use as a pre-regulator for the LDOs. The output voltage of each of the buck converters and regulators is programmable in software through control registers. DC-DC3 and DC-DC4 can be ganged together in dual mode, providing an increased current capability for higher power processor voltage domains.

The WM8325 can execute programmable sequences of enabling and disabling the DC-DC Converters and LDO Regulators as part of the transitions between the ON, OFF and SLEEP power states. The WM8325 power management circuits can also interface with configurable hardware control functions supported via GPIO pins. These include GPIO inputs for selecting alternate voltages or operating modes, and GPIO outputs for controlling external power management circuits.

The configuration of the power management circuits, together with some of the GPIO pins and other functions, may be stored in the integrated OTP memory. This avoids any dependence on a host processor to configure the WM8325 at start-up.

BUCKWISE™ TECHNOLOGY

The BuckWise™ converter is the first Valley mode DC-DC converter integrated into a system PMIC. This technology has several key benefits:

FEATURE	BENEFITS
Market leading transient performance	Able to use smaller capacitors to meet processor transient requirements. Processors are able to operate at lower voltages (saving power) without hitting minimum voltage specifications.
Valley Mode Control (VMC)	Ensures there is no performance degradation at low output voltages (0.6V). Will support next-generation processors (<45nm) with low voltage requirements.
>90% efficiency	Longer battery life in portable devices.
Multiple modes of operation	Maintains high efficiency across the full load range, increasing battery life.
Dynamic Voltage Scaling (DVS) control with a single register write or via hardwired GPIO pin.	Allows the regulator to slew from one output voltage to another with a programmable slew rate. Enables processor to switch seamlessly between power modes for optimum processor performance at the lowest possible power.

The BuckWise™ load transient performance is illustrated in Figure 1.

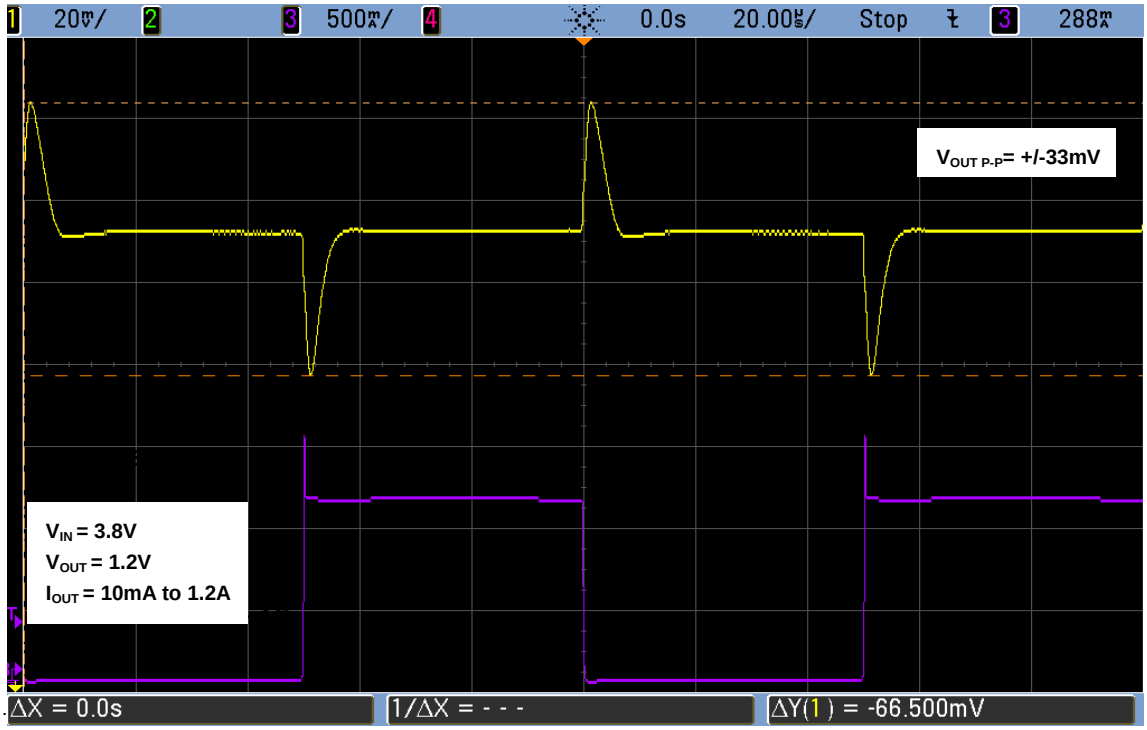


Figure 1 BuckWise™ Load Transient Response

Note: C_{out}=22µF, L_{out}=0.5µH, Load rise time =200ns

NON VOLATILE MEMORY SYSTEM CONFIGURATION

- Customisable standard product using the OTP integrated non-volatile memory (NVM) to store system startup sequence and regulator voltage defaults
- InstantConfig™ EEPROM (ICE) development mode to facilitate rapid system prototyping
- PCB production line or in-factory configuration flows for OTP are supported
- All main application processor start-up requirements are accommodated with 5 startup/shutdown timeslots and flexible GPIO and Interrupt model

The WM8325 is a highly configurable device which can be tailored specifically to the requirements of a complex system application. The sequencing and voltage control of the integrated DC-DC Converters and LDO Regulators in the ON, OFF, and SLEEP power state conditions can be programmed in 5 startup and shutdown timeslots. Together with a flexible GPIO and interrupt model, this allows the WM8325 to be a customized solution for each application. The WM8325 reads system configuration information from the internal OTP memory and also from an external EEPROM, if connected.

In the development phase, the WM8325 permits designers to modify or experiment with different settings of the control sequences by writing to the applicable registers in the OFF state prior to commanding an 'ON' state transition. Configuration settings can also be stored on an external EEPROM and loaded onto the WM8325 as required. In this case, the external EEPROM data takes precedence over any data programmed into the internal non volatile memory.

For production use, the WM8325 the on-chip non volatile memory is typically used, in which the essential parameters for starting up the device can be programmed. This allows the WM8325 to start up and shut down the system with no dependency on any other devices for application-specific configuration parameters. The WM8325 can be supplied unprogrammed or with the customer's system configuration data pre-programmed. Note that there is an alternate flow whereby the device can program itself with data from an external EEPROM when on the PCB.

POWER STATES

The WM8325 has 6 main power states, which are described below. Different levels of functionality are associated with each of the power states. Some of the state transitions are made autonomously by the WM8325 (eg. transitions to/from BACKUP are scheduled according to the available power supply conditions). Other transitions are initiated as a result of instructions issued over the Control Interface or as a result of software functions (eg. Watchdog timer) or hardware functions such as the $\overline{ON}$ pin. The valid transitions and the associated conditions are detailed below.

NO POWER - This is the device state when no power is available. All functions are disabled and all register data is lost.

OFF - This is the device state when power is available but the device is switched off. The RTC is enabled and the register map contents are maintained. The $\overline{RESET}$ pin is pulled low in this state. LDO11 may optionally be enabled in this state; all other DC-DCs and LDOs are disabled (except LDO12 and LDO13, which support internal functions).

ON - This is the normal operating state when the device is switched on. All device functions are available in this state.

SLEEP - This is a user-configurable operating state which is intended for a low-power operating condition. Selected functions may be enabled, disabled or re-configured according to the user's requirements. A programmable configuration sequence for the DC-DCs and LDOs is executed on transition to/from SLEEP mode.

BACKUP - This is the operating state when the PVDD power supply is below the reset threshold of the device. Typically, this means that the PVDD supply has been removed. All DC-DC converters and LDO regulators are disabled in this state. The RTC and oscillator and a 'software scratch' memory area can be maintained from the backup supply (if available) in this state. All other functions and registers are reset in BACKUP. (Note that, for power saving, an 'unclocked' mode, in which the RTC is held constant, may be selected if required.)

PROGRAM - This is a special operating state which is used for programming the integrated OTP memory with the device configuration data. The settings stored in the OTP define the device configuration in the ON state, and also the time/sequencing data associated with ON/OFF power state transitions.

The valid power state transitions are illustrated in Figure 2.

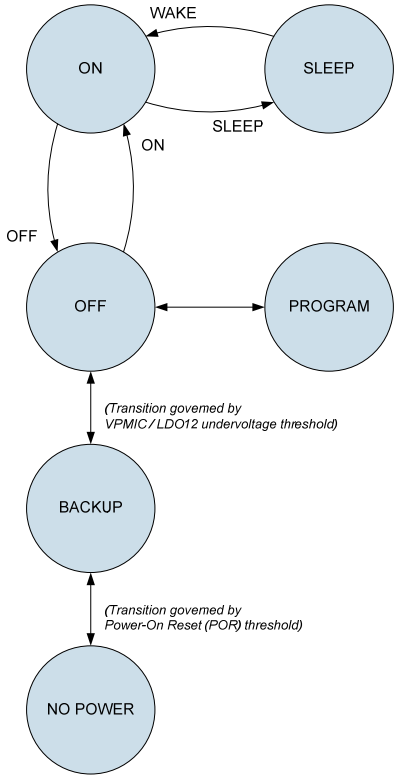


Figure 2 Power States and Transitions

State transitions to/from the NO POWER state are controlled automatically by the internal supply (VPMIC) voltage generated by LDO12. The device is in the NO POWER state when this voltage is below the Power-On Reset (POR) threshold.

State transitions to/from the BACKUP state are controlled automatically by the internal supply (VPMIC) voltage generated by LDO12. The device is in the BACKUP state when this voltage is below the Device Reset threshold.

State transitions to/from the PROGRAM state are required to follow specific control sequences.

The remaining transitions between the OFF, ON and SLEEP states may be initiated by a number of different mechanisms - some of them automatic, some of them user-controlled. Transitions between these states are time-controlled sequences of events are programmable, using data stored in the integrated OTP memory or else data loaded from an external InstantConfig™ EEPROM (ICE) memory.

BACKUP DOMAIN FOR RTC AND SYSTEM CONFIGURATION RETENTION

- Clocked Backup state quiescent current of 2µA with Real Time Clock (RTC) running
- Unclocked Backup state quiescent current of 100nA with RTC paused
- Backup state supported using coin cell, super/gold capacitor, or standard capacitor, connected to the LDO12VOUT pin (via 22kΩ series resistor)
- Constant voltage charging of backup power source
- Up to 5 minutes of data retention with a 22µF capacitor in unclocked backup state
- Automatic transition to backup power source
- 32kHz Crystal oscillator
- RTC with alarm function
- Secure-RTC tamper detection mechanism for unauthorised updates to the RTC

AUXILIARY ADC

- 12-bit Auxiliary ADC (AUXADC) for system supervision and resistive touch panel
- Monitors up to 3 external sources, plus key internal parameters and voltages
- 4 digital comparators with selectable input source

The WM8325 incorporates a 12-bit Auxiliary ADC (AUXADC). This can be used to perform a number of system measurements (PVDD supply voltage or chip temperature) and can also be used to measure analogue voltages from external sources and sensors.

External inputs to the AUXADC should be connected to the pins GPIO10, GPIO11, GPIO12. The maximum voltage that can be measured is determined by the power domain associated with each (DBVDD or PVDD).

SYSTEM CONTROL AND SUPERVISION

- I^2C or SPI compatible primary control interface
- Output fault monitoring on all regulator outputs (overcurrent or undervoltage) with programmable fault action
- Programmable system undervoltage (UV) level
- Chip thermal monitor and programmable warning level interrupt
- Watchdog timer function
- Two-tier interrupts with full masking
- Configurable GPIO power domain
- GPIO control for regulator functions for lower latency/flexibility

GPIOS

The WM8325 has 12 general-purpose input/output (GPIO) pins, GPIO1 - GPIO12. These can be configured as inputs or outputs, active high or active low, with optional on-chip pull-up or pull-down resistors. GPIO outputs can either be CMOS driven or Open Drain configuration. Each GPIO pin can be tri-stated and can also be used to trigger Interrupts. The function of each GPIO pin is selected individually. Different voltage power domains are selectable on a pin by pin basis for GPIOs 1-12, see Table 2.

GPIO	DEFAULT POWER DOMAIN	ALTERNATE POWER DOMAIN
GPIO1, GPIO2, GPIO3	DBVDD	VPMIC (LDO12VOUT)
GPIO4, GPIO5, GPIO6	DBVDD	PVDD
GPIO7, GPIO8, GPIO9	DBVDD	VPMIC (LDO12VOUT)
GPIO10, GPIO11, GPIO12	DBVDD	PVDD

Table 2 GPIO Power Domains

In addition to the default inputs and outputs, GPIOs have a wide range of secondary input and output functions. Input functions include power state change requests, DVS requests and hardware control of regulator modes. Outputs include functions such as power state notifications, 32kHz clock, DVS complete and system power or converter power good flags.

INTERRUPTS

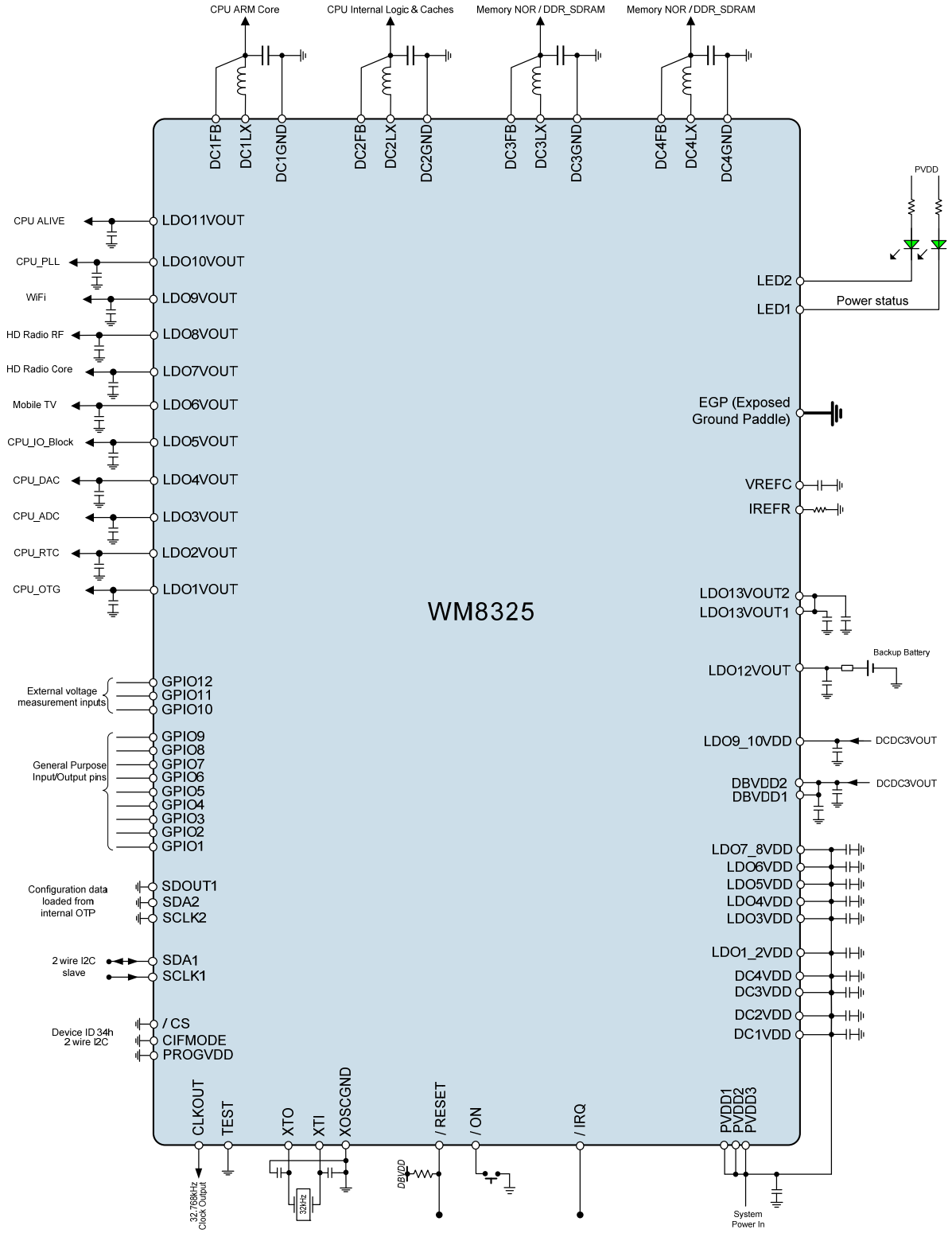
The WM8325 has a comprehensive Interrupt logic capability. The dedicated $\overline{IRQ}$ pin can be used to alert a host processor to selected events or fault conditions. Each of the interrupt conditions can be individually enabled or masked. Following an interrupt event, the host processor should read the interrupt registers in order to determine what caused the interrupt, and take appropriate action if required.

The WM8325 interrupt controller has two levels:

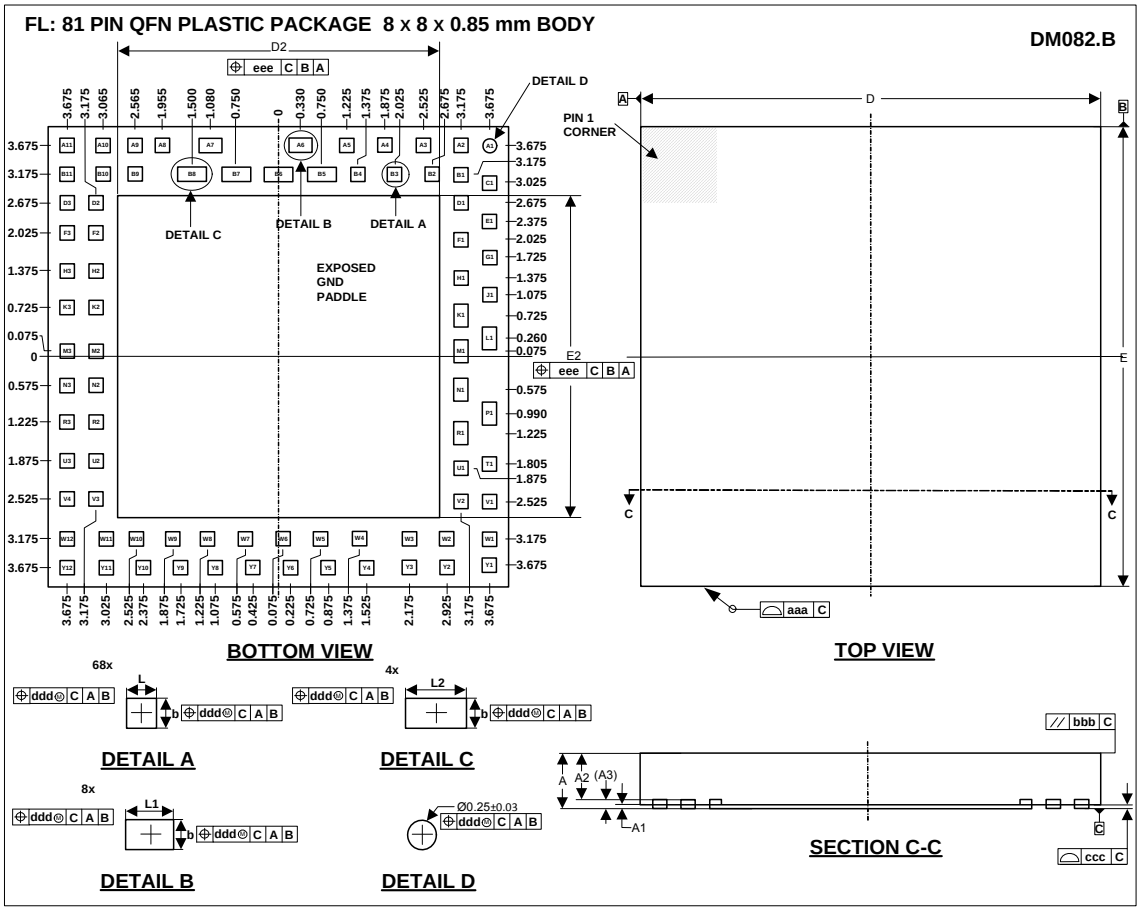
Secondary interrupts indicate a single event in one of the circuit blocks. The event is indicated by setting a register bit. This bit is a latching bit - once it is set, it remains at logic 1 even if the trigger condition is cleared. The secondary interrupts are cleared by writing a logic 1 to the relevant register bit. Note that reading the register does not clear the secondary interrupt.

Primary interrupts are the logical OR of the associated secondary interrupts (usually all the interrupts associated with one particular circuit block). Each of the secondary interrupts can be individually masked or enabled as an input to the corresponding primary interrupt.

TYPICAL CONNECTIONS



PACKAGE DIAGRAM



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	---	---	0.85	
A1	0.02	0.05	0.08	
A2	0.64	0.675	0.71	
A3	0.12	0.13	0.14	
b	0.22	0.25	0.28	
D		8 BSC		
D2	5.55	5.60	5.65	
E		8 BSC		
E2	5.55	5.60	5.65	
L	0.22	0.25	0.28	
L1	0.37	0.4	0.43	
L2	0.47	0.5	0.53	
Tolerances of Form and Position				
aaa	0.10			
bbb	0.20			
ccc	0.05			
ddd	0.08			
eee	0.10			
REF	JEDEC, MO-220			

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES
2. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-002.
3. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
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REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	CHANGED BY
05/10/10	1.4	Updated DC-DC efficiency in Power Management summary CLKIN renamed as TEST	PH
15/09/11	4.0	Backup battery power details updated. LDO11 maximum output current increased (only for PVDD ≥ 3.1V).	PH