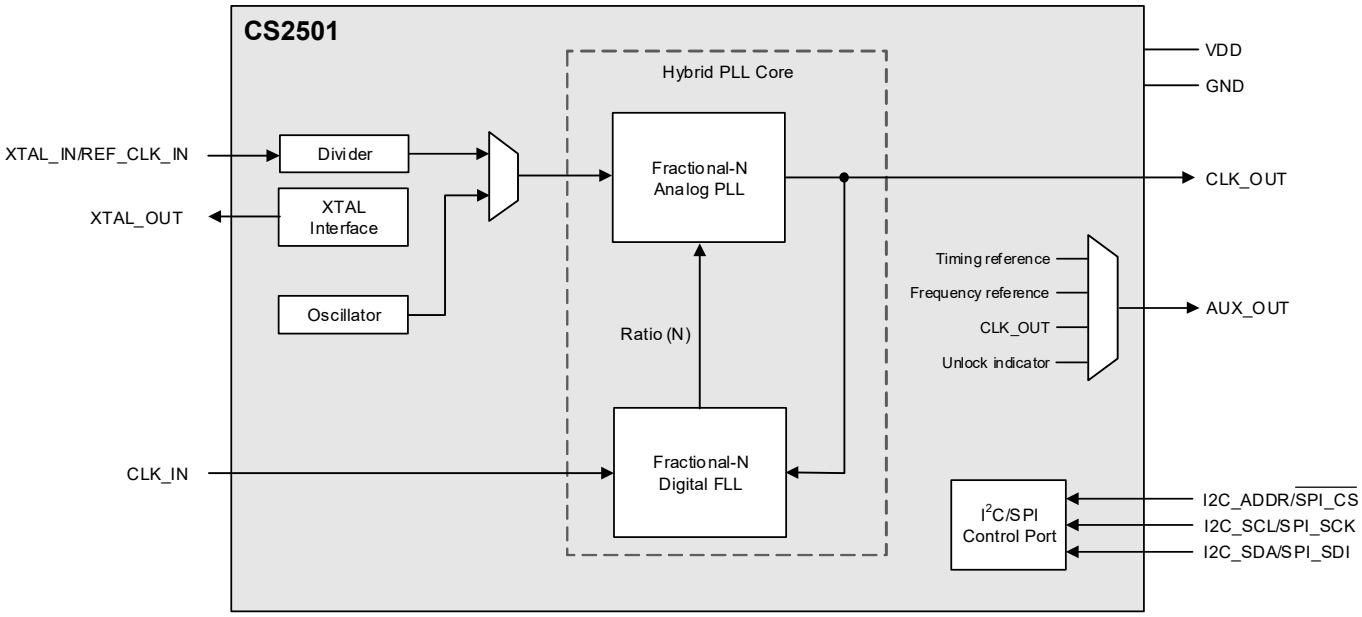
Fractional-N Clock Multiplier

Features

- Fractional clock multiplier and jitter reduction using hybrid analog/digital PLL
  - Generates low-jitter 6–75 MHz clock (CLK_OUT), synchronized to a 50 Hz–30 MHz low-quality or intermittent frequency reference (CLK_IN)
- Flexible timing reference source
  - External clock, external crystal, or built-in oscillator
- High resolution PLL ratio (1 PPM)
- 18 ps_{RMS} period jitter (external timing reference), 18 ps_{RMS} period jitter (oscillator reference)
- Glitchless clock output generated from intermittent input
- I²C/SPI control port
- Configurable auxiliary clock/status output
- Minimal board space required
  - No external analog loop-filter components
- Pin-to-pin, register map, and control compatible with CS2100 and CS2300
- Single-supply operation at 1.8 V or 3.3 V

Applications

- Automotive audio systems
- Digital audio systems
- Network and USB audio interfaces
- IoT sensor and transducer systems
- Embedded systems



General Description

The CS2501 is a system-clocking device incorporating a programmable phase-locked loop (PLL). The hybrid analog/digital PLL architecture comprises a delta-sigma fractional-N analog PLL and a digital frequency-locked loop (FLL). The CS2501 enables clock generation from a stable timing reference clock. The device can generate low-jitter clocks from a noisy clock reference at frequencies as low as 50 Hz. An internal oscillator can provide the timing reference clock, enabling a reduction in external component requirements. The CS2501 can be configured using a control interface supporting I^2C and SPI modes of operation.

The CS2501 can be powered from a single 1.8 V or 3.3 V supply. The device combines high performance with low power consumption.

The CS2501 is available in commercial-grade 10-pin TSSOP package for operation from –40°C to +85°C. The device is also available in the AEC-Q100-qualified grade-2 package for operation from –40°C to +105°C. See Section 12 for ordering information.

Table of Contents

1 Pin Assignments and Descriptions

These sections show pin assignments and describe pin functions.

1.1 TSSOP Pin Assignments (Top View, Through Package)

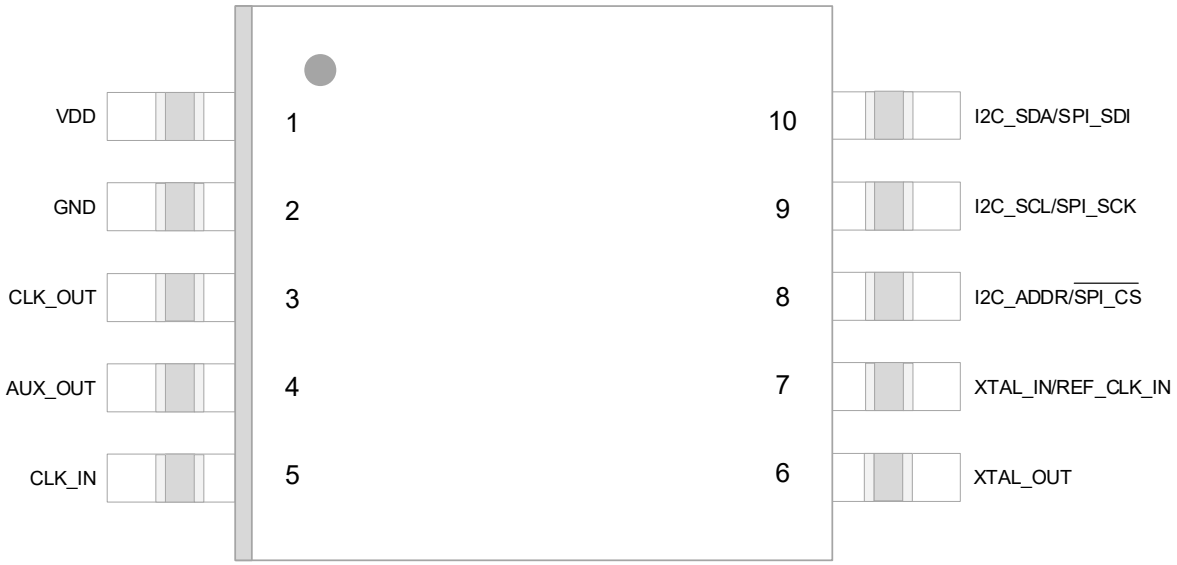


Figure 1-1. TSSOP 10-Pin Diagram (Top View, Through-Package)

Note the CS2501 is pin-to-pin compatible with CS2100 and CS2300.

1.2 Pin Descriptions

Table 1-1. Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description
VDD	1	—	—	**Power Supply.** 3.3 V/1.8 V supply for the digital and analog blocks.
GND	2	—	—	**Ground**.
CLK_OUT	3	VDD	O	**Clock Output.** PLL clock output.
AUX_OUT	4	VDD	O	**Auxiliary Output.** Configurable clock output or status output.
CLK_IN	5	VDD	I	**Clock Input.** Frequency reference input for the digital FLL.
XTAL_OUT	6	VDD	O	**Crystal Connection.** Output for an external crystal. Connect to GND for internal oscillator reference clock. (A capacitor connection is also supported for legacy PCB designs, as shown in Section 2.)
XTAL_IN/REF_CLK_IN	7	VDD	I	**Crystal Connection.** Input for an external crystal. **Reference Clock.** External low-jitter timing reference clock input. Connect to GND for internal oscillator reference clock.
I2C_ADDR/$\overline{\text{SPI\_CS}}$	8	VDD	I	**I²C Control-Port Address.** Chip address input for the I²C interface. **SPI Control-Port Chip Select.** Active-low chip select input for the SPI interface.
I2C_SCL/SPI_SCK	9	VDD	I	**I²C Control-Port Clock.** Clock input for the I²C interface. **SPI Control-Port Clock.** Clock input for the SPI interface.
I2C_SDA/SPI_SDI	10	VDD	I/O	**I²C Control-Port Data.** Data input/output for the I²C interface. **SPI Control-Port Serial Data In.** SPI data input.

1.3 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS2501 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

2 Typical Connections

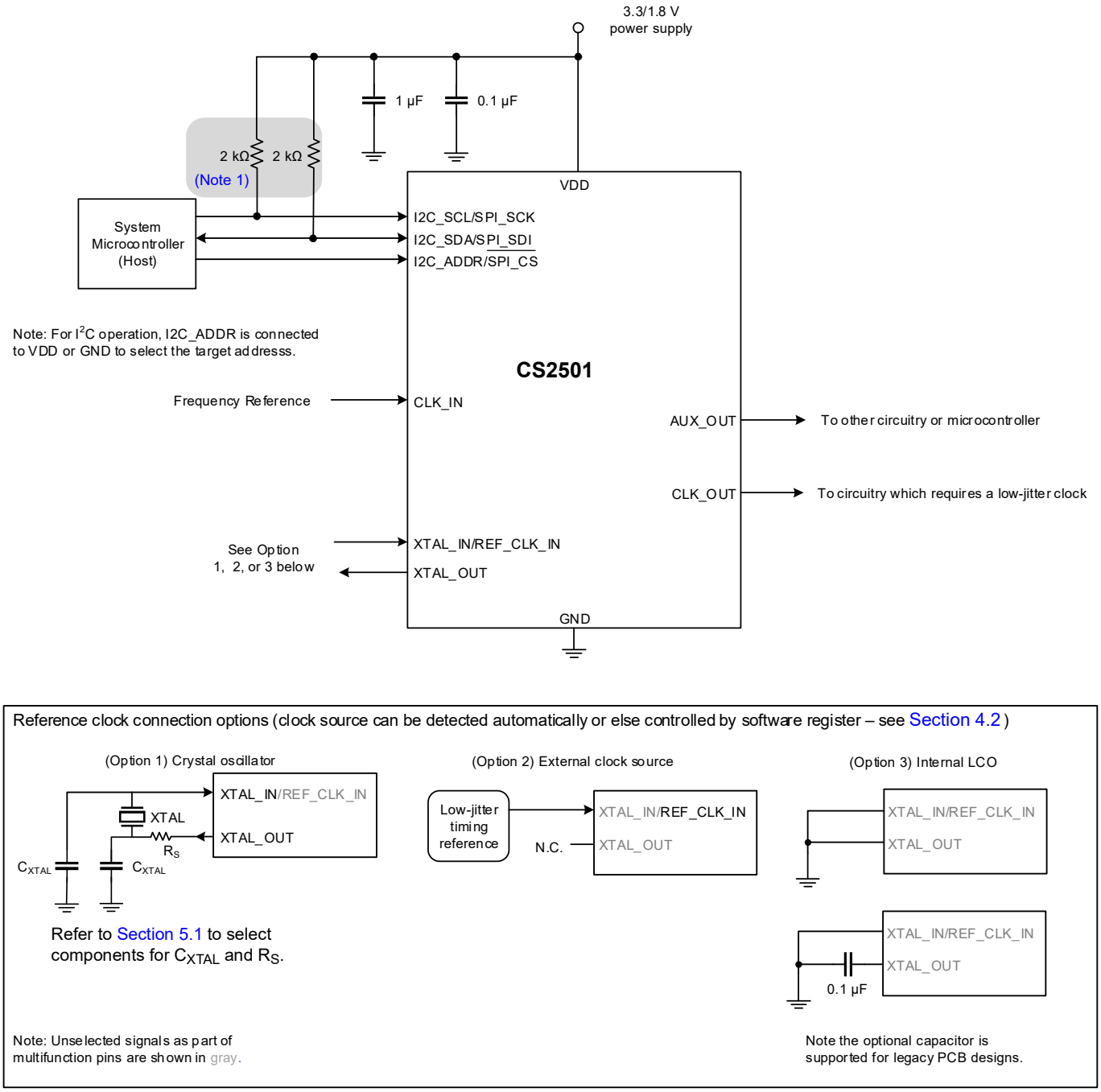


Figure 2-1. Typical Connection Diagram

Note referenced in the typical connection diagram:

1. The pull-up resistors are required only for I2C operation. The diagram shows 2 kΩ pull-up, but higher impedance can be supported depending on clock speed and bus capacitance.

3 Characteristics and Specifications

Table 3-1. Recommended Operating Conditions

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters		Symbol	Min	Typ	Max	Units
DC power supply	Nominal 3.3 V Nominal 1.8 V	VDD	3.1 1.71	3.3 1.8	3.5 1.89	V V
Supply ramp up/down		t_{PWR_UD}	0.01	—	10	ms
Ambient temperature	Commercial Grade AEC-Q100 Grade 2	T_A	–40 –40	— —	85 105	°C °C

Table 3-2. Absolute Maximum Ratings

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters	Symbol	Min	Max	Units
DC power supply	VDD	–0.3	4.32	V
External voltage applied to digital input/output	V_{INDI}	–0.3	VDD + 0.3	V
Input current	I_{in}	—	±10	mA
Ambient temperature	T_A	–55	125	°C
Storage temperature	T_{STG}	–65	150	°C

Table 3-3. DC Electrical Characteristics

Test Conditions (unless specified otherwise): T_A = 25°C; timing reference = 12 MHz (external clock or crystal).

Parameters		Symbol	Min	Typ	Max	Units
Power supply current—unloaded [1]		I_{VDD}	—	4	—	mA
Input leakage current (per pin)		I_{IN}	—	—	±10	µA
Input capacitance (per pin)		I_C	—	—	5	pF
High-level input voltage		V_{IH}	0.70 × VDD	—	—	V
Low-level input voltage		V_{IL}	—	—	0.30 × VDD	V
High-level output voltage		V_{OH}	0.90 × VDD	—	—	V
Low-level output voltage		V_{OL}	—	—	0.10 × VDD	V
VDD power-on reset (POR) threshold	VDD rising VDD falling	V_{POR}	1.40 1.38	— —	1.59 1.55	V V
VDD power-on reset duration [2]		t_{POR}	100	—	—	ms

1. To calculate the additional current consumption due to loading (per output pin), multiply clock output frequency by load capacitance (C_L) and power supply voltage (VDD).
2. To trigger a power-on reset, VDD must be held below the reset threshold for longer than this duration. Note that VDD interruption shorter than this duration may result in incorrect device behavior.

Table 3-4. AC Electrical Characteristics

Test Conditions (unless specified otherwise): T_A = –40°C to 85°C (commercial grade); T_A = –40°C to 105°C (AEC-Q100 grade-2); Load capacitance (C_L) = 15 pF.

Parameters		Symbol	Min	Typ	Max	Units
Crystal frequency	REF_CLK_IN_DIV = 10 REF_CLK_IN_DIV = 01 REF_CLK_IN_DIV = 00	f_{XTAL}	8 16 32	— — —	18.75 37.50 50	MHz MHz MHz
Crystal interface transconductance (T_A = 25°C)	VDD = 3.3 V, XOSC_GEARn_3V3_DRV = 0 VDD = 3.3 V, XOSC_GEARn_3V3_DRV = 1 VDD = 1.8 V	—	— — —	13 26 43	— — —	mS mS mS
Reference clock input frequency	REF_CLK_IN_DIV = 10 REF_CLK_IN_DIV = 01 REF_CLK_IN_DIV = 00	$f_{REF\_CLK\_IN}$	8 16 32	— — —	18.75 37.50 75	MHz MHz MHz
Reference clock input duty cycle		$D_{REF\_CLK\_IN}$	45	—	55	%
Clock input frequency		f_{CLK_IN}	50	—	30 ×10^6	Hz
Clock input pulse width	$f_{CLK\_IN} < f_{SYSCLK} / 96$ [1] $f_{CLK\_IN} > f_{SYSCLK} / 96$ [1]	pw_{CLK_IN}	2 10	— —	— —	UI [2] ns
Clock skipping timeout		t_{CS}	20	—	—	ms
Clock skipping input frequency		f_{CLK_SKIP}	50	—	80 ×10^3	Hz
CLK_OUT frequency range		f_{CLK_OUT}	6	—	75	MHz
Clock output duty cycle	measured at VDD / 2	t_{OD}	45	50	55	%
Clock output rise time	10% to 90% of VDD	t_{OR}	—	1.8	—	ns
Clock output fall time	90% to 10% of VDD	t_{OF}	—	1.8	—	ns
CLK_OUT period jitter [3,4]	external timing reference internal oscillator reference	t_{JIT}	— —	18 18	25 25	ps_{RMS} ps_{RMS}
CLK_OUT baseband TIE jitter [3,5]	external timing reference internal oscillator reference	—	— —	21 170	70 350	ps_{RMS} ps_{RMS}
CLK_OUT wideband TIE jitter [3,6]	external timing reference internal oscillator reference	—	— —	90 200	160 380	ps_{RMS} ps_{RMS}
PLL lock time	f_{CLK_IN} < 200 kHz f_{CLK_IN} ≥ 200 kHz	t_{LC}	— —	100 1	200 3	UI [7] ms
CLK_OUT frequency resolution [3,8]	high resolution high multiplication	—	— —	1 244	— —	ppm ppm
Oscillator frequency	at 25°C	—	11.76	12.0	12.24	MHz
Oscillator frequency thermal sensitivity	at 25°C	—	—	90	—	ppm/°C
Oscillator frequency stability (relative to 25°C)	–40 to 85°C –40 to 105°C	—	–1.0 –1.3	— —	0.8 0.8	% %
Clock output frequency deviation	CLK_IN stopped, holdover enabled	—	—	—	0.1	%

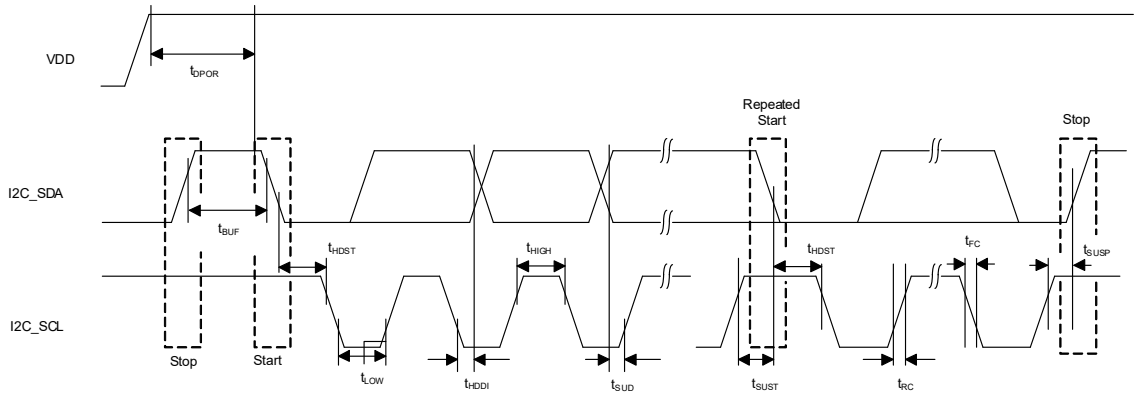
1. The internal timing reference clock (SYSCLK) is derived from REF_CLK_IN (see Section 4.2).
2. UI (unit interval) corresponds to t_{SYSCLK} or 1 / f_{SYSCLK}.
3. REF_CLK_IN is a 12 MHz timing reference clock, with phase noise 20 dB lower than the output clock noise. The clock output frequency (f_{CLK_OUT}) is 24.576 MHz.
4. Sample size is 10000.
5. Using 3rd order 100 Hz–40 kHz bandpass filter as defined in AES-12id-2020 Section 3.4.2.
6. Using 3rd order 100 Hz high pass filter as defined in AES-12id-2020 Section 3.4.1.
7. UI (unit interval) corresponds to t_{CLK_IN} or 1 / f_{CLK_IN}.
8. The frequency accuracy of the PLL clock output is directly proportional to the accuracy of the clock input.

Table 3-5. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds; T_A = 25°C.

Parameters [1,2]		Symbol	Min	Max	Units
SCL clock frequency		f_{SCL}	—	400	kHz
Clock low time		t_{LOW}	1.3	—	µs
Clock high time		t_{HIGH}	0.6	—	µs
Start condition hold time (before first pulse clock)		t_{HDST}	0.6	—	µs
Setup time for repeated start		t_{SUST}	0.6	—	µs
Rise time of SCL and SDA	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz	t_{RC}	— —	1000 300	ns ns
Fall time SCL and SDA	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz	t_{FC}	— —	300 300	ns ns
Setup time for stop condition		t_{SUSP}	0.6	—	µs
SDA setup time to SCL rising		t_{SUD}	100	—	ns
SDA input hold time from SCL falling		t_{HDDI}	0	—	ns
Bus free time between transmissions		t_{BUF}	1.3	—	µs
Start-up time from power-up/software reset to control port ready [3]		t_{DPOR}	—	200	µs

1. The I²C control port uses a 8-bit register address and 8-bit data words.
2. I²C control-port timing.



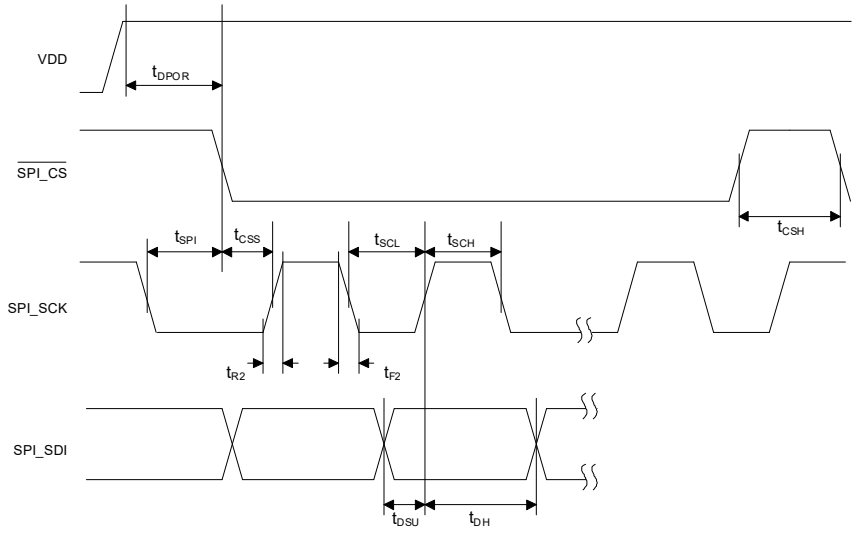
3. Time from power-up measured from when VDD is within the recommended operating conditions (see Table 3-1).

Table 3-6. Switching Specifications—SPI Control Port

Test conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds; T_A = 25°C.

Parameters [1,2]	Symbol	Min	Max	Units
SCK clock frequency	f_{SCL}	—	6	MHz
SCK edge to $\overline{CS}$ falling [3]	t_{SPI}	500	—	ns
$\overline{CS}$ high time between transmissions	t_{CSH}	1	—	µs
$\overline{CS}$ falling to SCK rising edge	t_{CSS}	20	—	ns
SCK pulse width low	t_{SCL}	66	—	ns
SCK pulse width high	t_{SCH}	66	—	ns
SDI to SCK rising setup time	t_{DSU}	40	—	ns
SCK rising to SDI hold time [4]	t_{DH}	15	—	ns
Rise time of SCK and SDI [5]	t_{R2}	—	100	ns
Fall time of SCK and SDI [5]	t_{F2}	—	100	ns
Delay from supply voltage stable to control port ready [6]	t_{DPOR}	—	200	µs

1. The SPI control port uses a 7-bit register address and 8-bit data words.
2. SPI control-port timing.



3. t_{SPI} is only needed before first falling edge of $\overline{CS}$ after power is applied; t_{SPI} is 0 all other times.
4. Data must be held for sufficient time to bridge the transition time of SCK.
5. For f_{SCK} < 1 MHz.
6. The supply voltage is considered stable when VDD is within the recommended operating conditions (see Table 3-1).

4 Functional Description

4.1 Device Architecture

The CS2501 is a highly versatile clock generator. It combines an analog PLL and digital FLL to provide high-resolution clock multiplier capability. The delta-sigma architecture enables low-jitter clock generation across a wide range of fractional operating ratios; it also supports fast transitions between different ratios and output frequencies. Configurable bandwidth of the digital FLL enables optimized behavior under dynamic operating conditions.

The analog PLL generates the main clock output (CLK_OUT), using the timing reference as its input. The timing reference is a stable low-jitter clock source, derived from the REF_CLK_IN input, external crystal, or the internal oscillator. The timing reference is used to ensure the time and phase stability of the PLL output. The PLL frequency ratio determines the multiplier ratio between the timing-reference input and the clock output.

The digital FLL provides input to the analog PLL to configure the frequency ratio. The digital FLL uses the frequency reference (CLK_IN) as its input and generates the PLL frequency ratio as a control signal to the analog PLL. The capability of the digital FLL is enhanced by its configurable bandwidth; a wide bandwidth is used to achieve lock in a short time, while a narrow bandwidth is used to provide optimal jitter performance.

The user-defined frequency ratio is an input to the digital FLL and defines the CLK_OUT:CLK_IN frequency ratio. The FLL monitors the input and output clocks and controls the analog PLL frequency ratio to achieve the required CLK_OUT frequency. The frequency ratio is dynamically controlled to maintain the required output ratio.

The hybrid analog/digital PLL is illustrated in Fig. 4-1. The user-defined multiplier ratio is defined by the *M_Ratio* parameter.

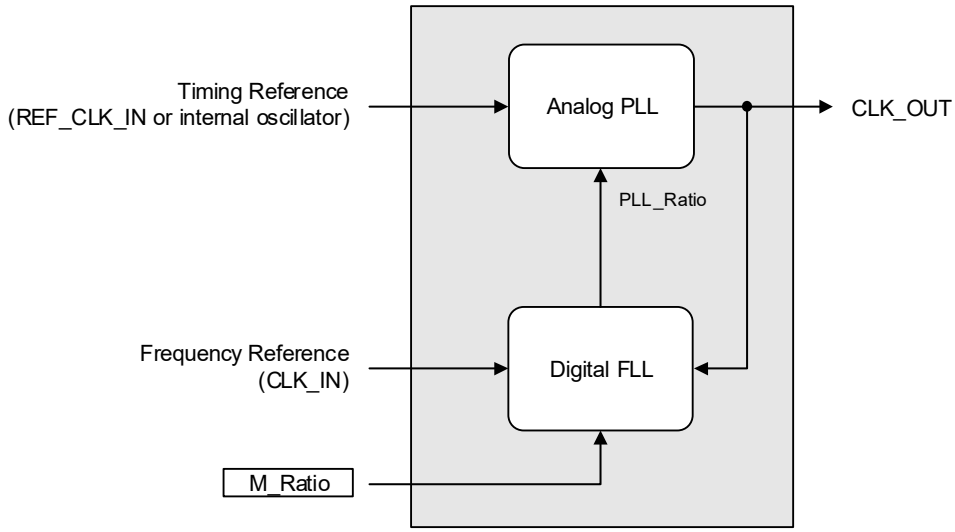


Figure 4-1. Hybrid Analog/Digital PLL

4.2 Timing Reference Configuration

The low-jitter timing reference is provided either by an external source (clock input or crystal), or by the internal oscillator. By default, the timing reference is selected automatically depending on the external pin connections, as shown Section 2. It is recommended to use SYSCLK_SRC to select the internal or external source, as shown in Fig. 4-2.

The frequency range for the external timing reference is described in Table 3-4. Note that the supported frequency range differs depending on the applicable source.

The internal timing reference, SYSCLK, is derived from the selected timing source. A programmable divider is provided for the external timing reference; the divider must be configured using REF_CLK_IN_DIV to bring the reference frequency within the valid SYSCLK range of 8–18.75 MHz.

The timing reference configuration is shown in Fig. 4-2.

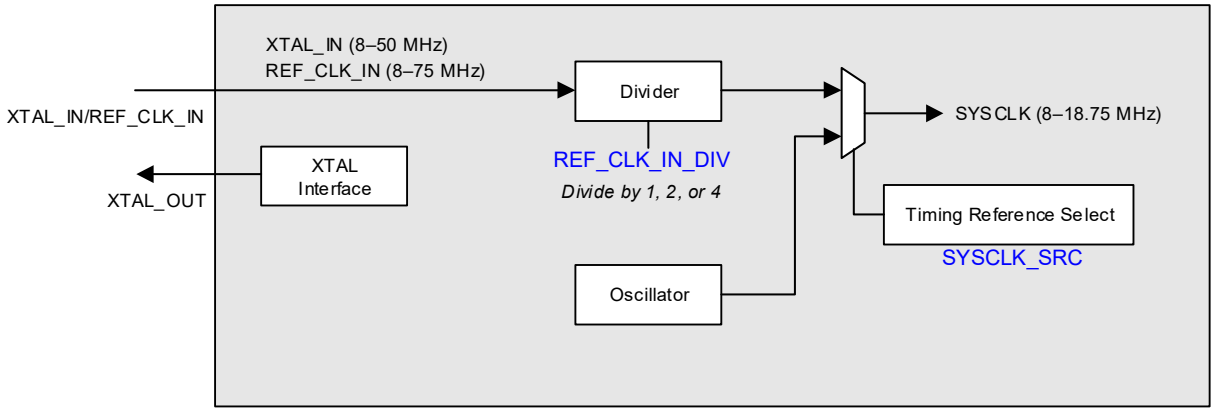


Figure 4-2. Timing Reference Configuration

4.2.1 Crystal Oscillator

The crystal oscillator uses an external crystal to generate the timing reference. Load capacitors are connected to the crystal as shown in Fig. 4-3. A series resistor (R_S) may also be required to configure the drive level for the selected crystal.

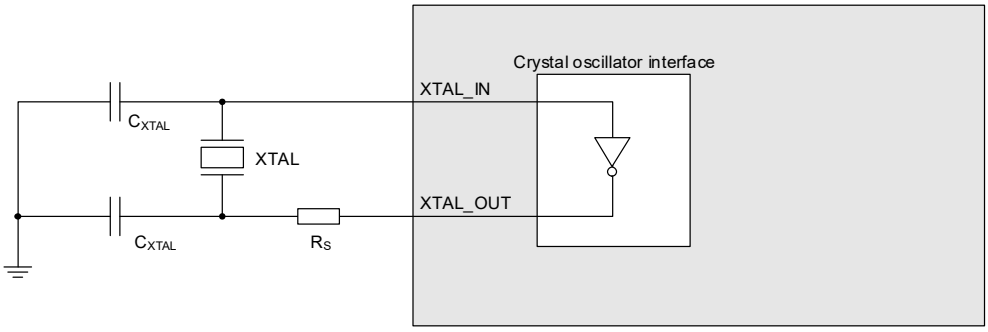


Figure 4-3. Crystal Oscillator Connection

Guidance on selecting a suitable crystal and associated components is provided in Section 5.1. The suitability of the external crystal is calculated as a function of the operating voltage (VDD) and the transconductance of the crystal interface, as defined in Table 3-4.

Under 3.3 V operating conditions, the transconductance is configurable using the register fields described below. This can be used to optimize the crystal oscillator for the selected external crystal.

- If REF_CLK_IN_DIV = 10 (Divide by 1), the transconductance is configured using XOSC_GEAR1_3V3_DRV
- If REF_CLK_IN_DIV = 01 (Divide by 2), the transconductance is configured using XOSC_GEAR2_3V3_DRV
- If REF_CLK_IN_DIV = 00 (Divide by 4), the transconductance is configured using XOSC_GEAR3_3V3_DRV

4.3 Hybrid PLL Configuration

The PLL is enabled and configured as described in the following sections.

4.3.1 Enable and Lock Status

The PLL is enabled by setting PLL_EN1 and PLL_EN2 (both bits must be set in order to enable the PLL). Note there are no sequencing requirements—the bits may be set or cleared in any order.

Note: The device should be fully configured by writing to the applicable control registers before enabling the PLL. When changing the configuration, it is recommended to disable the PLL before updating the register fields; this ensures there is no unexpected transient behavior. See Section 4.7.3 for further details of configuration restrictions.

The PLL lock status is dependent on the clock inputs and the device configuration. Changes in the clock inputs or to the configuration registers can cause the PLL to lose lock. If the PLL loses lock, the quality of the clock output cannot be assured.

The PLL lock status is indicated using UNLOCK. This bit reads 1 if the PLL has unlocked since the last read of the field. This is a read-only bit and is automatically cleared after it has been read.

- If UNLOCK = 0, the PLL is locked and has remained locked since the last read.
- If UNLOCK = 1, one of two possible conditions applies—either (1) the PLL is unlocked, or (2) the PLL is locked, but had previously unlocked since the last read. In this case, a second read of the UNLOCK bit is required in order to confirm the current lock status—if the second read indicates 0, the PLL is locked; if the second read indicates 1, the PLL is unlocked.

The lock status can be indicated on the auxiliary output pin as described in Section 4.6. The lock status can be used to automatically disable the clock outputs—see Section 4.5 for further details.

4.3.2 Ratio Configuration

The PLL is configured using a ratio that determines the output frequency as a function of the frequency reference, CLK_IN.

- The output frequency is defined by the following equation: $f_{CLK\_OUT} = f_{CLK\_IN} \times$ PLL Ratio
  For example, to generate a 24.576 MHz output from a 48 kHz frequency reference, a ratio of 512 is required.

The PLL ratio is a 32-bit value, configured using RATIO_n. The ratio can be defined in high-resolution (12.20) or high-multiplication (20.12) format; the format is selected using RATIO_CFG.

- In high-resolution (12.20) format, the 12 MSBs represent the integer portion of the ratio, and the remaining 20 bits represent the fractional portion. This format supports a maximum multiplication factor of ~4096, with a resolution of 0.954 ppm.
- In high-multiplication (20.12) format, the 20 MSBs represent the integer portion of the ratio, and the remaining 12 bits represent the fractional portion. This format supports a maximum multiplication factor of ~1,048,576, with a resolution of 244 ppm.

Note: If the desired ratio is less than 4096, the 12.20 format is recommended, to ensure the accuracy of the PLL output.

The PLL ratio is also configured using RATIO_MOD, allowing additional multiplication/division factors to be applied to the RATIO_n selection.

The ratio modifier can be used to simplify the selection of related frequency ratios, while using the same RATIO_n value. It can also be used to support high multiplication ratios in 12.20 format (multiplying by 2, 4, or 8) or to enable greater precision in 20.12 format (dividing by 2, 4, 8, or 16).

Note that, regardless of the ratio format and the ratio modifier, the PLL ratio cannot exceed a multiplication factor of 1,048,576 or a resolution of 0.954 PPM. If the configured parameters exceed these limits, the effective multiplication or resolution is truncated.

If the selected PLL ratio is invalid, the output clocks are disabled. Normal operation resumes when a valid ratio is detected (either due to register configuration or a change in CLK_IN frequency).

The ratio configuration is illustrated in Fig. 4-4.

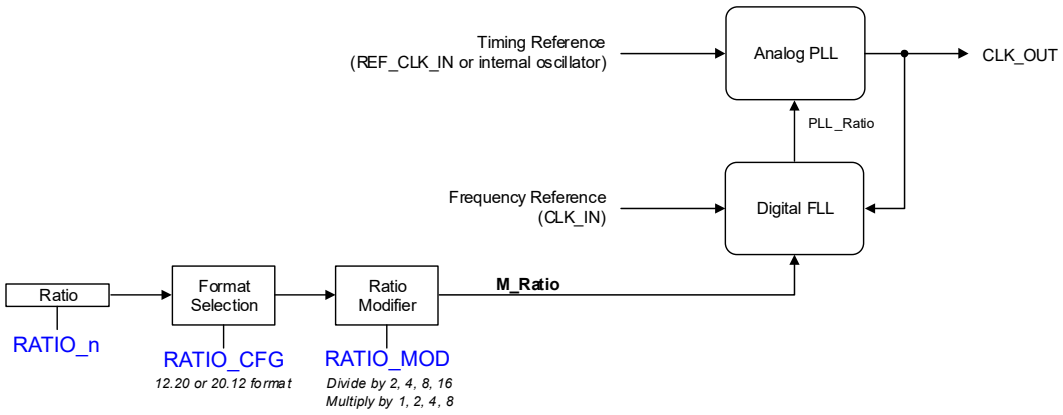


Figure 4-4. PLL Ratio Configuration

4.4 Frequency Reference Configuration

The frequency reference (CLK_IN) is an input to the digital FLL, which is used to generate the dynamic ratio for the analog PLL. The digital FLL monitors the input and output clocks and controls the analog PLL frequency ratio to achieve the required CLK_OUT frequency. The hybrid PLL/FLL architecture allows the low-jitter timing reference to be used to generate the clock output, while using a separate clock (CLK_IN) as a frequency reference. The frequency range for CLK_IN is defined in Table 3-4.

The CS2501 is tolerant of intermittent or unstable characteristics on the CLK_IN frequency reference. The behavior of the device is configurable as described in the following sections.

4.4.1 Clock Skipping and Intermittent CLK_IN

The CLK_IN signal is monitored to confirm the frequency reference is present. If the CLK_IN signal is not present, the CS2501 responds in a number of ways, depending on the duration of the interruption and on other configurable options. The clock-skipping option allows short interruptions to CLK_IN to be permitted without affecting the CLK_OUT signal.

Note: Clock skipping is supported for software compatibility with earlier devices; for new designs, it is recommended to configure the CS2501 in Holdover Mode as described in Section 4.4.2.

If CLK_IN is interrupted for longer than 2^{23} SYSCLK cycles (447–1048 ms), the PLL unlocks and the PLL output is no longer valid. The PLL remains unlocked indefinitely while CLK_IN is interrupted. When CLK_IN resumes, the PLL locks to CLK_IN and the valid CLK_OUT signal is restored.

If the PLL is not locked, the PLL output is invalid. To avoid spurious clock generation, the OUT_GATE bit can be used to disable the clock output whenever the PLL is not locked. If OUT_GATE = 0, the clock output is disabled whenever the PLL is not locked. See Section 4.5 for other options supported when the PLL is unlocked.

Note: If the clock output is disabled as a result of the PLL lock status, the CS2501 controls the CLK_OUT signal to ensure there is no partial clock period—the output is disabled at the end of a complete clock period.

The CLK_IN interruption longer than 2^{23} SYSCLK cycles is illustrated in Fig. 4-5.

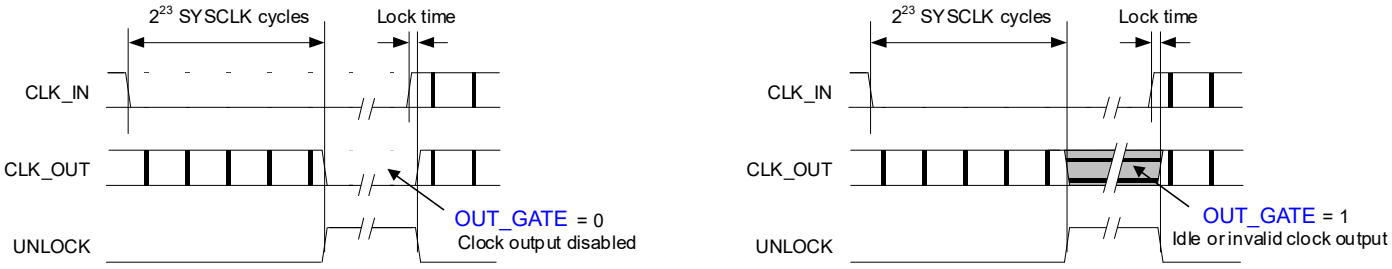


Figure 4-5. CLK_IN Interruption > 2^{23} SYSCLK Cycles

If CLK_IN is interrupted for a period shorter than 2^{23} SYSCLK cycles, the PLL remains locked for the duration of the interruption. When CLK_IN resumes, the PLL unlocks temporarily and relocks to CLK_IN. Note the PLL output is not valid for the period while the PLL is unlocked; the clock output while the PLL is unlocked depends on OUT_GATE.

The CLK_IN interruption shorter than 2^{23} SYSCLK cycles is illustrated in Fig. 4-6.

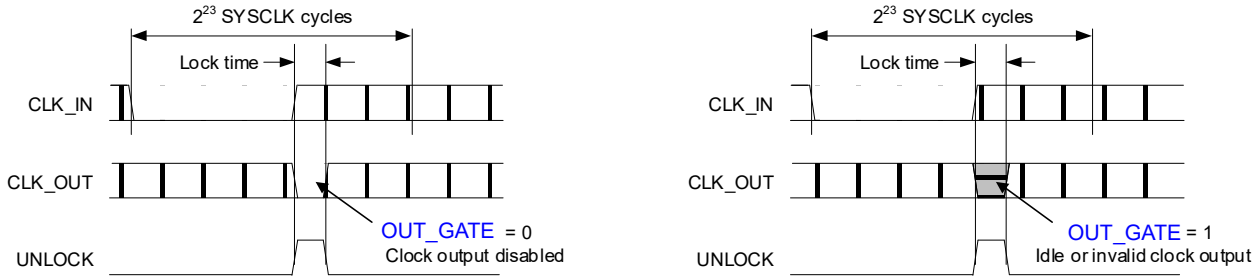


Figure 4-6. CLK_IN Interruption < 2^{23} SYSCLK Cycles

The clock-skipping feature allows the CS2501 to tolerate short interruptions to CLK_IN without causing the PLL to unlock. By maintaining the PLL lock, a valid CLK_OUT signal can be generated without any glitch or interruption.

Clock skipping is enabled by setting CLK_IN_SKIP_EN. If clock skipping is enabled and CLK_IN is interrupted for a period shorter than the timeout period (typically ~20 ms), the PLL remains locked and resynchronizes to CLK_IN.

Note that clock skipping is only supported for CLK_IN frequencies < 80 kHz. The clock-skipping timeout period (i.e., the maximum permitted CLK_IN interruption) varies depending on the reference frequency and PLL ratio configuration.

Note: Clock skipping is not valid if the holdover function is enabled (see Section 4.4.2). Clock skipping is automatically disabled if the holdover function is enabled.

The clock-skipping behavior is illustrated in Fig. 4-7.

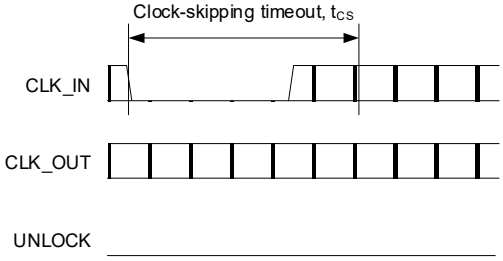


Figure 4-7. Clock Skipping for CLK_IN Interruption

4.4.2 Holdover Mode

The CLK_IN signal is monitored to confirm the frequency reference is present and stable. The holdover function enables a valid clock output to be maintained under conditions where the reference is missing or unstable. The holdover function is enabled by setting HOLDOVER_EN.

If CLK_IN is missing or unstable, the CS2501 freezes the dynamic PLL ratio at its current setting. The PLL remains locked and the CLK_OUT signal continues without any glitch or interruption.

When a valid CLK_IN is detected, the PLL resynchronizes to the frequency reference. If the frequency reference aligns with the previous CLK_IN frequency, the PLL remains locked and maintains a glitchless output.

4.4.3 Digital FLL Bandwidth

The bandwidth of the digital FLL can be configured to suit different operating conditions. The FLL bandwidth determines the extent to which any jitter on the CLK_IN signal is attenuated or is passed through to the output clocks. In some applications, it is desirable to reject all jitter as far as possible; in other applications, it may be preferable to preserve the low-frequency variations in the reference clock while attenuating jitter at higher frequencies.

The FLL bandwidth is configured using FLL_BW and FLL_BW_MOD. The FLL_BW field selects a value 1–128 Hz; the FLL_BW_MOD selects multiplication factor of ×1 or ×16. The combination of two fields allows bandwidth selections in the range 1–2048 Hz.

Notes: If the internal oscillator is used as the timing reference (see Section 4.2), the FLL bandwidth selection must be 16 Hz or greater.

The CS2501 automatically limits the FLL bandwidth to ensure optimal performance; the bandwidth is limited to a maximum of f_{CLK_IN} / 23.4 (rounded down to the nearest valid bandwidth selection).

The FLL bandwidth scales with the SYSCLK frequency; the nominal values selected using FLL_BW and FLL_BW_MOD are valid for 12 MHz SYSCLK.

A narrow bandwidth is typically recommended in applications where the CLK_OUT signal provides a new clock domain from which all other system clocks are derived. In these circumstances, the system benefits from maximum jitter rejection, as illustrated in Fig. 4-8.

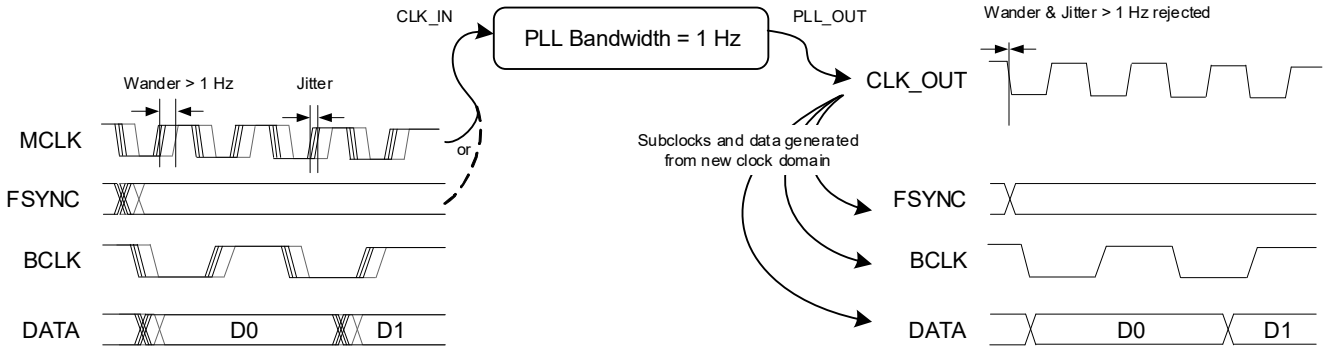


Figure 4-8. Narrow Bandwidth Application

A wide bandwidth is typically recommended in applications where some of the system clocks are referenced to CLK_OUT, while others are derived from CLK_IN. In these circumstances, it may be necessary to preserve some of the input reference variation in the clock output, in order to maintain phase alignment.

The FLL bandwidth should be set to the lowest setting that does not cause system-timing errors between the CLK_IN and CLK_OUT domains. The wide bandwidth use case is illustrated in Fig. 4-9.

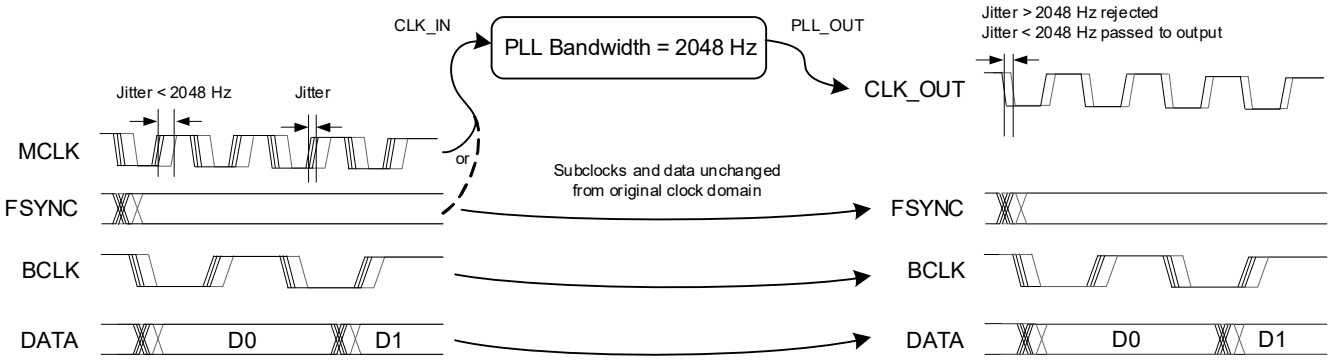


Figure 4-9. Wide Bandwidth Application

4.5 Output Configuration

The clock output from the hybrid PLL is provided on the CLK_OUT pin. The output is enabled by default and is disabled by setting CLK_OUT_DIS. If the output is disabled, the driver is configured in a high-impedance (Hi-Z) state.

The CLK_OUT signal is valid if the PLL is enabled and locked. If the PLL is not locked, the PLL output is invalid. To avoid spurious clock generation, the OUT_GATE bit can be used to stop the output whenever the PLL is not locked. If OUT_GATE = 0, the clock output is stopped whenever the PLL is not locked.

If OUT_GATE = 1 and IDLE_CLK_EN = 1, an idle clock output is generated if the PLL is enabled while CLK_IN is not present. The idle clock is derived from the SYSCLK internal timing reference (see Section 4.2). The frequency of the idle clock is configured using IDLE_CLK_FREQ. The idle clock can be used to ensure a CLK_OUT signal is generated if the PLL is enabled before CLK_IN is present. When CLK_IN is provided, the PLL locks to the clock reference and the output transitions to the configured frequency.

If OUT_GATE = 1 and the PLL is unlocked after previously having been locked, the CLK_OUT signal is invalid. The invalid output may be a fixed logic level or may be an undefined frequency.

The PLL lock status is indicated using UNLOCK. This bit is set if the PLL is not locked (including if the PLL is disabled).

If the clock output is stopped as a result of the PLL lock status, the CS2501 controls the CLK_OUT signal to ensure there is no partial clock period—the output is stopped at the end of a complete clock period. The stopped CLK_OUT signal is Logic 0.

If the PLL is disabled, the CLK_OUT signal is stopped immediately; the stopped CLK_OUT signal can be either Logic 0 or Logic 1. Note that the clock output is restored to Logic 0 during PLL enable, prior to starting the clock output; the timing is controlled to ensure there is no partial clock period.

The clock-output logic is described in Table 4-1.

Table 4-1. Clock Output Logic

CLK_OUT_DIS	PLL Enable [1]	UNLOCK	OUT_GATE	IDLE_CLK_EN	CLK_OUT pin
1	—	—	—	—	Hi-Z
0	Disabled	—	—	—	0 or 1
	Enabled	0	—	—	Valid Clock
		1	0	—	0
			1	0	Invalid Clock [2]
				1	Idle or Invalid Clock [3]

1.The PLL is enabled by setting PLL_EN1 and PLL_EN2. See Section 4.3.1 for further details.
2.The invalid clock may be a fixed logic level or may be an undefined frequency.
3.The idle clock is generated if the PLL is enabled while CLK_IN is absent. The output is invalid in other cases where the PLL is not locked.

4.6 Auxiliary Output

The CS2501 supports an auxiliary output (AUX_OUT) which can be configured as a clock or status output. The auxiliary output is configured using AUX_OUT_SEL. The supported output functions are:

- Timing reference clock (REF_CLK_IN or internal oscillator)
- Frequency reference clock (CLK_IN)
- Output clock (CLK_OUT)
- PLL unlock status (asserted if PLL is not locked)

A glitchless transition is provided if the auxiliary output is switched between the timing reference and the output clock, ensuring there are no partial clock periods in the output signal. The glitchless transition is illustrated in Fig. 4-10.

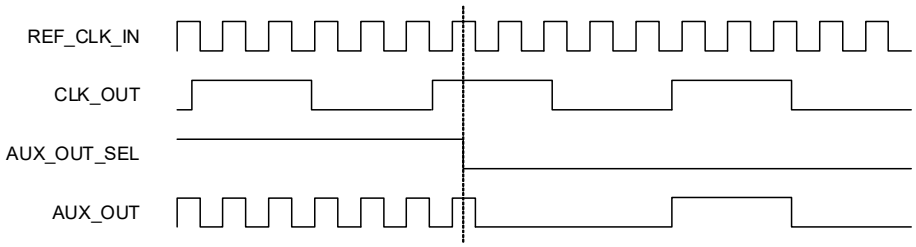


Figure 4-10. Glitchless Transition between Clock Signals

If the auxiliary output is configured as the PLL unlock indication, the output driver can be configured as either CMOS (active high) or open drain (active low). The output driver is configured using AUX_OUT_CFG.

Note: If the auxiliary output is configured as a clock output, the output driver is CMOS in all cases.

The output driver can be configured to high impedance by setting AUX_OUT_DIS.

The auxiliary output is illustrated in Fig. 4-11.

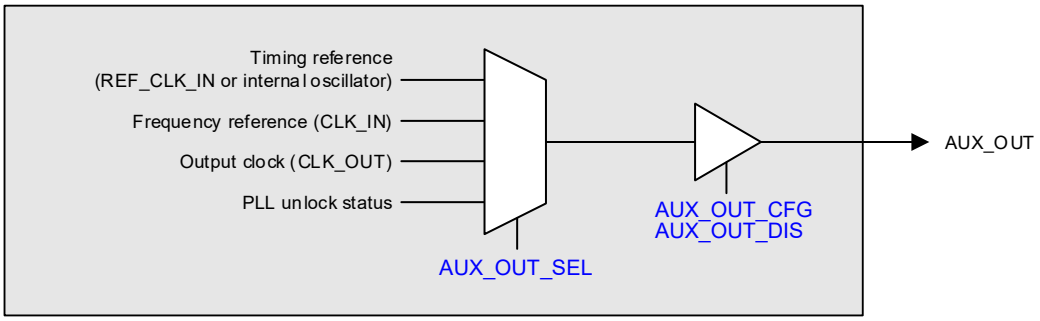


Figure 4-11. Auxiliary Output Configuration

4.7 I²C/SPI Control Port

The CS2501 incorporates a control port, supporting I²C or SPI modes of operation. In Software Control Mode, the CS2501 is configured by writing to control registers using the control port.

The control port is configured in I²C mode or SPI mode using the I2C_ADDR/ $\overline{\text{SPI\_CS}}$ pin.

- I²C mode is selected by connecting the I2C_ADDR/ $\overline{\text{SPI\_CS}}$ pin to VDD or GND. The pin connection is used to select the target address on the I²C bus.
- SPI mode is selected by a high-to-low transition on the I2C_ADDR/$\overline{\text{SPI\_CS}}$ pin after power-on.

4.7.1 I²C Interface

The I²C control port is supported using the I2C_SCL and I2C_SDA pins.

The CS2501 is a target device on the I²C bus—SCL is a clock input, SDA is a bidirectional data pin. To allow arbitration of multiple targets (and/or multiple controllers) on the same interface, the CS2501 transmits Logic 1 by tristating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the Logic 1 can be recognized by the controller.

In order to allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit target address (this is not the same as the address of each register in the register map). Note that the LSB of the target address is the read/write bit; this bit is set to Logic 1 for read and Logic 0 for write.

The I²C device address is configured using the I2C_ADDR/$\overline{\text{SPI\_CS}}$ pin as described in Table 4-2.

Table 4-2. I²C Address Selection

I2C_ADDR Pin Connection	I²C Address
Pull-up to VDD	0x9E (write), 0x9F (read)
Pull-down to GND	0x9C (write), 0x9D (read)

The host device indicates the start of data transfer with a high-to-low transition on SDA while SCL remains high. This indicates that a device address and subsequent address/data bytes follow. The CS2501 responds to the start condition and shifts in the next eight bits on SDA (8-bit target address, including read/write bit, MSB first). If the target address received matches the target address of The CS2501, it responds by pulling SDA low on the next clock pulse (ACK). If the target address is not recognized, the CS2501 returns to the idle condition and waits for a new start condition.

If the target address matches the target address of the CS2501, the data transfer continues. The controller indicates the end of data transfer with a low-to-high transition on SDA while SCL remains high. After receiving a complete address and data sequence, the CS2501 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e., SDA changes while SCL is high), the device returns to the idle condition.

The I²C interface uses a 7-bit register address and 8-bit data words. Note that the full I²C message protocol also includes a target address, a read/ write bit, and other signaling bits (see Fig. 4-12 and Fig. 4-13).

The CS2501 supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. If auto-increment is enabled, the CS2501 automatically increments the register address after each data byte. Successive data bytes can be input/output continuously, separated by the acknowledge (ACK) bit.

The auto-increment option is configured using the MSB of the register-address byte. Setting this bit enables the auto-increment.

The I²C register write operation is shown in Fig. 4-12.

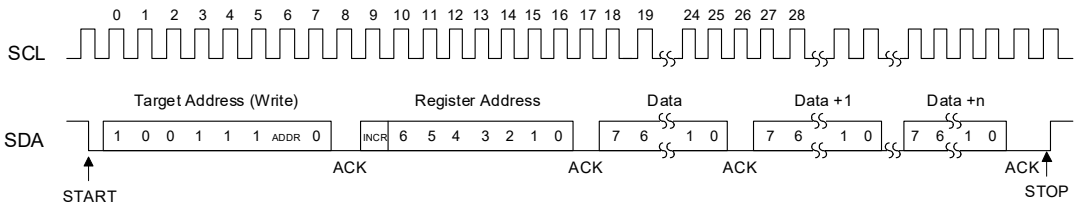


Figure 4-12. Control Interface I²C Register Write

The I²C register read operation is shown in Fig. 4-13.

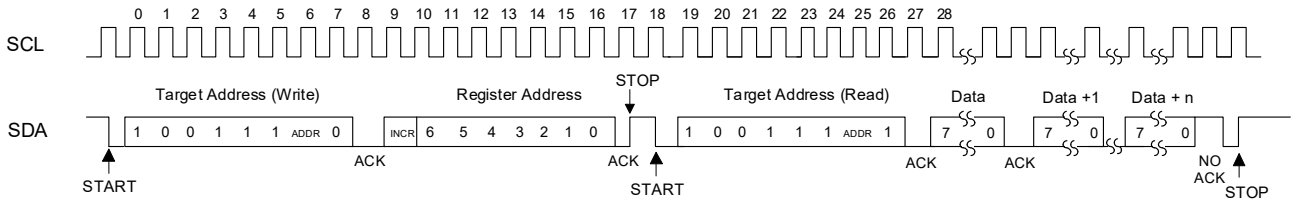


Figure 4-13. Control Interface I²C Register Read

4.7.2 SPI Interface

The SPI interface is supported using the $\overline{\text{SPI\_CS}}$, SPI_SCK, and SPI_SDI pins.

The $\overline{\text{SPI\_CS}}$ pin provides the chip-select input (active low). Data bits (on the SPI_SDI pin) are clocked in on the rising edge of SPI_SCK. Note the SPI interface supports write operations only; read operations are not supported.

The SPI write transaction starts with a high-to-low transition on $\overline{\text{SPI\_CS}}$. The first data byte contains the chip address, which must be 0x9E when writing to the CS2501. The next data byte contains the register address and auto-increment bit. This is followed by the data to be written to the selected register address.

Continuous (multiple) write mode allows register operations to be scheduled faster than is possible with single register writes. If auto-increment is enabled, the CS2501 automatically increments the register address after each data byte. Successive data bytes can be input every 8 clock cycles, allowing block writes of multiple registers.

The auto-increment option is configured using the MSB of the register-address byte. Setting this bit enables the auto-increment.

The SPI register write operation is shown in Fig. 4-14.

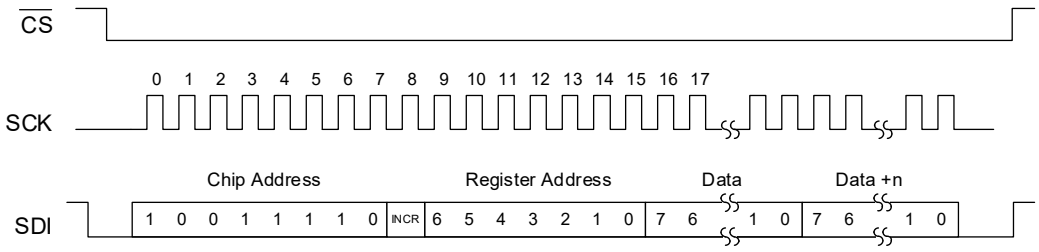


Figure 4-14. Control Interface SPI Register Write

4.7.3 Device Configuration

The device should be fully configured before enabling the PLL. When changing any register settings, it is recommended to disable the PLL, update the registers, then enable the PLL; this ensures there is no unintended behavior.

See Section 4.3.1 to enable and disable the PLL. Specific restrictions and exceptions on updating register fields are described in Section 4.7.3.2.

4.7.3.1 Freezable Fields

The register map supports a number of freezable fields, as listed in Table 4-3. If FREEZE_EN is set, these fields are frozen to their current values regardless of any register writes. If a new value is written, the value is buffered and does not become effective until FREEZE_EN is cleared. When FREEZE_EN is cleared, all of the frozen fields become active simultaneously.

Table 4-3. Freezable Fields

Address	Fields
0x02	CLK_OUT_DIS, AUX_OUT_DIS
0x03	AUX_OUT_SEL, RATIO_MOD

4.7.3.2 Field Update Restrictions

The fields listed in Table 4-4 can be configured at any time, and do not result in any partial clock period in the outputs.

Table 4-4. Register Fields with No Write Restrictions

Address	Fields
0x02	CLK_OUT_DIS, AUX_OUT_DIS
0x03	PLL_EN1, AUX_OUT_SEL
0x05	PLL_EN2, FREEZE_EN

The fields listed in Table 4-5 can be configured at any time, but may cause the PLL to lose lock temporarily.

Table 4-5. Register Fields with Restrictions

Address	Fields
0x03	RATIO_MOD
0x06–0x09	RATIO_1–RATIO_4
0x16	REF_CLK_IN_DIV
0x17	RATIO_CFG

Note that, for all other control fields (not listed in Table 4-4 or Table 4-5), the PLL should be disabled before reconfiguring; failure to do so may result in unintended behavior, and may require a software reset to restart the device.

4.7.4 Software Reset

A software reset is triggered by writing 0x5A to the SW_RST field. A software reset causes all of the CS2501 control registers to be reset to their default states.

4.7.5 Power-On Reset

The power-on reset (POR) sequence is scheduled on initial power-up, and following any interruption to the VDD supply. The POR causes all of the CS2501 control registers to be reset to their default states.

4.8 Device ID

The device ID, and other associated data, can be read from the control fields listed in Table 4-6.

Table 4-6. Device ID

Label	Description
DEVID_1, DEVID_2	Device ID
A_REV_ID	All-layer device revision
MTL_REV_ID	Metal-layer device revision

5 Applications

5.1 Crystal Component Selection

The crystal oscillator (see Section 4.2.1) uses an external crystal to generate the timing reference. Load capacitors are connected to the crystal as shown in Fig. 5-1. A series resistor (R_S) may also be required to configure the drive level for the selected crystal.

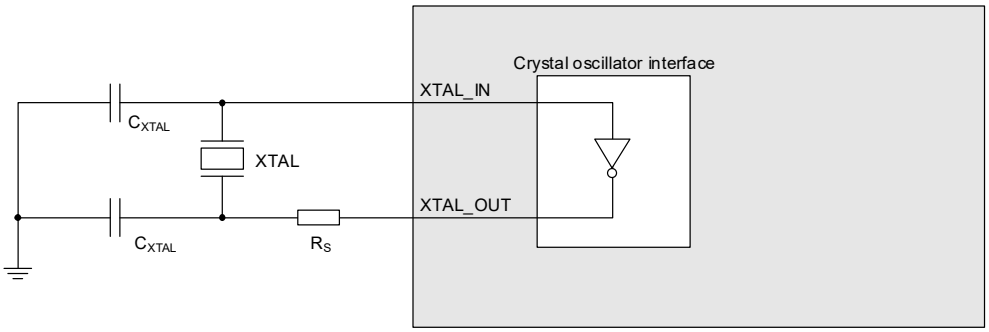


Figure 5-1. Crystal Oscillator Connection

The suitability of the selected crystal is determined by whether the gain margin and drive level are within the valid operating limits of the crystal. The gain margin and drive level can be calculated as a function of the transconductance of the crystal interface.

The transconductance of the crystal interface is dependent on the VDD operating voltage as described in Table 3-4. For 3.3 V use cases, the transconductance is configurable using the XOSC_GEARn_3V3_DRV fields as described in Section 4.2.1.

The recommended sequence for crystal component selection is as follows:

1. **Crystal selection.** The CS2501 is compatible with a wide variety of crystal components, including the NX3225SA, NX2016A, ECX-33Q, and ECX-2236Q families.
2. **Capacitor selection.** Capacitors should be selected according to the crystal manufacturer's specification for load capacitance (C_L). The recommended value for each C_{XTAL} capacitor is 2 × C_L.
3. **Series resistor.** In the first instance, assume the series resistor Rs is not required (0 Ω).
4. **Gain margin calculation.** The gain margin can be calculated from the transconductance of the crystal interface and the series resistor R_S, together with the crystal characteristics. If the gain margin is less than 5, adjust the transconductance parameter to achieve the required gain margin ≥5. If the required gain margin cannot be achieved, a different crystal selection must be made (Step 1).

   The gain margin is calculated as follows: $$\text{Gain Margin} = \frac{\text{Transconductance}}{4 \times (\text{ESR} + R_S) \times (2\pi \times f_{XTAL})^2 \times (C_0 + C_L)^2}$$

   where:

   Transconductance = transconductance of the crystal interface (S)

   ESR = equivalent series resistance (ESR) of the crystal (Ω)

   R_S = series resistance (Ω)

   f_{XTAL} = resonant frequency of the crystal (Hz)

   C_L = load capacitance of the crystal (F)

   C_0 = shunt capacitance of the crystal (F)

5. **Drive level calculation.** The drive level can be calculated using the crystal characteristics and the operating voltage. The operating voltage (peak voltage across the crystal) can be determined using measurement or else by simulation. If the drive level exceeds the maximum level for the crystal, adjust the series resistor R_S to meet the required specification. Increasing R_S results in a lower voltage across the crystal and a decrease in drive level.

   If the series resistor is adjusted, the gain margin must now be recalculated (Step 4). It is recommended to find the minimum series resistance that meets the required gain margin and drive level.

   The drive level (W) is calculated as follows: $\text{Drive Level} = 2 \times \text{ESR} \times (\pi \times f_{XTAL} \times V \times (C_L + C_0))^2$

   where:

   ESR = equivalent series resistance (ESR) of the crystal (Ω)

   f_{XTAL} = resonant frequency of the crystal (Hz)

   V = Peak voltage across the crystal (V)

   C_L = load capacitance of the crystal (F)

   C_0 = shunt capacitance of the crystal (F)

The sequence for crystal component selection is illustrated in Fig. 5-2.

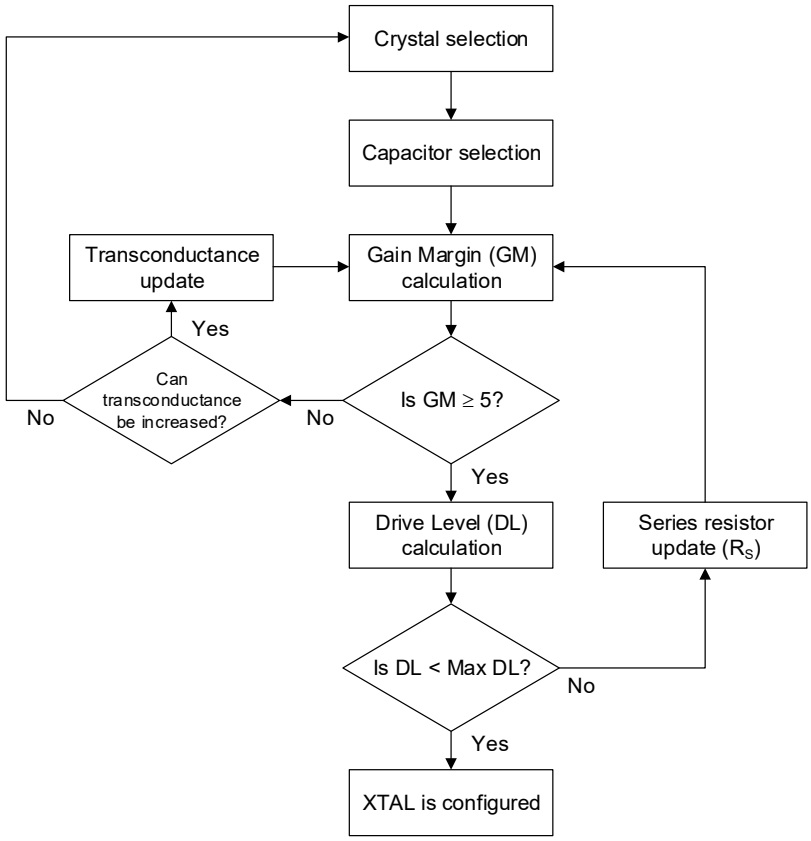


Figure 5-2. Crystal Oscillator Component Selection

6 Register Quick Reference

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

This register view is for the CS2501.

- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- Fields shown in orange are affected by the FREEZE bit.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

Table 6-1. Block Base Addresses

Base Address	Block Name	Register Quick Reference	Register Description Reference
0x0000 0000	**CONFIG**	Section 6.1	Section 7.1

6.1 CONFIG

Address	Register	7	6	5	4	3	2	1	0
0x0000 0002	PLL_CFG1	UNLOCK			—			AUX_OUT_DIS	CLK_OUT_DIS
p. 26		1	0	0	0	0	0	0	0
0x0000 0003	PLL_CFG2	RATIO_MOD			—		AUX_OUT_SEL		PLL_EN1
p. 26		0	0	0	0	0	0	0	0
0x0000 0004	PLL_CFG3	—				HOLDOVER_EN	—		
p. 27		0	0	0	0	0	0	0	0
0x0000 0005	PLL_CFG4	—				FREEZE_EN	—		PLL_EN2
p. 27		0	0	0	0	0	0	0	0
0x0000 0006	RATIO_REG_1	RATIO_1							
p. 27		0	0	0	0	0	0	0	0
0x0000 0007	RATIO_REG_2	RATIO_2							
p. 27		0	0	0	0	0	0	0	0
0x0000 0008	RATIO_REG_3	RATIO_3							
p. 27		0	0	0	0	0	0	0	0
0x0000 0009	RATIO_REG_4	RATIO_4							
p. 28		0	0	0	0	0	0	0	0
0x0000 0016	PLL_CFG5	CLK_IN_SKIP_EN	AUX_OUT_CFG	—	REF_CLK_IN_DIV		SYSCLK_SRC		—
p. 28		0	0	0	0	0	0	0	0
0x0000 0017	PLL_CFG6	—			OUT_GATE	RATIO_CFG	—		
p. 28		0	0	0	0	0	0	0	0
0x0000 001E	PLL_CFG7	FLL_BW_MOD	FLL_BW			—			
p. 28		1	0	0	0	0	0	0	0
0x0000 0054	DEV_ID_CS250X_0	DEVID_2							
p. 29		0	0	1	0	0	1	0	1
0x0000 0055	DEV_ID_CS250X_1	DEVID_1							
p. 29		0	0	0	0	0	0	0	1
0x0000 0056	REV_ID_CS250X_2	A_REV_ID				MTL_REV_ID			
p. 29		X	X	X	X	X	X	X	X
0x0000 0058	SW_RESET	SW_RST							
p. 29		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x0000 0068	XOSC_DRV1	XOSC_GEAR1_3V3_DRV				—			
p. 29		0	0	0	0	1	1	1	1
0x0000 0069	XOSC_DRV2	XOSC_GEAR2_3V3_DRV				—			
p. 30		0	0	0	0	1	1	1	1
0x0000 006A	XOSC_DRV3	XOSC_GEAR3_3V3_DRV				—			
p. 30		0	0	0	0	1	1	1	1
0x0000 0070	IDLE_CLK_CFG	—				IDLE_CLK_EN	IDLE_CLK_FREQ		
p. 30		0	0	0	0	1	1	0	0

7 Register Descriptions

This section describes each of the control port registers.

This register view is for the CS2501.

- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- Fields shown in orange are affected by the FREEZE bit.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

7.1 CONFIG

7.1.1 PLL_CFG1

Address: 0x0000 0002

	7	6	5	4	3	2	1	0
	UNLOCK	—					AUX_OUT_DIS	CLK_OUT_DIS
Access	RO	—					RW	RW
Default	1	0	0	0	0	0	0	0

Bits	Name	Description
7	UNLOCK	PLL frequency unlock indicator 0 = PLL has not unlocked since last read of this field 1 = (Default) PLL has unlocked since last read of this field
6:2	—	Reserved
1	AUX_OUT_DIS	AUX_OUT disable. If disabled, the output driver is high-impedance (Hi-Z). 0 = (Default) Output enabled 1 = Output disabled (Hi-Z)
0	CLK_OUT_DIS	CLK_OUT disable. If disabled, the output driver is high-impedance (Hi-Z). 0 = (Default) Output enabled 1 = Output disabled (Hi-Z)

7.1.2 PLL_CFG2

Address: 0x0000 0003

RW	7	6	5	4	3	2	1	0
	RATIO_MOD			—		AUX_OUT_SEL		PLL_EN1
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	RATIO_MOD	Ratio modifier control. Adjusts the PLL ratio by the selected multiplier/division factor. 000 = (Default) Multiply x1 001 = Multiply x2 010 = Multiply x4 011 = Multiply x8 100 = Divide /2 101 = Divide /4 110 = Divide /8 111 = Divide /16
4:3	—	Reserved
2:1	AUX_OUT_SEL	AUX_OUT function select 00 = (Default) REF_CLK_IN 01 = CLK_IN 10 = CLK_OUT 11 = PLL unlock (UNLOCK)
0	PLL_EN1	PLL enable. Note that PLL_EN2 must also be set to enable the PLL. 0 = (Default) Disabled 1 = Enabled

7.1.3 PLL_CFG3

Address: 0x0000 0004

RW	7	6	5	4	3	2	1	0
	—				HOLDOVER_EN	—		
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3	HOLDOVER_EN	Holdover enable. 0 = (Default) Disabled 1 = Enabled
2:0	—	Reserved

7.1.4 PLL_CFG4

Address: 0x0000 0005

RW	7	6	5	4	3	2	1	0
	—				FREEZE_EN	—		PLL_EN2
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3	FREEZE_EN	Freeze register control. If enabled, the freezable fields hold their current values. Any updates to these fields are buffered until FREEZE_EN is cleared. 0 = (Default) Disabled 1 = Enabled
2:1	—	Reserved
0	PLL_EN2	PLL enable. Note that PLL_EN1 must also be set to enable the PLL. 0 = (Default) Disabled 1 = Enabled

7.1.5 RATIO_REG_1

Address: 0x0000 0006

RW	7	6	5	4	3	2	1	0
	RATIO_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	RATIO_1	PLL ratio, bits [31:24]

7.1.6 RATIO_REG_2

Address: 0x0000 0007

RW	7	6	5	4	3	2	1	0
	RATIO_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	RATIO_2	PLL ratio, bits [23:16]

7.1.7 RATIO_REG_3

Address: 0x0000 0008

RW	7	6	5	4	3	2	1	0
	RATIO_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	RATIO_3	PLL ratio, bits [15:8]

7.1.8 RATIO_REG_4

Address: 0x0000 0009

RW	7	6	5	4	3	2	1	0
	RATIO_4							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	RATIO_4	PLL ratio, bits [7:0]

7.1.9 PLL_CFG5

Address: 0x0000 0016

RW	7	6	5	4	3	2	1	0
	CLK_IN_SKIP_EN	AUX_OUT_CFG	—	REF_CLK_IN_DIV		SYSCLK_SRC		—
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	CLK_IN_SKIP_EN	Clock-skipping enable 0 = (Default) Disabled 1 = Enabled
6	AUX_OUT_CFG	AUX1 and AUX2 driver configuration. Only valid for lock/status output signals; clock outputs are CMOS in all cases. 0 = (Default) CMOS. Active high (Logic 1 indicates unlock or clock-missing status). 1 = Open Drain. Active low (Logic 0 indicates unlock or clock-missing status).
5	—	Reserved
4:3	REF_CLK_IN_DIV	REF_CLK_IN input divider. 00 = (Default) Divide by 4 01 = Divide by 2 10 = Divide by 1 11 = Reserved
2:1	SYSCLK_SRC	Source selection for the PLL timing reference SYSCLK between REF_CLK_IN and the internal oscillator 00 = (Default) Automatic selection 01 = REF_CLK_IN 10 = Internal oscillator 11 = Reserved
0	—	Reserved

7.1.10 PLL_CFG6

Address: 0x0000 0017

RW	7	6	5	4	3	2	1	0
	—			OUT_GATE	RATIO_CFG		—	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4	OUT_GATE	Output gate control. Selects whether the clock outputs are stopped automatically if they are not valid. 0 = (Default) Enabled 1 = Disabled
3	RATIO_CFG	Ratio format control. 0 = (Default) High multiplication (20.12) 1 = High resolution (12.20)
2:0	—	Reserved

7.1.11 PLL_CFG7

Address: 0x0000 001E

RW	7	6	5	4	3	2	1	0
	FLL_BW_MOD	FLL_BW			—			
Default	1	0	0	0	0	0	0	0

Bits	Name	Description
7	FLL_BW_MOD	FLL bandwidth multiplication factor. Modifies the bandwidth selected by FLL_BW. 0 = FLL_BW is multiplied by 1 1 = (Default) FLL_BW is multiplied by 16

Bits	Name	Description
6:4	FLL_BW	FLL bandwidth select. Note the FLL bandwidth is also determined by the multiplication factor, FLL_BW_MOD. 000 = (Default) 1 Hz 001 = 2 Hz 010 = 4 Hz ... 111 = 128 Hz
3:0	—	Reserved

7.1.12 DEV_ID_CS250X_0

Address: 0x0000 0054

	7	6	5	4	3	2	1	0
RO	DEVID_2							
Default	0	0	1	0	0	1	0	1

Bits	Name	Description
7:0	DEVID_2	Device ID (MSB). A value of 0x2501 indicates the device is a CS2501.

7.1.13 DEV_ID_CS250X_1

Address: 0x0000 0055

	7	6	5	4	3	2	1	0
RO	DEVID_1							
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:0	DEVID_1	Device ID (LSB). A value of 0x2501 indicates the device is a CS2501.

7.1.14 REV_ID_CS250X_2

Address: 0x0000 0056

	7	6	5	4	3	2	1	0
RO	A_REV_ID				MTL_REV_ID			
Default	X	X	X	X	X	X	X	X

Bits	Name	Description
7:4	A_REV_ID	All-layer device revision. This field is incremented for every all-layer revision of the device.
3:0	MTL_REV_ID	Metal-layer device revision. This field is incremented for every metal-layer revision of the device.

7.1.15 SW_RESET

Address: 0x0000 0058

	7	6	5	4	3	2	1	0
WO	SW_RST							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	SW_RST	Software reset. Write 0x5A to execute a software reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved

7.1.16 XOSC_DRV1

Address: 0x0000 0068

	7	6	5	4	3	2	1	0
RW	XOSC_GEAR1_3V3_DRV				—			
Default	0	0	0	0	1	1	1	1

Bits	Name	Description
7:4	XOSC_GEAR1_3V3_DRV	Crystal oscillator transconductance control, 8-18.75 MHz, 3.3 V. Valid if REF_CLK_IN_DIV = 10 (Divide by 1). 0x0 = (Default) 13 mS 0x1 = 26 mS 0x2–0xF = Reserved
3:0	—	Reserved

7.1.17 XOSC_DRV2

Address: 0x0000 0069

RW	7	6	5	4	3	2	1	0
	XOSC_GEAR2_3V3_DRV				—			
Default	0	0	0	0	1	1	1	1

Bits	Name	Description
7:4	XOSC_GEAR2_3V3_DRV	Crystal oscillator transconductance control, 16-37.5 MHz, 3.3 V. Valid if REF_CLK_IN_DIV = 01 (Divide by 2). 0x0 = (Default) 13 mS 0x1 = 26 mS 0x2–0xF = Reserved
3:0	—	Reserved

7.1.18 XOSC_DRV3

Address: 0x0000 006A

RW	7	6	5	4	3	2	1	0
	XOSC_GEAR3_3V3_DRV				—			
Default	0	0	0	0	1	1	1	1

Bits	Name	Description
7:4	XOSC_GEAR3_3V3_DRV	Crystal oscillator transconductance control, 32-50 MHz, 3.3 V. Valid if REF_CLK_IN_DIV = 00 (Divide by 4). 0x0 = (Default) 13 mS 0x1 = 26 mS 0x2–0xF = Reserved
3:0	—	Reserved

7.1.19 IDLE_CLK_CFG

Address: 0x0000 0070

RW	7	6	5	4	3	2	1	0
	—				IDLE_CLK_EN	IDLE_CLK_FREQ		
Default	0	0	0	0	1	1	0	0

Bits	Name	Description
7:4	—	Reserved
3	IDLE_CLK_EN	Idle clock enable. If OUT_GATE=1 and IDLE_CLK_EN=1, the idle clock is output if the PLL is enabled while CLK_IN is absent. 0 = Disabled 1 = (Default) Enabled
2:0	IDLE_CLK_FREQ	Idle clock frequency 000–001 = Reserved 010 = SYSCLK /4 011 = SYSCLK /6 100 = (Default) SYSCLK /8 101 = SYSCLK /10 110 = SYSCLK /12 111 = SYSCLK /14

8 Performance Plots

Performance data is provided for a variety of test cases. Performance is measured at the main clock output (CLK_OUT).

Test conditions (unless otherwise specified): T_A = 25°C, output load = 15 pF, output drive strength = 10 mA, REF_CLK is jitter-free (phase noise at least 20 dB lower than the device phase noise), VDD is noise free (noise present does not impact on jitter specifications).

8.1 Jitter Performance

Sinusoidal phase-deviation tolerance is illustrated in Fig. 8-1. Phase deviation is applied to the CLK_IN frequency reference; the performance plots show the phase deviation that can be tolerated without losing PLL lock.

Test conditions: CLK_IN = 12.288 MHz, CLK_OUT = 12.288 MHz, REF_CLK = External 12 MHz or internal oscillator. (Performance is measured with external 12 MHz reference clock, 12 MHz crystal, and internal oscillator; the plot shows worst-case performance.)

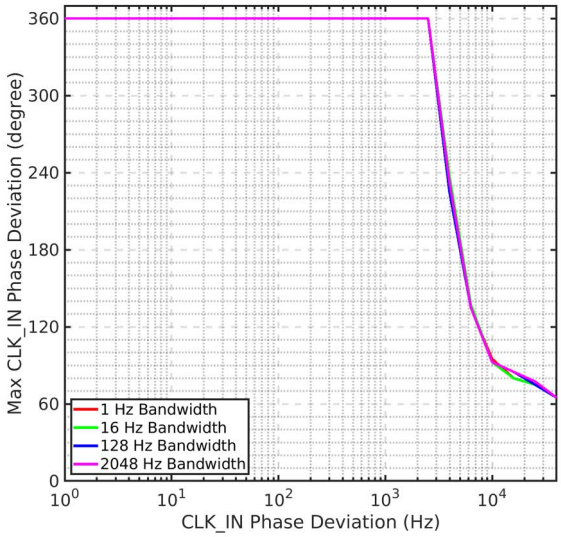


Figure 8-1. Sinusoidal Phase-Deviation Tolerance—External Clock or Internal Oscillator

Random TIE jitter rejection and tolerance is illustrated in Fig. 8-2 and Fig. 8-3. Jitter is applied to the CLK_IN frequency reference.

Test conditions: CLK_IN = 12.288 MHz, CLK_OUT = 12.288 MHz, REF_CLK = External 12 MHz or internal oscillator. (External clock is provided using 12 MHz reference or 12 MHz crystal; the plot shows worst-case performance.)

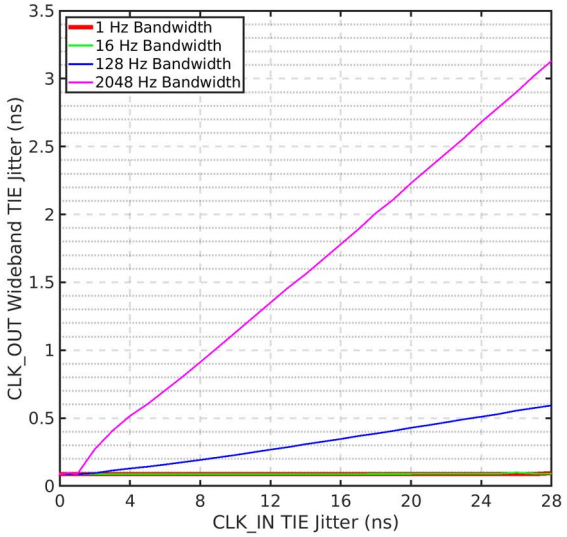


Figure 8-2. Random Jitter Rejection—External Clock

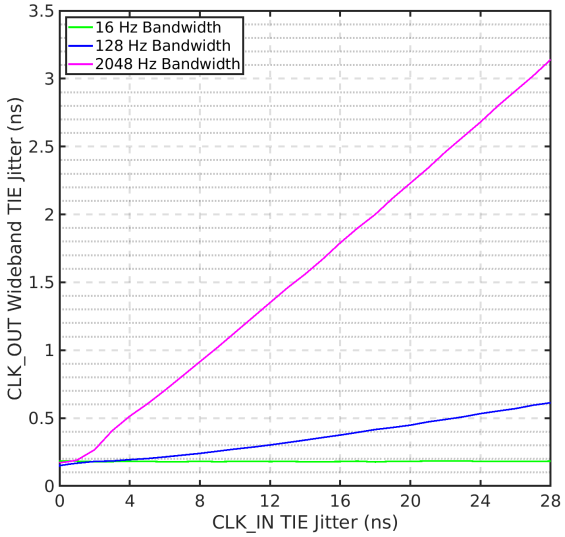


Figure 8-3. Random Jitter Rejection—Internal Oscillator

Sinusoidal TIE jitter transfer is illustrated in Fig. 8-4. Jitter is applied to the CLK_IN frequency reference; the performance plots show the output jitter level relative to the input jitter level.

Test conditions: CLK_IN = 12.288 MHz, CLK_OUT = 12.288 MHz, REF_CLK = External 12 MHz or internal oscillator. (Performance is measured with external 12 MHz reference clock, 12 MHz crystal, and internal oscillator; the plot shows worst-case performance.)

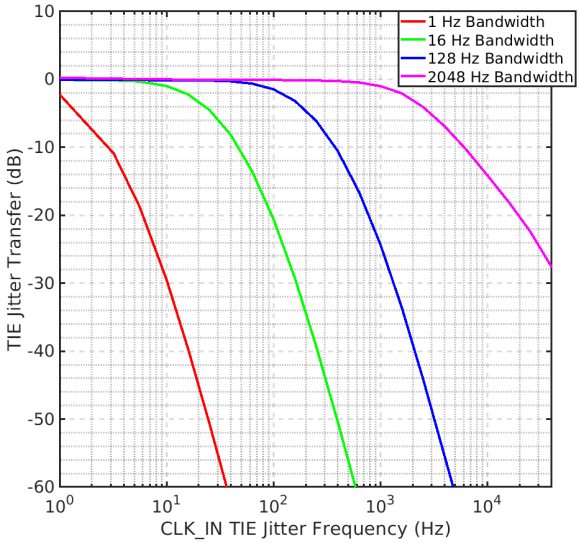


Figure 8-4. Sinusoidal Jitter Transfer—External Clock or Internal Oscillator

8.2 Phase Noise

The intrinsic phase-noise performance is illustrated in Fig. 8-5 and Fig. 8-6. The performance plots show the output phase noise under typical operating conditions. Note that the CLK_IN frequency reference is jitter-free for these tests.

Test conditions: CLK_IN = 48 kHz, CLK_OUT = 24.576 MHz, REF_CLK = External 12 MHz or internal oscillator. (External clock is provided using 12 MHz reference or 12 MHz crystal; the plot shows worst-case performance.)

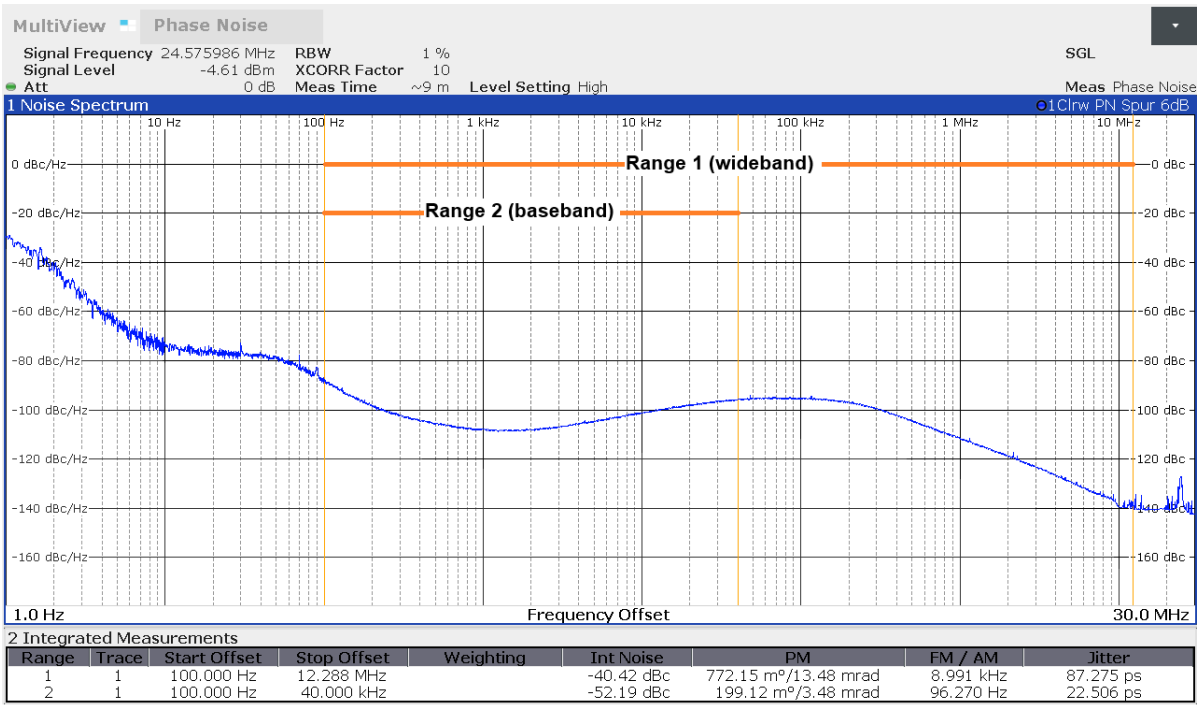


Figure 8-5. Phase Noise—External Clock

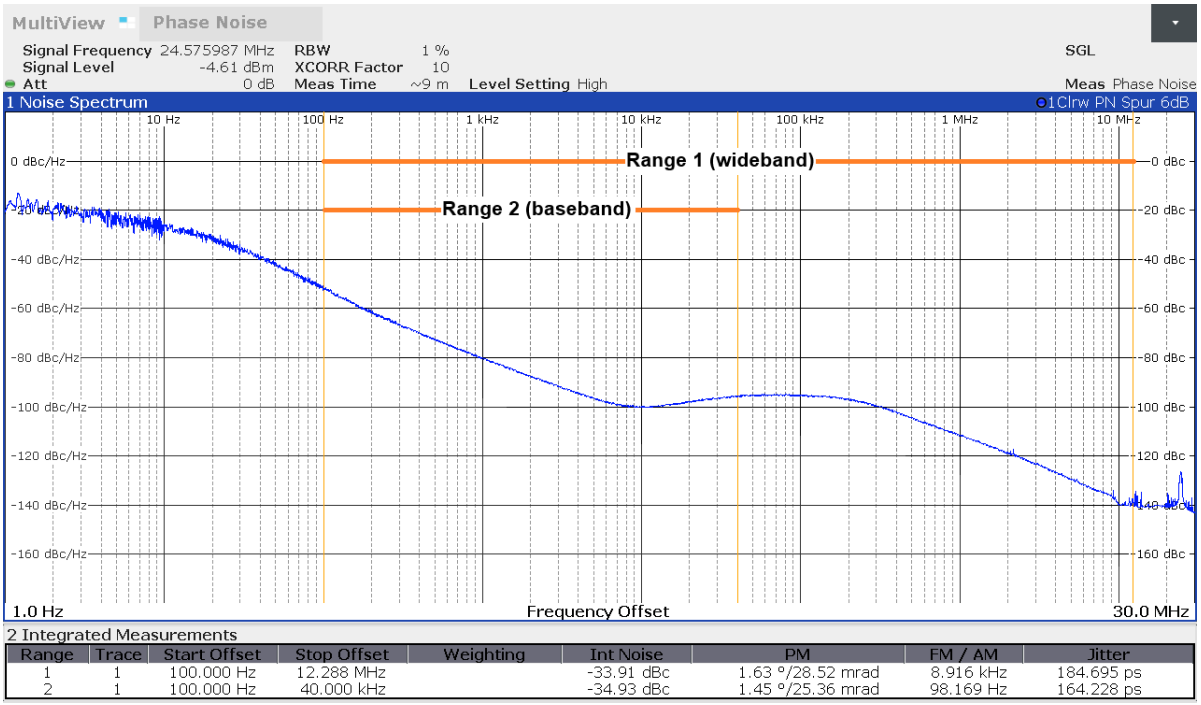


Figure 8-6. Phase Noise—Internal Oscillator

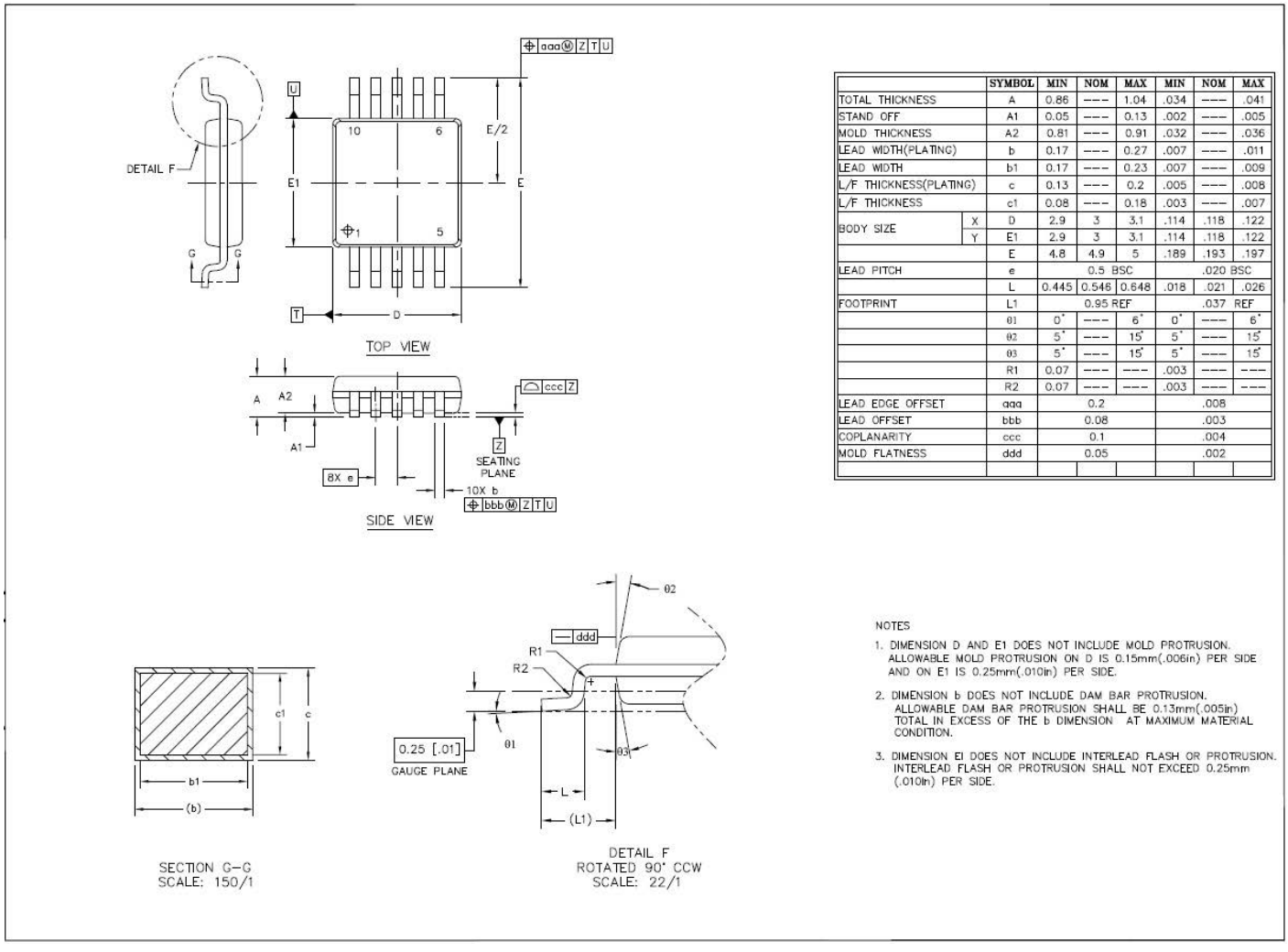
9 Thermal Characteristics

Table 9-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	TSSOP	Units
Junction-to-ambient thermal resistance	θ_{JA}	143.73	°C/W
Junction-to-board thermal resistance	θ_{JB}	184.21	°C/W
Junction-to-case (top) thermal resistance	θ_{JC}	194.48	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	126.27	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	14.25	°C/W

Notes:
- Natural convection at the maximum recommended operating temperature T_A (see Table 3-1)
- Four-layer, 2s2p PCB as specified by JESD51–9 and JESD51–11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51–12

10 Package Dimensions



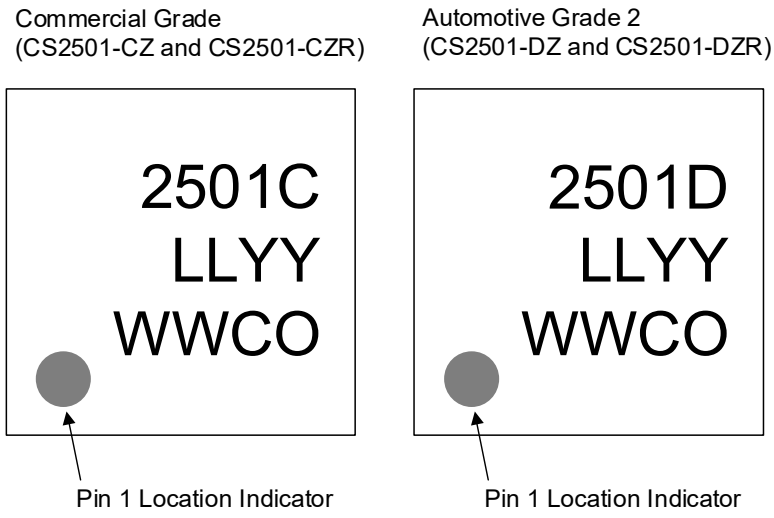
		SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS		A	0.86	---	1.04	.034	---	.041
STAND OFF		A1	0.05	---	0.13	.002	---	.005
MOLD THICKNESS		A2	0.81	---	0.91	.032	---	.036
LEAD WIDTH(PLATING)		b	0.17	---	0.27	.007	---	.011
LEAD WIDTH		b1	0.17	---	0.23	.007	---	.009
L/F THICKNESS(PLATING)		c	0.13	---	0.2	.005	---	.008
L/F THICKNESS		c1	0.08	---	0.18	.003	---	.007
BODY SIZE	X	D	2.9	3	3.1	.114	.118	.122
	Y	E1	2.9	3	3.1	.114	.118	.122
		E	4.8	4.9	5	.189	.193	.197
LEAD PITCH		e		0.5 BSC			.020 BSC	
		L	0.445	0.546	0.648	.018	.021	.026
FOOTPRINT		L1		0.95 REF			.037 REF	
		θ1	0°	---	6°	0°	---	6°
		θ2	5°	---	15°	5°	---	15°
		θ3	5°	---	15°	5°	---	15°
		R1	0.07	---	---	.003	---	---
		R2	0.07	---	---	.003	---	---
LEAD EDGE OFFSET		aaa		0.2			.008	
LEAD OFFSET		bbb		0.08			.003	
COPLANARITY		ccc		0.1			.004	
MOLD FLATNESS		ddd		0.05			.002	

NOTES

1. DIMENSION D AND E1 DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON D IS 0.15mm(.006in) PER SIDE AND ON E1 IS 0.25mm(.010in) PER SIDE.
2. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13mm(.005in) TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
3. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm (.010in) PER SIDE.

Figure 10-1. TSSOP Package Dimensions

11 Package Marking



Top Side Brand
Line 1: Part number
Line 2: Package mark
Line 3: Package mark

Package Mark Fields
LL = Lot sequence code
YY = Year of manufacture
WW = Work week of manufacture
CO = Country of origin

Figure 11-1. Package Marking

12 Ordering Information

Table 12-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number
CS2501	Clock Multiplier	10L-TSSOP	Yes	Commercial	–40 to +85°C	Tube	CS2501–CZ
						Tape and Reel	CS2501–CZR
				Automotive Grade 2	–40 to +105°C	Tube	CS2501–DZ
						Tape and Reel	CS2501–DZR

13 References

- NXP Semiconductors, UM10204 Rev. 7, October 2021, *I2C-Bus Specification and User Manual*, http://www.nxp.com

14 Revision History

Table 14-1. Revision History

Revision	Change
F1 APR 2025	• Initial production release
F2 JAN 2026	• Timing specifications updated to support I²C Fast Mode (Table 3-5) • Correction to package marking information, referencing the order-code suffixes –CZ, –CZR, –DZ, and –DZR (Section 11)

Important: Please check www.cirrus.com or with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.