Advanced Haptic Driver with Waveform Memory, Integrated DSP, Closed-Loop Algorithms, and Excursion Protection

Always on Haptic (AoH) With Ultra Low Latency Wakeup

- Wakeup from AoH Hibernate Mode in 5 ms (typ)
- 20 µA in AoH Hibernate Mode with RAM retention
- Fully-featured haptic firmware loaded from built-in ROM at power-on

Haptic Driver Features

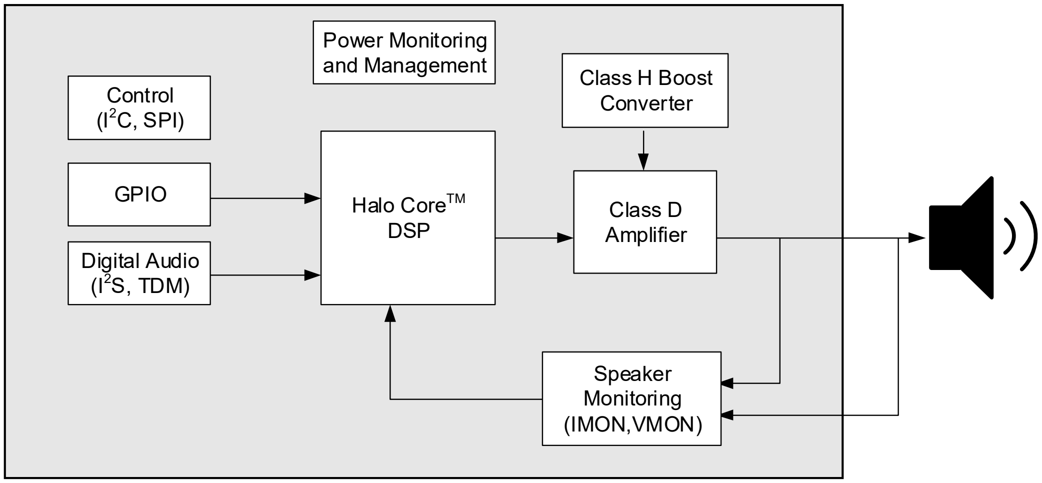
- 11 V maximum driver supply voltage for fast startup and braking
- Class D architecture with adaptive output stage reduces idle power consumption and switching losses
- Compatible with LRA impedances as low as 6 Ω
- Driver short-circuit protection

System Protection Features

- IC thermal self-protection against overtemperature
- System supply rail reactive brownout system protection
- Output current sensing via integrated current-monitoring sense resistor
- LRA protection
  - Coil resistance monitoring
  - DC input watchdog

Cirrus® Haptic Suite

- Excursion Protection for prevention of Linear Resonant Actuator (LRA) over-excursion events
- System Level Linear Resonant Actuator (LRA) resonance frequency calibration
- Advanced Closed Loop LRA control with SVC (Sensorless Velocity Control)
- Audio to Haptic for Gaming, Ringtones, and Alerts
- Dynamic F0 tracking
- Output voltage and current monitoring for software triggered haptic actuator impedance and resonance frequency reporting
- Pre-stored haptic waveforms triggerable by I^{2}C/GPI for gaming and user interface events
- Flexible haptic waveform generation
  - I^{2}C/GPI-triggered haptic effects rendered at measured resonant frequency for optimum efficiency
  - Haptic effects triggered by GPI for home button or side button switch replacement
  - Compensation in click waveform playback for actuator unit-to-unit variation in resonant frequency and coil resistance



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General Description

The CS40L27R integrates a self-contained haptic signal generator and driver optimized for high performance haptics in button-replacement type configurations and gaming applications with advanced close loop control. Hardware and digital signal processing are resonance-aware and designed specifically for optimal drive of highly-resonant linear resonant actuators (LRAs). There are banks of waveforms stored in ROM to match the LRA characteristics. The CS40L27R supports low power Standby and Hibernate Modes with fast wake upon GPI enable, always-available operation.

The device integrates a high-performance haptic driver, Halo Core™ DSP, and driver voltage boost converter. The integrated DSP executes all haptic algorithms. The device supports full haptics functionality at power-on with default settings that may be updated by the host. The CS40L27R supports hardware platforms with one GPI using the I²S interface.

The Class D driver features an advanced closed-loop architecture providing superior power supply rejection ratio (PSRR) and a complementary output stage. The digitally controlled boost converter boosts standard-voltage lithium-ion and lithium-polymer battery voltages up to 11 V. The elevated VBST supply generated by the boost converter allows the CS40L27R to deliver up to 7.9 Vpk into an 8 Ω load.

The CS40L27R includes self-protection and system-protection features. The boost and driver stages are protected against short circuits. IC overtemperature shutdown protection is provided in hardware. The supply voltage is continuously monitored. The boost converter and driver gains are automatically adjusted to preserve the supply voltage according to programmable voltage/current load-shedding set-points. The supply voltage protection adjustment of the driver is integrated with the IC thermal protection, ensuring seamless coordination of gain rollback if necessary.

The CS40L27R is available in a commercial-grade 0.4 mm pitch, 30-ball wafer level chip scale package for operation from –40° to +85°C See Section 4 for ordering information.

1 Pin Descriptions

These sections show pin assignments and describe pin functions.

1.1 WLCSP Package Drawing (Top View, Through Package)

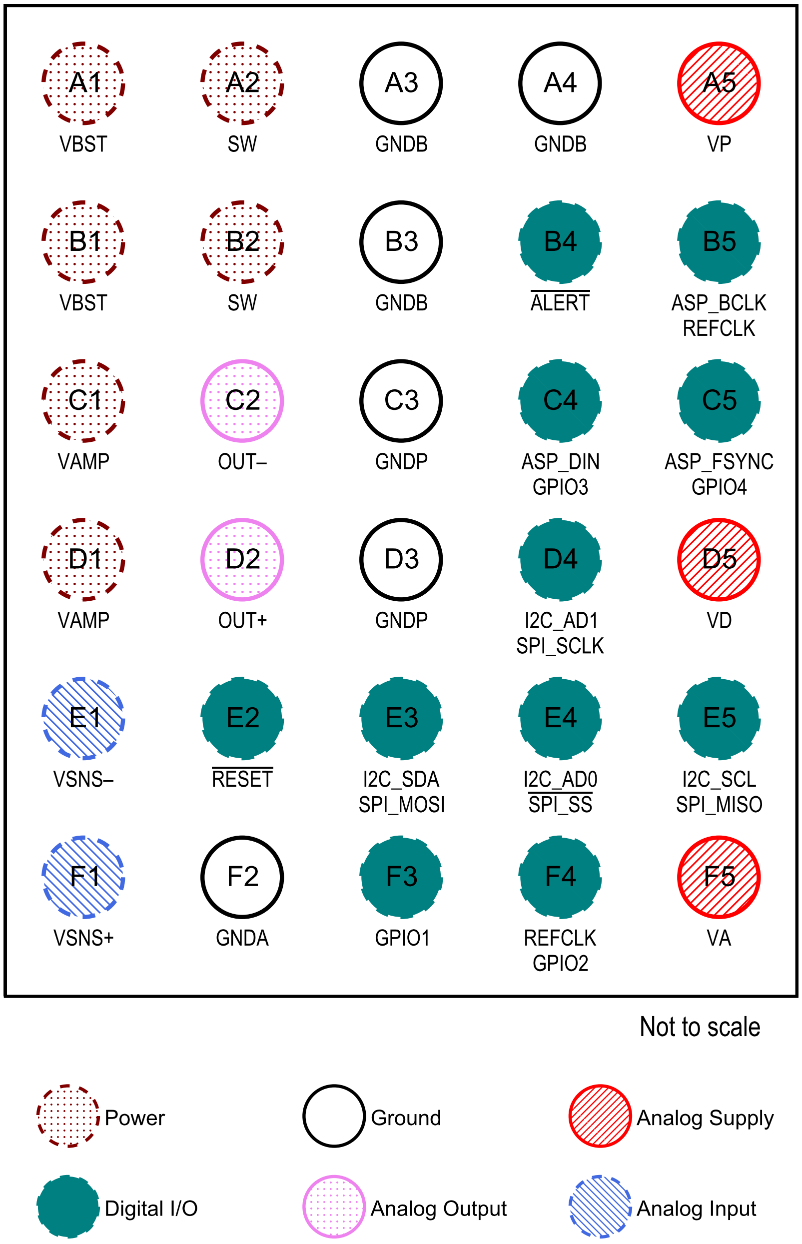


Figure 1-1. WLCSP 30-Ball Package Assignments (Top View, Through-Package)

1.2 Pin Descriptions

Table 1-1. WLCSP Pin Descriptions

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
ALERT	B4	VD	O	**Alert.** Active-low, open-drain interrupt output.	Weak pull-down	Weak pull-down
ASP_BCLK/ REFCLK	B5	VD	I/O	**Serial Port Clock.** Serial interface bit clock. **Reference Clock.** Reference clock input (if accurate clocking mode is required).	Weak pull-down	Weak pull-down
ASP_DIN/GPIO3	C4	VD	I/O	**Serial Port Data Input.** Serial interface data input. **General Purpose Input/Output Pin.** Programmable GPIO3. This input is wake capable in AoH Standby and AoH Hibernate.	Weak pull-down	Weak pull-down
ASP_FSYNC/ GPIO4	C5	VD	I/O	**Serial Port Frame Sync Clock.** Serial interface sync input. **General Purpose Input/Output Pin.** Programmable GPIO4. This input is wake capable in AoH Standby and AoH Hibernate.	Weak pull-down	Weak pull-down
GNDA	F2	—	—	**Analog and Digital Ground.** Ground reference for the analog and digital portions of the IC.	—	—
GNDB	A3, A4, B3	—	—	**Boost Converter Ground.** Ground reference for the internal boost converter.	—	—
GNDP	C3, D3	—	—	**Power Ground.** Ground reference for the boost converter and Class D amplifier's output stage.	—	—
GPIO1	F3	VD	I/O	**General Purpose Input/Output Pin.** Programmable GPIO, wake capable in AoH Standby and AoH Hibernate. Must be grounded if not used.	—	Hi-Z
I2C_AD0/SPI_SS	E4	VD	I	**I^{2}C Slave Device Address Select 0.** Used with I2C_AD1, connected to VD or GNDA, to select between four possible addresses. **SPI Control-Port Slave Select.** Active-low SPI Slave Select input.	—	—
I2C_AD1/ SPI_SCLK	D4	VD	I	**I^{2}C Slave Device Address Select 1.** Used with I2C_AD0, connected to VD or GNDA, to select between four possible addresses. **SPI Control-Port Clock.** SPI clock input.	—	—
I2C_SCL/ SPI_MISO	E5	VD	I/O	**I^{2}C Control-Port Clock.** Clock input for the I^{2}C interface. **SPI Control-Port Master In Slave Out.** SPI data output.	—	Hi-Z
I2C_SDA/ SPI_MOSI	E3	VD	I/O	**I^{2}C Control-Port Data.** Data input/output for the I^{2}C interface. **SPI Control-Port Master Out Slave In.** SPI data input.	—	Hi-Z
OUT+	D2	VAMP	O	**Differential Haptic Output.** Internal Class D amplifier output.	—	—
OUT–	C2	VAMP	O	**Differential Haptic Output.** Internal Class D amplifier output.	—	—
REFCLK/GPIO2	F4	VD	I/O	**Alternate Reference Clock.** Reference clock input (if accurate clocking mode is required). **General Purpose Input/Output Pin.** Programmable GPIO2. This input is wake capable in AoH Standby and AoH Hibernate. Must be grounded if not used.	—	—
RESET	E2	VD	I	**Reset.** If this pin is driven low, the device enters a low power mode, all register values are set to their default settings, and DSP volatile memory (RAM) contents are invalidated.	—	—
SW	A2, B2	VBST	I	**Boost Switch.** Input to internal boost FETs. Connect to L$_{BST}$ inductor.	—	—
VA	F5	—	I	**Analog Power.** Power supply for internal analog and digital sections.	—	—
VAMP	C1, D1	—	I	**Driver Power.** Power supply for the Class D amplifier's output stage. Must be connected to VBST externally.	—	—
VBST	A1, B1	—	O	**Boosted Supply from Boost Converter.** Internal boost converter output which must be connected to VAMP externally.	—	—
VD	D5	—	I	**Digital I/O Power.** Power supply for the digital core and digital I/O circuitry on the CS40L27R.	—	—

Table 1-1. WLCSP Pin Descriptions *(Cont.)*

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
VP	A5	—	I	**Boost Converter Power.** Power supply for the boost converter and portions of the Class D amplifier.	—	—
VSNS+	F1	VAMP	I	**Voltage Sense Input.** Sense voltage input for monitoring OUT+.	—	—
VSNS–	E1	VAMP	I	**Voltage Sense Input.** Sense voltage input for monitoring OUT-.	—	—

2 Typical Connection Diagrams

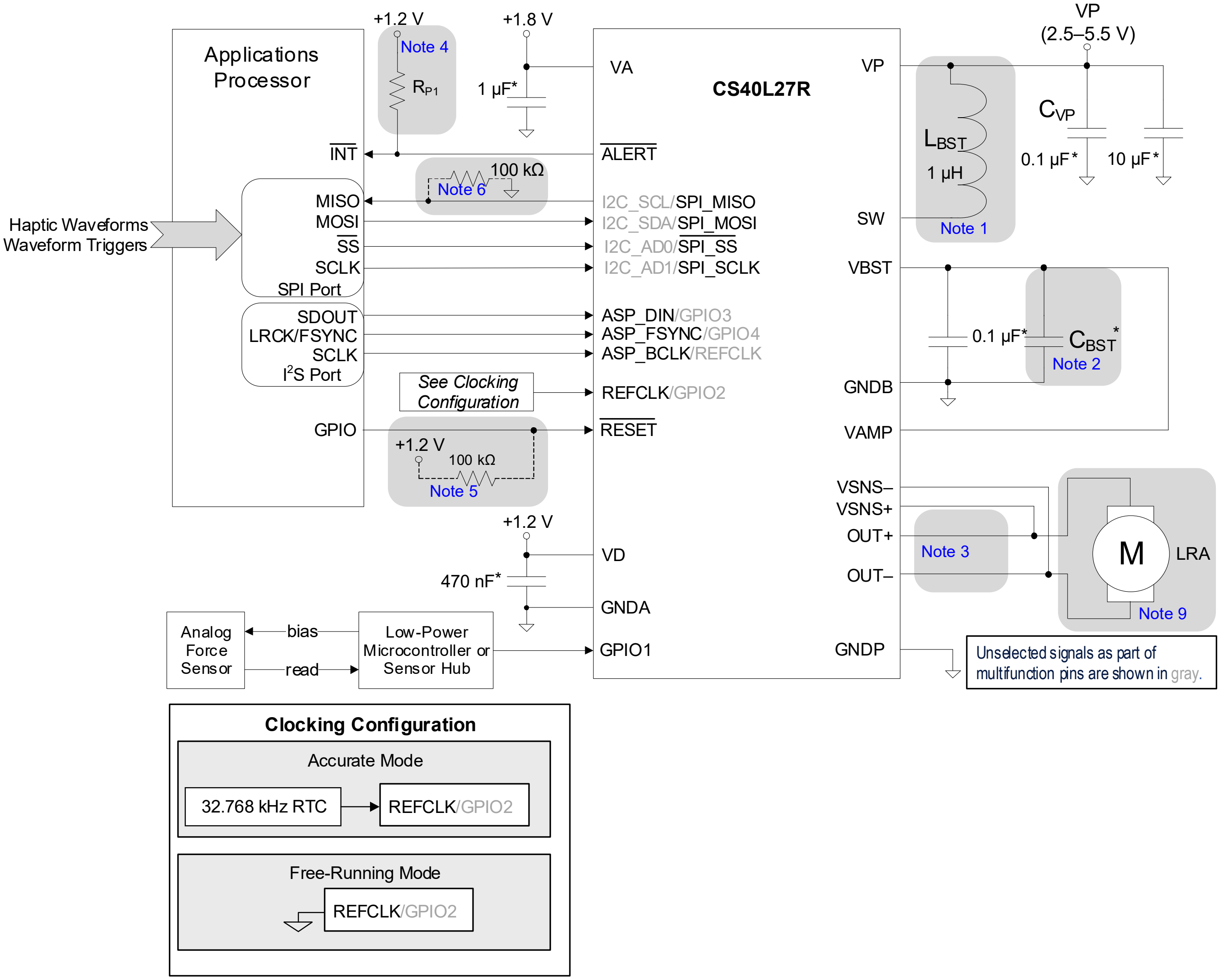


Figure 2-1. Typical Connection Diagram—SPI with GPI and I²S Support

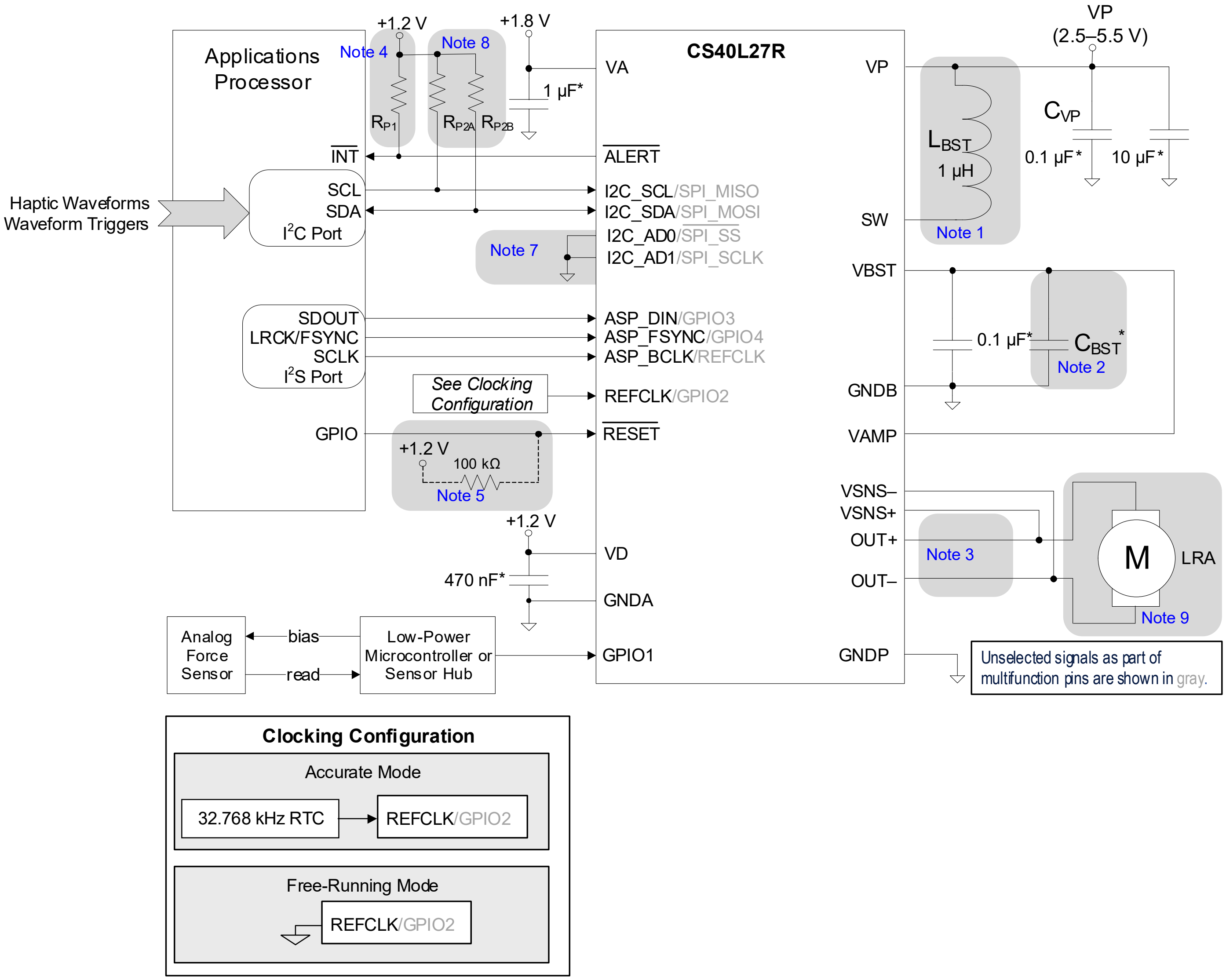


Figure 2-2. Typical Connection Diagram—I²C Interface with GPI and I²S Support

Notes referenced in the typical connection diagrams:

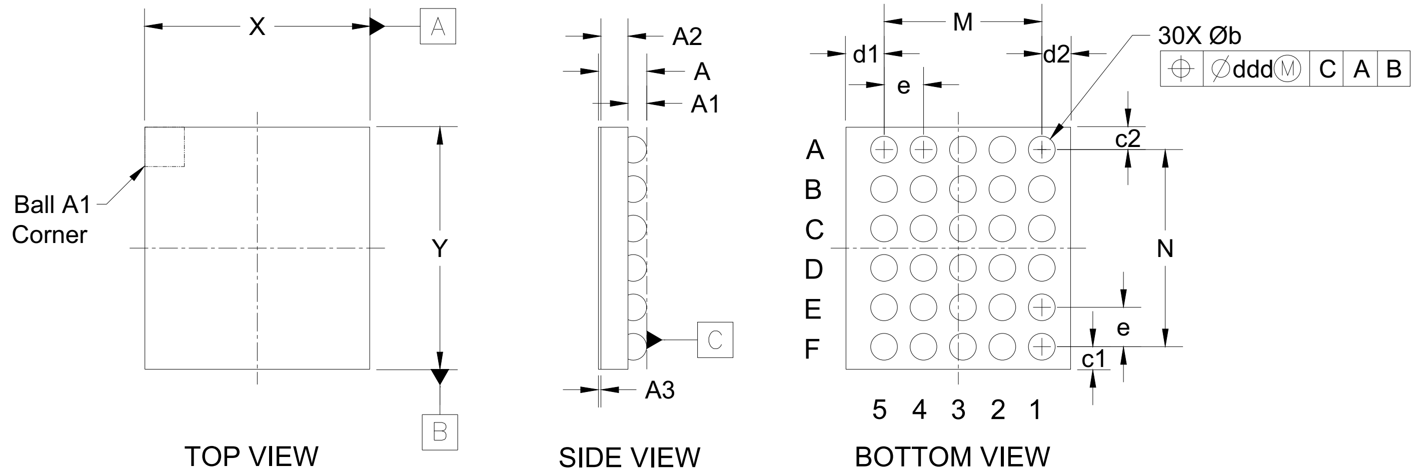
1. The L_{BST} inductor must not derate to an inductance of less than 0.7 µH during device operation to maintain proper loop stability. The inductor saturation current rating must not be less than the boost converter current limit.
2. The C_{BST} capacitor must not derate to a combined capacitance value of less than 3.6 µF with 11.0 VDC applied. The maximum supported derated capacitance is 50 µF. The WLCSP package requires a common connection among all VBST and VAMP balls. All VBST balls/pins must be connected together on the PCB and connected to the capacitors shown.
3. Location of optional EMI suppressor capacitors between OUT± and GNDP (typically 470 pF) which may be used in addition to the edge-rate control of the CS40L27R, depending on the application requirements. It is recommended that the value of these components not exceed 2 nF, as higher capacitances increase switching losses.
4. The value for R_{P1} on the ALERT pin may be calculated based on the minimum ALERT pull-down resistance, the minimum level of the 1.2 Vsupply, and the maximum VIH of the host input driven by the ALERT pin.
5. An optional, external pull-up resistor toVD (or pull-down to GND) is only required when the applications processor GPIO is unable to drive RESET at all times while the CS40L27R is powered.
6. An external pull-down resistor is required on SPI_MISO in SPI applications with more than one slave device.

7. The CS40L27R supports four I^2C device address options selected by connecting I2C_AD0 and I2C_AD1 directly to VD or GND (no pull-up or pull-down resistors), as close to the CS40L27R device as possible for correct operation. While configured as shown here, the device responds to an address of 0x80 for writes and 0x81 for reads. The I^2C address is latched at hardware reset or power-on reset.
8. Minimum $R_{P2A/B}$ values may be determined from the maximum VD level, the minimum sink current strength of their respective output, and the maximum low-level output voltage (VOL). Maximum $R_{P2A/B}$ values may be determined by how fast their associated signals must transition, taking into account load capacitance.
9. The CS40L27R is intended for driving Linear Resonant Actuator (LRA) devices. The CS40L27R is compatible with multiple types of LRAs with an impedance as low as 6 Ω and a resonant frequency in 50–561 Hz range.

General notes and recommendations:

- Fig. 2-1–Fig. 2-2 are examples intended to describe the connectivity of each functional block within the CS40L27R, and do not limit all possible use cases.
- The CS40L27R requires a 32.768 kHz clock only if running in Accurate Mode. Connect the 32.768 kHz clock to the ASP_BCLK/REFCLK or REFCLK/GPIO2 inputs.
- If REFCLK/GPIO2 is used as a playback trigger source, connect the 32.768 kHz clock to the ASP_BCLK/REFCLK input. Note that driving the 32.768 kHz clock into the ASP_BCLK/REFCLK input precludes the use of the auxiliary serial port for I^2S.
- All external passive component values listed are nominal values.
- Use low ESR, X7R/X5R capacitors for capacitors denoted with *.

3 Package Dimensions



Dimension	**Millimeters**		
	Minimum	**Nominal**	**Maximum**
A	0.46000	0.49000	0.52000
A1	0.17500	0.19000	0.20500
A2	0.26000	0.27500	0.29000
A3	REF	0.02500	REF
b	0.24000	0.27000	0.30000
c1	0.20269	0.22769	0.25269
c2	0.20309	0.22809	0.25309
d1	0.36253	0.38753	0.41253
d2	0.26595	0.29095	0.31595
e	BSC	0.40000	BSC
M	BSC	1.60000	BSC
N	BSC	2.00000	BSC
X	2.25348	2.27848	2.30348
Y	2.43078	2.45578	2.48078
ddd=0.015			

Notes: Controlling dimension is millimeters.
Dimensioning and tolerances per ASME Y 14.5-2009. The Ball A1 position indicator is for illustration purposes only. Dimension "b" applies to the solder sphere diameter and is measured at the maximum solder sphere diameter, parallel to primary Datum C.
X/Y Tolerances can apply to an individual edge increasing or decreasing by 25um.

Figure 3-1. WLCSP Package Dimensions

4 Ordering Information

Table 4-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number
CS40L27R	Boosted Haptics Driver with integrated DSP supporting one GPI + I^2S	30-ball WLCSP	Yes	Commercial	–40°C to +85°C	Tape and Reel	CS40L27R-CWZR

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.

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