CS40L51/52/53

Advanced Haptic Driver with Integrated Boost, Waveform Memory, and Closed-Loop Algorithms

Features

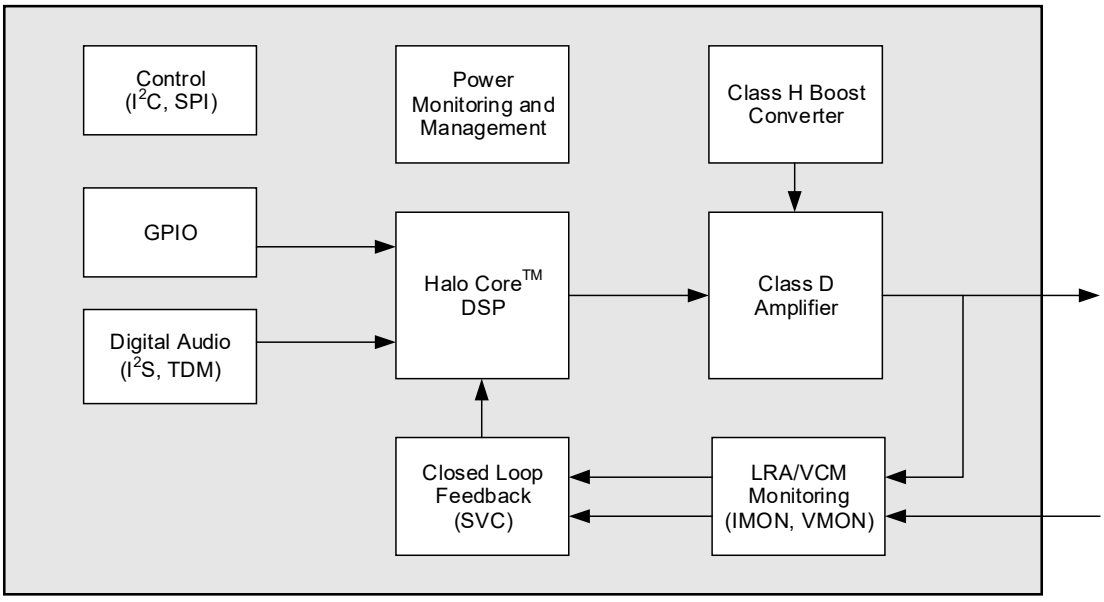
- Closed-loop hardware and algorithms (SVC)
  - Fast startup and braking for crisp/strong haptic feedback
  - Extended actuator bandwidth supports textured effects
  - Ensures consistent performance across actuator manufacturing variations, temperature, and aging
  - Removes need for factory production-line calibration
- Integrated 15 V Class H boost converter
  - Provides high output power for fast closed-loop response
  - Enables consistent performance across battery conditions
  - Supports multiple actuators driven in parallel (3 Ω minimum)
- Optimized low-latency and low-power hardware architecture
  - Ultrafast wake-to-haptics enables imperceptible latency between touch/press events and haptic feedback
  - Low-power Hibernate State with memory retention
  - ROM/RAM-stored waveforms triggered by I²C/SPI/GPIO
- Haptics waveform memory
  - Simplifies system integration and reduces latency
  - Enables software-configurable vehicles
  - Stores PWLE and PCM waveforms in RAM
- AEC Q100 Grade-2 qualified for automotive applications, operating temperature –40 to 105ºC

Specifications

- 13.8 V_{PK} output into 8 Ω load
- 3.0 V–15.0 V input supply
- 15 V Class H boost converter
- Ultra-low power
  - 3.6 µA current consumption in Reset State
  - 12 µA current consumption in Hibernate State
- Ultra-low latency
  - 4.6 ms wake-to-haptics from Reset State
  - 3.3 ms wake-to-haptics from Hibernate State
- Support for 1.8 V and 3.3 V digital input/output
- 34-pin wettable-flank QFN package, 4 × 4.5 mm, 0.4 mm pitch

Applications

- Virtual buttons/smart surfaces
- Displays and interface panels
- Steering-wheel switches
- HVAC control panel
- Infotainment control panel
- Door/window/seat controls



Important Notice: No license to any intellectual property right is included with this component, and certain uses or product designs, including certain haptics-related uses or haptics-system designs, may require an intellectual property license from one or more third parties.

Advanced Product Information

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Haptic Driver Features

- Always on with ultra-low latency wakeup
  - 4.6 ms wake-to-haptics from Reset State
  - 3.3 ms wake-to-haptics from Hibernate State
- Class D architecture minimizes idle power consumption and switching losses
- 15 V driver supply voltage (maximum) from internal boost converter for fast startup and braking
- High performance with internal or external amplifier supply
  - 13.8 V_{PK} output into 8 Ω load
- Compatible with LRA/VCM impedances as low as 3 Ω
- Configurable amplifier output edge rate to reduce EMI

Monitoring Features

- Driver current monitoring via integrated sense circuit
- Driver voltage sensing via dedicated pins (VMON_N/VMON_P)
- Current and voltage monitor data on I²S or TDM interface

Efficiency and Power Consumption

- Internal boost operation from 3.0 V–15 V supply
- 89% overall efficiency (boost + amplifier) at 1 W output (8 Ω load, 5 V external supply)
- 3.6 µA current consumption in reset
- 12 µA current consumption in hibernate (RAM contents retained, monitoring for I²C or activity on GPIO/SPI pins)

Cirrus Logic Haptic Suite

- System-level LRA/VCM actuator resonance frequency calibration
- Runtime haptics enables dynamic haptic-waveform generation with minimized delays
- Dynamic F_0 and Re_{DC} tracking
- Driver voltage and current monitoring for software-triggered haptic actuator impedance and resonance frequency reporting
- Prestored (ROM or RAM) haptic waveforms triggerable by I²C/GPIO for user-interface events
- Flexible haptic-waveform generation
- I²C/GPIO-triggered haptic effects rendered at measured resonant frequency for optimum efficiency
- Haptic effects triggered by GPIO for virtual buttons on smart surfaces
- Compensation in click waveform playback for actuator unit-to-unit variation in resonant frequency and coil resistance

Digital Boost Converter Features

- Programmable boost output voltage up to 15 V
- Advanced boost Class-H engine tracks audio envelope to maximize power efficiency
- Programmable boost inductor current limits up to 4 A
- Integrated boost and rectification FETs
- High-bandwidth digital control loop
- Synchronous rectification in Active Mode
- Discontinuous Conduction Mode (DCM) for improved efficiency during low-power quiescent operation

System Hardware Protection Features

- IC thermal self-protection
- Boost/amplifier battery-brownout protection engine (BPE)
- Boost converter overvoltage/undervoltage protection
- VDD_B/VBST undervoltage lockout (UVLO)
- Boost/amplifier short-circuit protection
- LRA/VCM protection
  - Coil resistance monitoring
  - Coil short-circuit detection
  - DC input watchdog

Clocking and Data Interface Features

- Clocks generated from audio serial port using internal phase-locked loop (PLL)
- Open-loop PLL mode for autonomous waveform playback with no external clock required
- Audio/haptic data serial port (ASP)
  - Sample rates 8, 16, and 48 kHz
  - I²S and TDM interface formats
  - Configurable audio/data packet formatting
  - Flexible clock rates and sample depth
  - Tristate data output pin supports multi-device bus sharing
- I²C or SPI control port
  - I²C High Speed, Fast-mode and Fast-mode Plus (Fm+) modes
  - Up to eight unique I²C target address instances
  - Supports I²C broadcast address to enable simultaneous code download to multiple devices
  - SPI operation up to 17 MHz
- Multidevice synchronization and communication of device power-up and protection events
- Programmable and maskable interrupts with hardware interrupt pin (push-pull/open-drain) and software polling support
- GPIO pins with multiple features
  - Optional external reference clock
  - Device power up/down transitions
  - Hardware trigger for buzz waveform playback
  - Configurable by I²C or SPI interface or by DSP core

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General Description

The CS40L5x integrates a self-contained haptic signal generator and driver, optimized for high-definition haptic smart surfaces, steering wheels, interactive displays, and car-seat applications. The hardware and the digital signal processing are resonance-aware and designed specifically for optimal drive of highly resonant linear resonant actuators (LRAs) and voice coil motors (VCMs).

The CS40L5x incorporates a 130 MIPS Halo Core™ DSP, which is used to execute the haptic-control algorithms. Waveforms are stored in ROM or RAM to match the LRA/VCM characteristics. Ultra-low power reset and hibernate states enable always-on operation with fast wake-up via GPIO. ROM-defined waveforms can be output within 4.6 ms of wake up from reset. Additional waveforms can be downloaded to RAM during run time; these are retained in the low-power Hibernate State and can be output within 3.3 ms of wake-up from hibernate. Runtime haptic-waveform synthesis allows application-specific waveforms to be generated using PCM or PWLE-coded parameters.

The CS40L51/52/53 devices support different algorithm features:

Feature	CS40L51	CS40L52	CS40L53
Calibration (R_E and F_0)	Yes	Yes	Yes
Click compensation (R_E and F_0)	Yes	Yes	Yes
Haptics synthesizer	Yes	Yes	Yes
Runtime haptics (RTH)	Yes	Yes	Yes
Load diagnostics	Yes	Yes	—
Closed-loop algorithms (SVC)	Yes	Yes	—
Audio to haptics (A2H)	Yes	—	—
Live F_0 tracking (LF0T)	Yes	—	—
Active vibration compensation	Yes	—	—
Wavetable sample rate	8 kHz, 24 kHz	8 kHz	8 kHz

The Class D amplifier supports supply voltages up to 15.0 V. The amplifier incorporates an advanced closed-loop architecture and a differential output stage. The digitally controlled boost converter supports Class-H tracking and generates up to 15 V output from typical system supply rails (e.g., 5 V or 12 V). The CS40L5x delivers up to 13.8 V_{PK} into an 8 Ω load.

The CS40L5x includes self-protection and system-protection features. The boost and driver stages are protected against short circuits; IC over-temperature shutdown protection is provided in hardware. The input voltage is continuously monitored. The boost converter and driver gain are automatically adjusted for the supply voltage according to programmable voltage/current thresholds; the adjustment of the driver is integrated with the IC thermal protection, ensuring seamless gain adjustment if necessary.

The CS40L5x is available in a commercial-grade 0.4 mm pitch, 34-pin wettable-flank QFN package for operation from –40° to +105°C. The CS40L5x is AEC-Q100 Grade 2 qualified for automotive applications.

See Section 6 for ordering information.

Table of Contents

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1 Pin Assignments and Descriptions

1.1 34-Pin QFN (Top View, Through-Package)

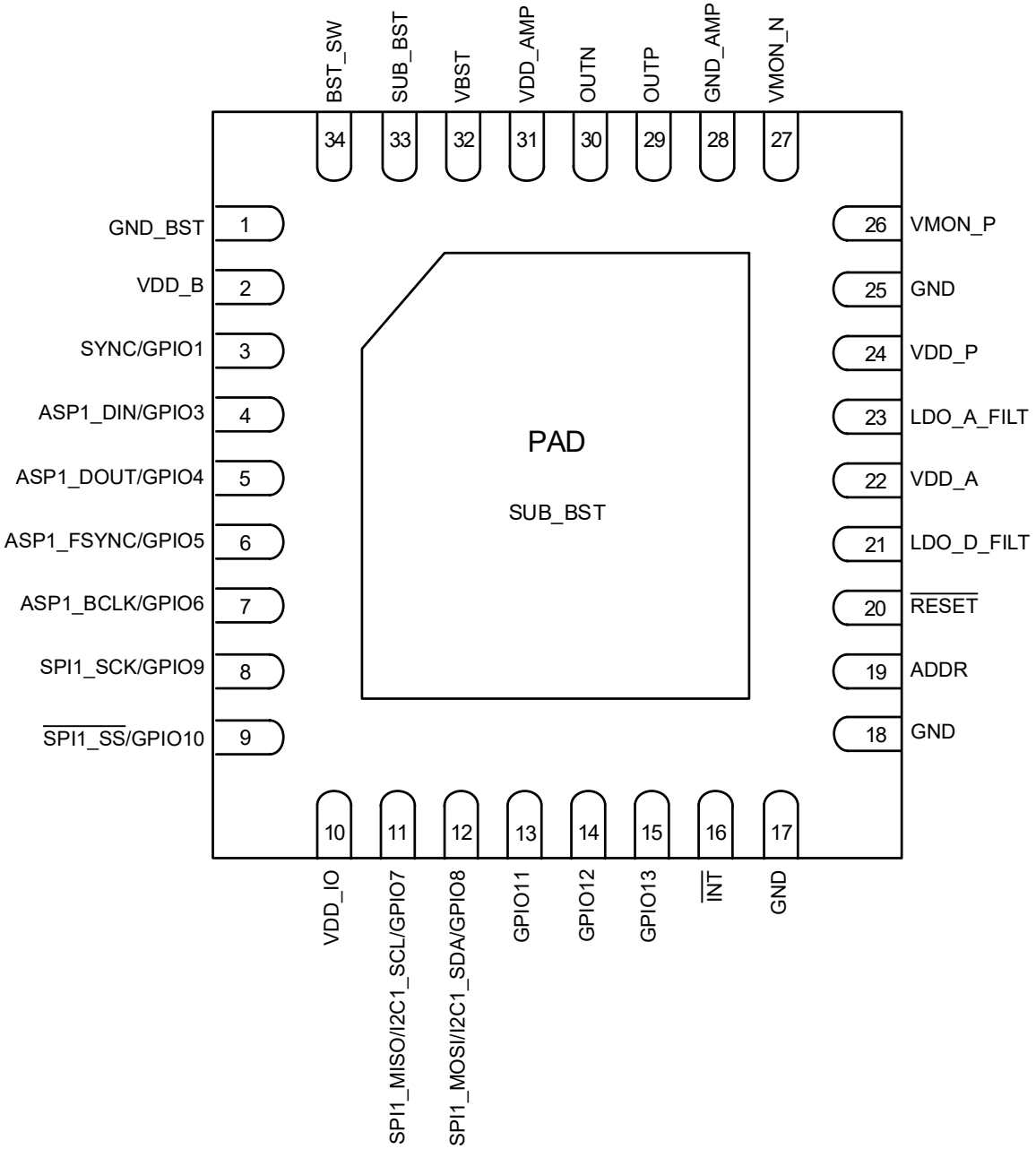

Figure 1-1. QFN 34-pin diagram (Top View, Through Package)

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1.2 QFN Pin Descriptions

Table 1-1. QFN Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description	Internal Connection	State at Reset
				Digital I/O		
ASP1_BCLK/GPIO6	7	VDD_IO	I/O	**Audio Serial Port Bit Clock.** Serial shift clock for ASP interface. Optional clock reference for PLL. **GPIO6.** General-purpose input/output.	Programmable (pull-up, pull-down)	Input, passive pull down
ASP1_DIN/GPIO3	4	VDD_IO	I/O	**Audio Serial Port Data Input.** Serial data input for ASP interface. **GPIO3.** General-purpose input/output.	Programmable (pull-up, pull-down)	Input, passive pull down
ASP1_DOUT/GPIO4	5	VDD_IO	I/O	**Audio Serial Port Data Output.** Serial data output for ASP interface. **GPIO4.** General-purpose input/output.	Programmable (pull-up, pull-down)	Output, passive pull down
ASP1_FSYNC/GPIO5	6	VDD_IO	I/O	**Audio Serial Port Frame Sync.** Frame sync for ASP interface. Optional clock source for PLL. **GPIO5.** General-purpose input/output.	Programmable (pull-up, pull-down)	Input, passive pull down
GPIO13	15	VDD_IO	I/O	**GPIO13.** General-purpose input/output. **MCLK.** External clock reference input. **WAKE.** External trigger to wake from Hibernate State.	Programmable (pull-up, pull-down)	Input, Hi-Z
$\overline{\text{INT}}$	16	VDD_IO	I/O	**Interrupt.** Programmable open-drain interrupt output.	Programmable (pull-up, pull-down)	Output, Hi-Z
$\overline{\text{RESET}}$	20	See Note [1]	I	**Reset.** Active-low reset input.	—	Input
SPI1_MISO/I2C1_SCL/ GPIO7	11	VDD_IO	I/O	**SPI Control-Port Master In Slave Out.** SPI data input. **I²C Control-Port Clock.** Clock input for the I²C interface. **GPIO7.** General-purpose input/output. **WAKE.** External trigger to wake from Hibernate State.	Programmable (pull-up, pull-down)	Input, Hi-Z
SPI1_MOSI/I2C1_SDA/ GPIO8	12	VDD_IO	I/O	**SPI Control-Port Master Out Slave In.** SPI data output. **I²C Control-Port Data.** Data input/output for the I²C interface. **GPIO8.** General-purpose input/output. **WAKE.** External trigger to wake from Hibernate State.	Programmable (pull-up, pull-down)	Output, Hi-Z
SPI1_SCK/GPIO9	8	VDD_IO	I/O	**SPI Control-Port Clock.** Clock input for the SPI interface. **GPIO9.** General-purpose output.	Programmable (pull-up, pull-down)	Input, passive pull down
$\overline{\text{SPI1\_SS}}$/GPIO10	9	VDD_IO	I/O	**SPI Control-Port Slave Select.** Active-low Slave Select input for the SPI interface. **GPIO10.** General-purpose input/output.	Programmable (pull-up, pull-down)	Input, Hi-Z
GPIO11	13	VDD_IO	I/O	**GPIO11.** General-purpose input/output. **MCLK.** External clock reference input. **WAKE.** External trigger to wake from Hibernate State.	Programmable (pull-up, pull-down)	Input, Hi-Z
GPIO12	14	VDD_IO	I/O	**GPIO12.** General-purpose input/output. **WAKE.** External trigger to wake from Hibernate State.	Programmable (pull-up, pull-down)	Input, Hi-Z
SYNC/GPIO1	3	VDD_IO	I/O	**Multidevice Synchronization.** Serial data bus connecting devices in multi-channel applications. **GPIO1.** General-purpose input/output. **MCLK.** External clock reference input.	Programmable (pull-up, pull-down)	Input, passive pull down
				Analog I/O		
ADDR	19	VDD_A	I	**I²C Address Input.** Address pin for I²C Target address. Latched on POR or hard reset.	—	—
BST_SW	34	—	I	**Boost Switch.** Input to internal boost FETs.	—	—
LDO_A_FILT	23	VDD_P	O	**LDO_A Output.** Decoupling point for analog supply (if powered from internal LDO).	—	—

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Table 1-1. QFN Pin Descriptions *(Cont.)*

Pin Name	Pin #	Power Supply	I/O	Description	Internal Connection	State at Reset
LDO_D_FILT	21	VDD_A	O	**LDO_D Output.** Decoupling point for digital supply, powered from LDO_D.	—	—
OUTN	30	VDD_AMP	O	**Differential Output.** Internal Class D amplifier output.	—	—
OUTP	29	VDD_AMP	O	**Differential Output.** Internal Class D amplifier output.	—	—
VBST	32	—	O	**Boosted Supply from Boost Converter.** Internal boost converter output.	—	—
VMON_N	27	VDD_AMP	I	**Output Monitor.** Voltage-sense input for OUTN. Must be connected to OUTN via 4.99 kΩ (1%) resistor.	—	—
VMON_P	26	VDD_AMP	I	**Output Monitor.** Voltage-sense input for OUTP. Must be connected to OUTP via 4.99 kΩ (1%) resistor.	—	—
				Power Supplies		
GND	17, 18, 25	—	—	**Note: Analog and Digital Ground.** Ground return for the analog and digital functional blocks throughout the device.	—	—
GND_AMP	28	—	—	**Power Ground.** Ground reference for the Class D amplifier output stage.	—	—
GND_BST	1	—	—	**Boost Converter Power Ground.** Ground reference for the boost converter.	—	—
SUB_BST	33, PAD	—	—	**Boost Substrate Ground and Thermal Pad.** The thermal pad must be connected to ground.	—	—
VDD_A	22	—	I	**Analog Supply.** Power supply for the internal analog circuits. Also powers digital circuits via internal regulator.	—	—
VDD_P	24	—	I	**System Supply.** Power supply for always-on (Hibernate) circuits. Also powers the LDO_A regulator, which can be used to generate the VDD_A supply.	—	—
VDD_AMP	31	—	I	**Amplifier Supply.** Power supply for the Class D amplifier.	—	—
VDD_B	2	—	I	**Boost Supply.** Power supply for boost converter. (Note this is primarily a monitor pin; the boost current is conducted via the inductor to BST_SW.)	—	—
VDD_IO	10	—	I	**Digital I/O Supply.** Power supply for digital input/output.	—	—

1.5 V-tolerant input, supply-independent

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2 Typical Connection Diagram

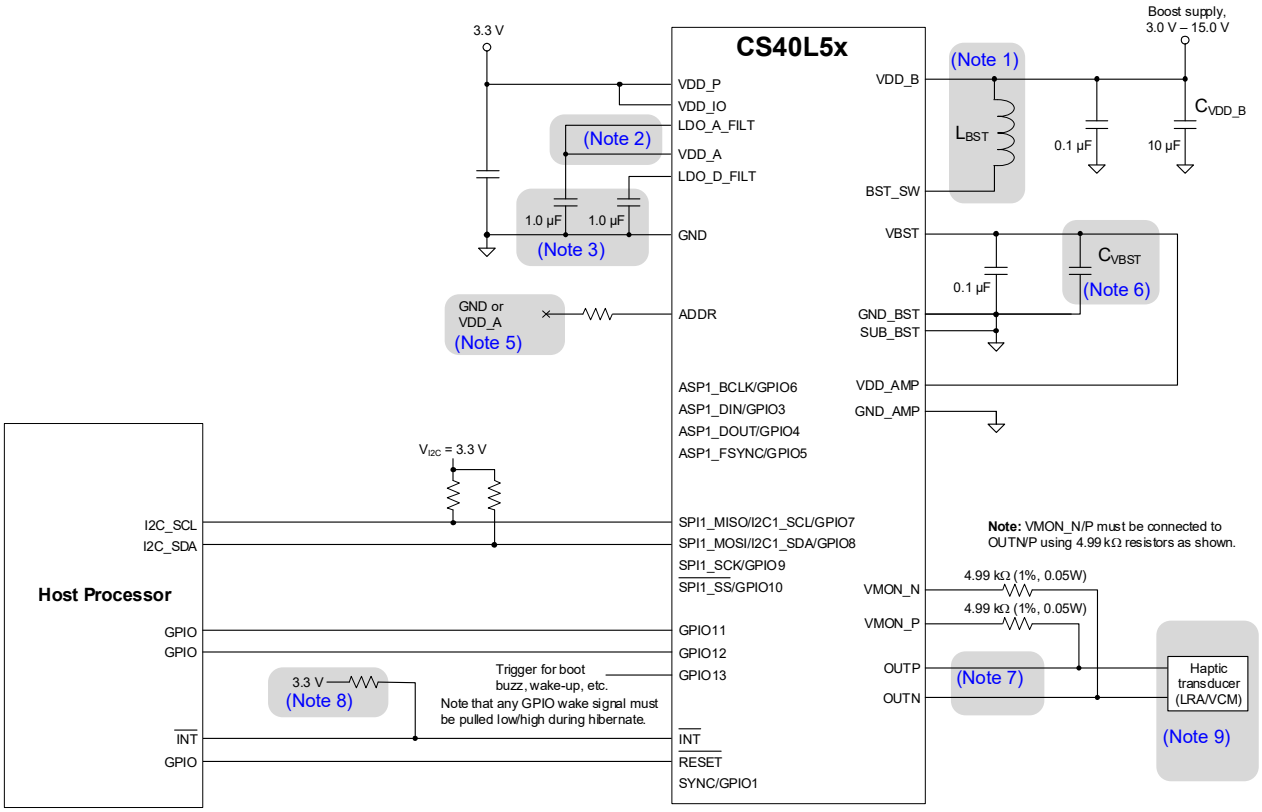

Figure 2-1. Typical configuration with internal boost power source

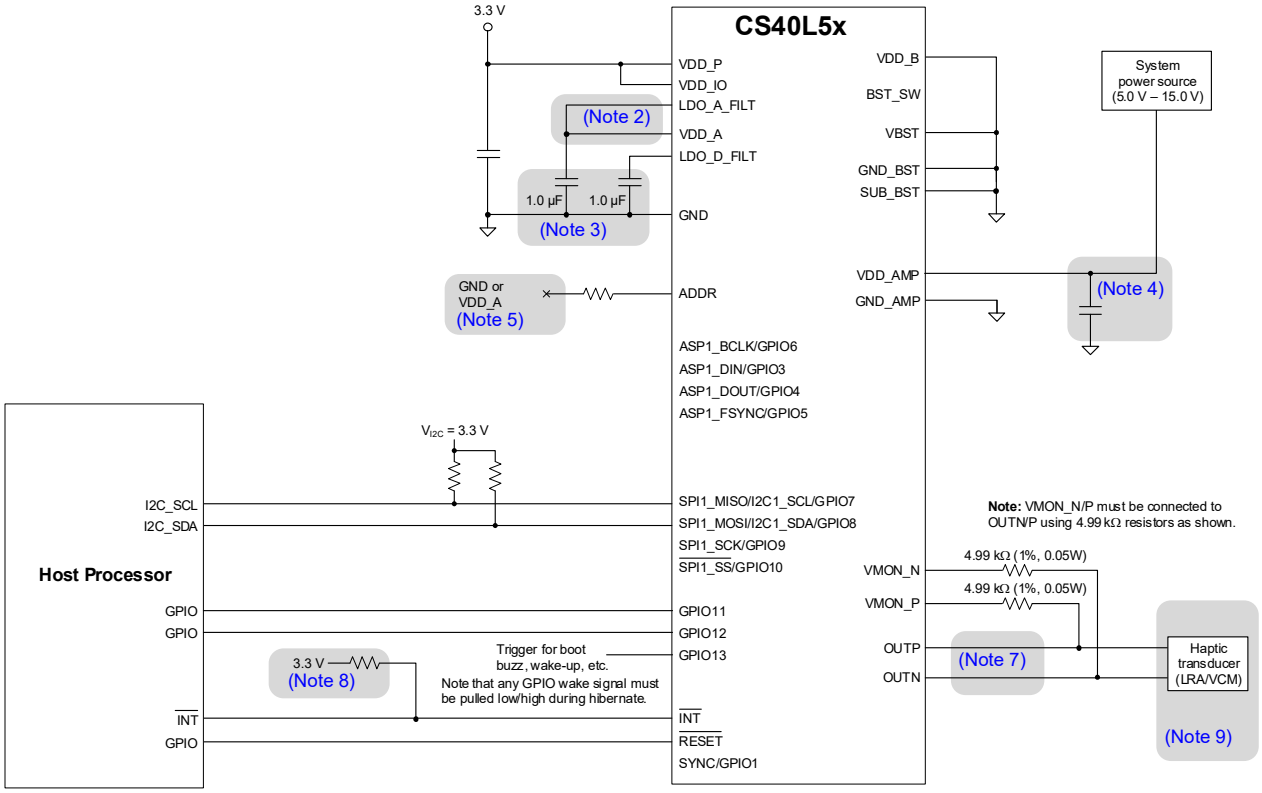

Figure 2-2. Typical configuration with external amplifier power source

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Notes referenced in the typical connection diagrams:

1. The L_{BST} inductor must not derate to a value less than 0.5 µH. Inductance of 1.0 µH is recommended for typical applications.
2. In the configuration shown, the LDO_A regulator is used to generate the analog supply. The VDD_A supply pin is connected to the LDO output, LDO_A_FILT.
3. The LDO_A_FILT capacitor must not de-rate to a value less than 500 nF at 1.8 V. The LDO_D_FILT capacitor must not de-rate to a value less than 390 nF at 1.25 V.
4. The C_{VDD_AMP} capacitor must not derate to a value less than 2 µF at 15 V.
5. The I²C device address are configured using a resistor connected between the ADDR pin and GND, or else between the ADDR pin and VDD_A. The capacitive loading on the ADDR pin must not exceed 100 pF.
6. The C_{VBST} capacitor must not derate to a value less than 2 µF at 15 V.
7. Optional EMI-suppression capacitors between OUTx and GND_AMP may be used, depending on the application requirements. The capacitance should not exceed 470 pF, as higher capacitance increases switching losses.
8. In the configuration shown, the CS40L5x $\overline{\text{INT}}$ pin is configured as an open-drain output and an external pull-up resistor (e.g., 100 kΩ) to VDD_IO is required.
9. When using a simulated load of 8 Ω + 33 µH, a Coilcraft DO5040H–333MLB inductor is used.

General notes and recommendations:

- Fig. 2-1 through Fig. 2-2 are examples intended to describe the connectivity of each functional block within the CS40L5x, and do not limit all possible use cases.
- All external passive component values listed are nominal values.

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3 Characteristics and Specifications

Note: The default register field configurations are used unless specified otherwise in the test conditions.

Table 3-1. Recommended Operating Conditions

Test conditions (unless specified otherwise): Ground = GND = GND_AMP = GND_BST = 0 V; voltages are with respect to ground.

Parameter [1]			Symbol	Minimum	Maximum	Unit
DC power supply	Analog and digital supply		VDD_P	3.0	5.5	V
	Digital I/O supply		VDD_IO	1.71	3.6	V
	Analog supply [2]		VDD_A	1.71	1.89	V
	Boost converter [3, 4]		VDD_B	3.0	15.0	V
	Amplifier supply [5, 6]		VDD_AMP	5.0	15.0	V
Supply ramp up/down		VDD_P, VDD_IO, VDD_A VDD_B, VDD_AMP	t_{PWR-UD}	0.1 0.2	100 100	ms ms
External voltage applied to digital input/output		VDD_IO input/output pins [7] RESET pin	V_{INDI}	–0.3 –0.3	VDD_IO + 0.3 5.5	V V
External voltage applied to analog inputs		ADDR pin	V_{INAI}	–0.3	VDD_A + 0.3	V
External voltage applied to analog inputs		VMON_x pins	$V_{IN-VMON}$	–0.3	VDD_AMP + 0.3	V
External voltage applied to analog outputs		OUTP, OUTN pins	$V_{IN-OUTx}$	–0.3	VDD_AMP + 0.3	V
Ambient temperature			T_A	–40	+105	ºC

Note: The device is fully functional and meets all parametric specifications in this section if operated within the specified conditions. Functionality and parametric performance is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

1. There are no sequencing requirements associated with any of the supplies—each can be enabled or removed independently of the other supplies.
2. The analog supply can be generated by the internal LDO (powered from VDD_P), or else provided externally. If the LDO is used, the VDD_A pin must be connected to the LDO output pin (LDO_A_FILT) and must not be connected to any external supply.
3. Note VDD_B is the voltage-monitor point for the boost converter; the load current path is through the inductor to the BST_SW.
4. If the amplifier is powered directly using an external supply to VDD_AMP, the VDD_B supply is not required.
5. The amplifier supply can be generated by the boost converter, or else provided externally. If the boost converter is used, the VDD_AMP pin must be connected to the boost-converter output pin, VBST.
6. Note the VDD_AMP voltage may exceed these operating limits if generated by the CS40L5x boost converter.
7. All digital I/O pins except RESET.

Table 3-2. Absolute Maximum Ratings

Test conditions (unless specified otherwise): Ground = GND = GND_AMP = GND_BST = 0 V; voltages are with respect to ground.

Parameter			Symbol	Minimum	Maximum	Unit
DC power supply	Analog and digital supply		VDD_P	–0.3	6	V
	Digital I/O supply		VDD_IO	–0.3	4.32	V
	Analog supply		VDD_A	–0.3	2.27	V
	Boost converter		VDD_B	–0.3	18	V
	Amplifier supply		VDD_AMP	VDD_B – 0.3	18	V
Input current		digital I/O (per pin) ADDR pin	I_{in}	— —	±10 ±10	mA mA
Output load impedance			Z_{L1}	3	—	Ω
Ambient operating temperature (local to device, power applied)			T_A	–50	+115	°C
Junction operating temperature (power applied)			T_J	–40	+150	°C
Storage temperature			T_{STG}	–65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-1, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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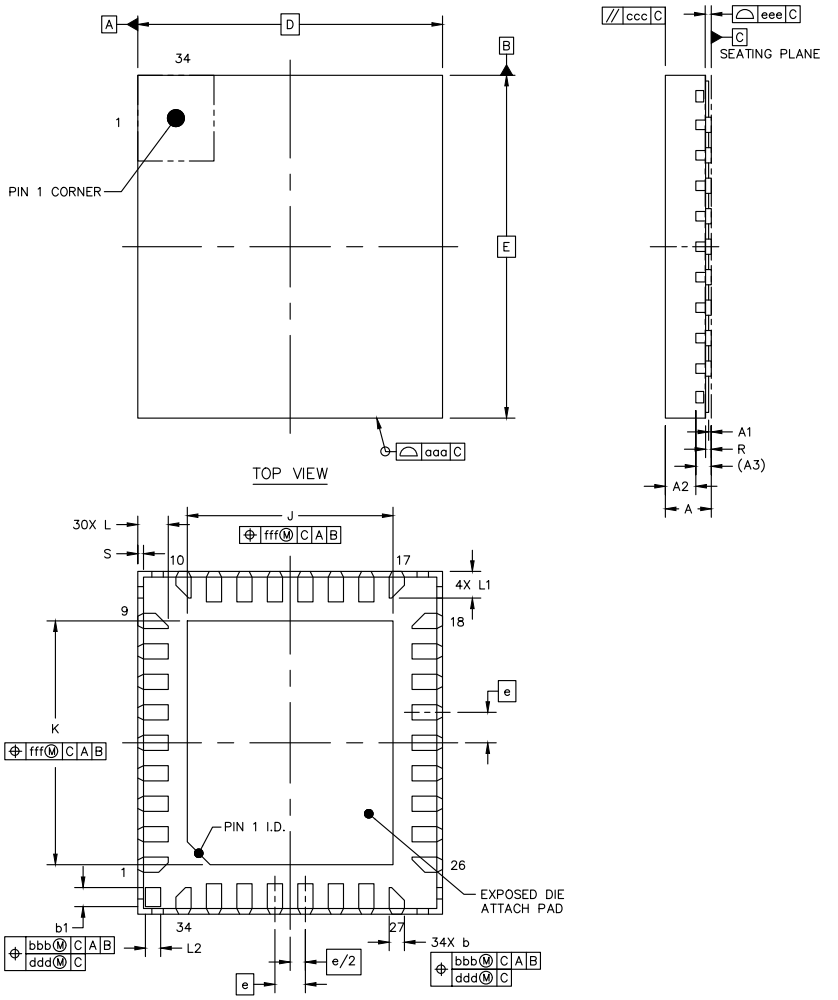
4 Package Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.55	0.6	0.65
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3	0.203		REF
LEAD WIDTH		b	0.15	0.2	0.25
		b1	0.2	0.25	0.3
BODY SIZE	X	D	4		BSC
	Y	E	4.5		BSC
LEAD PITCH		e	0.4		BSC
EP SIZE	X	J	2.6	2.7	2.8
	Y	K	3.1	3.2	3.3
LEAD LENGTH		L	0.3	0.4	0.5
		L1	0.25	0.35	0.45
		L2	0.15	0.2	0.25
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD OFFSET		bbb	0.07		
		ddd	0.05		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
EXPOSED PAD OFFSET		fff	0.1		
HALF-CUT DEPTH		R	0.075	---	---
HALF-CUT WIDTH		S	---	---	0.075

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
2.0 TOTAL THICKNESS NOT INCLUDE SAW BURR.
3.0 STEP CUT TYPE.

Figure 4-1. Wettable-Flank QFN Package Drawing

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5 Package Marking

Top Side Brand
Line 1: Part number
Line 2: Package mark
Line 3: Package mark
Line 4: Encoded wafer/device ID

Package Mark Fields
C1 = Cirrus Logic Index Code 1
C2 = Cirrus Logic Index Code 2
RR = Device revision code
LL = Lot sequence code
YY = Year of manufacture
WW = Work week of manufacture
CO = Country of origin (CO)

Figure 5-1. Package Marking

6 Ordering Information

Table 6-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number
CS40L51	Advanced Haptic Driver with Integrated Boost, Waveform Memory, and Closed-Loop Algorithms	34-pin QFN	Yes	Commercial [1]	–40 to +105°C	Tape and Reel	CS40L51–ENR
CS40L52	Advanced Haptic Driver with Integrated Boost, Waveform Memory, and Closed-Loop Algorithms	34-pin QFN	Yes	Commercial [1]	–40 to +105°C	Tape and Reel	CS40L52–ENR
CS40L53	Advanced Haptic Driver with Integrated Boost, Waveform Memory, and Closed-Loop Algorithms	34-pin QFN	Yes	Commercial [1]	–40 to +105°C	Tape and Reel	CS40L53–ENR

1.AEC-Q100 Grade 2 qualified

7 Revision History

Table 7-1. Revision History

Revision	Changes
R1 MAY 2025	• Initial version

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