CS4332S

High Performance Two-Channel Audio DAC

Features

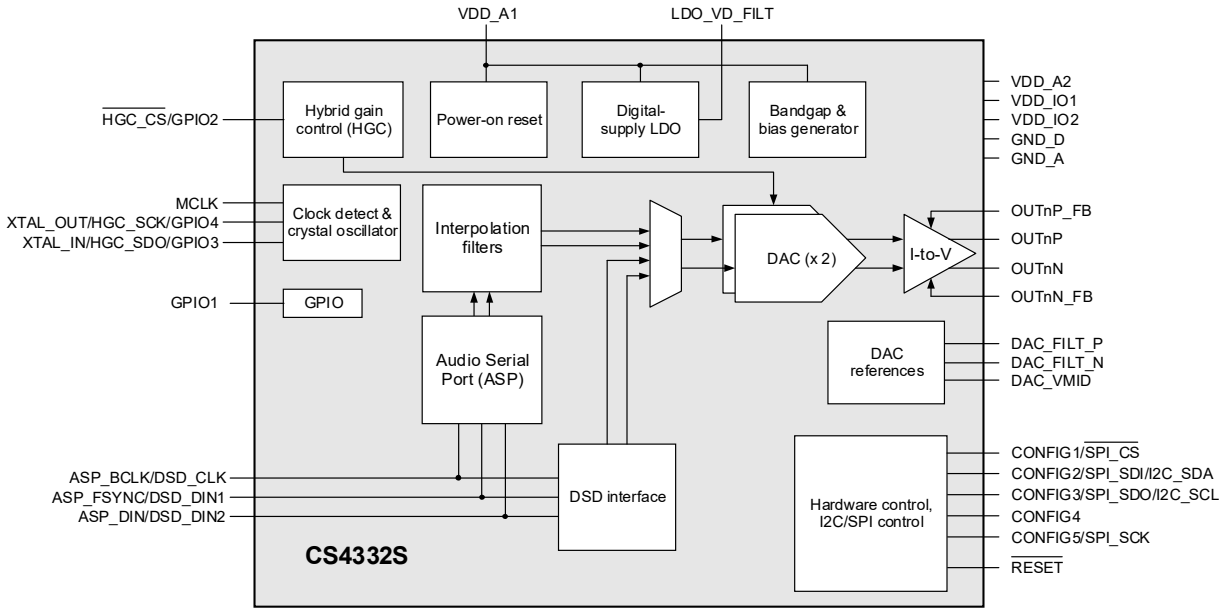
- High performance two-channel DAC
  - Differential analog architecture
  - High-resolution 32-bit digital design
  - Low-latency digital filters and digital volume control
- Crystal oscillator interface
- Sample timing alignment across multiple devices
- Hybrid gain control (HGC)
  - Synchronized control of external analog, and internal digital gain
- Audio serial port (ASP) sample rates up to 384 kHz
  - I²S, left-justified, and TDM data formats
- Direct Stream Digital® (DSD) input path supporting direct playback modes at up to 256×Fs oversample rate
- Hardware and software control modes
  - I²C control port up to 1 MHz
  - SPI control port up to 24 MHz
  - Hardware control with no host processor required
- Single-supply operation at 3.3 V
  - Support for 1.8 V–3.3 V digital input/output
  - 40-pin QFN package

Specifications

- Enhanced oversampling sigma-delta voltage-output DAC
  - 115 dB dynamic range (A-weighted)
  - –105 dB total harmonic distortion + noise (THD+N)
  - 4.6/Fs group delay at 48 kHz sample rate (slow roll-off, minimum phase)
  - 2 V_{RMS} full-scale output

Applications

- A/V receivers
- Digital mixing consoles
- Powered speakers
- Power amplifiers
- High-performance speakers and soundbars
- DAW interfaces
- Musical instruments
- Commercial audio systems



Advanced Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product without notice.

General Description

The CS4332S is a high-performance, 32-bit resolution, two-channel DAC. The CS4332S supports differential analog output, and 32-bit digital input via the audio serial port (ASP) at sample rates up to 384 kHz. A Direct Stream Digital® (DSD) input path is also available, supporting direct playback modes at up to 256×Fs oversample rate.

The voltage-output DAC incorporates a proprietary analog FIR architecture to reduce out-of-band noise and minimize the external component requirements. Configurable low-latency digital-interpolation filters are provided. The analog output supports configurable out-of-band filtering, enabling flexible integration, and optimal dynamic range for the target application.

The CS4332S can be configured using a control interface supporting I²C and SPI modes of operation. The device can also be operated in hardware mode, using external resistors to select the required configuration. Multiple hardware-control options are supported, including system clocking source, ASP format, digital-filter selection, and sample rate.

The low-latency digital filters are optimized for the applicable sample rate. Fast, slow, and balanced roll-off filters can be combined with minimum or linear phase responses to support the desired signal characteristics. A de-emphasis filter is provided in the output path.

The CS4332S supports synchronized control of external analog gain associated with each DAC output path. The external gain settings can be configured through either the HGC serial interface or the GPIO pins. Dual VDD_IO supplies support independent voltage domains for the HGC function and the control interface. Updates to the external and internal gain settings are fully synchronized.

The ASP supports operation in I²S, left-justified, and TDM data formats. Tristate control of the data-output pin allows multiple devices to operate on a shared bus.

Clocking for the CS4332S is provided by a separate clock source (MCLK) or else from the crystal oscillator. The DAC-conversion timing is referenced to the ASP data frame, enabling time-aligned operation across multiple devices sharing a common data bus.

The CS4332S can be powered from a single 3.3 V supply. Digital input at 1.8 V logic levels is also possible using a separate external supply. The device combines high performance with low power consumption.

The CS4332S is available in a commercial-grade 0.4 mm pitch, 40-pin QFN package for operation from -40°C to +85°C.

See Section 11 for ordering information.

Table of Contents

1 Pin Assignments and Descriptions

1.1 40-Pin QFN (Top View, Through-Package)

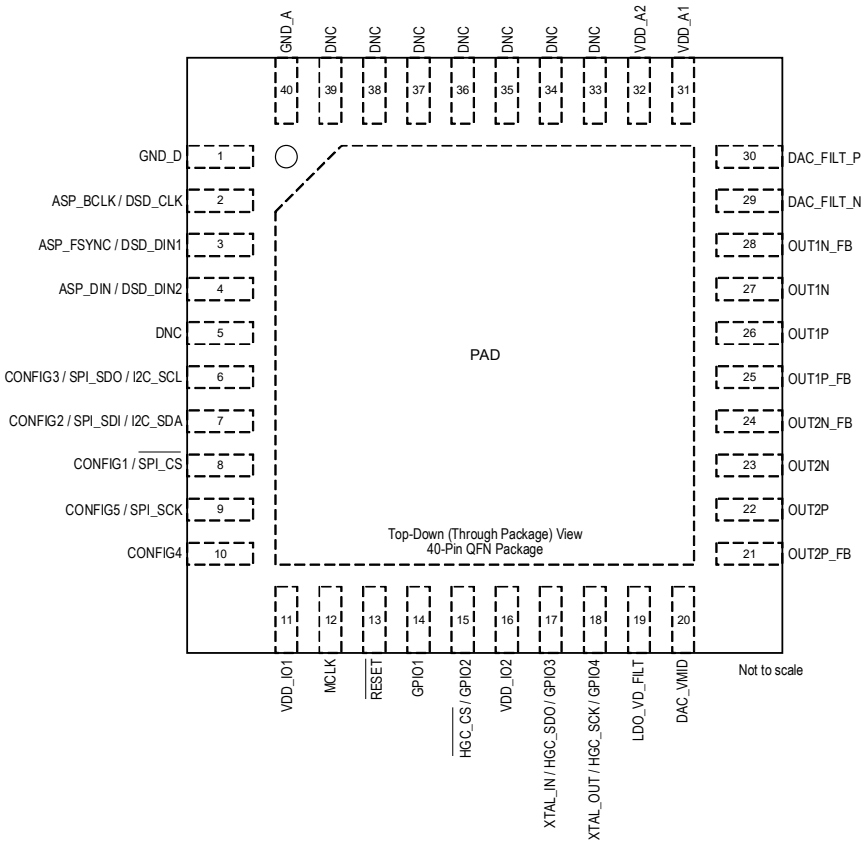


Figure 1-1. QFN 40-Pin Diagram (Top View, Through Package)

1.2 QFN Pin Descriptions

Table 1-1. QFN Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description
		Digital I/O		
ASP_BCLK/DSD_CLK	2	VDD_IO1	I/O	Audio serial port bit clock/DSD clock.
ASP_DIN/DSD_DIN2	4	VDD_IO1	I	Audio serial port data input/DSD data Input 2.
ASP_FSYNC/DSD_DIN1	3	VDD_IO1	I/O	Audio serial port frame sync/DSD data Input 1.
GPIO1	14	VDD_IO2	I/O	General-purpose input/output.
$\overline{\text{HGC\_CS}}$/GPIO2	15	VDD_IO2	I/O	Hybrid gain control (HGC) chip select/General-purpose input/output.
MCLK	12	VDD_IO1	I/O	Master clock input/output.
$\overline{\text{RESET}}$	13	VDD_IO1	I	Hardware reset control (active low).
XTAL_IN/HGC_SDO/GPIO3	17	VDD_IO2	I/O	Input for an external crystal/HGC data output/General-purpose input/output.
XTAL_OUT/HGC_SCK/GPIO4	18	VDD_IO2	I/O	Output for an external crystal/HGC clock/General-purpose input/output.

Table 1-1. QFN Pin Descriptions *(Cont.)*

Pin Name	Pin #	Power Supply	I/O	Description
			Analog I/O	
CONFIG1/$\overline{\text{SPI\_CS}}$	8	VDD_IO1	I	Hardware control pins.
CONFIG2/SPI_SDI/I2C_SDA	7	VDD_IO1	I/O	In software control mode, CONFIG1-3 and CONFIG5 support the SPI/I^2C interface.
CONFIG3/SPI_SDO/I2C_SCL	6	VDD_IO1	I/O	
CONFIG4	10	VDD_IO1	I	In software control mode, CONFIG1 selects the I^2C target address.
CONFIG5/SPI_SCK	9	VDD_IO1	I	
DAC_FILT_N	29	VDD_A1	O	DAC external capacitor connection.
DAC_FILT_P	30	VDD_A1	O	
DAC_VMID	20	VDD_A1	O	DAC mid-rail voltage reference output.
LDO_VD_FILT	19	VDD_A1	O	LDO_D regulator external capacitor connection.
OUT1N_FB	28	VDD_A1	O	Analog Output 1 feedback connection.
OUT1P_FB	25	VDD_A1	O	
OUT2N_FB	24	VDD_A1	O	Analog Output 2 feedback connection.
OUT2P_FB	21	VDD_A1	O	
OUT1N	27	VDD_A1	O	Analog Output 1.
OUT1P	26	VDD_A1	O	
OUT2N	23	VDD_A1	O	Analog Output 2.
OUT2P	22	VDD_A1	O	
			Power Supplies	
VDD_A1	31	—	—	Analog Supply 1.
VDD_A2	32	—	—	Analog Supply 2.
VDD_IO1	11	—	—	Digital I/O Supply 1.
VDD_IO2	16	—	—	Digital I/O Supply 2.
GND_A	40, PAD	—	—	Analog ground [1].
GND_D	1	—	—	Digital ground [1].
			No Connect	
DNC	5, 33, 34, 35, 36, 37, 38, 39	—	—	Do not connect.

1. All ground pins, including the ground paddle, must be tied to a common ground plane directly underneath the CS4332S. It is recommended that each ground pin is connected separately to the ground plane, using multiple vias to connect the ground paddle.

1.3 Termination of Unused Pins

Table 1-2 shows the required termination for unused pins (i.e., if the functionality of the pin is not being used). Pins not listed must be connected as shown in the typical connection drawings (see Section 2).

Table 1-2. Termination of Unused Pins

Name	Termination if unused
MCLK [1]	Float
ASP_DIN/DSD_DIN2	10 kΩ pull-down to GND
ASP_FSYNC/DSD_IN1	
CONFIG3/SPI_SDO/I2C_SCL	
CONFIG4	
CONFIG5/SPI_SCK	
GPIO1	
$\overline{\text{HGC\_CS}}$/GPIO2	
XTAL_IN/HGC_SDO/GPIO3	
XTAL_OUT/HGC_SCK/GPIO4	
OUTnX [2]	Connect to OUTnX_FB
$\overline{\text{RESET}}$	Connect to VDD_IO1

1. If the system clock is provided by the crystal oscillator and an MCLK output is not required, MCLK should be left floating.
2. See Section 5.1.3 for requirements in case of single-ended output configurations.

1.4 Electrostatic Discharge (ESD) Protection

ESD-sensitive device. The CS4332S is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD protection standards.

2 Typical Connection Diagrams

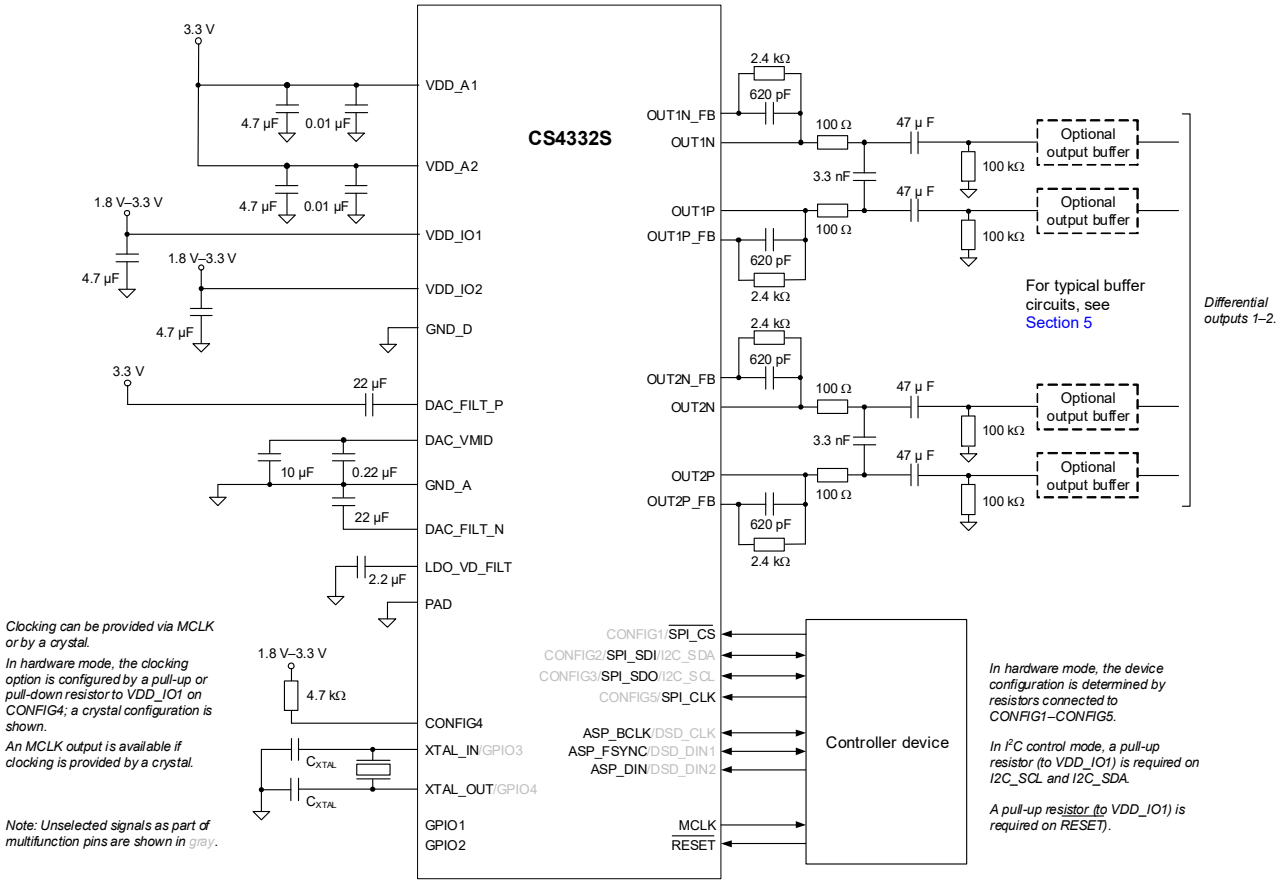


Figure 2-1. Typical Connections

3 Characteristics and Specifications

Note: Table 3-1 defines parameters as they are characterized in this section. Default register field configurations are used unless specified otherwise in the test conditions.

Table 3-1. Parameter Definitions

Parameter	Definition
Channel separation	The difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
Dynamic range	The difference in level between the maximum full-scale output signal and the sum of all harmonic distortion products plus noise with a low-level input signal applied (an input signal level 60 dB below full scale is used).
Power-supply rejection ratio (PSRR)	The ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
Total harmonic distortion plus noise (THD+N)	The ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth relative to the RMS amplitude of the fundamental (i.e., test frequency) output.

Note: Unless specified otherwise, all performance measurements are for a 10 Hz to 20 kHz bandwidth.

Table 3-2. Recommended Operating Conditions

Test conditions (unless specified otherwise): Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Analog supply [1]	VDD_A1, VDD_A2	3.13	3.47	V
	Digital I/O supply	VDD_IO1, VDD_IO2	1.71	3.63	V
Supply ramp up/down (all supplies)		t_{PWR-UD}	0.01	10	ms
Ambient temperature	Commercial Grade	T_A	–40	85	ºC

Note: The device is fully functional and meets all parametric specifications in this section if operated within the specified conditions. Functionality and parametric performance is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

Table 3-3. Absolute Maximum Ratings

Test conditions (unless specified otherwise): Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground.

Parameter			Symbol	Minimum	Maximum	Unit
DC power supply	Analog supply [1]		VDD_A1, VDD_A2	–0.3	4.32	V
	Digital I/O supply		VDD_IO1, VDD_IO2	–0.3	4.32	V
External voltage applied to digital input/ output		VDD_IO1 logic pins VDD_IO2 logic pins	V_{INDI}	–0.3 –0.3	VDD_IO1 + 0.3 VDD_IO2 + 0.3	V V
External voltage applied to analog inputs			V_{INAI}	–0.3	VDD_A + 0.3	V
Input current		digital input/output analog inputs	I_{IN}	— —	±10 ±10	mA mA
Ambient operating temperature			T_A	–40	+115	°C
Junction operating temperature			T_J	–40	+125	°C
Storage temperature			T_{STG}	–65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

Table 3-4. DAC Path Characteristics

Test conditions (unless specified otherwise): External components as shown in Fig. 2-1 incorporating the typical output circuit illustrated in Fig. 5-1; VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data, MCLK = 24.576 MHz.

Parameter		Min	Typ	Max	Units
Full scale differential output signal level (OUTnP to OUTnN)	0 dBFS input	—	2.00	—	V_{RMS}
Dynamic range	A-weighted	112	115	—	dB
	unweighted	109	112	—	dB
THD+N	0 dBFS input	—	–105	–99	dB
	–20 dBFS input	—	–92	—	dB
	–60 dBFS input	—	–52	—	dB
Idle channel noise	A-weighted	—	3.55	—	μV_{RMS}
Channel separation	1 kHz	—	110	—	dB
	20 kHz	—	100	—	dB
DC offset error		—	±0.5	—	mV
PSRR (VDD_A)	100 mV (peak-peak) 1 kHz sine wave	—	75	—	dB
Load resistance		3	—	—	kΩ
Load capacitance		—	—	100	pF

Table 3-5. DAC Filter Characteristics

Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter				Min	Typ	Max	Units
Fs = 16 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.49	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	100	—	—	dB
		Group delay [1]	linear phase	—	32.5/Fs	—	s
			minimum phase	—	4.6/Fs	—	s
Fs = 32 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.49	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	100	—	—	dB
		Group delay [1]	linear phase	—	32.5/Fs	—	s
			minimum phase	—	4.6/Fs	—	s
Fs = 44.1 kHz or 48 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.49	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	100	—	—	dB
		Group delay [1]	linear phase	—	32.6/Fs	—	s
			minimum phase	—	4.7/Fs	—	s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.47	Fs
		Passband ripple	f ≤ 0.42 Fs	–0.004	—	0.005	dB
		Stopband attenuation	f ≥ 0.59 Fs	101	—	—	dB
		Group delay [1]	linear phase	—	17.1/Fs	—	s
			minimum phase	—	4.6/Fs	—	s
Fs = 88.2 kHz or 96 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.49	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	101	—	—	dB
		Group delay [1]	linear phase	—	32.9/Fs	—	s
			minimum phase	—	5.0/Fs	—	s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.39	Fs
		Passband ripple	f ≤ 0.23 Fs	–0.005	—	0.005	dB
		Stopband attenuation	f ≥ 0.70 Fs	90	—	—	dB
		Group delay [1]	linear phase	—	7.4/Fs	—	s
			minimum phase	—	4.5/Fs	—	s
	Balanced roll-off	Passband	to –3 dB corner	—	—	0.35	Fs
		Passband ripple	f ≤ 0.23 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	101	—	—	dB
		Group delay [1]	linear phase	—	11.6/Fs	—	s
			minimum phase	—	5.2/Fs	—	s

Table 3-5. DAC Filter Characteristics *(Cont.)*

Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter				Min	Typ	Max	Units
Fs = 176.4 kHz or 192 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.48	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.004	—	0.005	dB
		Stopband attenuation	f ≥ 0.55 Fs	101	—	—	dB
		Group delay [1]	linear phase	—	34.7/Fs	—	s
			minimum phase	—	6.3/Fs	—	s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.36	Fs
		Passband ripple	f ≤ 0.11 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.80 Fs	108	—	—	dB
		Group delay [1]	linear phase	—	7.6/Fs	—	s
			minimum phase	—	5.4/Fs	—	s
	Balanced roll-off	Passband	to –3 dB corner	—	—	0.28	Fs
		Passband ripple	f ≤ 0.11 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	109	—	—	dB
		Group delay [1]	linear phase	—	10.6/Fs	—	s
			minimum phase	—	6.7/Fs	—	s
Fs = 352.8 kHz or 384 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.28	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.004	—	0.000	dB
		Stopband attenuation	f ≥ 0.55 Fs	116	—	—	dB
		Group delay [1]	linear phase	—	14.2/Fs	—	s
			minimum phase	—	7.5/Fs	—	s
	Balanced roll-off	Passband	to –3 dB corner	—	—	0.22	Fs
		Passband ripple	f ≤ 0.11 Fs	–0.001	—	0.000	dB
		Stopband attenuation	f ≥ 0.55 Fs	116	—	—	dB
		Group delay [1]	linear phase	—	10.8/Fs	—	s
			minimum phase	—	7.6/Fs	—	s

1. Group delay is measured from the start of the FSYNC frame containing the audio data on the ASP_DIN pin to the time at which the signal is presented on the output pins (OUTnP/OUTnN).

Table 3-6. DAC High-Pass Filter (HPF)

Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground;
T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter		Min	Typ	Max	Units
Passband	–0.01 dB corner	—	19	—	Hz
	–3 dB corner	—	1	—	Hz
Phase deviation	f = 20 Hz	—	0.001	—	degree
Filter settling time		—	0.4	—	s

Table 3-7. Device Power Consumption

Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Use Configuration		Typical Current (mA)			Total Power (mW)
		I_{VDD_A}	I_{VDD_IO1}	I_{VDD_IO2}	
Reset	$\overline{RESET}$ = Logic 0	0.70	0.04	0.04	2.574

Table 3-8. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise): Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC.

Parameter		Symbol	Minimum	Maximum	Unit
Input leakage current (per pin)		I_{IN}	—	±10	µA
Input capacitance (per pin)		C_{IN}	—	5	pF
Digital I/O (VDD_IO1 logic pins; see Section 1)[1]	High-level output	V_{OH}	0.9×VDD_IO1	—	V
	Low-level output	V_{OL}	—	0.1×VDD_IO1	V
	High-level input	V_{IH}	0.7×VDD_IO1	—	V
	Low-level input	V_{IL}	—	0.3×VDD_IO1	V
Digital I/O (VDD_IO2 logic pins; see Section 1)[1]	High-level output	V_{OH}	0.9×VDD_IO2	—	V
	Low-level output	V_{OL}	—	0.1×VDD_IO2	V
	High-level input	V_{IH}	0.7×VDD_IO2	—	V
	Low-level input	V_{IL}	—	0.3×VDD_IO2	V

1.If the system clock is not supplied by the crystal oscillator, the XTAL_IN and XTAL_OUT pins are used to support HGC (Section 4.6).

Table 3-9. DC Characteristics

Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC.

Parameter			Minimum	Typical	Maximum	Unit
LDO_VD_FILT	Nominal voltage		—	1.2	—	V
DAC_FILT [1]	Nominal voltage	VDD_A to DAC_FILT_P DAC_FILT_N to GND	— —	1.95 1.9	— —	V V
DAC_VMID	Nominal voltage		—	1.65	—	V
	Maximum output current		—	50	—	nA
VDD_A power-on reset (POR) threshold (V_{POR})		VDD_A rising VDD_A falling	2.0 2.0	— —	2.8 2.8	V V
VDD_IO1 power-on reset (POR) threshold (V_{POR})		VDD_IO1 rising VDD_IO1 falling	1.08 0.99	— —	1.58 1.43	V V
VDD_IO2 power-on reset (POR) threshold (V_{POR})		VDD_IO2 rising VDD_IO2 falling	0.45 0.45	— —	0.75 0.74	V V

1.DAC_FILT characteristics are provided as a guide for external component selection. The output current (arising from capacitor leakage) must be less than the maximum output current of the DAC_FILT_x pin.

Table 3-10. Switching Specifications—Reset and Clock References

Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC.

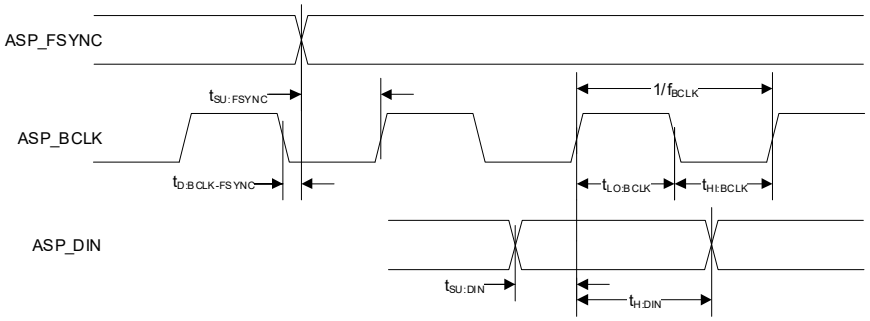
Parameter			Symbol	Minimum	Typical	Maximum	Unit
Reset	$\overline{\text{RESET}}$ low (logic 0) pulse width		t_{RLPW}	1	—	—	ms
	$\overline{\text{RESET}}$ rising edge to control port active		t_{IRS}	—	—	5	ms
MCLK input	MCLK frequency		f_{MCLK}	— — — —	24.576 22.5792 49.152 45.1584	— — — —	MHz MHz MHz MHz
	MCLK duty cycle		D_{MCLK}	45	—	55	%
	MCLK frequency tolerance		—	–1	—	1	%
MCLK output	MCLK frequency		f_{MCLK}	— — — —	24.576 22.5792 49.152 45.1584	— — — —	MHz MHz MHz MHz
	MCLK duty cycle		D_{MCLK}	45	—	55	%
	MCLK frequency accuracy		—	–1	—	1	%
Crystal	Oscillator frequency		f_{XTAL}	— — — —	24.576 22.5792 49.152 45.1584	— — — —	MHz MHz MHz MHz
	Interface transconductance	VDD_IO2 = 3.3 V VDD_IO2 = 1.8 V	—	— —	26 43	— —	mS mS

Table 3-11. Switching Specifications—Audio Serial Port (ASP)

Test conditions (unless specified otherwise): VDD_A = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-8); T_A = 25°C.

Parameter [1,2]		Symbol	Minimum	Maximum	Unit
Secondary Mode, VDD_IO1 = 3.3 V	ASP_FSYNC input sample/frame rate	Fs	16	384	kHz
	ASP_FSYNC pulse width	$t_{HI:FSYNC}$	$1/f_{ASP\_BCLK}$	—	ns
	ASP_BCLK frequency	f_{BCLK}	1.024	24.576	MHz
	ASP_BCLK high period	$t_{HI:BCLK}$	18	—	ns
	ASP_BCLK low period	$t_{LO:BCLK}$	18	—	ns
	ASP_FSYNC setup time before ASP_BCLK latching edge	$t_{SU:FSYNC}$	5	—	ns
	ASP_FSYNC hold time after ASP_BCLK latching edge	$t_{H:FSYNC}$	5	—	ns
	ASP_DIN setup time before ASP_BCLK latching edge	$t_{SU:DIN}$	10	—	ns
	ASP_DIN hold time after ASP_BCLK latching	$t_{H:DIN}$	5	—	ns
Primary Mode, VDD_IO1 = 3.3 V	ASP_FSYNC output sample/frame rate	Fs	16	384	kHz
	ASP_BCLK frequency	f_{BCLK}	2.8224	24.576	MHz
	ASP_BCLK duty cycle	D_{BCLK}	45	55	%
	ASP_FSYNC delay time after ASP_BCLK launching edge	$t_{D:BCLK–FSYNC}$	0	20	ns
	ASP_DIN setup time before ASP_BCLK latching edge	$t_{SU:DIN}$	6	—	ns
	ASP_DIN hold time after ASP_BCLK latching edge	$t_{H:DIN}$	5	—	ns
	ASP_DIN load capacitance ASP_BCLK ASP_FSYNC	—	0 0	50 50	pF pF
Secondary Mode, VDD_IO1 = 1.8 V	ASP_FSYNC input sample/frame rate	Fs	16	384	kHz
	ASP_FSYNC pulse width	$t_{HI:FSYNC}$	$1/f_{ASP\_BCLK}$	—	ns
	ASP_BCLK frequency	f_{BCLK}	1.024	24.576	MHz
	ASP_BCLK high period	$t_{HI:BCLK}$	18	—	ns
	ASP_BCLK low period	$t_{LO:BCLK}$	18	—	ns
	ASP_FSYNC setup time before ASP_BCLK latching edge	$t_{SU:FSYNC}$	5	—	ns
	ASP_FSYNC hold time after ASP_BCLK latching edge	$t_{H:FSYNC}$	5	—	ns
	ASP_DIN setup time before ASP_BCLK latching edge	$t_{SU:DIN}$	10	—	ns
	ASP_DIN hold time after ASP_BCLK latching	$t_{H:DIN}$	5	—	ns
Primary Mode, VDD_IO1 = 1.8 V	ASP_FSYNC output sample/frame rate	Fs	16	384	kHz
	ASP_BCLK frequency	f_{BCLK}	2.8224	24.576	MHz
	ASP_BCLK duty cycle	D_{BCLK}	45	55	%
	ASP_FSYNC delay time after ASP_BCLK launching edge	$t_{D:BCLK–FSYNC}$	0	20	ns
	ASP_DIN setup time before ASP_BCLK latching edge	$t_{SU:DIN}$	6	—	ns
	ASP_DIN hold time after ASP_BCLK latching edge	$t_{H:DIN}$	5	—	ns
	ASP_DIN load capacitance ASP_BCLK ASP_FSYNC	—	0 0	50 50	pF pF

1. ASP timing in I²S and Left-Justified Modes. ASP_BCLK can be inverted if required; the figure shows the default polarity.



2.ASP timing in TDM Mode.
ASP_BCLK can be inverted if required; the figure shows the default polarity.

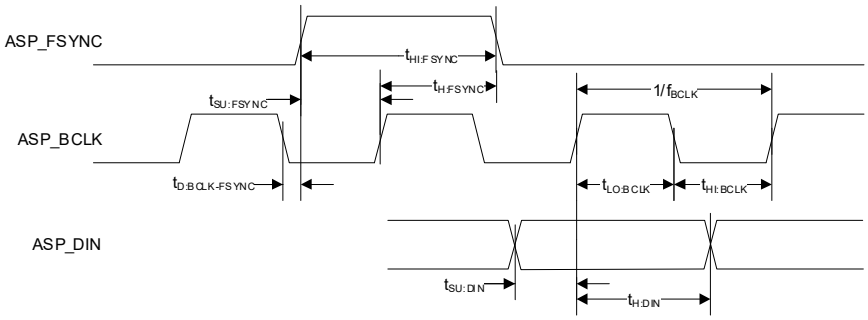
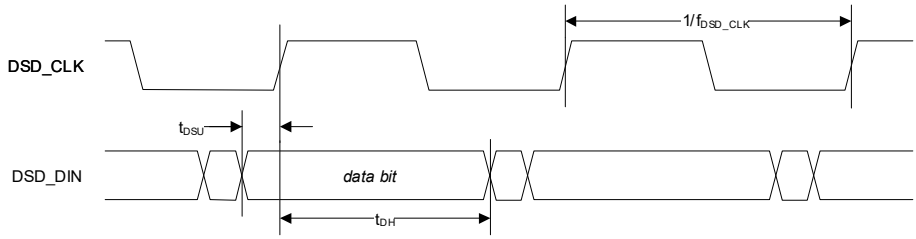


Table 3-12. Switching Specifications—Direct Stream Digital (DSD) Interface

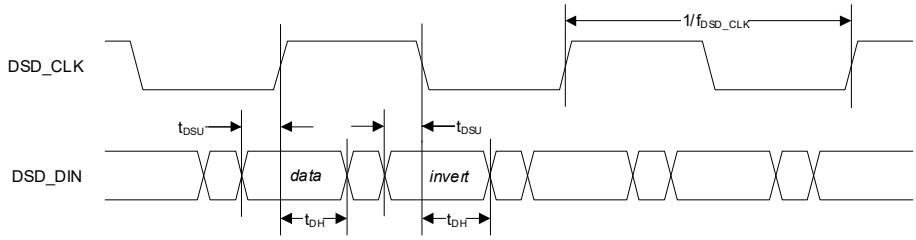
Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-8); T_A = 25°C.

Parameter [1,2,3]		Symbol	Minimum	Maximum	Unit
Normal Mode	DSD_CLK frequency	f_{DSD_CLK}	2.8224	22.5792	MHz
	DSD_CLK duty cycle	—	45	55	%
	DSD_DIN setup time to active DSD_CLK edge	t_{DSU}	10	—	ns
	DSD_DIN fall time from active DSD_CLK edge	t_{DH}	10	—	ns
Phase Modulation Mode	DSD_CLK frequency 64fs CLK (DSD_PM_SEL = 1) 128fs CLK (DSD_PM_SEL = 0)	f_{DSD_CLK}	2.8224 5.6448	2.8224 5.6448	MHz MHz
	DSD_CLK duty cycle	—	45	55	%
	DSD_DIN setup time to active DSD_CLK edge	t_{DSU}	10	—	ns
	DSD_DIN fall time from active DSD_CLK edge	t_{DH}	10	—	ns

1.DSD Normal Mode.



2.DSD Phase Modulation, (64fs CLK).



3.DSD Phase Modulation, (128fs CLK).

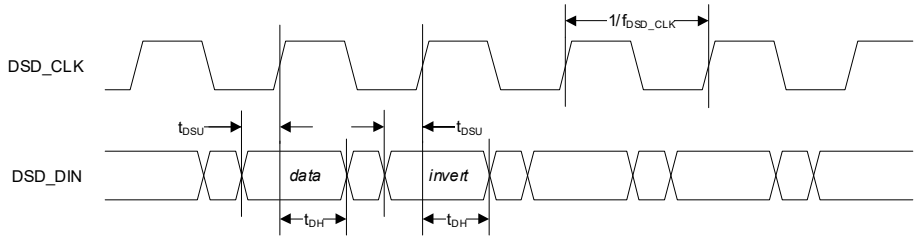
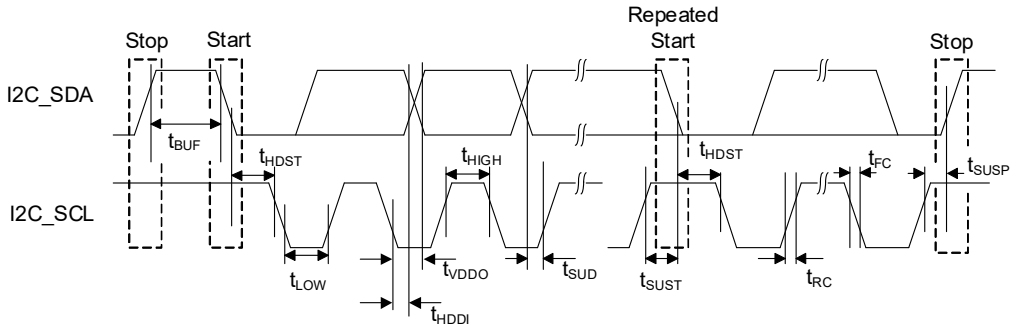


Table 3-13. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-8); T_A = 25°C.

Parameter [1,2]		Symbol	Minimum	Maximum	Unit
SCL clock frequency		f_{SCL}	—	1000	kHz
Clock low time		t_{LOW}	500	—	ns
Clock high time		t_{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)		t_{HDST}	260	—	ns
Setup time for repeated start		t_{SUST}	260	—	ns
Rise time of SCL and SDA	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{RC}	600 180 72	1000 300 120	ns ns ns
Fall time of SCL and SDA	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{FC}	6.5 6.5 6.5	300 300 120	ns ns ns
Rise time variation between SDA and SCL		—	—	1.67	ns
Fall time variation between SDA and SCL	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	—	— — —	100 100 75	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
SDA setup time to SCL rising		t_{SUD}	50	—	ns
SDA input hold time from SCL falling [3]		t_{HDDI}	0	—	ns
Output data valid (Data/ACK) [4]	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
SDA bus capacitance		C_B	—	550	pF
SCL/SDA pull-up resistance		R_P	500	—	Ω
Pulse width of spikes to be suppressed		t_{ps}	0	50	ns

1.All timing is relative to thresholds specified in Table 3-8, V_{IL} and V_{IH} for input signals, and V_{OL} and V_{OH} for output signals.
2.I²C control-port timing.



3.Data must be held long enough to bridge the transition time, t_{FC}, of SCL.
4.Time from falling edge of SCL until data output is valid.

Table 3-14. Switching Specifications—SPI Control Port

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-8); T_A = 25°C.

Parameter [1]	Symbol	Minimum	Maximum	Unit
SPI_SCK frequency	f_{SCY}	—	24	MHz
$\overline{\text{SPI\_CS}}$ falling edge to SPI_SCK rising edge	t_{SSU}	5	—	ns
SPI_SCK falling edge to $\overline{\text{SPI\_CS}}$ rising edge	t_{SHO}	0.5	—	ns
SPI_SCK pulse width low	t_{SCL}	18.5	—	ns
SPI_SCK pulse width high	t_{SCH}	18.5	—	ns
SPI_SDI to SPI_SCK setup time	t_{DSU}	5	—	ns
SPI_SDI to SPI_SCK hold time	t_{DHO}	2.5	—	ns
SPI_SCK falling edge to SPI_SDO transition	t_{DL}	0	15	ns
$\overline{\text{SPI\_CS}}$ rising edge to SPI_SDO output high-Z	—	0	15	ns
Bus free time between active $\overline{\text{SPI\_CS}}$	t_{SH}	20	—	ns

1.SPI control-port timing.

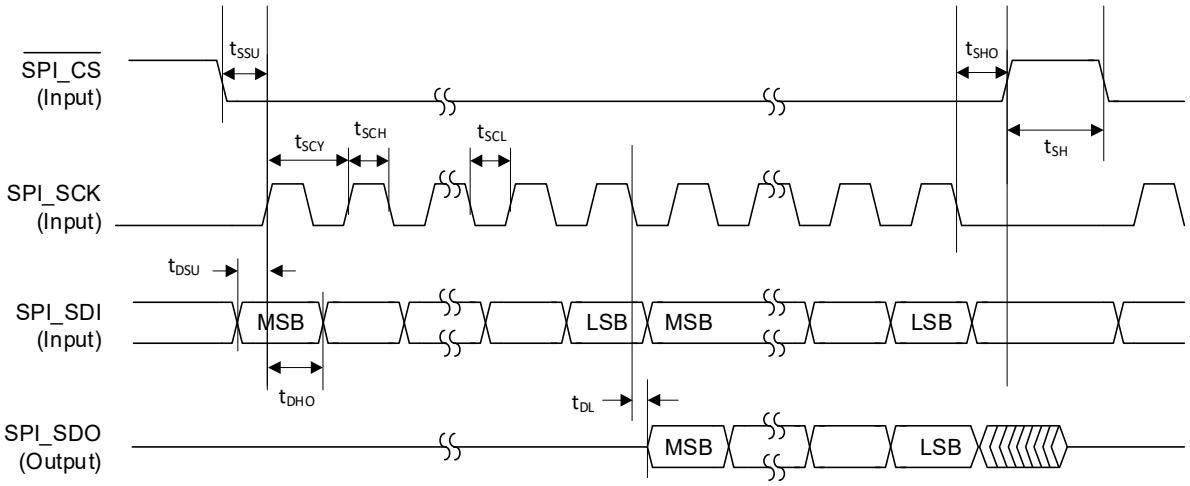
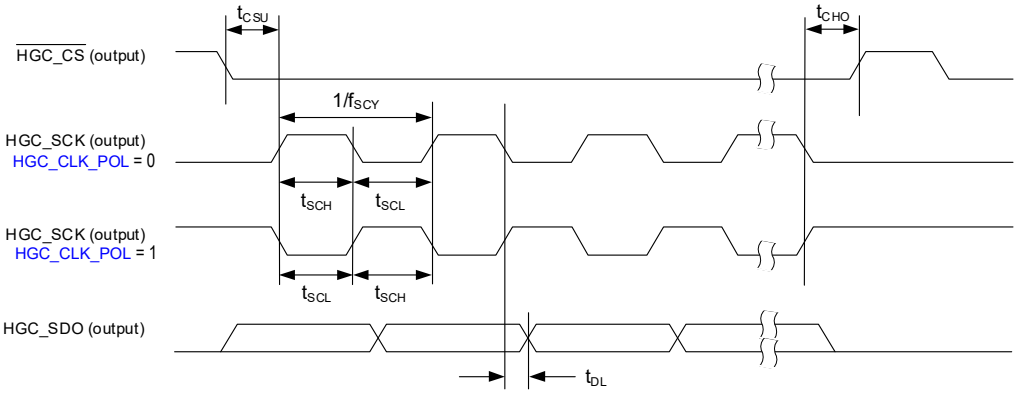


Table 3-15. Switching Specifications—SPI Controller (Hybrid Gain Control)

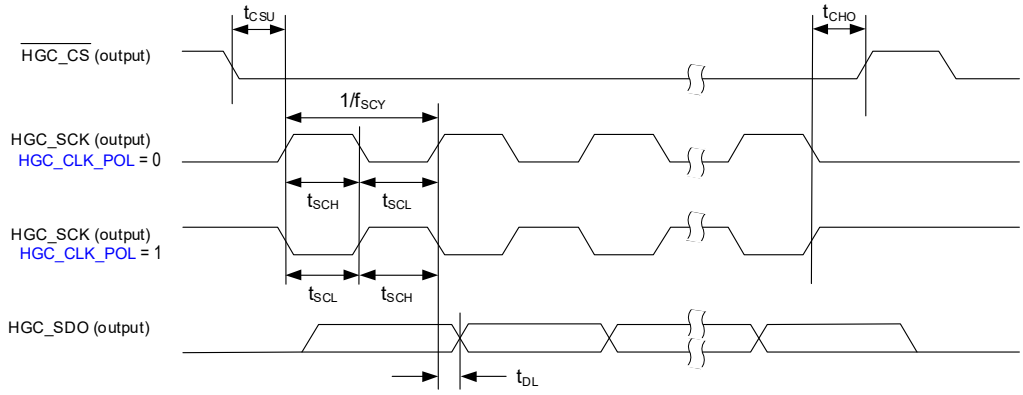
Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO2 logic (as specified in Table 3-8); T_A = 25°C.

Parameter [1,2]		Symbol	Minimum	Maximum	Unit
HGC_SCK frequency		f_{SCY}	—	12.288	MHz
$\overline{\text{HGC\_CS}}$ falling edge to HGC_SCK rising edge		t_{CSU}	30	—	ns
HGC_SCK falling edge to $\overline{\text{HGC\_CS}}$ rising edge		t_{CHO}	30	—	ns
HGC_SCK pulse width low		t_{SCL}	40	—	ns
HGC_SCK pulse width high		t_{SCH}	40	—	ns
HGC_SCK falling edge to HGC_SDO transition	C_{LOAD} (HGC_SDO) = 30 pF C_{LOAD} (HGC_SDO) = 60 pF	t_{DL}	–15 –20	15 20	ns ns

1.SPI Master timing, HGC_CLK_PHA = 0.



2.SPI Master timing, HGC_CLK_PHA = 1.



4 Functional Description

4.1 Device Power and Reset

The CS4332S is powered using VDD_A1, VDD_A2, VDD_IO1, and VDD_IO2 external supplies.

Notes: The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

VDD_IO1 and VDD_IO2 are independent power domains. VDD_IO1 supplies host-related interfaces (e.g., SPI control interface); VDD_IO2 supplies external interfaces (e.g., crystal oscillator connections). Integrated level shifters are included for direct interface to logic levels from 1.8 V to 3.3 V.

There are no power-sequencing requirements—supplies can be enabled in any order.

The CS4332S is in reset if the $\overline{\text{RESET}}$ pin is asserted (Logic 0), or if the VDD_A supply is below the respective reset threshold defined in Table 3-9.

All ground pins, including the ground paddle, must be tied to a common ground (GND) plane directly underneath the CS4332S.

4.2 Hardware Configuration

The CS4332S supports hardware and software control modes. In hardware mode, the device configuration is determined entirely by external resistors connected to the hardware-control pins. In software mode, the I²C/SPI control port is used to configure the device.

In hardware mode, the audio serial port (ASP) configuration is selected using the CONFIG1 and CONFIG2 pins as described in Table 4-1. See Section 4.4 for more details of the sample-rate selection and Section 4.8 for more details of the ASP operation.

Note: The DSD interface (Section 4.9) is not supported in hardware control mode.

Table 4-1. Hardware Control—ASP Configuration

Pin Name	Pin Configuration		Description
CONFIG1	Pull-up to VDD_IO1	0 Ω	Software control mode (I²C/SPI)
		4.7 kΩ	In I²C Mode, the pull-up resistor is used to select the device address—see Section 4.10.
		22 kΩ	In SPI Mode, it is recommended to use a 100 kΩ pull-up resistor.
		100 kΩ	
	Pull-down to GND_D	100 kΩ	ASP Primary Mode, 176.4 kHz, 192 kHz sample rate
		22 kΩ	ASP Primary Mode, 88.2 kHz, 96 kHz sample rate
		4.7 kΩ	ASP Primary Mode, 44.1 kHz, 48 kHz sample rate
		0 Ω	ASP Secondary Mode, autodetect sample rate
CONFIG2	Pull-up to VDD_IO1	0 Ω	ASP TDM Mode—minimum time slots [1], ASP_FSYNC_TYPE = pulse
		4.7 kΩ	ASP TDM Mode—maximum time slots [2], ASP_FSYNC_TYPE = pulse
		22 kΩ	—
		100 kΩ	ASP TDM Mode—minimum time slots [1], ASP_FSYNC_TYPE = square wave (50% duty cycle) [3]
	Pull-down to GND_D	100 k	ASP TDM Mode—maximum time slots [2], ASP_FSYNC_TYPE = square wave (50% duty cycle) [3]
		22 kΩ	—
		4.7 kΩ	ASP Left-Justified Mode
		0 Ω	ASP I²S Mode

1. The ASP data format is configured to support two time slots; this is the minimum necessary for the CS4332S input.
2. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate, refer to Table 4-11.
3. ASP_FSYNC_TYPE = square wave (50% duty cycle) is available in ASP Primary Mode only, as described in Section 4.8.

If the ASP is configured for TDM data format with maximum time slots, the TDM slot selection is determined using the CONFIG3 pin as described in Table 4-2. See Section 4.8 for more details of the ASP TDM modes.

Table 4-2. Hardware Control—TDM Slot Selection

Pin Name	Pin Configuration		Description
CONFIG3	Pull-up to VDD_IO1	0 Ω	Slots 14–15 [1]
		4.7 kΩ	Slots 12–13 [1]
		22 kΩ	Slots 10–11 [1]
		100 kΩ	Slots 8–9 [1]
	Pull-down to GND_D	100 kΩ	Slots 6–7 [2]
		22 kΩ	Slots 4–5 [2]
		4.7 kΩ	Slots 2–3
		0 Ω	Slots 0–1

1.Slots 8–15 are only valid in 16-slot TDM Mode.
2.Slots 4–7 are only valid in 8-slot or 16-slot TDM Mode.

The clock-reference configuration is determined using the CONFIG4 pin as described in Table 4-3. See Section 4.4 for more details of the CS4332S clocking architecture

Table 4-3. Hardware Control—Clocking Configuration

Pin Name	Pin Configuration		Clock Reference	Reference Clock Frequency (MHz) [1]
CONFIG4	Pull-up to VDD_IO1	0 Ω	XTAL	1024 fs(base)
		4.7 kΩ	XTAL	512 fs(base)
		22 kΩ	MCLK	1024 fs(base)
		100 kΩ	MCLK	512 fs(base)

1.fs(base) is the base sample rate. fs(base) = 48 kHz for 48 kHz-related sample rates; or 44.1 kHz for 44.1 kHz-related sample rates.

In hardware mode, the digital filter is selected using the CONFIG5 pin. See Section 4.7 for more details of the digital filters.

The filter selection is defined in Table 4-4. The filter selection is dependent on the sample rate, as described in Footnote 1 in Table 4-4.

Table 4-4. Hardware Control—Digital Filter Selection

Pin Name	Pin Configuration		DAC Interpolation Filter		High-Pass Filter (HPF)
			16–48 kHz Sample Rate [1]	88.2–384 kHz Sample Rate	
CONFIG5	Pull-up to VDD_IO1	0 Ω	Minimum phase, slow roll-off	Minimum phase, balanced roll-off	Bypassed
		4.7 kΩ	Minimum phase, fast roll-off	Minimum phase, fast roll-off	
		22 kΩ	Linear phase, slow roll-off	Linear phase, balanced roll-off	
		100 kΩ	Linear phase, fast roll-off	Linear phase, fast roll-off	
	Pull-down to GND_D	100 kΩ	Linear phase, fast roll-off	Linear phase, fast roll-off	Enabled
		22 kΩ	Linear phase, slow roll-off	Linear phase, balanced roll-off	
		4.7 kΩ	Minimum phase, fast roll-off	Minimum phase, fast roll-off	
		0 Ω	Minimum phase, slow roll-off	Minimum phase, balanced roll-off	

1.Fast roll-off filters are supported for all sample rates. Slow roll-off filters are not valid for 16 kHz or 32 kHz sample rates.

In hardware mode, the device configuration is latched when reset is released (either power-on reset or deassertion of the $\overline{\text{RESET}}$ pin). In hardware mode, the configuration cannot be changed while the device is operational. To update the device configuration, the $\overline{\text{RESET}}$ pin must be asserted (Logic 0), or the device power cycled, in order to read new settings on the CONFIGx pins.

If software mode is selected (i.e., CONFIG1 is pulled-up to VDD_IO1), the device configuration and the digital-filter selection are controlled by register writes via the applicable control interface, as described in Section 4.10. Unused CONFIGx pins should be terminated as described in Section 1.3.

Note: In software mode, the CONFIG1 pin is used to select the I²C target address (see Section 4.10). If the SPI control interface is used, it is recommended to connect the CONFIG1 pin to VDD_IO1 via a 100 kΩ resistor.

4.3 Software Configuration

Software control mode is enabled if the CONFIG1 pin is pulled-up to VDD_IO1; note that $\overline{\text{RESET}}$ must remain asserted (i.e., Logic_0) until CONFIG_1/$\overline{\text{SPI\_CS}}$ is deasserted (i.e., Logic_1). In software control mode, the CS4332S is configured by writing to control registers using the control port.

The control port supports I²C and SPI modes of operation; the applicable mode is detected automatically on the respective interface pins. In I²C mode, the target address is selectable using the CONFIG1 pin. See Section 4.10 for further details of the I²C/SPI control port.

In software control mode, GLOBAL_EN is used as the global control field for enabling/disabling the CS4332S functions. The device should be configured using the applicable control registers before setting GLOBAL_EN.

Notes: The clocking (Section 4.4) and ASP (Section 4.8) control registers are only valid on the rising edge of GLOBAL_EN. Writing to these registers has no effect at any other time. It is recommended to select the disabled state (GLOBAL_EN = 0) before writing to these registers.

To minimize the CS4332S power consumption when all output paths are disabled, see Section 4.5.5.

A reset of the CS4332S can be triggered by writing 0x5A to the SW_RESET field. A software reset disables all functions and sets the control registers to their default states.

4.4 System Clocking

Clocking for the CS4332S is provided using either the MCLK input or the crystal oscillator. In each case, the frequency must be 1024 fs(base) or 512 fs(base); where fs(base) = 48 kHz (for 48 kHz-related sample rates), or 44.1 kHz (for 44.1 kHz-related sample rates). The specifications for the clocking sources are described in Table 3-10; for optimal out-of-band noise performance a system clock rate of 1024 fs(base) is recommended.

In hardware mode, the clock source is configured using the CONFIG4 pin, as detailed in Table 4-3. In software mode, the clocking source is selected using SYSCLK_SRC.

The crystal oscillator uses an external crystal (XTAL) to generate the system clock. Load capacitors are connected to the crystal as shown in Fig. 4-1. A series resistor (R_S) may also be required to configure the drive level for the selected crystal.

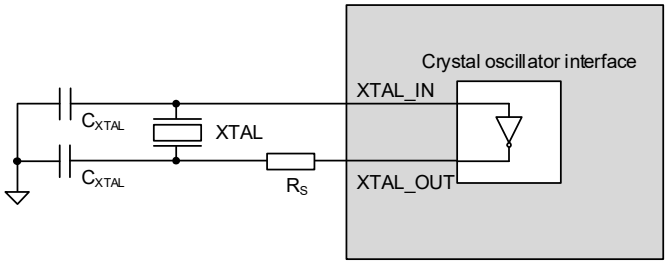


Figure 4-1. Crystal Oscillator Connection

Guidance on selecting a suitable crystal and associated components is provided in Section 5.2. The suitability of the external crystal is calculated as a function of the operating voltage (VDD_IO2) and the transconductance of the crystal interface, as defined in Table 3-10.

If clocking is provided using the crystal oscillator, the CS4332S outputs a clock on the MCLK pin. The frequency of the MCLK output clock matches the crystal oscillator frequency. The output clock can be used to drive other devices.

In ASP Secondary Mode, the ASP_FSYNC input is used to control the DAC-conversion timing, enabling multiple CS4332S devices to operate synchronously (sample timing is phase aligned) in a system. The external clocks ASP_FSYNC and ASP_BCLK must be derived from a common clock source (i.e., the MCLK input, or the MCLK output when clocking is provided using the crystal oscillator). See Section 4.8 for more details of the ASP.

The clocking architecture is illustrated in Fig. 4-2.

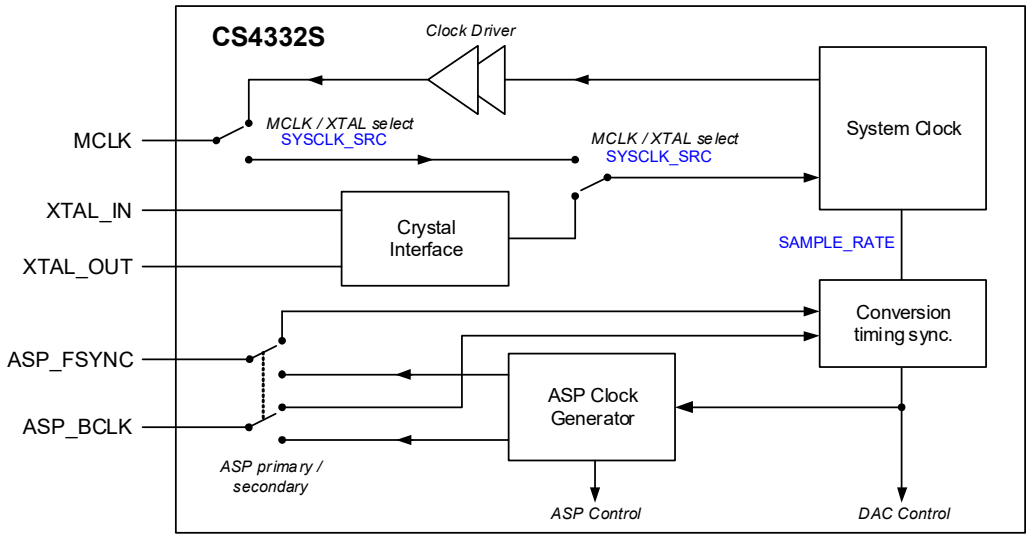


Figure 4-2. System Clocking

4.4.1 Hardware Control Mode

In hardware control mode, the system clock can be sourced from the MCLK pin or from the crystal oscillator. In each case, the frequency must be 1024 fs(base) or 512 fs(base); where fs(base) = 48 kHz (for 48 kHz-related sample rates), or 44.1 kHz (for 44.1 kHz-related sample rates). The clock source is configured using the CONFIG4 pin as described in Section 4.2.

The sample rate is selected using the CONFIG1 pin as described in Section 4.2. Sample rates 44.1 kHz–192 kHz can be configured, or else the autodetect option (sample rates 16 kHz–192 kHz) automatically configures the device according to the ASP interface clock signals. The autodetect sample-rate option is only valid if the ASP is operating in Secondary Mode (see Section 4.8).

The supported clocking configurations are summarized in Table 4-5.

Table 4-5. System Clock Configuration

Reference Source	Reference Frequency (MHz)	ASP Operating Conditions [1]
MCLK or XTAL	24.576 or 49.152	Primary or Secondary Mode, I²S, left-justified, or TDM data formats, sample rates 48, 96, and 192 kHz Primary Mode, or sample rates 16, 32, 48, 96, and 192 kHz in Secondary Mode (autodetect only).
MCLK or XTAL	22.5792 or 45.1584	Primary or Secondary Mode, I²S, left-justified, or TDM data formats, sample rates 44.1, 88.2, 176.4 kHz in Primary Mode, or sample rates 44.1, 88.2, 176.4 kHz in Secondary Mode (autodetect only).

1. See Section 4.8 for details of the audio serial port (ASP).

The sample rate must be related to the system clock reference as described in Table 4-6.

Table 4-6. Hardware Control Mode Sample Rate Options

Reference Source	Reference Frequency (MHz)	MCLK Out (MHz)	Sample Rate (kHz)
MCLK	22.5792 or 45.1584	—	44.1, 88.2, 176.4
	24.576 or 49.152		16, 32, 48, 96, 192
XTAL	22.5792 or 45.1584	22.5792 or 45.1584	44.1, 88.2, 176.4
	24.576 or 49.152	24.576 or 49.152	16, 32, 48, 96, 192

If the ASP is configured in ASP Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important. If clocking for the CS4332S is provided using the crystal oscillator, then the BCLK and FSYNC signals should be derived from the common clock source provided by the CS4332S MCLK output, see Section 4.8.

4.4.2 Software Control Mode—ASP Input

In software (I²C/SPI) control mode, with the ASP interface selected as the audio source (see Section 4.8), the clocking configuration is selected using the following control fields:

- The sample rate is configured using SAMPLE_RATE. Sample rates 16 kHz–384 kHz can be configured, or else the autodetect option automatically configures the device according to the ASP interface signals. The sample-rate autodetect option is only valid for sample rates 16 kHz–192 kHz.
- The system clock source is selected using SYSCLK_SRC. The clock source can be either the crystal oscillator or MCLK.
- The system clock frequency is configured using SYSCLK_FREQ. The system clock frequency must be 1024 fs(base) or 512 fs(base); where fs(base) = 48 kHz (for 48 kHz-related sample rates), or 44.1 kHz (for 44.1 kHz-related sample rates).

The sample rate must be related to the system clock reference as described in Table 4-7.

Table 4-7. Software Control Mode Sample Rate Options

Reference Source	Reference Frequency (MHz)	MCLK Out (MHz)	Sample Rate (kHz)
MCLK	22.5792 or 45.1584	—	44.1, 88.2, 176.4, 352.8
	24.576 or 49.152		16, 32, 48, 96, 192, 384
XTAL	22.5792 or 45.1584	22.5792 or 45.1584	44.1, 88.2, 176.4, 352.8
	24.576 or 49.152	24.576 or 49.152	16, 32, 48, 96, 192, 384

The sample-rate autodetect option (16 kHz–192 kHz) is only valid if the ASP is operating in Secondary Mode (see Section 4.8).

If the ASP is configured in ASP Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important. If clocking for the CS4332S is provided using the crystal oscillator, then the BCLK and FSYNC signals should be derived from the common clock source provided by the CS4332S MCLK output, see Section 4.8.

4.4.3 Software Control Mode—DSD Input

In software (I²C/SPI) control mode, with the DSD interface selected as the audio source (see Section 4.9), the clocking configuration is selected using the following control fields:

- The system clock source is selected using SYSCLK_SRC. The clock source can be either the crystal oscillator or the MCLK input.
- The system clock frequency is configured using SYSCLK_FREQ. The system clock frequency must be 22.5792 MHz.
- The DSD clock, DSD_CLK, frequency is configured using DSD_OSR as described in Section 4.9.2.

The external clocks; i.e., the system clock (MCLK or crystal oscillator) and DSD_CLK must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important. If clocking for the CS4332S is provided using the crystal oscillator, then the DSD_CLK signal should be derived from the common clock source provided by the CS4332S MCLK output, see Section 4.8.

4.5 DAC and Analog Output

The CS4332S supports up to two analog output channels, each incorporating a high-performance sigma-delta digital-to-analog converter (DAC). Digital volume and mute control is provided on each output channel.

The digital volume and mute controls are supported in software (I^2C/SPI) control mode only. In hardware control mode, all channels are enabled with 0 dB volume.

4.5.1 Path Enable

The analog outputs and DAC paths are enabled using OUTx_DAC_EN (where x indicates the channel number 1–2).

When the output paths are enabled for the first time after power-up or after the DAC reference has been disabled (described in Section 4.5.5), the paths do not become active until a startup delay has elapsed; the delay ensures the noise floor of the output path has settled before it becomes active and mitigates any audible artifacts. The time delay (1 s) is applied when the output paths are enabled using OUTx_DAC_EN.

The polarity of the DAC output can be inverted using OUTx_INV for the respective channel.

The CS4332S supports a mono output configuration; this can be used in applications where stereo sound is unnecessary, such as voice playback, alarms, or devices with a single speaker. If mono operation is required, it is recommended to configure the CS4332S with a single output path enabled prior to initial startup to minimize any audible artifacts.

4.5.2 Digital Volume and Mute

The signal path incorporates a digital volume control, supporting a gain range of –127.5 dB to 0 dB in 0.5 dB steps. Volume ramping and digital mute is also supported.

The digital volume is configured using OUTx_VOL for the respective output channel. The digital mute is enabled by setting OUTx_MUTE.

Writing to the volume or mute fields has no effect on the signal path until a 1 is written to OUT_VU. Writing 1 to OUT_VU causes the volume and mute settings to be updated on all output paths simultaneously.

When the volume or mute is changed, the gain of the affected signal paths is ramped up or down to the new setting. For increasing gain, the rate is controlled by OUT_RAMP_RATE_INC; for decreasing gain, the rate is controlled by OUT_RAMP_RATE_DEC.

Note: The OUT_RAMP_RATE_INC and OUT_RAMP_RATE_DEC fields should not be changed while a volume ramp is in progress.

4.5.3 DAC Digital Gain

The DAC signal path incorporates digital gain, supporting a range of –32 dB to +31.875 dB in 0.125 dB steps. The digital gain provides fine adjustment of the overall output path gain. The digital gain is configured for each channel using OUTx_DIG_GAIN. Gain ramping is also supported (as described in Section 4.6).

The gain changes are applied upon register write using OUTx_UPDATE.

Note: The digital volume and digital gain are configured separately. The total digital gain of the output path is the sum of the digital volume and digital gain.

4.5.4 Power Optimization

A Class A amplifier is provided in the output path to convert the current output to a voltage output. An external feedback circuit is required, as described in Section 5.1.

A voltage output of 2 V_{RMS} is provided; this supports a minimum resistive load of 3 kΩ in parallel with a maximum capacitive load of 100 pF. If the load has a higher-impedance, the CS4332S can optimize power consumption by adjusting the drive current while maintaining an output of 2 V_{RMS}. In this case, a minimum resistive load of 10 kΩ in parallel with a maximum capacitive load of 100 pF is supported.

The maximum load impedance is selected using OUT_LOAD_CFG.

4.5.5 DAC Shutdown

To minimize power consumption when all output paths are disabled, the DAC reference circuit can be disabled. Note that power consumption is only reduced if the output paths have previously been enabled. Until they are enabled for the first time, the power consumption is already minimized.

In software mode, the DAC reference circuit is disabled using DAC_SHUTDOWN. If this bit is set, all paths are disabled regardless of the status of the OUTx_DAC_EN bits. Prior to disabling the DAC reference circuit, it is recommended to mute the output paths, as described in Section 4.5.2.

Note: If the DAC_SHUTDOWN bit is cleared, any output paths where OUTx_DAC_EN is set are enabled.

In hardware mode, the DAC shutdown function incorporates a controlled shutdown sequence to mitigate any audible artifacts. The shutdown sequence slowly ramps down the digital volume and then ramps down the DAC output voltage prior to disabling the DAC reference circuit.

The shutdown sequence is selected using a rising-edge logic input on the GPIO1 pin. GPIO1 must be held low (i.e., Logic 0) during device startup.

To enable the DAC reference circuit after a hardware shutdown, the $\overline{\text{RESET}}$ pin must be asserted (Logic 0), or the device power cycled.

4.6 Hybrid Gain Control

The CS4332S provides the capability to control an external gain stage associated with the output path. In typical applications, a separate gain control manages the external gain changes. The hybrid gain control (HGC) function enables synchronized adjustments across the combined external and internal gain range; this enables fine-resolution gain changes without audible artifacts due to external gain step changes.

The external analog gain can be controlled by the CS4332S using the HGC SPI control interface implemented on the $\overline{\text{HGC\_CS}}$, HGC_SCK, and HGC_SDO pins, as illustrated in Fig. 4-3. The HGC SPI control interface is not available if the system clock is supplied using the crystal oscillator.

Note: If the HGC SPI control interface is selected, GPIO functions are not supported on the GPIO2, GPIO3, GPIO4 pins.

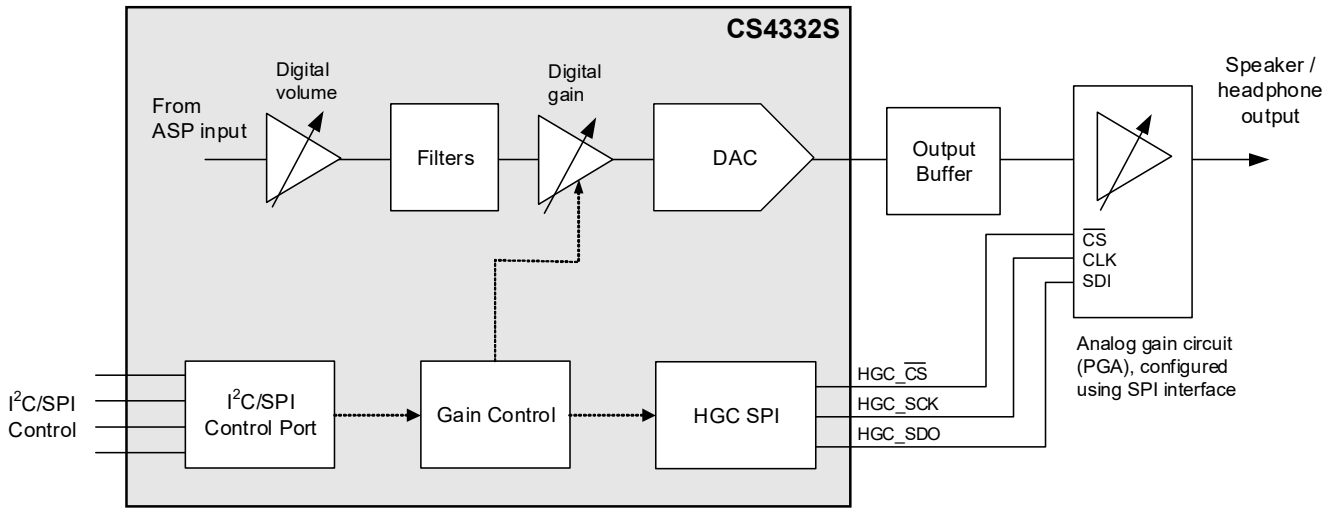


Figure 4-3. Hybrid Gain Control using HGC SPI

Alternatively, the GPIO pins can be configured to control the external analog gain; an example using GPIO1 and GPIO2 is shown in Fig. 4-4. The control type, SPI (default) or GPIO, is selected using HGC_CTRL_INTERFACE.

Note: GPIO3 and GPIO4 are not available if the system clock is supplied using the crystal oscillator.

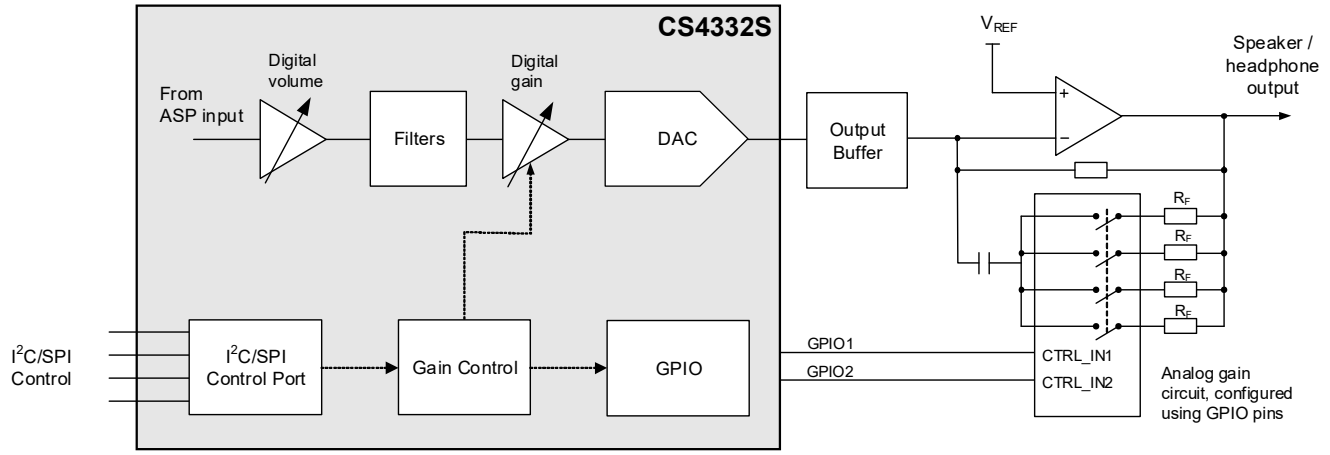


Figure 4-4. Hybrid Gain Control using GPIO Pins

The HGC function can be used to attenuate the output path; an example using GPIO pins is illustrated in Fig. 4-5.

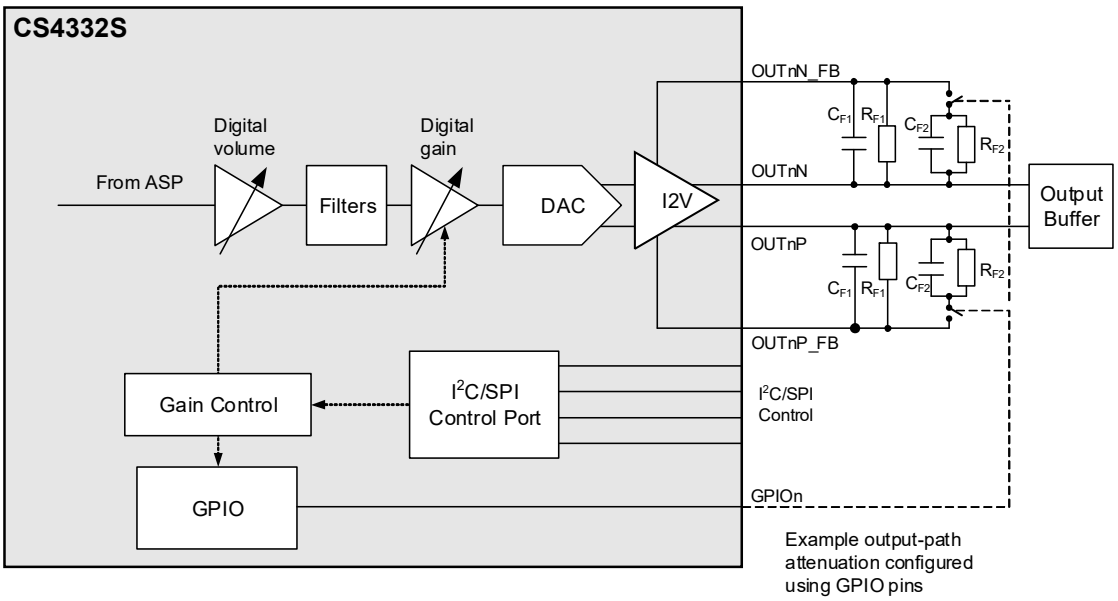


Figure 4-5. Example of Output Path Attenuation using GPIO Pins

To configure the signal path, the host processor writes gain control data to the CS4332S. If the HGC SPI interface has been selected, the CS4332S forwards the data to the external analog gain stage; if the GPIOs have been selected, the CS4332S configures the required GPIO output logic levels. If HGC SPI control is used, multiple external analog gain stages can be independently controlled in a configurable daisy-chain arrangement, as described in Section 4.6.1.

Zero-cross detection is used to synchronize the external gain configuration with the output signal and with the internal gain configurations ensuring seamless operation across the combined gain range.

Volume ramping is supported on the digital volume (see Section 4.5.2); the volume ramp is coordinated with the internal and external gain controls, enabling smooth transitions across the full range of the internal and external gain selections.

Note: The digital volume and digital gain are configured separately. The total digital gain of the output path is the sum of the digital volume and digital gain.

The HGC SPI controller interface can also be used to control auxiliary functions associated with the output path using a port expander or similar external IC.

4.6.1 HGC SPI Controller Interface Configuration

The HGC SPI controller interface is supported using the $\overline{\text{HGC\_CS}}$/GPIO2, XTAL_IN/HGC_SDO/GPIO3, and XTAL_OUT/HGC_SCK/GPIO4 pins, which must be configured for the SPI function if required. The HGC SPI function is selected using HGC_CTRL_INTERFACE. The interface comprises three connections as follows:

- HGC_SCK = Clock output
- HGC_SDO = Data output
- $\overline{\text{HGC\_CS}}$ = Chip select ($\overline{\text{CS}}$), active low

Note: The HGC SPI interface connections are powered by VDD_IO2; see Table 3-8 for digital I/O levels.

The CS4332S configures the external analog gain circuits using a bit pattern that is transmitted to each of the connected devices in a daisy-chain manner. The bit pattern is shifted through each of the connected devices according to a configurable position in the chain, allowing each device to be individually controlled via a shared data interface.

The HGC SPI interface is fully configurable and flexible to support a wide variety of external gain-control implementations. The HGC SPI data definition is not fixed on the CS4332S; the HGC SPI data can be configured to support whatever bit patterns are required in the specific application.

A maximum of four devices can be controlled, including two auxiliary devices, as described in Section 4.6.6. The number of bits associated with each connected device is configured for the respective audio channel using OUTx_BIT_PATT_LENGTH, and for the auxiliary devices using AUXx_BIT_PATT_LENGTH.

Each connected device is allocated a position in the daisy chain using the respective OUTx_SPI_POSITION, and AUXx_SPI_POSITION bits. The devices must be assigned to consecutive positions, starting with position 000. The daisy-chain wiring of the external devices must be in the same order as the allocated positions; this ensure each device is configured with its corresponding bit pattern.

The bit pattern length and device position bits should be set to 0 for any audio channel where there is no associated device to be controlled.

If the bit pattern or the device position bits are updated, the new settings are latched internally and are not reflected in the HGC SPI data output until a 1 is written to HGC_INIT_UPDATE. The host processor must confirm that the gain controller is idle (HGC_BUSY_STS = 0) before writing to HGC_INIT_UPDATE.

Example connections are shown in Fig. 4-6.

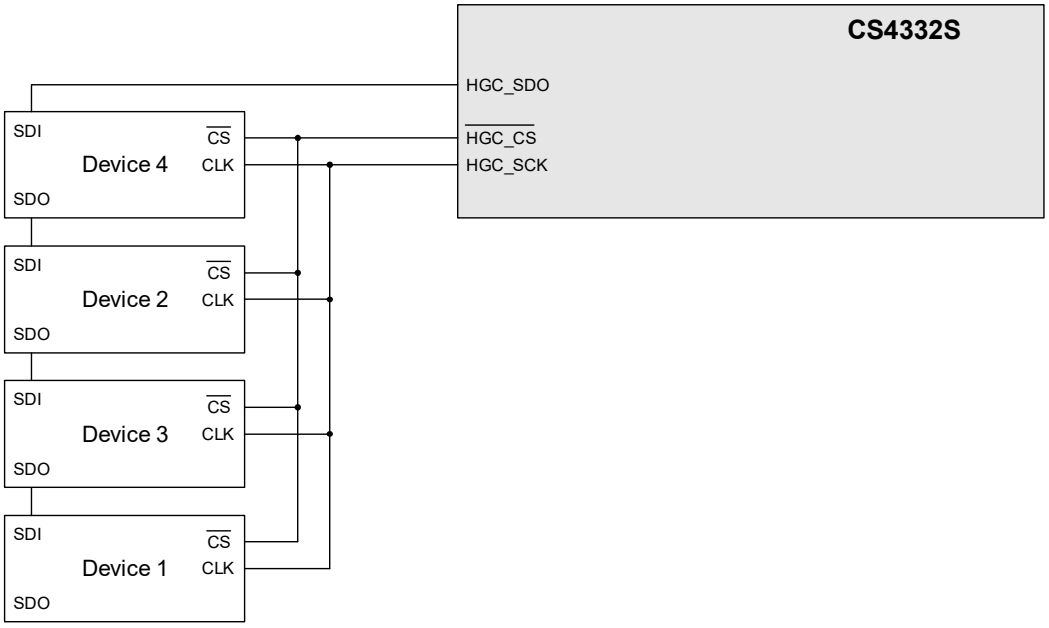


Figure 4-6. HGC SPI Daisy Chain Example Connections

In this example, Device 1 and Device 3 are connected to output channels 1 and 2 respectively and there are two auxiliary devices, Device 2 and Device 4. The order that the devices are to be serviced in, i.e., the order that they are connect in the daisy chain is Device 1, Device 3, Device 2, and Device 4 Table 4-8.

Table 4-8. Example SPI Position Configuration

Device	Position	Configuration
Device 1	1	OUT1_SPI_POSITION = 000
Device 2	3	AUX1_SPI_POSITION = 010
Device 3	2	OUT2_SPI_POSITION = 001
Device 4	4	AUX2_SPI_POSITION = 011

The HGC SPI controller is configurable to support different timing and signal-polarity options. The HGC_CLK_POL bit controls the polarity of the clock output; the HGC_CLK_PHA bit controls which phase of the clock cycle the data output is valid. See Table 3-15 for timing specifications.

The HGC SPI clock rate is derived as an integer division of the system clock. The HGC SPI clock rate is configured using HGC_SCK_DIV, supporting divisors of 512 fs(base) or 1024 fs(base); where fs(base) = 48 kHz (for 48 kHz-related sample rates), or 44.1 kHz (for 44.1 kHz-related sample rates). The fastest HGC SPI clock is 12.288 MHz or 11.2896 MHz, depending on sample rate. Slower clock rates can be used to ensure correct timing of the bus signals in applications where a large load capacitance is connected to the HGC SPI outputs.

The minimum idle period between HGC SPI transactions is configured using HGC_CSB_IDLE_DUR. The delay between the falling $\overline{CS}$ edge and the first SCK edge is configured using HGC_CSB_FALL_DLY. The minimum delay between the last SCK edge and the rising $\overline{CS}$ edge is configured using HGC_CSB_RISE_DLY.

In normal operation, the timing of the rising $\overline{CS}$ edge is controlled automatically by the zero-cross detection; the HGC_CSB_RISE_DLY field determines the minimum delay.

4.6.2 GPIO Configuration

External gain control using GPIO output is supported using pins GPIO1, HGC_CS/GPIO2, XTAL_IN/HGC_SDO/GPIO3, and XTAL_OUT/HGC_SCK/GPIO4, which must be configured for GPIO use if required. External gain configuration using the GPIO output is selected using HGC_CTRL_INTERFACE.

The GPIO pins are configured as outputs using OUTx_GPO1_SEL to OUTx_GPO4_SEL (where x indicates the channel number 1–2). Pins GPIO3 and GPIO4 are not available if the system clock is supplied by the crystal oscillator.

The GPIO pins are powered by VDD_IO2; see Table 3-8 for digital I/O levels.

4.6.3 Gain Control Optimization

The CS4332S provides tunable parameters to minimize any audible artifacts when changing the gain configuration. After configuring the external gain, by clocking out the HGC SPI bit pattern or configuring the required GPIO control fields, the CS4332S pauses the external gain change (by asserting the $\overline{CS}$ signal or maintaining the current GPIO output logic levels). The CS4332S then completes the required internal digital gain change. The digital gain change process is dependent on whether a positive or negative external gain change is required:

- If a positive gain change is required, the CS4332S waits for a zero-cross point in the affected audio channel before completing the digital gain step and ramp.
- If a negative gain step is required, the CS4332S ramps down the digital gain and then waits for the zero-cross point in the affected audio channel before completing the digital gain step.

Gain ramping is described in Section 4.6.5.

The CS4332S waits for a configurable external delay, to ensure the digital gain change has time to propagate through the DAC and any external delay (i.e., the output buffer and external amplifier), before completing the external gain change (by deasserting the $\overline{CS}$ signal or updating the GPIO output logic levels). This ensures the analog step is aligned with the zero-cross point, reducing any audible artifacts. The external delay is configured using OUT_EXT_GAIN_DLY. A timeout for zero-cross point detection is configured using OUT_ZC_TIMEOUT.

4.6.4 Audio Channel Gain Control

The host processor configures the external analog and internal digital gain for each audio channel by writing to the respective OUTx_ANA_GAIN, and OUTx_DIG_GAIN fields.

The host must also write the OUTx_BIT_PATT fields to provide the bit pattern to configure the external device for the required analog gain. If the GPIOs are used, the GPIO output logic levels are determined by bits 12–15 of the OUTx_BIT_PATT_1 fields.

Note: The OUTx_BIT_PATT bit pattern is a maximum of 32 bits (the size is configured using OUTx_BIT_PATT_LENGTH). If the bit pattern is 16 bits or less, it is stored in the OUTx_BIT_PATT_1 field. The MSB represents the first-transmitted bit of the pattern; one or more of the LSBs may be unused, depending on the size of the bit pattern. If the bit pattern is more than 16 bits, the remaining bits are stored in OUTx_BIT_PATT_0.

The analog and digital gain settings do not become effective immediately on updating the control fields. Writing 1 to OUTx_UPDATE initiates the update for the respective audio channel and queues the update to be applied; the CS4332S services each updated channel in turn and applies the respective gain settings at the earliest opportunity, dependent on the zero-cross detection for each affected channel.

The HGC_BUSY_STS bit, if set, indicates that gain updates are pending for one or more audio channels (i.e., gain settings have been written to the CS4332S, but not yet applied to the respective audio paths). The bit is cleared automatically when all updates have been applied to the respective channels.

The gain settings, including external gain bit patterns or GPIO output level settings, for each audio channel can be written at any time, regardless of whether an earlier update is currently pending for that channel.

If an audio channel is enabled, but does not have any associated HGC SPI- or GPIO-controlled external gain circuit, the external and internal analog gain and digital gain for the respective channel must be maintained at 0 dB (default).

For efficiency of the host-processor interactions, the output path bit pattern and gain fields can be written as a contiguous block (i.e., one auto-incrementing I²C/SPI write operation). The OUTx_UPDATE bits can be set in the same I²C/SPI operation as writing to the corresponding OUTx_DIG_GAIN bits.

Note: If the OUTx_UPDATE bits are written 0 when updating the gains or bit-pattern fields, the settings are latched internally but the updates are not applied to the audio path and do not cause the HGC_BUSY_STS bit to be set. Writing 0 to OUTx_UPDATE is used in the initialization steps described in Section 4.6.7. Prior to writing 1 to any of the OUTx_UPDATE bits, HGC must be initialized as described in Section 4.6.7.

4.6.5 Gain Ramping Control

The CS4332S supports independent control of the external analog and digital gain stages of the output path. When the digital gain is updated, the gain is ramped up or down to the new value. When the external analog gain is updated, the CS4332S uses digital control to provide a ramped response, masking the larger step size of the analog gain.

For example, if the external analog gain is decreased by –3 dB, the digital gain is smoothly ramped up by 3 dB gain. Following this the analog gain increase is canceled out by decreasing the digital gain by –3 dB.Gain ramping is supported for changes in analog gain up to a maximum step size of ±32 dB. The digital adjustment used to cancel the initial analog step is supported using a combination of the digital gain and digital volume functions.

Note there is no restriction on whether the external and internal gains are updated in the same operation—the gain ramping is supported for all combinations.

The gain ramping is illustrated in Fig. 4-8.

In Fig. 4-7, the initial overall gain is 2 dB and a gain of 4 dB is required. The analog gain is updated by +3 dB from 0 dB to 3 dB. The digital gain is initially set to –1 dB, providing the -3 dB counter step to the analog gain step, and then ramped to +1 dB. This gives a smooth transition from 2 dB to 4 dB in the overall (analog + digital) response.

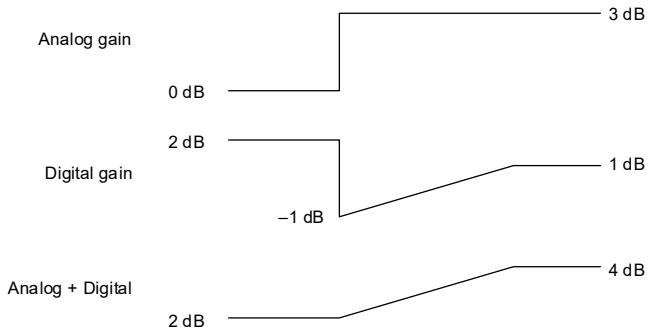


Figure 4-7. Positive Gain Ramping

In Fig. 4-8, the initial overall gain is 5 dB and an overall gain of 1 dB is required. The analog gain is updated by -3 dB from 3 dB to 0 dB. The digital gain ramps down by 4 dB from 2 dB to -2 dB and then steps up by +3 dB, providing the analog counter step. This gives an smooth transition from 5 dB to 1 dB in the overall (analog + digital) response,

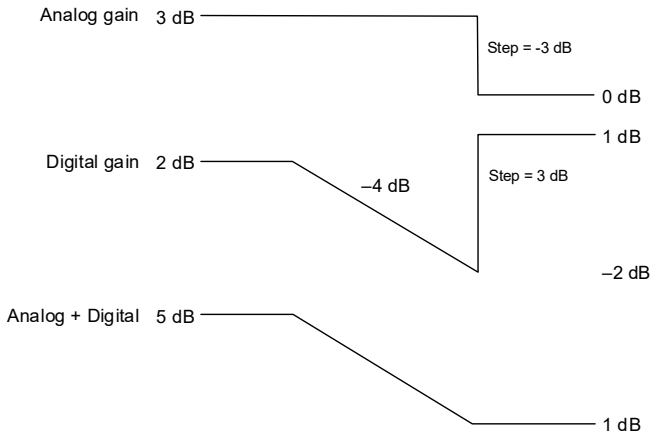


Figure 4-8. Negative Gain Ramping

The digital gain counter step and ramp response is configured using OUT_STEP_RAMP_EN. If this bit is set, the CS4332S applies the digital gain counter step to mask the analog gain steps. If this bit is clear, there is no masking of the analog gain steps.

For increasing gain, the ramp rate is controlled by OUT_RAMP_RATE_INC; for decreasing gain, the rate is controlled by OUT_RAMP_RATE_DEC.

Notes: If the digital gain ramping is enabled, (OUT_STEP_RAMP_EN = 1), the volume increasing/decreasing ramp rates must be set to nonzero values. See Section 4.5.2 to configure the volume ramp rates.

The OUT_RAMP_RATE_INC and OUT_RAMP_RATE_DEC fields should not be changed while a volume ramp is in progress.

4.6.6 Auxiliary Device Control

Auxiliary device control is supported if the HGC SPI control interface is used, for details refer to Section 4.6.1. The host processor configures the auxiliary devices by writing to the respective AUXx_BIT_PATT fields. Each field contains the bit pattern to configure the respective external device as required.

Note: The bit pattern is a maximum of 32 bits (the size is configured using AUXx_BIT_PATT_LENGTH). If the bit pattern is 16 bits or less, it is stored in the AUXx_BIT_PATT_1 field. The MSB represents the first-transmitted bit of the pattern; one or more of the LSBs may be unused, depending on the size of the bit pattern. If the bit pattern is more than 16 bits, the remaining bits are stored in AUXx_BIT_PATT_0.

If the auxiliary bit patterns are updated, the new settings are latched internally and are not reflected in the SPI data output until a 1 is written to HGC_INIT_UPDATE. The host processor must confirm that the gain controller is idle (HGC_BUSY_STS = 0) before writing to HGC_INIT_UPDATE.

4.6.7 Initialization

Hybrid gain control must be initialized to ensure correct gain-ramping behavior. The host processor should configure the bit patterns and all gain fields for all channels—writing OUTx_UPDATE = 0 for each audio channel—and then write 1 to HGC_INIT_UPDATE to transmit the bit patterns and initialize the internal gain-control algorithms. If a pending update (OUTx_UPDATE = 1) is superseded by another update (OUTx_UPDATE = 0), the former is ignored. Note that the host processor must confirm that the gain controller is idle (HGC_BUSY_STS = 0) before writing to HGC_INIT_UPDATE.

Note: There is no zero-cross detection when using HGC_INIT_UPDATE, so audible artifacts may occur. It is recommended to mute all audio channels (using OUTx_MUTE) to suppress any unintended transients.

Writing to HGC_INIT_UPDATE has no effect if HGC_BUSY_STS = 1, indicating that gain updates are pending for one or more audio channels. The host processor can cancel any pending gain updates by writing 1 to HGC_ABORT—this can be used to return the controller to the idle state as quickly as possible, in readiness for initializing the system with a new configuration.

If the HGC_ABORT bit is written, the CS4332S does not become idle until it has finished applying the updates to the audio channel currently being processed. The host processor must always check the controller is idle (HGC_BUSY_STS = 0) before writing to HGC_INIT_UPDATE.

Note: Any gain updates that are canceled using the HGC_ABORT bit may result in an inconsistency between the register map and the respective gain settings. The HGC_ABORT bit should only be used as part of a control sequence that also uses HGC_INIT_UPDATE to apply a new configuration to all channels.

4.6.8 HGC Interrupts

The HGC function provides inputs to the interrupt controller, as described in Section 4.11. An interrupt is triggered if any of the following interrupt bits are set:

- HGC_SPI_ERROR_INT: indicates an invalid (zero-length) SPI transaction
- HGC_ABORT_ERROR_INT: the HGC operation has been aborted using the HGC_ABORT bit
- HGC_ERROR_INT: indicates a gain update error
- HGC_DONE_INT: indicates gain updates have completed successfully

These bits are latching fields which, once set, remain set until a 1 is written to the respective bit; these bits can be polled at any time or in response to the interrupt being asserted.

4.7 Digital Filter Selection

The DAC output path incorporates an interpolation filter and a high-pass filter. Six types of filter are supported:

- Fast roll-off, minimum phase
- Fast roll-off, linear phase
- Slow roll-off, minimum phase
- Slow roll-off, linear phase
- Balanced roll-off, minimum phase
- Balanced roll-off, linear phase

The phase-responses are characterized as follows:

- The **minimum-phase** filters offer the lowest latency and an impulse response with no pre-ringing, at the expense of potential in-band phase distortion.
- The **linear-phase** filters have no phase distortion, but also higher latency and a symmetric impulse response.

The frequency-response options are characterized as follows:

- The **fast roll-off** filters maximize the audio signal bandwidth (as a function of the selected sample rate). The fast roll-off filters also provide deep stopband attenuation in the DAC output path.The signal bandwidth and stopband attenuation are prioritized over impulse response and group delay. The deep stopband attenuation minimizes out-of-band noise and aliased signal content.
- The **slow roll-off** filters are optimized for impulse response and group delay, with flat passband over the audible range to 20 kHz. The slow roll-off filters provide a more relaxed stopband specification in the DAC output path. The enhanced impulse response may improve perceived sound quality, especially for transient signal content.
- The **balanced roll-off** filters offer a superior impulse response and group delay as compared with the fast roll-off filters, while retaining a flat passband over the audible range to 20 kHz and deep stopband attenuation.

The DAC output path supports filter options for different sample rates as indicated in Table 4-9.

Table 4-9. Digital Filter Options

Description	Sample Rate (kHz)									
	16	32	44.1	48	88.2	96	176.4	192	352.8	384
Fast roll-off, minimum phase	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Fast roll-off, linear phase	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Slow roll-off, minimum phase	—	—	Yes	Yes	Yes	Yes	Yes	Yes	—	—
Slow roll-off, linear phase	—	—	Yes	Yes	Yes	Yes	Yes	Yes	—	—
Balanced roll-off, minimum phase	—	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes
Balanced roll-off, linear phase	—	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes

In hardware control mode, the filter selection is determined by the CONFIG5 pin (see Section 4.2).

In software (I²C/SPI) control mode, the interpolation filter is selected using OUT_FILTER_SEL; the high-pass filter is enabled using OUT_HPF_EN.

A deemphasis filter can also be enabled in the DAC output path. The filter provides standard *Red Book* deemphasis, with corner frequencies corresponding to 15 µs/50 µs time constants, as illustrated in Fig. 4-9.

The deemphasis filter is supported for 16 kHz, 32 kHz, 44.1 kHz, and 48 kHz sample rates. The filter is enabled using OUT_DEEMPH_EN. If the sample rate is 44.1 kHz or 48 kHz, the applicable rate must be configured using OUT_DEEMPH_FILT_SEL.

Note: The deemphasis filter is not supported for sample rates above 48 kHz; enabling the filter at sample rates higher than 48 kHz has no effect.

The de-emphasis filter response is illustrated in Fig. 4-9.

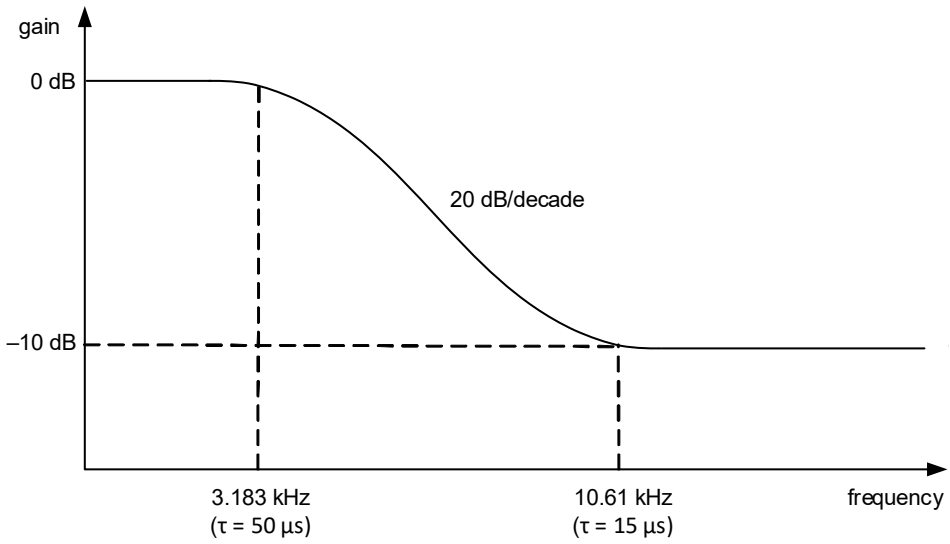


Figure 4-9. Deemphasis Filter Response

Note: The interpolation and deemphasis filters are not supported on the DSD signal path (see Section 4.9).

4.8 Audio Serial Port (ASP)

The multichannel ASP supports the input of digital audio samples to the CS4332S. The ASP can be configured as a primary or secondary interface, and supports I²S, left-justified, and TDM data formats.

In hardware control mode, the ASP data format is determined by the CONFIG1 and CONFIG2 pins (see Section 4.2). In software (I²C/SPI) control mode, the ASP data format is configured using register fields.

In hardware mode, sample rates 16 kHz–192 kHz are supported (sample rates 16 kHz and 32 kHz are supported using autodetect in ASP Secondary Mode only). In software mode, sample rates 16 kHz–384 kHz are supported; sample rate 384 kHz is not supported by autodetect. The supported sample rates in ASP Primary Mode and ASP Secondary Mode are summarized in Table 4-10.

Table 4-10. Supported Sample Rates in ASP Primary Mode and ASP Secondary Mode

	ASP Primary Mode		ASP Secondary Mode	
Sample Rate (kHz)	**Hardware Control Mode**	**Software Control Mode**	**Hardware Control Mode**	**Software Control Mode**
16–32	—	Configurable using SAMPLE_RATE	Determined using autodetect only	Configurable using SAMPLE_RATE (autodetect available)
44.1–192	Determined by CONFIG1 pin			
352.8, 384	—		—	Configurable using SAMPLE_RATE (autodetect not available)

Note: The ASP interface is not supported if the DSD interface is enabled (see Section 4.9).

4.8.1 Primary and Secondary Operation

The ASP interface can operate as a primary or secondary interface. In the primary configuration, the BCLK and FSYNC signals are generated by the CS4332S. In the secondary configuration, the BCLK and FSYNC pins are inputs, allowing another device to drive the respective signals.

In ASP Secondary Mode, the external clocks (MCLK, BLCK, and FSYNC) must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important.

If clocking is provided by the crystal oscillator and the CS4332S is operating in ASP Secondary Mode, then the FSYNC and the BCLK signals should be derived from the common clock source provided by the CS4332S MCLK output.

In hardware control mode, the ASP is configured as a primary or secondary interface using the CONFIG1 pin (see Section 4.2). In software control mode, the ASP primary/secondary configuration is selected using ASP_PRIMARY.

The ASP operation as a primary or secondary interface with MCLK as the clocking source is illustrated in Fig. 4-10 and Fig. 4-11.

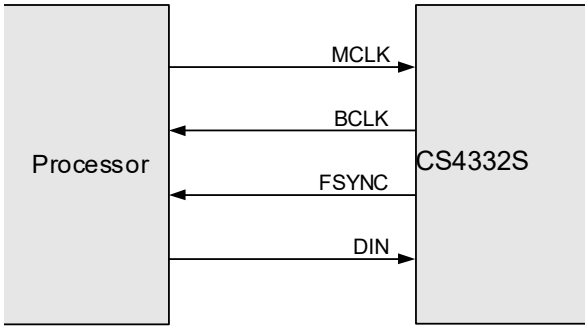


Figure 4-10. Primary Mode, MCLK Clocking Source

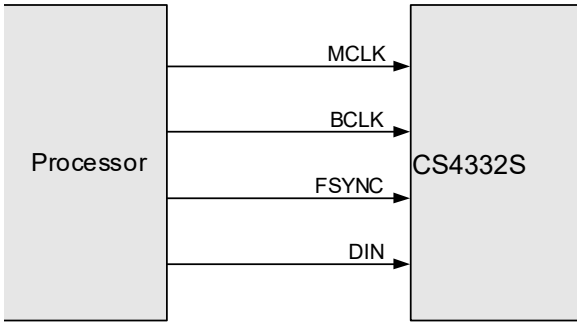


Figure 4-11. Secondary Mode, MCLK Clocking Source

The ASP operation as a primary or secondary interface with a crystal as the clocking source is illustrated in Fig. 4-12 and Fig. 4-13.

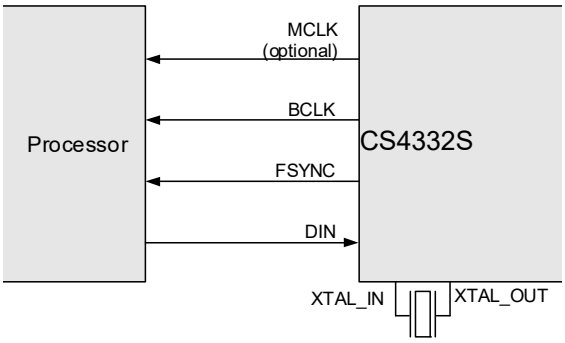


Figure 4-12. Primary Mode, XTAL Clocking Source

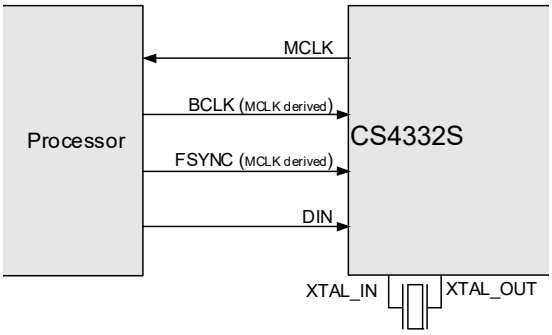


Figure 4-13. Secondary Mode, XTAL Clocking Source

4.8.2 ASP Data Formats

The ASP interface can be configured to operate in I²S, left-justified, or TDM data formats as illustrated in Fig. 4-14 through Fig. 4-16. The data-bit order is MSB first in each case; data words are encoded in 2's complement (signed, fixed-point) format. Each audio sample is allocated a time slot within the FSYNC frame.

- In I²S Mode, the MSB is valid on the second BCLK rising edge following an FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  I²S Mode data format is shown in Fig. 4-14.

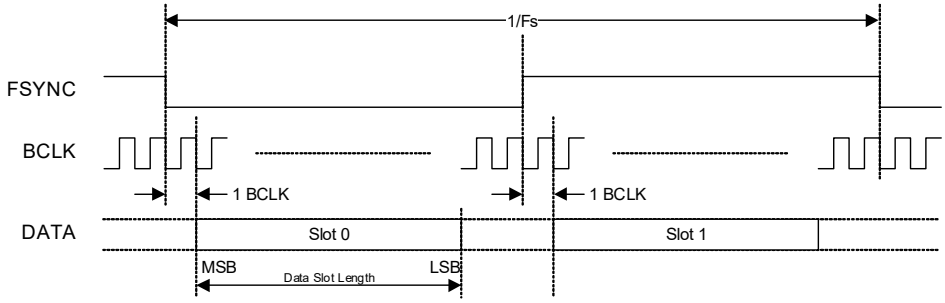


Figure 4-14. I²S Data Format

- In Left-Justified Mode, the MSB is valid on the first BCLK rising edge following an FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  Left-Justified Mode data format is shown in Fig. 4-15.

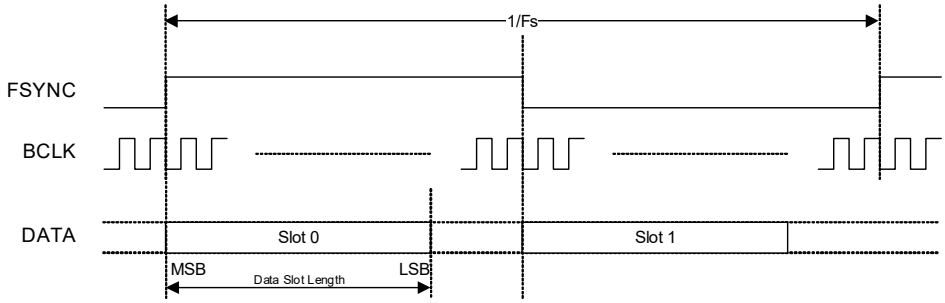


Figure 4-15. Left-Justified Data Format

- In TDM Mode, if the ASP is configured in Secondary Mode, the MSB of the first channel is valid on the second BCLK rising edge following a rising FSYNC edge. The other bits up to the LSB are valid on each successive BCLK cycle.

  If the ASP is configured in Primary Mode, the FSYNC signal can be configured as a pulse (default) or a square wave (with a 50% duty cycle). If the FSYNC signal is configured as a pulse, the MSB of the first channel is valid on the second BCLK rising edge following a rising FSYNC edge. The other bits up to the LSB are valid on each successive BCLK cycle.

  In ASP Secondary Mode and in ASP Primary Mode with the FSYNC signal configured as a pulse, the subsequent channels follow immediately after the first channel. The pulse duration can be anything less than 1/Fs, provided the falling edge of the frame pulse occurs at least one BCLK period before the rising edge of the next frame pulse. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  TDM Mode data format in ASP Secondary Mode and ASP Primary Mode with FSYNC configured as a pulse is shown in Fig. 4-16.

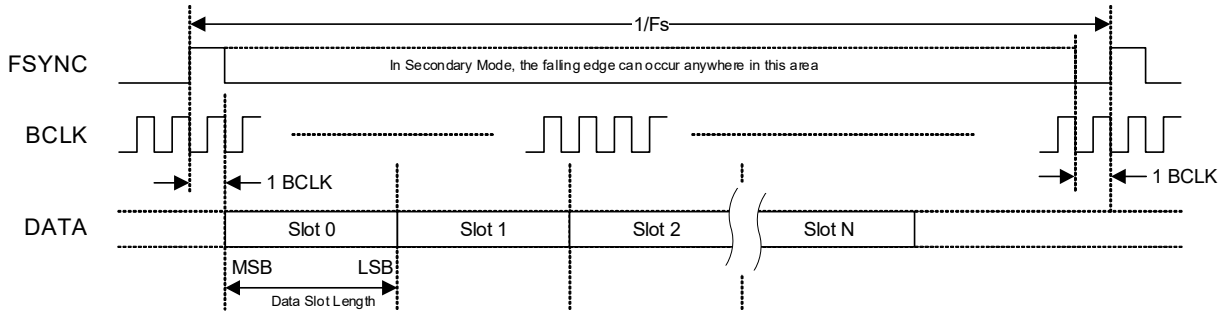


Figure 4-16. TDM Data Format Primary Mode (FSYNC = Pulse) and Secondary Mode

  In ASP Primary Mode with the FSYNC signal configured as a square wave, the slots are aligned with both rising and falling edges of FSYNC and half of the available slots occur within each phase of the FSYNC cycle. The total number of available slots is determined by the sample rate, as described in Table 4-11.

- The MSB of the first channel in each phase of the FSYNC cycle is valid on the second BCLK rising edge following the rising and falling FSYNC edge respectively. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, sample rate, and number of available slots, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  TDM Mode data format in ASP Primary Mode with FSYNC configured as a square wave is shown in Fig. 4-17.

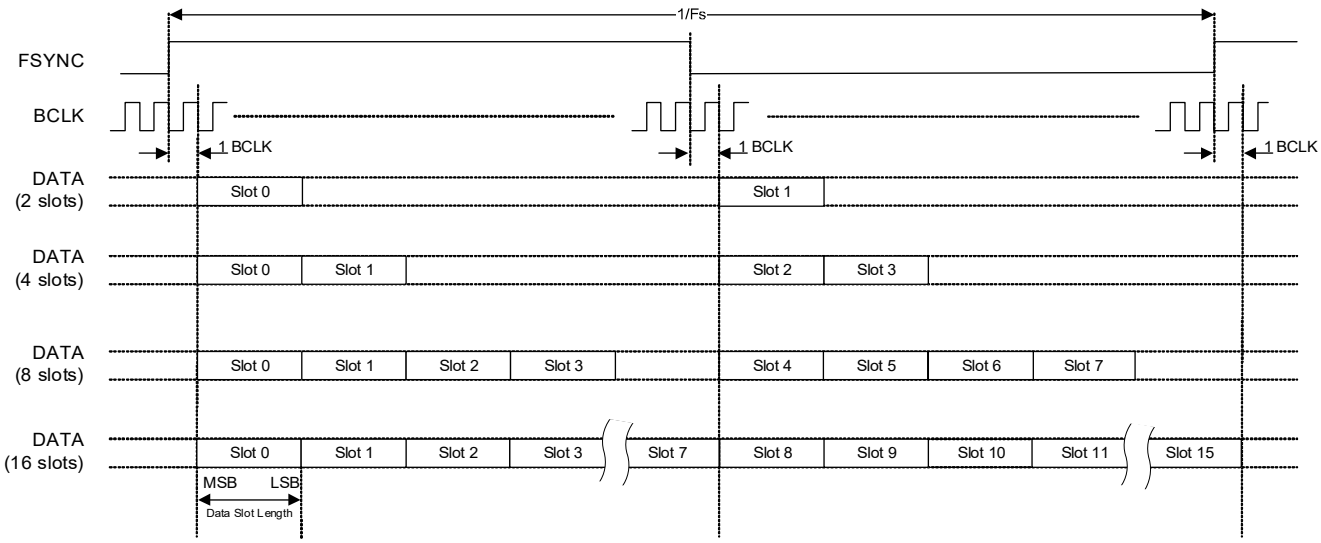


Figure 4-17. TDM Data Format Primary Mode (FSYNC = Square Wave)

4.8.3 ASP Configuration

In hardware control mode, the ASP data format is determined by the CONFIG1 and CONFIG2 pins (see Section 4.2).

In software control mode, the ASP data format is configured using SAMPLE_RATE, and ASP_FORMAT. If ASP Primary Mode is selected (see Section 4.8.1), the BCLK frequency is configured using ASP_BCLK_FREQ and the FSYNC waveform type (pulse or square wave) is configured using ASP_FSYNC_TYPE.

In software control mode, the BCLK polarity is selected using ASP_BCLK_INV. The polarity selection is valid in Primary and Secondary Modes, and determines whether the data is valid for sampling on the rising edge or the falling edge.

The BCLK polarity is illustrated in Fig. 4-18 and Fig. 4-19. In hardware control mode, the BCLK polarity is assumed to be noninverted.

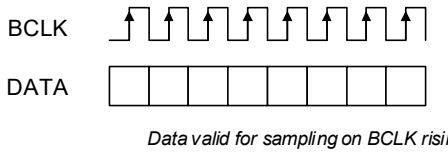


Figure 4-18. Noninverted BCLK

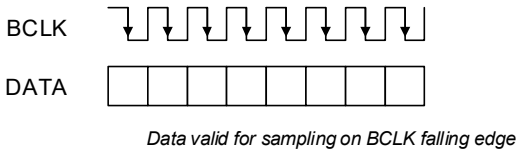


Figure 4-19. Inverted BCLK

In TDM Mode, the two data-format options are supported as follows:

- TDM Mode—minimum slots. The ASP data format is configured to support two slots. This mode allows the BCLK rate to be as low as possible, equating to a minimum of 128 BCLK cycles per audio sample at a minimum sample rate of 64 Fs.
- TDM Mode—maximum time slots. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate. The mode is designed for the maximum BCLK rate (22.5792 MHz for 44.1 kHz-related sample rates, or 24.576 MHz for 48 kHz-related sample rates), enabling the maximum possible bandwidth on the ASP data bus to be shared with other devices.

The ASP configuration depends on the sample rate and the selected data format as described in Table 4-11.

Table 4-11. ASP Data Format

ASP Format [1]	ASP Sample Rate [2,3]	Time Slots per Frame [4]	BCLK Rate[5,6]
I²S, Left-Justified	16 kHz	2	BCLK ≥ 64×Fs[7]
	32 kHz		BCLK ≥ 64×Fs[8]
	44.1 kHz, 48 kHz		BCLK ≥ 64×Fs
	88.2 kHz, 96 kHz		BCLK ≥ 64×Fs
	176.4 kHz, 192 kHz		BCLK ≥ 64×Fs
	352.8 kHz, 384 kHz		BCLK ≥ 64×Fs
	Autodetect (16 kHz–192 kHz)		BCLK ≥ 64×Fs
TDM—minimum time slots	16 kHz		BCLK ≥ 64×Fs[7]
	32 kHz		BCLK ≥ 64×Fs[8]
	44.1 kHz, 48 kHz		BCLK ≥ 64×Fs
	88.2 kHz, 96 kHz		BCLK ≥ 64×Fs
	176.4 kHz, 192 kHz		BCLK ≥ 64×Fs
	352.8 kHz, 384 kHz		BCLK ≥ 64×Fs
	Autodetect (16 kHz–192 kHz)		BCLK ≥ 64×Fs
TDM—maximum time slots	16 kHz	16	BCLK ≥ 512×Fs[7]
	32 kHz		BCLK ≥ 512×Fs[8]
	44.1 kHz, 48 kHz		BCLK = 512×Fs
	88.2 kHz, 96 kHz	8	BCLK = 256×Fs
	176.4 kHz, 192 kHz	4	BCLK = 128×Fs
	352.8 kHz, 384 kHz	2	BCLK = 64×Fs
	Autodetect (16 kHz–192 kHz)	4	BCLK ≥ 128×Fs

1.The ASP format is selected using the CONFIG2 pin (in hardware control mode) or ASP_FORMAT (in software control mode).

2. The sample rate is selected using the CONFIG1 pin (in hardware control mode) or SAMPLE_RATE (in software control mode).
3. Sample rates 16 kHz–192 kHz are supported in hardware and software control modes; sample rate 384 kHz is supported in software control mode only.
4. Time slots per frame is the number of data-sample time slots supported on the DIN pin.
5. The BCLK rate must be a constant integer multiple of the sample rate (Fs).
6. In ASP Primary Mode (hardware control), the BCLK frequency is the minimum specified rate. In ASP Primary Mode (software control), the BCLK frequency is configured using ASP_BCLK_FREQ.
7. In ASP Primary Mode, the specified minimum BCLK frequency for 16 kHz sample rate is not supported. The available options correspond to 192×Fs, 384×Fs, 768×Fs, or 1536×Fs
8. In ASP Primary Mode, the specified minimum BCLK frequency for 32 kHz sample rate is not supported. The available options correspond to 96×Fs, 192×Fs, 384×Fs, or 768×Fs.

The ASP data format in I²S, Left-Justified, and TDM interface modes as illustrated in Fig. 4-20 through Fig. 4-23. Refer to Table 4-11 for the applicable definition.

- If I²S data format is selected, the ASP supports audio channels 1–2 as shown in Fig. 4-20. The minimum BCLK rate is 64×Fs (where Fs is the sample rate). In ASP Primary Mode, the minimum BCLK rate of 64×Fs is not supported for sample rates of 16 kHz or 32 kHz. A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

  The input data is provided on ASP_DIN.

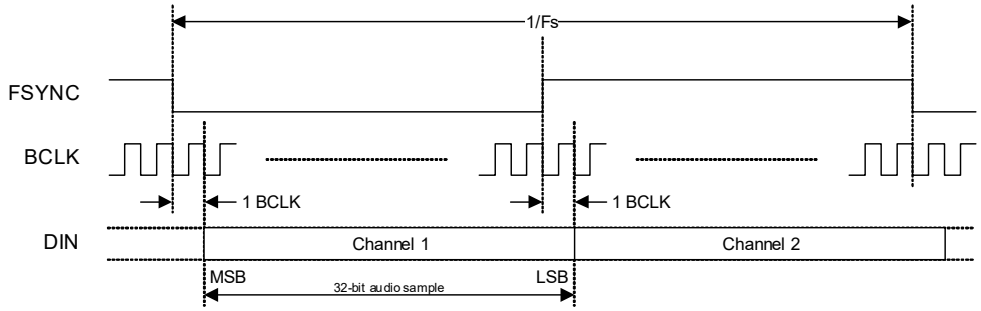


Figure 4-20. I²S Data Format

- If Left-Justified data format is selected, the ASP supports audio channels 1–2 as shown in Fig. 4-21. The minimum BCLK rate is 64×Fs (where Fs is the sample rate). In ASP Primary Mode, the minimum BCLK rate of 64×Fs is not supported for sample rates of 16 kHz or 32 kHz. A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

  The input data is provided on ASP_DIN.

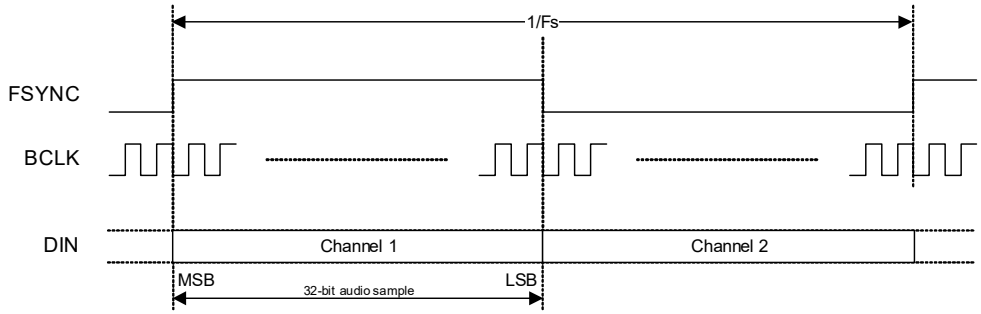


Figure 4-21. Left-Justified Data Format

- In TDM Mode, the FSYNC frame is configured for 2, 4, 8, or 16 slots as specified in Table 4-11.

  In 4-, 8-, and 16-slot modes, the slot assignment for audio channels 1–2 is selected using the CONFIG3 pin (in hardware control mode—see Section 4.2) or else using ASP_TDM_SLOT (in software control mode). In 2-slot modes, the default slot assignment (slots 0–1) should be selected.

  The BCLK rate is related to the sample rate (Fs) as described in Table 4-11. Where applicable, the BCLK rate can be higher than the stated minimum, resulting in additional unused BCLK cycles between the last slot in the frame and the start of the next frame.

The input data is provided on ASP_DIN.

An example of the 4-slot TDM format in ASP Secondary Mode and in ASP Primary Mode with the FSYNC signal configured as a pulse is shown in Fig. 4-22. In this example, audio channels 1–2 occupy TDM slots 0–1 respectively.

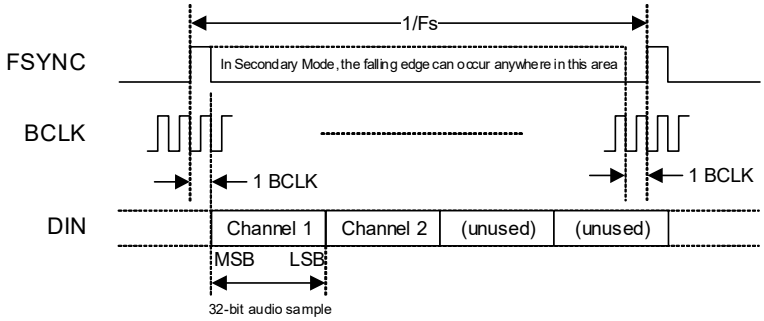


Figure 4-22. TDM Data Format, 4-Slot Example (FSYNC = Pulse)

An example of the 4-slot TDM format in ASP Primary Mode with the FSYNC signal configured as a square wave is shown in Fig. 4-23. In this example, audio channels 0 and 1 occupy TDM slots 0 and 1 in the high (Logic 1) phase of the FSYNC signal, TDM slot 0 and 1 in the low (Logic 1) phase of the FSYNC signal are unused.

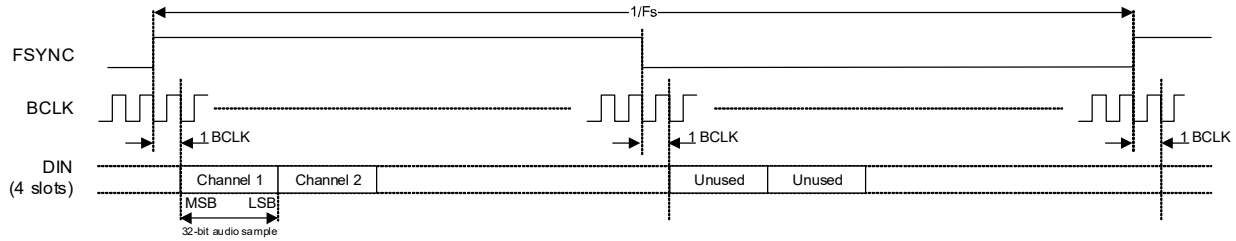


Figure 4-23. TDM Data Format, 4-Slot Example (FSYNC = Square Wave)

4.9 DSD Interface

Direct Stream Digital (DSD) is a high-resolution audio-coding standard that employs 1-bit sampling at high oversample rates. The DSD interface uses noise shaping and other filters to decode the data for the purposes of analog audio playback. The CS4332S supports a two-channel DSD interface.

The DSD interface supports digital input at oversample rates up to 256×Fs. Phase modulation of the digital input is also supported at 64×Fs oversample rate. A selectable high-pass filter is provided in the DSD signal path.

Note the DSD interface is supported in software control mode only.

4.9.1 DSD Enable

The DSD interface is enabled using DSD_EN. The ASP interface (see Section 4.8) is disabled if the DSD interface is enabled.

The DSD interface supports two-channel input using the respective DSD_DINn data pins. The timing of the DSD data is supported using the DSD_CLK clock input. The DSD interface connections are illustrated in Fig. 4-24.

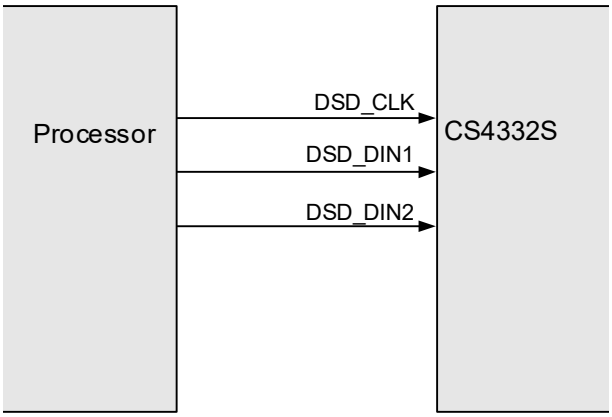


Figure 4-24. DSD Interface Connection

4.9.2 DSD Format

The DSD interface format is shown in Fig. 4-25. In this default configuration, a new data bit is received on each falling CLK edge, for sampling at the next rising edge. See Table 3-12 for timing specifications.

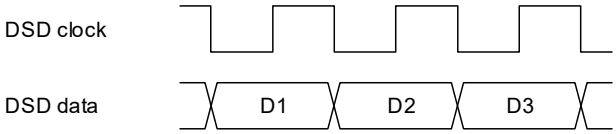


Figure 4-25. DSD Interface Timing

The oversample rate is configured using DSD_OSR. This field must be configured to match the DSD input stream. Oversample rates 64×Fs, 128×Fs, and 256×Fs rates are supported (where Fs = 44.1 kHz).

The CS4332S supports DSD phase modulation, where the DSD data is represented in *data plus data-inverted* format as shown in Fig. 4-26. Phase modulation is configured using DSD_PM_EN. Phase modulation is supported for 64×Fs data rate only.

If phase modulation is enabled, the DSD clock rate is configured using DSD_PM_SEL. By default, the clock rate is 128×Fs (i.e., 2 x OSR rate). The clock rate can be adjusted to 64×Fs if required.

The phase-modulation data formats are shown in Fig. 4-26 and Fig. 4-27.

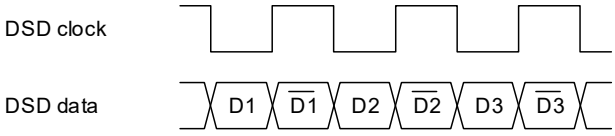


Figure 4-26. DSD Phase Modulation—64×Fs CLK

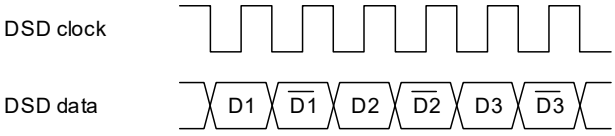


Figure 4-27. DSD Phase Modulation—128×Fs CLK

4.9.3 Signal Level Control

The scaling of the DSD signal level, relative to the full-scale level of the CS4332S DAC output path, is configurable using DSD_ZERODB. The scaling is defined with reference to the SACD standard for DSD signal levels.

4.9.4 High-Pass Filter

A high-pass filter is incorporated in the DSD signal path. The filter is enabled using DSD_HPF_EN. The filter is enabled by default.

Note: The digital filters described in Section 4.7 are not supported on the DSD path.

4.10 I²C/SPI Control Port

The CS4332S incorporates a control port, supporting I²C or SPI modes of operation; this is selected using CONFIG1, as described in Table 4-1. If the SPI control interface is required, it is recommended to use a pull-up resistor of 100 kΩ. In software control mode, the CS4332S is configured by writing to control registers using the control port.

The control port is automatically configured in I²C mode or SPI mode following the first valid I²C/SPI activity detected after power-on or hardware reset.

4.10.1 I²C Control Port

The I²C control port is supported using the following pins, which must be configured for the I²C function if required:

- CONFIG2/SPI_SDI/I2C_SDA
- CONFIG3/SPI_SDO/I2C_SCL

The CS4332S is a target device on the I²C bus—SCL is a clock input, while SDA is a bidirectional data pin. To allow arbitration of multiple targets (and/or multiple controllers) on the same interface, the CS4332S transmits Logic 1 by tristating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the Logic 1 can be recognized by the controller.

In order to allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit device address (this is not the same as the address of each register in the CS4332S). The LSB of the device address is the read/write bit; this bit is set to Logic 1 for read and Logic 0 for write.

The I²C device address is configured using the CONFIG1 pin as described in Table 4-12.

Table 4-12. I2C Address Selection—CONFIG1 pin

Pin Configuration		I2C Address
Pull-up to VDD_IO1	0 kΩ	0x36 (write), 0x37 (read)
	4.7 kΩ	0x34 (write), 0x35 (read)
	22 kΩ	0x32 (write), 0x33 (read)
	100 kΩ	0x30 (write), 0x31 (read)

The host device indicates the start of data transfer with a high-to-low transition on SDA while SCL remains high. This indicates that a device address and subsequent address/data bytes follow. The CS4332S responds to the start condition and shifts in the next 8 bits on SDA (8-bit device address, including read/write bit, MSB first). If the device address received matches the device address of the CS4332S, the CS4332S responds by pulling SDA low on the next clock pulse (ACK). If the device address is not recognized or the R/W bit is set incorrectly, the CS4332S returns to the idle condition and waits for a new start condition.

If the device address matches the device address of the CS4332S, the data transfer continues. The controller indicates the end of data transfer with a low-to-high transition on SDA while SCL remains high. After receiving a complete address and data sequence the CS4332S returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e., SDA changes while SCL is high), the device returns to the idle condition.

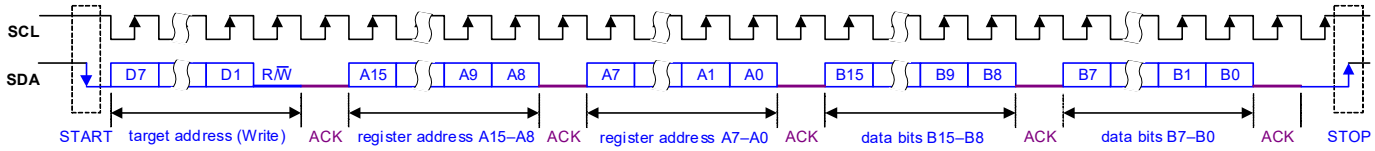
The I²C interface uses a 16-bit register address and 16-bit data words. The register address must be aligned to a 16-bit word boundary (i.e., the LSB must be 0). The full I²C message protocol also includes a device address, a read/write bit, and other signaling bits (see Fig. 4-28 and Fig. 4-29).

The CS4332S supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. In these modes, the CS4332S automatically increments the register address after each data word. Successive data words can be input/output every two data bytes.

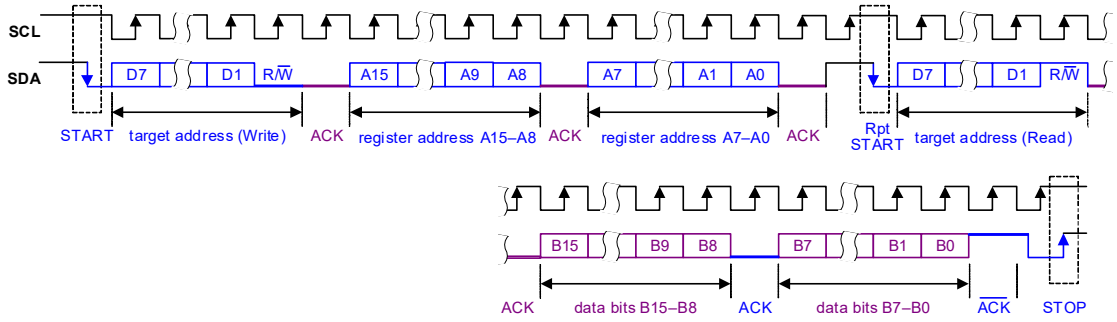
The I²C protocol for a single, 16-bit register write operation is shown in Fig. 4-28.



Note: The SDA pin is used as input for the control register address and data; SDA is pulled low by the receiving device to provide the acknowledge (ACK) response

Figure 4-28. Control Interface I²C Register Write

The I²C protocol for a single, 16-bit register read operation is shown in Fig. 4-29.



Note: The SDA pin is driven by both the controller and target devices in turn to transfer target address, register address, data and ACK responses

Figure 4-29. Control Interface I²C Register Read

The control interface also supports other register operations; the interface protocol for these operations is shown in Fig. 4-30 through Fig. 4-33. The terminology used in the following figures is detailed in Table 4-13.

Table 4-13. Control Interface (I2C) Terminology

Terminology	Description
S	Start condition
Sr	Repeated start
A	Acknowledge (SDA low)
$\overline{A}$	No Acknowledge (SDA high)
P	Stop condition
R/$\overline{W}$	Read/not Write: 0 = Write, 1 = Read
[White field]	Data flow from bus controller to CS4332S
[Gray field]	Data from CS4332S to bus controller

Fig. 4-30 shows a single register write to a specified address.

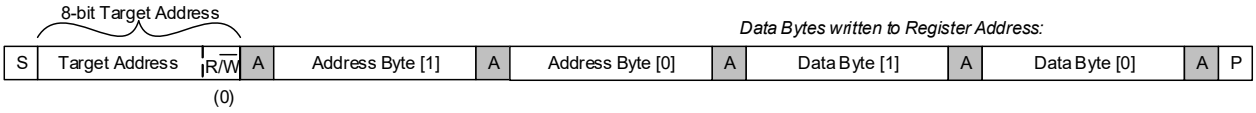


Figure 4-30. Single-Register Write to Specified Address

Fig. 4-31 shows a single register read from a specified address.

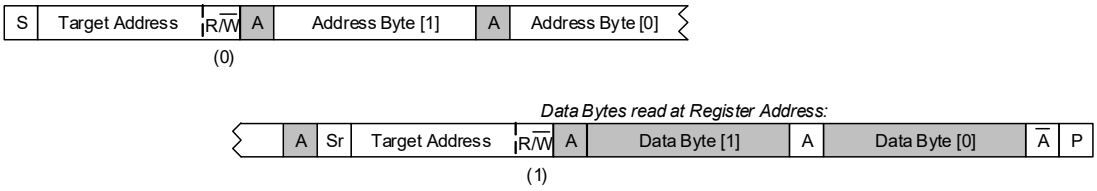


Figure 4-31. Single-Register Read from Specified Address

Fig. 4-32 shows a multiple register write to a specified address.

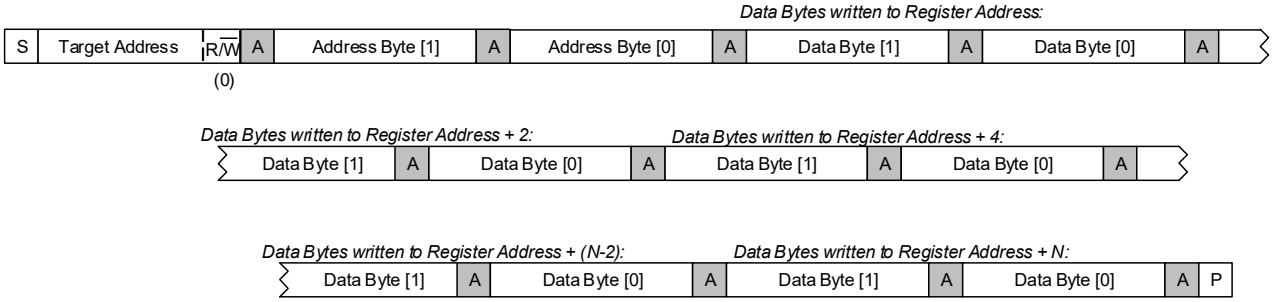


Figure 4-32. Multiple-Register Write to Specified Address

Fig. 4-33 shows a multiple register read from a specified address.

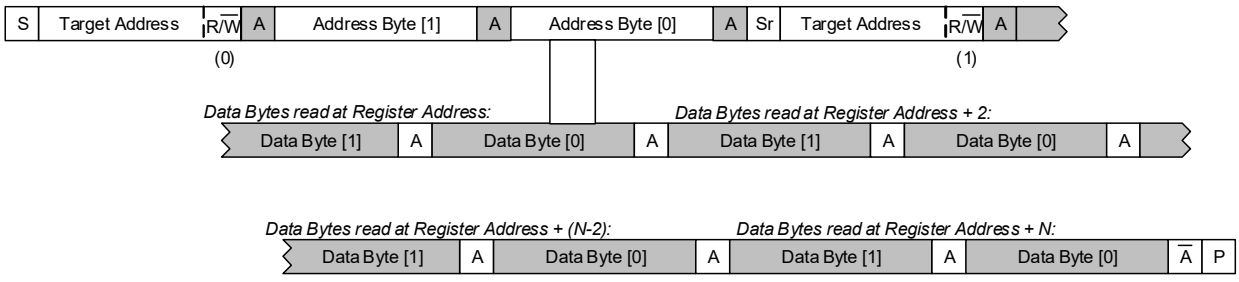


Figure 4-33. Multiple-Register Read from Specified Address

4.10.2 SPI Interface

The SPI interface is supported using the following pins, which must be configured for the SPI function if required:

- CONFIG1/$\overline{\text{SPI\_CS}}$
- CONFIG2/SPI_SDI/I2C_SDA
- CONFIG3/SPI_SDO/I2C_SCL
- CONFIG5/SPI_SCK

To ensure that the control port is inactive prior to use, SPI_CS must be deasserted (i.e., Logic 1) during device startup; RESET must remain asserted (i.e., Logic_0) until SPI_CS is deasserted (i.e., Logic_1), timing information is provided in Table 3-10.

The SDI (data-input) pin supports the following behavior:

- In write operations (R/W = 0), the SDI pin input is driven by the controlling device.
- In read operations (R/W = 1), the SDI pin is ignored following receipt of the valid register address.

The SDO (data-output) pin supports the following behavior:

- If CS is asserted (Logic 0), the SDO output is actively driven when outputting data and is high impedance at other times. If CS is not asserted, the SDO output is high impedance.
- The high-impedance state of the SDO output allows the pin to be shared with other peripheral devices.
- The output (SDO) data bit is available to the host device at the rising edge of SCK. See Table 3-14 for timing information.

The SPI interface uses a 15-bit register address and 16-bit data words. The full SPI message protocol also includes a read/write bit and a 16-bit padding phase (see Fig. 4-34 and Fig. 4-35).

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS4332S automatically increments the register address at the end of each data word, for as long as CS is held low and SCK is toggled. Successive data words can be input/output every 16 clock cycles.

The SPI protocol is shown in Fig. 4-34 and Fig. 4-35.

Fig. 4-34 shows a single register write to a specified address.

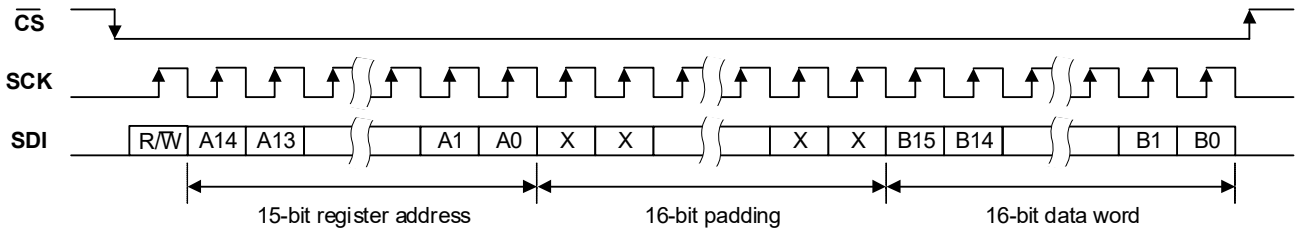


Figure 4-34. Control Interface SPI Register Write

Fig. 4-35 shows a single register read from a specified address.

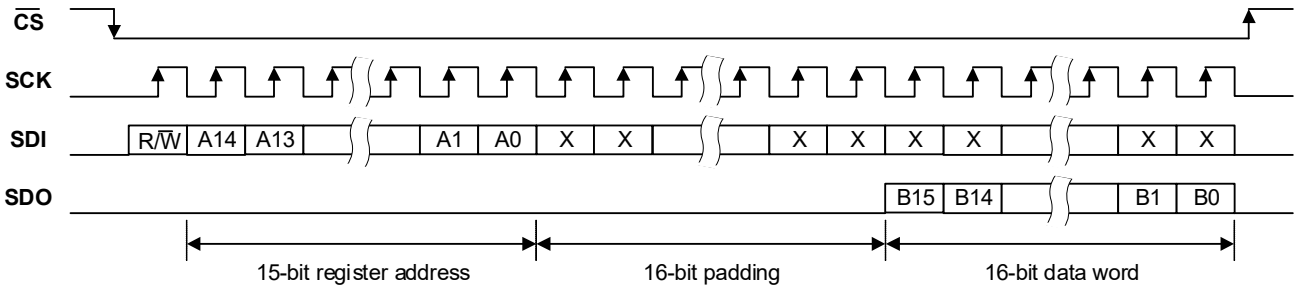


Figure 4-35. Control Interface SPI Register Read

Fig. 4-36 shows a multiple register write to a specified address.

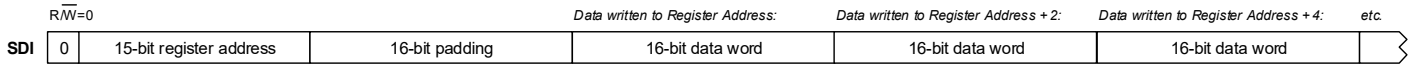


Figure 4-36. Multiple-Register Write to Specified Address

Fig. 4-37 shows a multiple register read from a specified address.

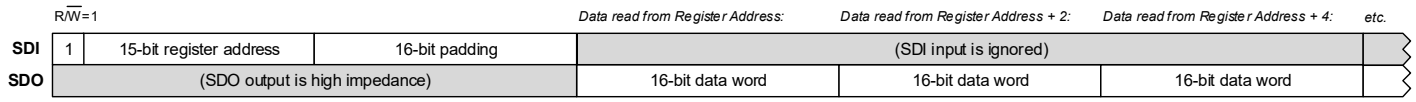


Figure 4-37. Multiple-Register Read from Specified Address

4.11 Interrupts

The CS4332S incorporates an interrupt controller for monitoring event conditions. Inputs to the interrupt controller include HGC warning/error conditions.

Any of these input conditions can be used to assert the IRQ output signal. The IRQ signal can be configured as an output on different pins as described in Table 4-14.

Table 4-14. IRQ Event Logic Output Pins

Pin Name	Power Supply	Control Field	Notes
GPIO1 [1]	VDD_IO2	GPIO1_IRQ_EN	IRQ not supported if or HGC external gain control.
$\overline{\text{HGC\_CS}}$/GPIO2 [1]	VDD_IO2	GPIO2_IRQ_EN	
CONFIG4	VDD_IO1	CONFIG4_IRQ_EN	—
SPI_SCK	VDD_IO1	SPI_SCK_IRQ_EN	IRQ not supported if SPI control interface is used.

1. The GPIO logic levels are referenced to the VDD_IO2 domain; level shifting may be required if connecting to a host interface operating at a different level (see Table 3-8 for details).

An interrupt register bit, x_INT, is associated with each interrupt input, indicating that the respective event has been detected. The interrupt bits are latching fields which, once set, remain set until a 1 is written to the respective bits. The interrupt register bits can be polled at any time or in response to the IRQ output signal being asserted.

Mask bits, x_MASK, are provided for each input condition, to enable or disable the respective functions from contributing to the interrupt logic output. The interrupt register bits (x_INT) remain valid—even if masked—but the masked interrupts do not cause the interrupt logic output to be asserted.

The output can be either CMOS driven or open drain; this is selected using IRQ_OP_CFG.

- If the output is configured as CMOS driven, the IRQ output signal is active high, i.e., Logic 1 if one or more unmasked interrupt is asserted.
- If the output is configured as open drain, the IRQ output signal is active low, i.e., Logic 0 if one or more unmasked interrupt is asserted.

The IRQ signal represents the logical OR of the unmasked interrupt registers. The IRQ output remains asserted until all of the associated interrupts have been either masked or reset.

The IRQ status is indicated using IRQ_STS; this bit is set if one or more unmasked interrupt is asserted.

4.12 Device ID

The device ID, and other associated data, can be read from the control fields listed in Table 4-15.

Table 4-15. Device ID

Label	Description
DEVID_0	Lower bytes of the Device ID
DEVID_1	Upper bytes of the Device ID
AREVID	All-layer device revision
MTLREVID	Metal-layer device revision

5 Applications

5.1 Output Buffer Circuit

The CS4332S incorporates a high-performance sigma-delta current-mode DAC with integrated operational amplifiers for current-to-voltage conversion. External components for the current-to-voltage conversion and out-of-band filtering can be selected for flexible integration and to optimize dynamic range.

5.1.1 Typical Output Circuit

A typical output connection circuit is shown in Fig. 5-1. The circuit produces a 2 V_{RMS} differential output from a full-scale (0 dBFS) digital input.

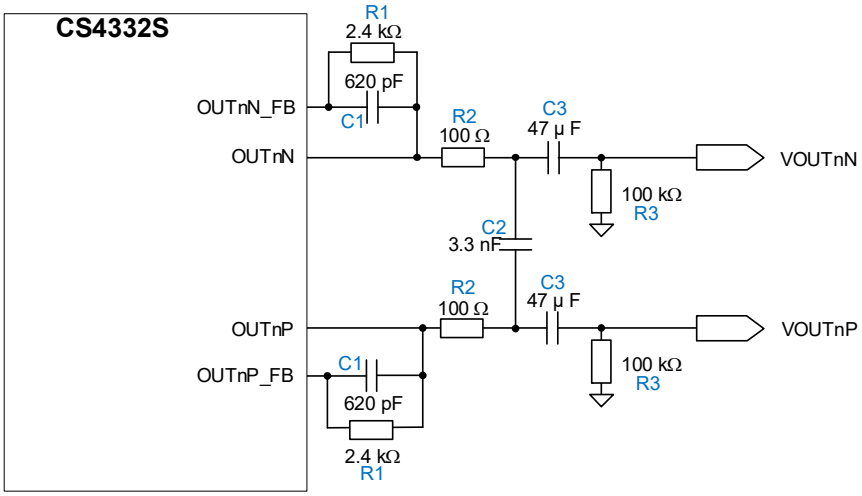


Figure 5-1. Typical Output Connection Circuit

The feedback resistor, R_1 determines the full-scale differential output voltage; a maximum output voltage of 2 V_{RMS} is supported at the OUTn and OUTnP pins. R_1 is calculated as follows:

$$R_1 = \frac{\text{Full-scale Output Voltage } (V_{RMS})}{0.835\ mA_{RMS}} = \frac{2}{0.835 \times 10^{-3}} = 2.4\ k\Omega$$

The filter is provided by the integrated operational amplifiers and associated feedback components C_1 and R_1. The objective is to provide a flat passband for the audio output bandwidth. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 2400 \times 620 \times 10^{-12}} = 107\ kHz$$

R_2 and C_2 create an output filter to reduce out-of-band noise of the output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_2 2C_2} = \frac{1}{2\pi \times 100 \times (2 \times 3.3 \times 10^{-9})} = 241\ kHz$$

R_3 and C_3 form a high-pass filter, which removes the DC bias of the voltage output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_3 C_3} = \frac{1}{2\pi \times 100 \times 10^3 \times 47 \times 10^{-6}} = 0.033\ Hz$$

5.1.2 Alternative Output Circuits

The typical circuit shown in Fig. 5-1 is recommended for optimal performance. Example line driver circuits are described in Section 5.1.2.1 and Section 5.1.2.2; specifications detailed in Section 3 are not applicable.

5.1.2.1 Example Active Differential Line Driver Circuit

An example of an active differential line-driver circuit is shown in Fig. 5-2, the output connection circuit shown produces a 2.2 V_{RMS} differential output from a full-scale (0 dBFS) digital input.

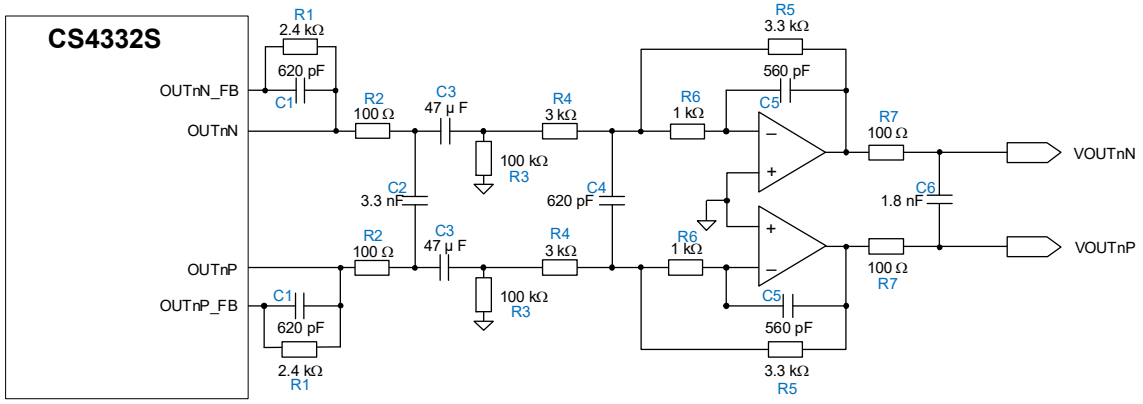


Figure 5-2. Example Active Differential Line Driver Circuit

The feedback resistor, R1 determines the full-scale differential output voltage; a maximum output voltage of 2 V_{RMS} is supported at the OUTnN and OUTnP pins. R1 is calculated as follows

$$R_1 = \frac{\text{Full-scale Output Voltage } (V_{RMS})}{0.835\ mA_{RMS}} = \frac{2}{0.835 \times 10^{-3}} = 2.4\ k\Omega$$

The filter is provided by the integrated operational amplifiers and associated feedback components C1 and R1. The objective is to provide a flat passband for the audio output bandwidth. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 2400 \times 620 \times 10^{-12}} = 107\ kHz$$

R2 and C2 create an output filter to reduce the out-of-band noise of the output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_2 2C_2} = \frac{1}{2\pi \times 100 \times (2 \times 3.3 \times 10^{-9})} = 241\ kHz$$

C3 removes the DC bias of the CS4332S output and forms a high-pass filter with parallel resistance of R3 and R4. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi\left(\frac{R3 \times R4}{R3 + R4}\right) C_3} = \frac{1}{2\pi \times \left(\frac{100 \times 10^3 \times 3 \times 10^3}{100 \times 10^3 + 3 \times 10^3}\right) \times 47 \times 10^{-6}} = 1.16\ Hz$$

R4 and C4 create a low-pass filter. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_4 2C_4} = \frac{1}{2\pi \times 3 \times 10^3 \times (2 \times 620 \times 10^{-9})} = 42.8\ kHz$$

R5, R6, and C5 create a low-pass filter within the operational amplifier feedback loop. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi(R_5 + R_6)C_5} = \frac{1}{2\pi \times (3.3 \times 10^3 + 1 \times 10^3) \times 560 \times 10^{-9}} = 66.1\ \text{kHz}$$

The gain of the output buffer is set by R4 and R5:

$$\text{Gain} = \frac{R_5}{R_4} = \frac{3 \times 10^3}{3.3 \times 10^3} = 1.1$$

R7 and C6 limit the output current; this ensures stability of the output and filters any out-of-band noise introduced by the operational amplifiers. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_7 2C_6} = \frac{1}{2\pi \times 100 \times (2 \times 1.8 \times 10^{-9})} = 442.1\ \text{kHz}$$

5.1.2.2 Example Active Differential-to-Single-Ended Line Driver Circuit

An example of an active differential-to-single-ended output circuit is shown in Fig. 5-3. The circuit produces a 2.2 V_{RMS} single-ended output from a full-scale (0 dBFS) digital input.

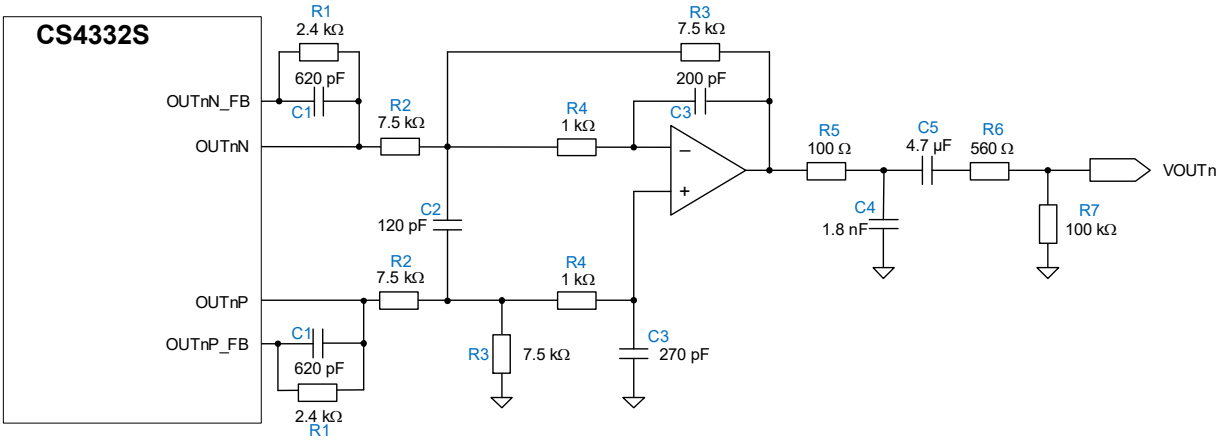


Figure 5-3. Example Differential-to-Single-Ended Output Circuit

The feedback resistor, R1 determines the full-scale differential output voltage; a maximum output voltage of 2 V_{RMS} is supported at the OUTnN and OUTnP pins. R1 is calculated as follows:

$$R_1 = \frac{\text{Full-scale Output Voltage } (V_{RMS})}{0.835\ \text{mA}_{RMS}} = \frac{2}{0.835 \times 10^{-3}} = 2.4\ \text{k}\Omega$$

The filter is provided by the integrated operational amplifiers and associated feedback components C1 and R1. The objective is to provide a flat passband for the audio output bandwidth. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 2400 \times 620 \times 10^{-12}} = 107\ \text{kHz}$$

R2 and C2 create an output filter to reduce the out-of-band noise of the output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_2 2C_2} = \frac{1}{2\pi \times (7.5 \times 10^3) \times (2 \times 120 \times 10^{-12})} = 88.4\ \text{kHz}$$

R3, R4, and C3 create a low-pass filter. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi(R_3 + R_4)C_3} = \frac{1}{2\pi \times (7.5 \times 10^3 + 1 \times 10^3) \times 200 \times 10^{-9}} = 93.6\ \text{kHz}$$

The gain of the output buffer is set by R2 and R3:

$$\text{Gain} = \frac{R_3}{R_2} = \frac{7.5 \times 10^3}{7.5 \times 10^3} = 1$$

R5, R6, R7, C4, and C5 remove the DC bias of the CS4332S output, limit the output current, ensure stability of the output, and filter any out-of-band noise introduced by the operation amplifiers.

The cut-off frequency of the high-pass filter is calculated as follows:

$$F_C = \frac{1}{2\pi(R_6 + R_7)C_5} = \frac{1}{2\pi \times (560 + 100 \times 10^3) \times (47 \times 10^{-6})} = 0.03\ \text{Hz}$$

The cut-off frequency of the low-pass filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_5 C_4} = \frac{1}{2\pi \times 100 \times (1.8 \times 10^{-9})} = 884.2\ \text{kHz}$$

5.1.3 Unused Output Pins

The typical output connection circuit (Fig. 5-1) provides a biased differential output. Alternative output buffer circuits may only provide a single-ended output configuration. In this case, or where an output channel is not used, any unused output pin (OUTnX) must be connected to its respective OUTnX_FB pin, as illustrated in Fig. 5-4.

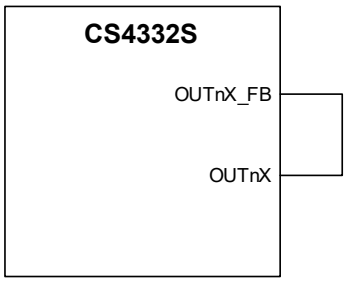


Figure 5-4. Unused Output Pin Connection

5.1.4 Recommended Components

To achieve the specified performance characteristics, the choice of external components should observe the following recommendations:

- Capacitors should be stable dielectric types, such as C0G (NP0) or electrolytic.
- Resistors should be low value where possible, to minimize thermal noise.
- Low-noise operational amplifiers should be used, such as Texas Instruments OPA1656. The operational amplifiers should meet the minimum performance requirements noted in Table 5-1.

Table 5-1. Op-Amp Specification

Parameter	Specification
Input noise	<5 nV/√Hz
Unity gain bandwidth	>15 MHz
Slew rate	5 V/µs
Total harmonic distortion plus noise (THD+N)	<-128 dB

5.2 Crystal Component Selection

The crystal oscillator (see Section 4.4) uses an external crystal to generate the timing reference. Load capacitors are connected to the crystal as shown in Fig. 5-5. A series resistor (R_S) may also be required to configure the drive level for the selected crystal.

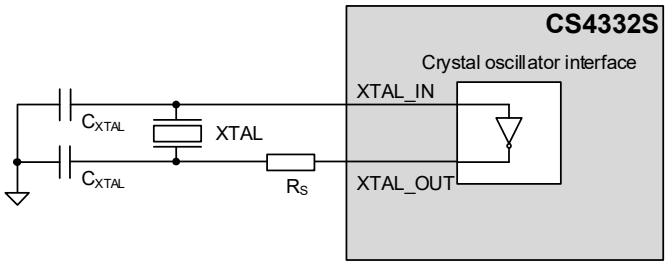


Figure 5-5. Crystal Oscillator Connection

The suitability of the selected crystal is determined by whether the gain margin and drive level are within the valid operating limits of the crystal. The gain margin and drive level can be calculated as a function of the transconductance of the crystal interface.

The transconductance of the crystal interface is dependent on the VDD_IO2 operating voltage as described in Table 3-10.

The recommended sequence for crystal component selection is as follows:

1. **Crystal selection.** The CS4332S is compatible with a wide variety of crystal components, including the KC3225Z series of oscillators. Note that for a reference frequency of 45.1584 MHz a custom crystal may be required.
2. **Capacitor selection.** Capacitors should be selected according to the crystal manufacturer's specification for load capacitance (C_L). The recommended value for each C_{XTAL} capacitor is 2 × C_L.
3. **Series resistor.** In the first instance, assume the series resistor Rs is not required (0 Ω).
4. **Gain margin calculation.** The gain margin can be calculated from the transconductance of the crystal interface and the series resistor R_S, together with the crystal characteristics. If the required gain margin is less than 5, a different crystal selection must be made (Step 1).

   The gain margin is calculated as follows: $$\text{Gain Margin} = \frac{\text{Transconductance}}{4 \times (\text{ESR} + R_S) \times (2\pi \times f_{XTAL})^2 \times (C_0 + C_L)^2}$$

   where:

   Transconductance = transconductance of the crystal interface (S)

   ESR = equivalent series resistance (ESR) of the crystal (Ω)

   R_S = series resistance (Ω)

   f_{XTAL} = resonant frequency of the crystal (Hz)

   C_L = load capacitance of the crystal (F)

   C_0 = shunt capacitance of the crystal (F)
5. **Drive level calculation.** The drive level can be calculated using the crystal characteristics and the operating voltage. The operating voltage (peak voltage across the crystal) can be determined using measurement or else by simulation. If the drive level exceeds the maximum level for the crystal, adjust the series resistor R_S to meet the required specification. Increasing R_S results in a lower voltage across the crystal and a decrease in drive level.

   If the series resistor is adjusted, the gain margin must now be recalculated (Step 4). It is recommended to find the minimum series resistance that meets the required gain margin and drive level.

The drive level (W) is calculated as follows: $\text{Drive Level} = 2 \times \text{ESR} \times (\pi \times f_{XTAL} \times V \times (C_L + C_0))^2$

where:

ESR = equivalent series resistance (ESR) of the crystal (Ω)

f_{XTAL} = resonant frequency of the crystal (Hz)

V = Peak voltage across the crystal (V)

C_L = load capacitance of the crystal (F)

C_0 = shunt capacitance of the crystal (F)

The sequence for crystal component selection is illustrated in Fig. 5-6

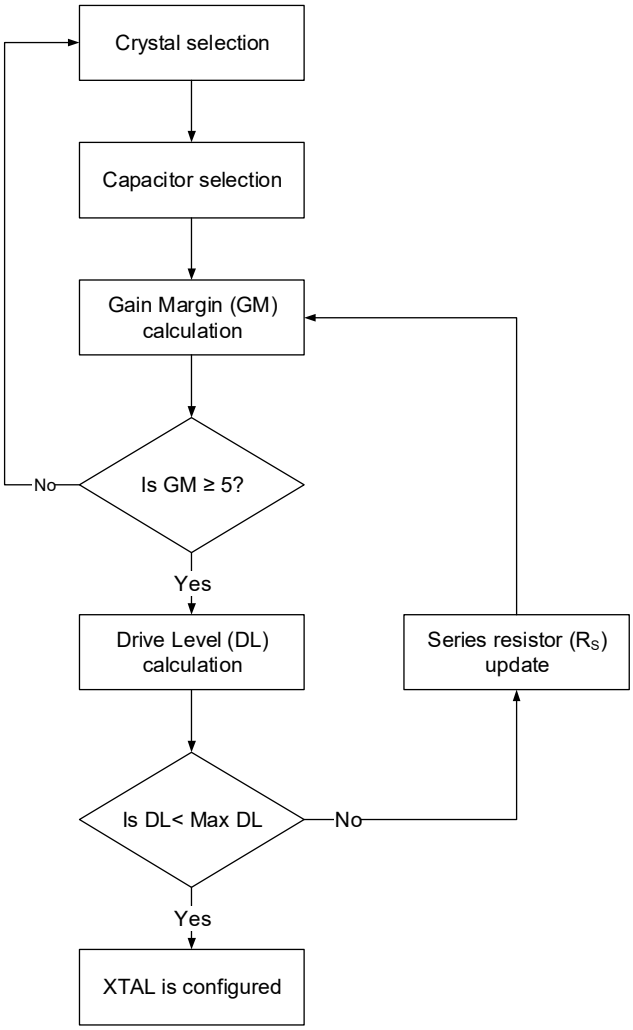


Figure 5-6. Crystal Oscillator Component Selection

6 Register Quick Reference

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

This register view is for the CS4332S.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

Table 6-1. Block Base Addresses

Base Address	Block Name	Register Quick Reference	Register Description Reference
0x0000 0000	**DEVID**	Section 6.1	Section 7.1
0x0000 0040	**CONFIG**	Section 6.2	Section 7.2
0x0000 00C0	**OUTPUT_PATH**	Section 6.3	Section 7.3
0x0000 2000	**HGC**	Section 6.4	Section 7.4
0x0000 3D00	**PIN_CONFIG**	Section 6.5	Section 7.5
0x0000 3E00	**IRQ_CONFIG**	Section 6.6	Section 7.6

6.1 DEVID

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0000	DEVID_0	DEVID_0															
p. 54		0	0	1	1	0	0	1	1	0	0	1	0	0	0	1	1
0x0000 0002	DEVID_1	DEVID_1															
p. 54		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0x0000 0004	REVID	—								AREVID				MTLREVID			
p. 54		0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
0x0000 0022	SW_RESET	SW_RESET								—							
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.2 CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0040	CLK_CFG	—		SYSCLK_FREQ	SYSCLK_SRC	—											
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0042	SAMPLE_RATE	—													SAMPLE_RATE		
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x0000 0044	CHIP_ENABLE	—															GLOBAL_EN
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0048	ASP_CFG	—									ASP_BCLK_INV	ASP_PRIMARY	—			ASP_BCLK_FREQ	
p. 56		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0050	SIGNAL_PATH_CFG	—									ASP_FSYNC_TYPE	ASP_TDM_SLOT			ASP_FORMAT		
p. 56		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.3 OUTPUT_PATH

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 00C0	OUT_ENABLES	—							OUT_LOAD_CFG	—						OUT2_DAC_EN	OUT1_DAC_EN
p. 56		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00C2	OUT_RAMP_SUM	—									OUT_RAMP_RATE_DEC			—		OUT_RAMP_RATE_INC	
p. 57		0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
0x0000 00C4	OUT_DEEMPH	—														OUT_DEEMPH_FILT_SEL	OUT_DEEMPH_EN
p. 57		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00C6	OUT_FILTER	—			OUT_HPF_EN	—	OUT_FILTER_SEL			—							
p. 57		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00CA	OUT_INV	—														OUT2_INV	OUT1_INV
p. 58		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0x0000 00D0	OUT1_VOL_CTRL	OUT1_MUTE	—							OUT1_VOL							
p. 58		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00D2	OUT2_VOL_CTRL	OUT2_MUTE	—							OUT2_VOL							
p. 58		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00E0	OUT_VOL_UPDATE	—															OUT_VU
p. 59		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00E4	SHUTDOWN_CTRL1	—															DAC_SHUTDOWN
p. 59		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00E8	DSD_CTRL	—									DSD_PM_SEL	DSD_PM_EN	DSD_ZERODB	DSD_OSR			DSD_EN
p. 59		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00EC	DSD_FILT	—											DSD_HPF_EN	—			
p. 59		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

6.4 HGC

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2000	HGC_CONTROL	—											HGC_ABORT	—			HGC_INIT_UPDATE
p. 60		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2004	HGC_STATUS	—															HGC_BUSY_STS
p. 60		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 200C	IO_CTRL	—					DB_TIME			—		SW_TYPE	—				HGC_CTRL_INTERFACE
p. 60		0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0
0x0000 2010	GPIO_STS	—				GPO_STS				—				GPI_STS			
p. 61		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2020	SPI_CLK	—								HGC_SCK_DIV				—		HGC_CLK_PHA	HGC_CLK_POL
p. 61		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2022	SPI_CSB	—				HGC_CSB_IDLE_DUR				HGC_CSB_RISE_DLY				HGC_CSB_FALL_DLY			
p. 61		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2500	OUT_CFG	—											OUT_STEP_RAMP_EN	OUT_ZC_TIMEOUT			
p. 62		0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0x0000 2504	OUT_PATH_EXT_DLY	—				OUT_EXT_GAIN_DLY											
p. 62		0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1
0x0000 2600	OUT1_CFG_SPI	—					OUT1_SPI_POSITION			—		OUT1_BIT_PATT_LENGTH					
p. 63		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2602	OUT1_CFG_GPIO	—			OUT1_GPI_POL	—								OUT1_GPO4_SEL	OUT1_GPO3_SEL	OUT1_GPO2_SEL	OUT1_GPO1_SEL
p. 63		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2604	OUT2_CFG_SPI	—					OUT2_SPI_POSITION			—		OUT2_BIT_PATT_LENGTH					
p. 63		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2606	OUT2_CFG_GPIO	—			OUT2_GPI_POL	—								OUT2_GPO4_SEL	OUT2_GPO3_SEL	OUT2_GPO2_SEL	OUT2_GPO1_SEL
p. 64		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2620	OUT1_BIT_PATT_0	OUT1_BIT_PATT_0															
p. 64		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2622	OUT1_BIT_PATT_1	OUT1_BIT_PATT_1															
p. 64		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2624	OUT1_VOL_ANA	—					OUT1_ANA_GAIN										
p. 65		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2626	OUT1_VOL_DIG	OUT1_UPDATE	—						OUT1_DIG_GAIN								
p. 65		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2628	OUT2_BIT_PATT_0	OUT2_BIT_PATT_0															
p. 65		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 262A	OUT2_BIT_PATT_1	OUT2_BIT_PATT_1															
p. 65		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 262C	OUT2_VOL_ANA	—					OUT2_ANA_GAIN										
p. 66		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 262E	OUT2_VOL_DIG	OUT2_UPDATE	—						OUT2_DIG_GAIN								
p. 66		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2900	AUX1_CFG	—					AUX1_SPI_POSITION			—		AUX1_BIT_PATT_LENGTH					
p. 66		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2904	AUX2_CFG	—					AUX2_SPI_POSITION			—		AUX2_BIT_PATT_LENGTH					
p. 66		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2920	AUX1_BIT_PATT_0	AUX1_BIT_PATT_0															
p. 67		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2922	AUX1_BIT_PATT_1	AUX1_BIT_PATT_1															
p. 67		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2924	AUX2_BIT_PATT_0	AUX2_BIT_PATT_0															
p. 67		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2926	AUX2_BIT_PATT_1	AUX2_BIT_PATT_1															
p. 67		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.5 PIN_CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 3D1C	PAD_IRQ_CFG	IRQ_OP_CFG	—						GPIO1_IRQ_EN	GPIO2_IRQ_EN	—		CONFIG4_IRQ_EN	SPI_SCK_IRQ_EN	—		
p. 68		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.6 IRQ_CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 3E04	IRQ_STS								—								IRQ_STS
p. 68		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 3E1E	IRQ_HGC_EVENT_INT						—						HGC_SPI_ERROR_INT	HGC_ABORT_ERROR_INT	—	HGC_ERROR_INT	HGC_DONE_INT
p. 68		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 3E2E	IRQ_HGC_EVENT_MASK						—						HGC_SPI_ERROR_MASK	HGC_ABORT_MASK	—	HGC_ERROR_MASK	HGC_DONE_MASK
p. 69		0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

7 Register Descriptions

This section describes each of the control port registers.

This register view is for the CS4332S.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

7.1 DEVID

7.1.1 DEVID_0

Address: 0x0000 0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	DEVID_0															
Default	0	0	1	1	0	0	1	1	0	0	1	0	0	0	1	1

Bits	Name	Description
15:0	DEVID_0	This register indicates the lower bytes of Device ID CS4332S 0x0000–0x3322 = Reserved 0x3323 = (Default) CS4332S 0x3324–0xFFFF = Reserved

7.1.2 DEVID_1

Address: 0x0000 0002

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	DEVID_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description
15:0	DEVID_1	This register indicates the upper bytes of Device ID CS4332S 0x0000–0x0003 = Reserved 0x0004 = (Default) CS4332S 0x0005–0xFFFF = Reserved

7.1.3 REVID

Address: 0x0000 0004

	15…8	7	6	5	4	3	2	1	0
RO	—	AREVID				MTLREVID			
Default	0x00	1	0	1	0	0	0	0	0

Bits	Name	Description
15:8	—	Reserved
7:4	AREVID	This field indicates the all-layer device revision. 0x0–0x9 = Reserved 0xA = (Default) Revision Ax 0xB–0xF = Reserved
3:0	MTLREVID	This field indicates the metal-layer device revision. 0x0 = (Default) Revision x0 0x1–0xF = Reserved

7.1.4 SW_RESET

Address: 0x0000 0022

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO	SW_RESET								—							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	SW_RESET	Software Reset. Writing 0x5A triggers a reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved
7:0	—	Reserved

7.2 CONFIG

7.2.1 CLK_CFG

Address: 0x0000 0040

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—		SYSCLK_FREQ	SYSCLK_SRC	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:14	—	Reserved
13	SYSCLK_FREQ	System clock frequency. 0 = (Default) 24.576/22.5792 MHz 1 = 49.152/45.1584 MHz
12	SYSCLK_SRC	System clock source. If XTAL is selected, the MCLK is the output clock. 0 = (Default) MCLK input 1 = XTAL input
11:0	—	Reserved

7.2.2 SAMPLE_RATE

Address: 0x0000 0042

	15…8	7	6	5	4	3	2	1	0
RW	—	—				SAMPLE_RATE			
Default	0x00	0	0	0	0	0	0	0	1

Bits	Name	Description
15:3	—	Reserved
2:0	SAMPLE_RATE	Audio sample frequency. Note the sample rate must be integer-related to the system clock frequency. Auto-detect is only valid if sample rate = 16-192 kHz, and the ASP is in Secondary Mode. 000 = 32 kHz 001 = (Default) 48/44.1 kHz 010 = 96/88.2 kHz 011 = 192/176.4 kHz 100 = 384/356.8 kHz 101 = Reserved 110 = Auto-detect 111 = 16 kHz

7.2.3 CHIP_ENABLE

Address: 0x0000 0044

	15…8	7	6	5	4	3	2	1	0
RW	—	—							GLOBAL_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	GLOBAL_EN	Global enable. Set to 1 to configure and enable all functions. Clear to 0 to disable. Note the clocking and ASP control registers are only valid on the rising edge of GLOBAL_EN. It is recommended to select the disabled state (GLOBAL_EN=0) before writing to these registers.

7.2.4 ASP_CFG

Address: 0x0000 0048

RW	15…8	7	6	5	4	3	2	1	0
	—	—	ASP_BCLK_INV	ASP_PRIMARY	—			ASP_BCLK_FREQ	
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6	ASP_BCLK_INV	ASP BCLK polarity. Selects the valid BCLK edge for data sampling. In non-inverted mode, DIN data is valid on BCLK rising edge. In inverted mode, DIN data is valid on BCLK falling edge. 0 = (Default) Non-inverted 1 = Inverted
5	ASP_PRIMARY	ASP Primary/Secondary Mode select. In ASP Primary Mode, BCLK and FSYNC are outputs. In ASP Secondary Mode, BCLK and FSYNC are inputs. 0 = (Default) Secondary Mode 1 = Primary Mode
4:2	—	Reserved
1:0	ASP_BCLK_FREQ	ASP BCLK frequency. The BCLK frequency must be high enough to support the required number of data bits at the selected sample rate. Only valid in ASP Primary Mode. Note the BCLK frequency is integer-related to the system clock frequency i.e., multiples of 3.072 MHz for 24.576 / 49.152 MHz system clock, or multiples of 2.8224 MHz for 22.5792 / 45.1584 MHz system clock. 00 = (Default) 3.072/2.8224 MHz 01 = 6.144/5.6448 MHz 10 = 12.288/11.2896 MHz 11 = 24.576/22.5792 MHz

7.2.5 SIGNAL_PATH_CFG

Address: 0x0000 0050

RW	15…8	7	6	5	4	3	2	1	0
	—	—	ASP_FSYNC_TYPE	ASP_TDM_SLOT			ASP_FORMAT		
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6	ASP_FSYNC_TYPE	Configure ASP_FSYNC as pulse or square wave (50% duty cycle) in TDM mode. Only applicable when ASP is in Primary Mode. 0 = (Default) FSYNC Pulse 1 = FSYNC Square Wave
5:3	ASP_TDM_SLOT	TDM slot select. Configures which TDM slots are used in TDM maximum-time-slots mode. 000 = (Default) Slots 0-1 001 = Slots 2-3 010 = Slots 4-5 011 = Slots 6-7 100 = Slots 8-9 101 = Slots 10-11 110 = Slots 12-13 111 = Slots 14-15
2:0	ASP_FORMAT	ASP data format. Selects how the audio samples are arranged within the FSYNC frame. 000 = (Default) I2S Mode 001 = Left-Justified Mode 010–101 = Reserved 110 = TDM Mode maximum time slots 111 = TDM Mode minimum time slots

7.3 OUTPUT_PATH

7.3.1 OUT_ENABLES

Address: 0x0000 00C0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—							OUT_LOAD_CFG	—						OUT2_DAC_EN	OUT1_DAC_EN
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:9	—	Reserved
8	OUT_LOAD_CFG	Output driving configuration. 0 = (Default) 3k load 1 = 10k load

Bits	Name	Description
7:2	—	Reserved
1	OUT2_DAC_EN	Channel 2 output enable. 0 = (Default) Disabled 1 = Enabled
0	OUT1_DAC_EN	Channel 1 output enable. 0 = (Default) Disabled 1 = Enabled

7.3.2 OUT_RAMP_SUM

Address: 0x0000 00C2

RW	15…8	7	6	5	4	3	2	1	0
	—	—	OUT_RAMP_RATE_DEC			—	OUT_RAMP_RATE_INC		
Default	0x00	0	0	1	0	0	0	1	0

Bits	Name	Description
15:7	—	Reserved
6:4	OUT_RAMP_RATE_DEC	DAC output volume decrease Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms
3	—	Reserved
2:0	OUT_RAMP_RATE_INC	DAC output volume increase Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms

7.3.3 OUT_DEEMPH

Address: 0x0000 00C4

RW	15…8	7	6	5	4	3	2	1	0
	—	—						OUT_DEEMPH_FILT_SEL	OUT_DEEMPH_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved
1	OUT_DEEMPH_FILT_SEL	Deemphasis filter sample-rate selection. 0 = (Default) 44.1 kHz 1 = 48.0 kHz
0	OUT_DEEMPH_EN	Deemphasis filter enable. 0 = (Default) Deemphasis disabled 1 = Deemphasis enabled

7.3.4 OUT_FILTER

Address: 0x0000 00C6

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			OUT_HPF_EN	—	OUT_FILTER_SEL			—							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12	OUT_HPF_EN	High-pass filter enable. 0 = (Default) HPF disabled 1 = HPF enabled
11	—	Reserved

Bits	Name	Description
10:8	OUT_FILTER_SEL	Digital filter select. Configures the interpolation filter. 000 = (Default) Minimum phase, Slow roll-off (44.1 kHz-192 kHz) 001 = Minimum phase, Fast roll-off (16 kHz-48 kHz)/Balanced roll-off (88.2 kHz-384 kHz) 010 = Linear phase, Slow roll-off (44.1 kHz-192 kHz) 011 = Linear phase, Fast roll-off (16 kHz-48 kHz)/Balanced roll-off (88.2 kHz-384 kHz) 100 = Reserved 101 = Minimum phase, Fast roll-off (88.2 kHz-384 kHz) 110 = Reserved 111 = Linear phase, Fast roll-off (88.2 kHz-384 kHz)
7:0	—	Reserved

7.3.5 OUT_INV

Address: 0x0000 00CA

RW	15…8	7	6	5	4	3	2	1	0
	—	—						OUT2_INV	OUT1_INV
Default	0x00	0	0	0	0	0	0	1	1

Bits	Name	Description
15:2	—	Reserved
1	OUT2_INV	Channel 2 DAC invert. 0 = No inversion 1 = (Default) DAC data invert
0	OUT1_INV	Channel 1 DAC invert. 0 = No inversion 1 = (Default) DAC data invert

7.3.6 OUT1_VOL_CTRL

Address: 0x0000 00D0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT1_MUTE	—							OUT1_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT1_MUTE	DAC output Channel 1 mute. 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	OUT1_VOL	DAC output Channel 1 volume, –127.5 dB to 0 dB in 0.5 dB steps. 0x00 = (Default) 0.0 dB 0x01 = –0.5 dB … 0xFF = –127.5 dB

7.3.7 OUT2_VOL_CTRL

Address: 0x0000 00D2

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT2_MUTE	—							OUT2_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT2_MUTE	DAC output Channel 2 mute. 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	OUT2_VOL	DAC output Channel 2 volume, –127.5 dB to 0 dB in 0.5 dB steps. 0x00 = (Default) 0.0 dB 0x01 = –0.5 dB … 0xFF = –127.5 dB

7.3.8 OUT_VOL_UPDATE

Address: 0x0000 00E0

WO	15…8	7	6	5	4	3	2	1	0
	—	—							OUT_VU
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	OUT_VU	Global output volume update trigger. 0 = (Default) No action 1 = Write 1 to trigger an update of all output volume/mute registers

7.3.9 SHUTDOWN_CTRL1

Address: 0x0000 00E4

RW	15…8	7	6	5	4	3	2	1	0
	—	—							DAC_SHUTDOWN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	DAC_SHUTDOWN	DAC reference shutdown control. Can be used to minimize power consumption if all output paths are disabled. 0 = (Default) Enable DAC reference 1 = Shutdown DAC reference

7.3.10 DSD_CTRL

Address: 0x0000 00E8

RW	15…8	7	6	5	4	3	2	1	0
	—	—	DSD_PM_SEL	DSD_PM_EN	DSD_ZERODB	DSD_OSR			DSD_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6	DSD_PM_SEL	DSD phase modulation mode clock rate select. 0 = (Default) DSD clock at 2 x OSR rate 1 = DSD clock at OSR rate
5	DSD_PM_EN	DSD phase modulation enable. 0 = (Default) Disabled 1 = Enabled
4	DSD_ZERODB	DSD input 0 dB level. 0 = (Default) SACD +3.1 dB level matches PCM 0 dBFS level 1 = SACD 0 dB level matches PCM 0 dBFS level
3:1	DSD_OSR	DSD oversample rate (OSR). 000 = (Default) 64 Fs 001 = 128 Fs 010 = 256 Fs 011–111 = Reserved
0	DSD_EN	DSD interface enable. Selects ASP or DSD signal path. 0 = (Default) Select ASP path 1 = Select DSD path

7.3.11 DSD_FILT

Address: 0x0000 00EC

RW	15…8	7	6	5	4	3	2	1	0
	—	—			DSD_HPF_EN	—			
Default	0x00	0	0	0	1	0	0	0	0

Bits	Name	Description
15:5	—	Reserved
4	DSD_HPF_EN	DSD high-pass filter enable. 0 = Disabled 1 = (Default) Enabled
3:0	—	Reserved

7.4 HGC

7.4.1 HGC_CONTROL

Address: 0x0000 2000

WO	15…8	7	6	5	4	3	2	1	0
	—	—			HGC_ABORT	—			HGC_INIT_UPDATE
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:5	—	Reserved
4	HGC_ABORT	Abort gain updates. Write 1 to abort any pending gain updates. Note that any updates already in progress will complete as normal and are not aborted. 0 = (Default) No action 1 = Write 1 to abort gain updates
3:1	—	Reserved
0	HGC_INIT_UPDATE	Initialize gain settings. Write 1 to transmit the SPI bit patterns and initialize all gain settings. Note the zero-cross detection is not applied when initializing gain settings. 0 = (Default) No action 1 = Write 1 to initialize gain settings

7.4.2 HGC_STATUS

Address: 0x0000 2004

RO	15…8	7	6	5	4	3	2	1	0
	—	—							HGC_BUSY_STS
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	HGC_BUSY_STS	Busy status. Indicates gain updates are pending for one or more audio channels. 0 = (Default) Idle 1 = Busy

7.4.3 IO_CTRL

Address: 0x0000 200C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				DB_TIME				—		SW_TYPE	—				HGC_CTRL_INTERFACE
Default	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0

Bits	Name	Description
15:11	—	Reserved
10:8	DB_TIME	GPI debounce time, base 32 kHz. 000 = 124 us 001 = 2 ms 010 = 4 ms 011 = (Default) 8 ms 100 = 16 ms 101 = 32 ms 110 = 64 ms 111 = 128 ms
7:6	—	Reserved
5	SW_TYPE	GPI type selection. Select toggle switch for rising-edge detection or latching switch for level detection. 0 = Toggle switch 1 = (Default) Latching switch
4:1	—	Reserved
0	HGC_CTRL_INTERFACE	Selects GPO/HGC_SPI control interface. 0 = (Default) HGC using SPI 1 = HGC using GPO

7.4.4 GPIO_STS

Address: 0x0000 2010

RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				GPO_STS				—				GPI_STS			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:12	—	Reserved
11:8	GPO_STS	GPO read back status.
7:4	—	Reserved
3:0	GPI_STS	GPI read back status.

7.4.5 SPI_CLK

Address: 0x0000 2020

RW	15…8	7	6	5	4	3	2	1	0
	—	HGC_SCK_DIV				—		HGC_CLK_PHA	HGC_CLK_POL
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	—	Reserved
7:4	HGC_SCK_DIV	SPI clock divider. Configures the SPI clock frequency as a division of the system clock. For 48 kHz-related sample rates, the SPI clock is a division of system clock (24.576 MHz). For 44.1 kHz-related sample rates, the SPI clock is a division of system clock (22.5792 MHz). 0x0 = (Default) Divide by 2 0x1 = Divide by 4 0x2 = Divide by 6 0x3 = Divide by 8 0x4 = Divide by 10 0x5 = Divide by 12 0x6 = Divide by 14 0x7 = Divide by 16 0x8 = Divide by 18 0x9 = Divide by 20 0xA = Divide by 22 0xB = Divide by 24 0xC = Divide by 26 0xD = Divide by 28 0xE = Divide by 30 0xF = Divide by 32
3:2	—	Reserved
1	HGC_CLK_PHA	SPI clock phase select. 0 = (Default) Negative SPI clock phase 1 = Positive SPI clock phase
0	HGC_CLK_POL	SPI clock polarity select. 0 = (Default) Negative SPI clock polarity 1 = Positive SPI clock polarity

7.4.6 SPI_CSB

Address: 0x0000 2022

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				HGC_CSB_IDLE_DUR				HGC_CSB_RISE_DLY				HGC_CSB_FALL_DLY			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:12	—	Reserved
11:8	HGC_CSB_IDLE_DUR	Minimum idle duration between SPI transactions (from CS rising edge to CS falling edge). The duration is defined in system-clock cycles. For 48 kHz-related sample rates, the system-clock period is 1/24.576 MHz. For 44.1 kHz-related sample rates, the system-clock period is 1/22.5792 MHz. 0x0 = (Default) 32 clock cycles 0x1 = 36 clock cycles 0x2 = 40 clock cycles 0x3 = 44 clock cycles 0x4 = 48 clock cycles 0x5 = 56 clock cycles 0x6 = 64 clock cycles 0x7 = 80 clock cycles 0x8 = 96 clock cycles 0x9 = 128 clock cycles 0xA = 160 clock cycles 0xB = 224 clock cycles 0xC = 288 clock cycles 0xD = 416 clock cycles 0xE = 544 clock cycles 0xF = 800 clock cycles

Bits	Name	Description
7:4	HGC_CSB_RISE_DLY	Chip Select (CS) rise delay. Configures the minimum time from SCLK active edge to CS rising edge (end of SPI transaction). The delay is defined in system-clock cycles. For 48 kHz-related sample rates, the system-clock period is 1/24.576 MHz. For 44.1 kHz-related sample rates, the system-clock period is 1/22.5792 MHz. 0x0 = (Default) 2 clock cycles 0x1 = 4 clock cycles 0x2 = 6 clock cycles 0x3 = 8 clock cycles 0x4 = 10 clock cycles 0x5 = 12 clock cycles 0x6 = 14 clock cycles 0x7 = 16 clock cycles 0x8 = 18 clock cycles 0x9 = 20 clock cycles 0xA = 22 clock cycles 0xB = 24 clock cycles 0xC = 26 clock cycles 0xD = 28 clock cycles 0xE = 30 clock cycles 0xF = 32 clock cycles
3:0	HGC_CSB_FALL_DLY	Chip Select (CS) fall delay. Configures the minimum time from SCLK active edge to CS falling edge (end of SPI transaction). The delay is defined in system-clock cycles. For 48 kHz-related sample rates, the system-clock period is 1/24.576 MHz. For 44.1 kHz-related sample rates, the system-clock period is 1/22.5792 MHz. 0x0 = (Default) 2 clock cycles 0x1 = 4 clock cycles 0x2 = 6 clock cycles 0x3 = 8 clock cycles 0x4 = 10 clock cycles 0x5 = 12 clock cycles 0x6 = 14 clock cycles 0x7 = 16 clock cycles 0x8 = 18 clock cycles 0x9 = 20 clock cycles 0xA = 22 clock cycles 0xB = 24 clock cycles 0xC = 26 clock cycles 0xD = 28 clock cycles 0xE = 30 clock cycles 0xF = 32 clock cycles

7.4.7 OUT_CFG

Address: 0x0000 2500

RW	15…8	7	6	5	4	3	2	1	0
	—	—			OUT_STEP_RAMP_EN	OUT_ZC_TIMEOUT			
Default	0x00	0	0	0	0	0	1	1	1

Bits	Name	Description
15:5	—	Reserved
4	OUT_STEP_RAMP_EN	Step ramp enable. Enables the digital gain to be used to compensate for step changes in the analog gain. 0 = (Default) Disabled 1 = Enabled
3:0	OUT_ZC_TIMEOUT	Timeout for zero-cross detection. 0x0 = 0 (OFF) 0x1–0x2 = Reserved 0x3 = 1 ms 0x4 = 2 ms 0x5 = 5 ms 0x6 = 10 ms 0x7 = (Default) 20 ms 0x8–0xF = Reserved

7.4.8 OUT_PATH_EXT_DLY

Address: 0x0000 2504

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				OUT_EXT_GAIN_DLY											
Default	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1

Bits	Name	Description
15:12	—	Reserved
11:0	OUT_EXT_GAIN_DLY	Wait for signal processing (SP) through interpolation to apply external gain changes. 0x000 = 0 1/24MHz 0x001 = 1 1/24MHz … 0x069 = (Default) 105 1/24MHz … 0x0FF = 255 1/24MHz 0x100–0xFFF = Reserved

7.4.9 OUT1_CFG_SPI

Address: 0x0000 2600

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—					OUT1_SPI_POSITION			—				OUT1_BIT_PATT_LENGTH			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:11	—	Reserved
10:8	OUT1_SPI_POSITION	Output Channel 1 device position in the SPI chain.
7:6	—	Reserved
5:0	OUT1_BIT_PATT_LENGTH	Output Channel 1 bit-pattern length for SPI gain control. 0x00 = (Default) 0 bits (device not present) 0x01 = 1 bits 0x02 = 2 bits … 0x20 = 32 bits 0x21–0x3F = Reserved

7.4.10 OUT1_CFG_GPIO

Address: 0x0000 2602

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			OUT1_GPI_POL	—								OUT1_GPO4_SEL	OUT1_GPO3_SEL	OUT1_GPO2_SEL	OUT1_GPO1_SEL
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12	OUT1_GPI_POL	GPI polarity for output Channel 1. 0 = (Default) GPI not inverted 1 = GPI inverted
11:4	—	Reserved
3	OUT1_GPO4_SEL	Select GPIO4 pin as GPO for output Channel 1. 0 = (Default) Disabled 1 = Enabled
2	OUT1_GPO3_SEL	Select GPIO3 pin as GPO for output Channel 1. 0 = (Default) Disabled 1 = Enabled
1	OUT1_GPO2_SEL	Select GPIO2 pin as GPO for output Channel 1. 0 = (Default) Disabled 1 = Enabled
0	OUT1_GPO1_SEL	Select GPIO1 pin as GPO for output Channel 1. 0 = (Default) Disabled 1 = Enabled

7.4.11 OUT2_CFG_SPI

Address: 0x0000 2604

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—					OUT2_SPI_POSITION			—				OUT2_BIT_PATT_LENGTH			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:11	—	Reserved
10:8	OUT2_SPI_POSITION	Output Channel 2 device position in the SPI chain.
7:6	—	Reserved
5:0	OUT2_BIT_PATT_LENGTH	Output Channel 2 bit-pattern length for SPI gain control. 0x00 = (Default) 0 bits (device not present) 0x01 = 1 bits 0x02 = 2 bits … 0x20 = 32 bits 0x21–0x3F = Reserved

7.4.12 OUT2_CFG_GPIO

Address: 0x0000 2606

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			OUT2_GPI_POL	—								OUT2_GPO4_SEL	OUT2_GPO3_SEL	OUT2_GPO2_SEL	OUT2_GPO1_SEL
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12	OUT2_GPI_POL	GPI polarity for output Channel 2. 0 = (Default) GPI not inverted 1 = GPI inverted
11:4	—	Reserved
3	OUT2_GPO4_SEL	Select GPIO4 pin as GPO for output Channel 2. 0 = (Default) Disabled 1 = Enabled
2	OUT2_GPO3_SEL	Select GPIO3 pin as GPO for output Channel 2. 0 = (Default) Disabled 1 = Enabled
1	OUT2_GPO2_SEL	Select GPIO2 pin as GPO for output Channel 2. 0 = (Default) Disabled 1 = Enabled
0	OUT2_GPO1_SEL	Select GPIO1 pin as GPO for output Channel 2. 0 = (Default) Disabled 1 = Enabled

7.4.13 OUT1_BIT_PATT_0

Address: 0x0000 2620

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT1_BIT_PATT_0															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	OUT1_BIT_PATT_0	Output Channel 1 SPI bit pattern for external gain control, bits 1-16. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused.

7.4.14 OUT1_BIT_PATT_1

Address: 0x0000 2622

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT1_BIT_PATT_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	OUT1_BIT_PATT_1	Output Channel 1 SPI bit pattern for external gain control, bits 17-32. Only used if the bit pattern is longer than 16 bits. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. If the external gain is controlled using GPIOs, the GPIO1-4 output logic levels are determined by bits 12–15 respectfully.

7.4.15 OUT1_VOL_ANA

Address: 0x0000 2624

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				OUT1_ANA_GAIN											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:11	—	Reserved
10:0	OUT1_ANA_GAIN	Output Channel 1 analog gain. The selected value must match the analog gain of the associated SPI bit pattern. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB 0x002 = 0.250 dB … 0x23F = 71.875 dB 0x240–0x5BF = Reserved 0x5C0 = –72.000 dB … 0x7FF = –0.125 dB

7.4.16 OUT1_VOL_DIG

Address: 0x0000 2626

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT1_UPDATE	—			OUT1_DIG_GAIN											
Access	WO	—			RW											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT1_UPDATE	Output Channel 1 gain update. Write 1 to apply the Channel 1 gain selection and SPI bit pattern. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14:9	—	Reserved
8:0	OUT1_DIG_GAIN	Output Channel 1 digital gain. Note that the signal level is also controlled by the digital volume (OUTx_VOL). 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB 0x002 = 0.250 dB … 0x05F = 11.875 dB 0x060–0x09F = Reserved 0x0A0 = –12.000 dB … 0x0FF = –0.125 dB 0x100–0x1FF = Reserved

7.4.17 OUT2_BIT_PATT_0

Address: 0x0000 2628

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT2_BIT_PATT_0															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	OUT2_BIT_PATT_0	Output Channel 2 SPI bit pattern for external gain control, bits 1-16. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. If the external gain is controlled using GPIOs are used, the GPIO1-4 output logic levels are determined by bits 12–15 respectfully.

7.4.18 OUT2_BIT_PATT_1

Address: 0x0000 262A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT2_BIT_PATT_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	OUT2_BIT_PATT_1	Output Channel 1 SPI bit pattern for external gain control, bits 17-32. Only used if the bit pattern is longer than 16 bits. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. If the external gain is controlled using GPIOs, the GPIO1-4 output logic levels are determined by bits 12–15 respectfully.

7.4.19 OUT2_VOL_ANA

Address: 0x0000 262C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				OUT2_ANA_GAIN											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:11	—	Reserved
10:0	OUT2_ANA_GAIN	Output Channel 2 analog gain. The selected value must match the analog gain of the associated SPI bit pattern. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB 0x002 = 0.250 dB … 0x23F = 71.875 dB 0x240–0x5BF = Reserved 0x5C0 = –72.000 dB … 0x7FF = –0.125 dB

7.4.20 OUT2_VOL_DIG

Address: 0x0000 262E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT2_UPDATE	—							OUT2_DIG_GAIN							
Access	WO	—							RW							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT2_UPDATE	Output Channel 2 gain update. Write 1 to apply the Channel 2 gain selection and SPI bit pattern. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14:9	—	Reserved
8:0	OUT2_DIG_GAIN	Output Channel 2 digital gain. Note that the signal level is also controlled by the digital volume (OUTx_VOL). 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB 0x002 = 0.250 dB … 0x05F = 11.875 dB 0x060–0x09F = Reserved 0x0A0 = –12.000 dB … 0x0FF = –0.125 dB 0x100–0x1FF = Reserved

7.4.21 AUX1_CFG

Address: 0x0000 2900

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				AUX1_SPI_POSITION				—		AUX1_BIT_PATT_LENGTH					
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:11	—	Reserved
10:8	AUX1_SPI_POSITION	AUX Device 1 position in the SPI chain.
7:6	—	Reserved
5:0	AUX1_BIT_PATT_LENGTH	AUX Device 1 bit-pattern length for SPI AUX control. 0x00 = (Default) 0 bits (device not present) 0x01 = 1 bits 0x02 = 2 bits … 0x20 = 32 bits 0x21–0x3F = Reserved

7.4.22 AUX2_CFG

Address: 0x0000 2904

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				AUX2_SPI_POSITION				—		AUX2_BIT_PATT_LENGTH					
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:11	—	Reserved
10:8	AUX2_SPI_POSITION	AUX Device 2 position in the SPI chain.

Bits	Name	Description
7:6	—	Reserved
5:0	AUX2_BIT_PATT_ LENGTH	AUX Device 2 bit-pattern length for SPI AUX control. 0x00 = (Default) 0 bits (device not present) 0x01 = 1 bits 0x02 = 2 bits … 0x20 = 32 bits 0x21–0x3F = Reserved

7.4.23 AUX1_BIT_PATT_0

Address: 0x0000 2920

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AUX1_BIT_PATT_0															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	AUX1_BIT_PATT_0	AUX Device 1 SPI bit pattern, bits 1-16. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused.

7.4.24 AUX1_BIT_PATT_1

Address: 0x0000 2922

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AUX1_BIT_PATT_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	AUX1_BIT_PATT_1	AUX Device 1 SPI bit pattern, bits 17-32. Only used if the bit pattern is longer than 16 bits. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused.

7.4.25 AUX2_BIT_PATT_0

Address: 0x0000 2924

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AUX2_BIT_PATT_0															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	AUX2_BIT_PATT_0	AUX Device 2 SPI bit pattern, bits 1-16. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused.

7.4.26 AUX2_BIT_PATT_1

Address: 0x0000 2926

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AUX2_BIT_PATT_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	AUX2_BIT_PATT_1	AUX Device 2 SPI bit pattern, bits 17-32. Only used if the bit pattern is longer than 16 bits. The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused.

7.5 PIN_CONFIG

7.5.1 PAD_IRQ_CFG

Address: 0x0000 3D1C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ_OP_CFG	—						GPIO1_IRQ_EN	GPIO2_IRQ_EN	—		CONFIG4_IRQ_EN	SPI_SCK_IRQ_EN	—		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IRQ_OP_CFG	IRQ output configuration 0 = (Default) CMOS 1 = Open drain
14:9	—	Reserved
8	GPIO1_IRQ_EN	IRQ output to GPIO1 0 = (Default) GPIO1 1 = IRQ output
7	GPIO2_IRQ_EN	IRQ output to GPIO2 0 = (Default) GPIO2 1 = IRQ output
6:5	—	Reserved
4	CONFIG4_IRQ_EN	CONFIG4 pin function select 0 = (Default) HW config 1 = IRQ output
3	SPI_SCK_IRQ_EN	IRQ output to SPI_SCK 0 = (Default) SPI_SCK 1 = IRQ output
2:0	—	Reserved

7.6 IRQ_CONFIG

7.6.1 IRQ_STS

Address: 0x0000 3E04

RO	15…8	7	6	5	4	3	2	1	0
	—	—							IRQ_STS
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	IRQ_STS	IRQ status. Logical OR of all unmasked x_INT interrupts. 0 = (Default) Not asserted 1 = Asserted

7.6.2 IRQ_HGC_EVENT_INT

Address: 0x0000 3E1E

RW	15…8	7	6	5	4	3	2	1	0
	—	—			HGC_SPI_ERROR_INT	HGC_ABORT_ERROR_INT	—	HGC_ERROR_INT	HGC_DONE_INT
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:5	—	Reserved
4	HGC_SPI_ERROR_INT	HGC Gain update SPI error interrupt. Write 1 to clear. 0 = (Default) Normal 1 = HGC update SPI error
3	HGC_ABORT_ERROR_INT	HGC Gain update aborted interrupt. Write 1 to clear. 0 = (Default) Normal 1 = HGC update aborted
2	—	Reserved

Bits	Name	Description
1	HGC_ERROR_INT	HGC Gain updates failed interrupt. Write 1 to clear. 0 = (Default) Normal 1 = HGC update failed
0	HGC_DONE_INT	HGC Gain updates have completed sucessfully interrupt, rising-edge triggered. Write 1 to clear. 0 = (Default) Normal 1 = HGC gain changed

7.6.3 IRQ_HGC_EVENT_MASK

Address: 0x0000 3E2E

RW	15…8	7	6	5	4	3	2	1	0
	—	—			HGC_SPI_ERROR_MASK	HGC_ABORT_MASK	—	HGC_ERROR_MASK	HGC_DONE_MASK
Default	0x00	0	0	0	1	1	0	1	1

Bits	Name	Description
15:5	—	Reserved
4	HGC_SPI_ERROR_MASK	HGC Gain update SPI error interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
3	HGC_ABORT_MASK	HGC Gain update aborted interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
2	—	Reserved
1	HGC_ERROR_MASK	HGC Gain updates failed interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
0	HGC_DONE_MASK	HGC Gain updates have completed interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt

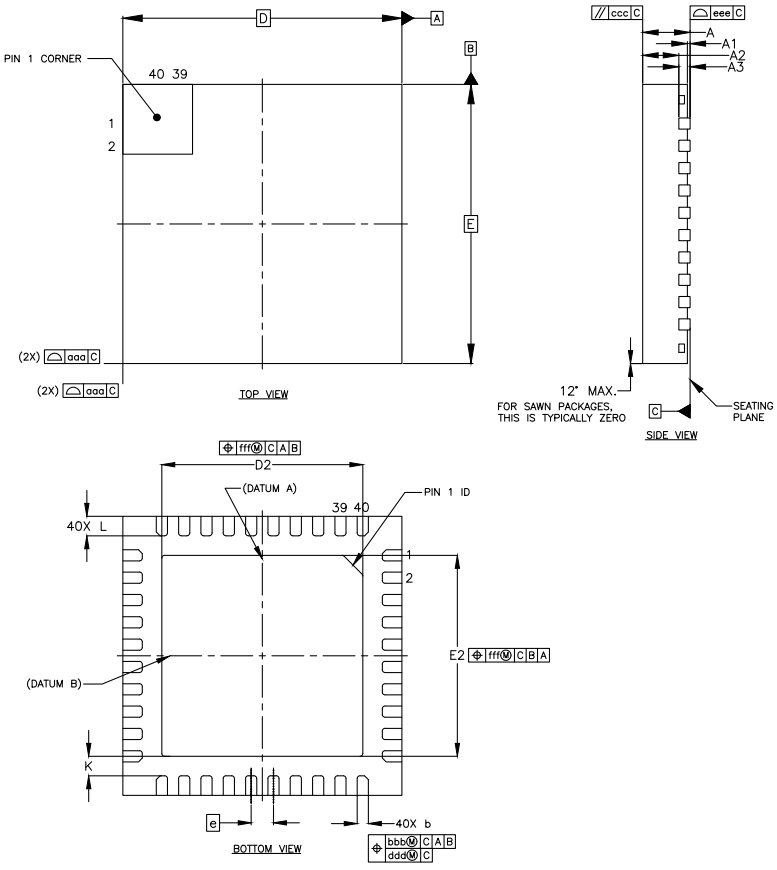
8 Thermal Characteristic

Table 8-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	QFN	Units
Junction-to-ambient thermal resistance	θ_{JA}	32.59	°C/W
Junction-to-board thermal resistance	θ_{JB}	19.57	°C/W
Junction-to-case (top) thermal resistance	θ_{JC}	98.16	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	18.28	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	3.89	°C/W

Notes:
- Natural convection at the maximum recommended operating temperature T_A (see Table 3-2)
- Four-layer, 2s2p PCB as specified by JESD51–9 and JESD51–11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51–12

9 Package Dimensions

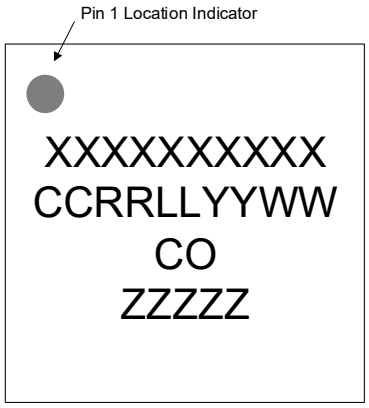


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	–	0.65	–
L/F THICKNESS		A3		0.20 REF.	
LEAD WIDTH		b	0.15	0.20	0.25
BODY SIZE	X	D		5.0 BSC	
	Y	E		5.0 BSC	
LEAD PITCH		e		0.40 BSC	
EP SIZE	X	D2	3.50	3.60	3.70
	Y	E2	3.50	3.60	3.70
LEAD LENGTH		L	0.30	0.35	0.40
LEAD TO EP CLEARANCE		K		0.35 REF.	
PACKAGE EDGE TOLERANCE		aaa		0.10	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	
MOLD FLATNESS		ccc		0.10	
COPLANARITY		eee		0.08	
EXPOSED PAD OFFSET		fff		0.10	

Figure 9-1. QFN Package Drawing

10 Package Marking

Figure 10-1. Package Marking



Top Side Brand
Line 1: Part number
Line 2: Package mark
Line 3: Country of origin (CO)
Line 4: Encoded wafer/device ID

Package Mark Fields
CC = Cirrus Logic Index Code
RR = Device revision code
LL = Lot sequence code
YY = Year of manufacture
WW = Work week of manufacture

11 Ordering Information

Table 11-1. Ordering Information

Product	Description	Package	Environmental Certifications	Grade	Temperature Range	Container	Orderable Part Number
CS4332S	High Performance Two-Channel Audio DAC	40-pin QFN	RoHS Compliant	Commercial	–40 to +85°C	Tray	CS4332S-DN
						Tape and Reel	CS4332S-DNR

12 References

- NXP Semiconductors, UM10204 Rev. 7, October 2021, *I2C-Bus Specification and User Manual*, http://www.nxp.com

13 Revision History

Important: Please check www.cirrus.com or with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Table 13-1. Revision History

Revision	Change
A2 MAY 2026	• Released for public distribution
A1 NOV 2025	• Initial version

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.