CS5312BSE

High Performance Two-Channel Audio ADC

Features

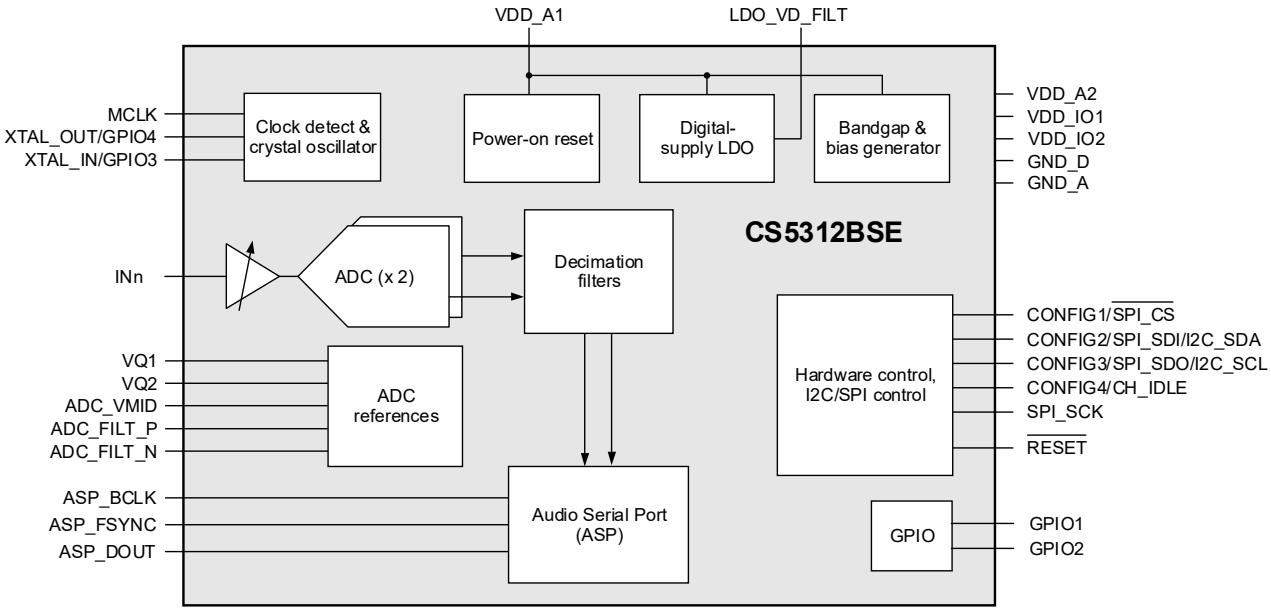
- High performance two-channel ADC
  - Single-ended analog architecture
  - High-resolution 32-bit digital design
  - Low-latency digital filters and digital volume control
- Crystal oscillator interface
- Sample timing alignment across multiple devices
- Virtual passive attenuation device (PAD)
- Clip detection
- Signal activity detection
- Audio serial port (ASP) sample rates up to 384 kHz
  - I²S, left-justified, and TDM data formats
- Hardware and software control modes
  - I²C control port up to 1 MHz
  - SPI control port up to 24 MHz
  - Hardware control with no host processor required
- Single-supply operation at 3.3 V
  - Support for 1.8 V–3.3 V digital input/output
  - 40-pin QFN package

Specifications

- Advanced multibit sigma-delta ADC
  - 110 dB dynamic range (A-weighted)
  - –100 dB total harmonic distortion + noise (THD+N)
  - 3.9/Fs group delay at 48 kHz sample rate
  - 1 V_{RMS} single-ended analog input
  - High-pass filter

Applications

- A/V receivers
- Digital mixing consoles
- Powered speakers
- Power amplifiers
- High-performance speakers and soundbars
- DAW interfaces
- Musical instruments
- Commercial audio systems



Advanced Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product without notice.

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General Description

The CS5312BSE is a high-performance, 32-bit resolution, two-channel ADC. The CS5312BSE supports single-ended analog input and 32-bit digital output via the audio serial port (ASP) at sample rates up to 384 kHz. The ADC input path incorporates internal analog gain for signal amplification without additional noise or increased power consumption, minimizing external component requirements. Overall system efficiency and performance is enhanced by delivering superior input-referred noise performance and maintaining signal integrity between different applications.

The ADC provides single-ended architecture, optimized for high performance combined with low power consumption. The CS5312BSE uses a 5th-order, multibit sigma-delta modulator followed by digital filtering and decimation.

The CS5312BSE can be configured using a control interface supporting I²C and SPI modes of operation. The device can also be operated in hardware mode, using external resistors to select the required configuration. Multiple hardware-control options are supported, including system clocking source, ASP format, and sample rate.

The low-latency digital filters are optimized for the applicable sample rate.

The CS5312BSE includes a virtual PAD function, to emulate a conventional PAD with minimal impact on the noise floor; this minimizes external component requirements leading to a more compact and efficient design. Zero-cross detection is used to synchronize the internal gain changes with zero points in the input signal, avoiding audible gain-change transients. An automatic PAD response feature is incorporated to prevent clipping of large signals at the ASP output.

The ASP supports operation in I²S, left-justified, and TDM data formats. Tristate control of the data-output pin allows multiple devices to operate on a shared bus.

Clocking for the CS5312BSE is provided by a separate clock source (MCLK) or else from the crystal oscillator. The ADC-sample timing is referenced to the ASP data frame, enabling time-aligned operation across multiple devices sharing a common data bus.

The CS5312BSE can be powered from a single 3.3 V supply. Digital output at 1.8 V logic levels is also possible using a separate external supply. The device combines high performance with low power consumption.

The CS5312BSE is available in a commercial-grade 0.4 mm pitch, 40-pin QFN package for operation from -40°C to +85°C.

See Section 11 for ordering information.

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1 Pin Assignments and Descriptions

1.1 40-Pin QFN (Top View, Through-Package)

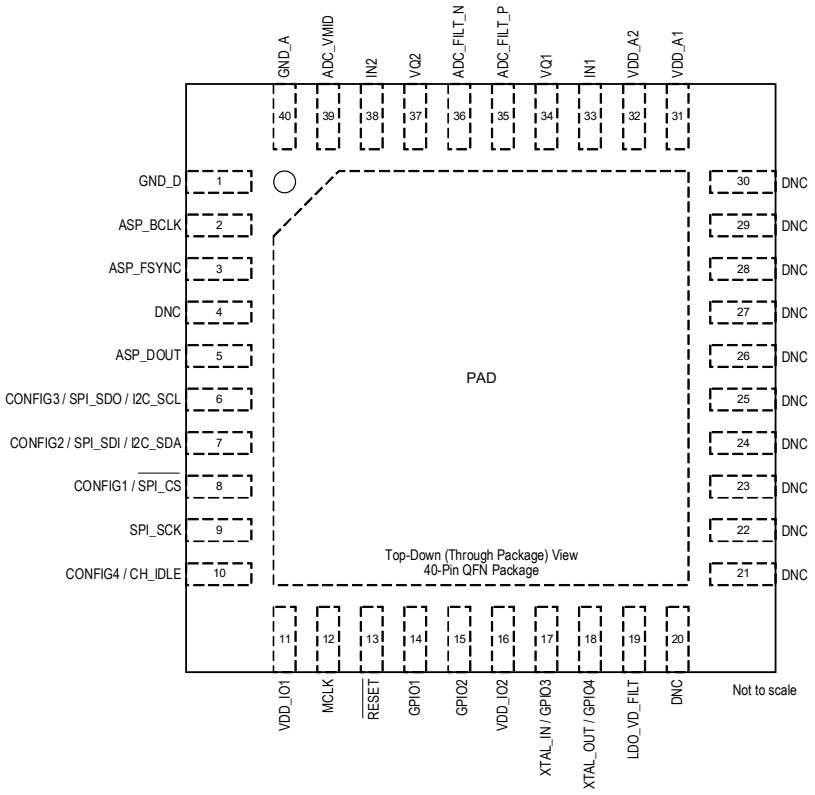


Figure 1-1. QFN 40-Pin Diagram (Top View, Through Package)

1.2 QFN Pin Descriptions

Table 1-1. QFN Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description
				Digital I/O
ASP_BCLK	2	VDD_IO1	I/O	Audio serial port bit clock.
ASP_DOUT	5	VDD_IO1	O	Audio serial port data output.
ASP_FSYNC	3	VDD_IO1	I/O	Audio serial port frame sync.
GPIO1	14	VDD_IO2	I/O	General-purpose input/output.
GPIO2	15	VDD_IO2	I/O	General-purpose input/output.
MCLK	12	VDD_IO1	I/O	Master clock input/output.
$\overline{\text{RESET}}$	13	VDD_IO1	I	Hardware reset control (active low).
XTAL_IN/GPIO3	17	VDD_IO2	I	Input for an external crystal/General-purpose input/output.
XTAL_OUT/GPIO4	18	VDD_IO2	O	Output for an external crystal/General-purpose input/output.
				Analog I/O
ADC_FILT_N	36	VDD_A2	O	ADC external capacitor connection.
ADC_FILT_P	35	VDD_A2	O	
ADC_VMID	39	VDD_A2	O	ADC mid-rail voltage reference output.

Table 1-1. QFN Pin Descriptions *(Cont.)*

Pin Name	Pin #	Power Supply	I/O	Description
CONFIG1/$\overline{\text{SPI\_CS}}$	8	VDD_IO1	I	Hardware control pins.
CONFIG2/SPI_SDI/I2C_SDA	7	VDD_IO1	I/O	In software control mode, CONFIG1–3 support the SPI/I²C interface.
CONFIG3/SPI_SDO/I2C_SCL	6	VDD_IO1	I/O	In software control mode, CONFIG1 selects the I²C target address.
CONFIG4/CH_IDLE	10	VDD_IO1	I/O	In software control mode, CONFIG4 supports Signal Activity Detection.
SPI_SCK	9	VDD_IO1	I	SPI clock input.
IN1	33	VDD_A2	I	Analog input.
IN2	38	VDD_A2	I	
LDO_VD_FILT	19	VDD_A1	O	LDO_D regulator external capacitor connection.
VQ1	34	VDD_A2	I	Quiescent voltage.
VQ2	37	VDD_A2	I	
Power Supplies				
VDD_A1	31	—	—	Analog Supply 1.
VDD_A2	32	—	—	Analog Supply 2.
VDD_IO1	11	—	—	Digital I/O Supply 1.
VDD_IO2	16	—	—	Digital I/O Supply 2.
GND_A	40, PAD	—	—	Analog ground [1].
GND_D	1	—	—	Digital ground [1].
No Connect				
DNC	4, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30	—	—	Do not connect.

1. All ground pins, including the ground paddle, must be tied to a common ground plane directly underneath the CS5312BSE. It is recommended that each ground pin is connected separately to the ground plane; using multiple vias to connect the ground paddle.

1.3 Termination of Unused Pins

Table 1-2 shows the required termination for unused pins (i.e., if the functionality of the pin is not being used). Pins not listed must be connected as shown in the typical connection drawings (see Section 2).

Table 1-2. Termination of Unused Pins

Name	Termination if unused
ASP_DOUT	Float
INn [1]	
MCLK [2]	
VQn [1]	
CONFIG3/SPI_SDO/I2C_SCL	10 kΩ pull-down to GND
CONFIG4/CH_IDLE	
GPIO1	
GPIO2	
SPI_SCK	
XTAL_IN/GPIO3	
XTAL_OUT/GPIO4	
$\overline{\text{RESET}}$	Connect to VDD_IO1

1. If one or more channel is unused, the unused input pin (INn) and the corresponding quiescent reference voltage (VQn) should be left floating (no connection).
2. If the system clock is provided by the crystal oscillator and an MCLK output is not required, MCLK should be left floating.

1.4 Electrostatic Discharge (ESD) Protection

ESD-sensitive device. The CS5312BSE is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD protection standards.

2 Typical Connection Diagrams

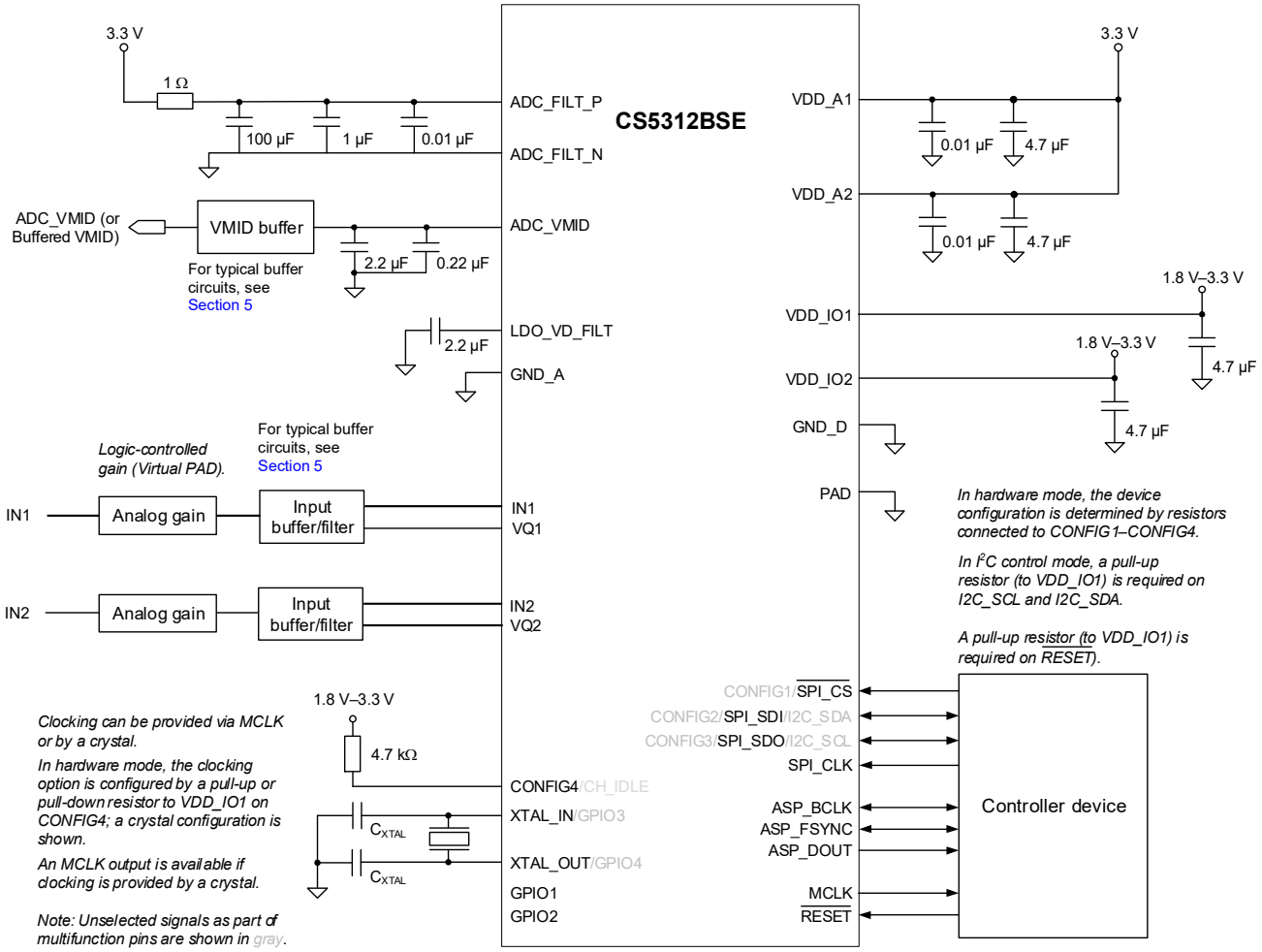


Figure 2-1. Typical Connections

3 Characteristics and Specifications

Note: Table 3-1 defines parameters as they are characterized in this section. Default register field configurations are used unless specified otherwise in the test conditions.

Table 3-1. Parameter Definitions

Parameter	Definition
Channel separation	The difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
Common-mode rejection ratio (CMRR)	The ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
Signal-to-noise ratio	The difference in level between the maximum full-scale output signal and the output with no input signal applied.
Dynamic range	The difference in level between the maximum full-scale output signal and the sum of all harmonic distortion products plus noise with a low-level input signal applied (an input signal level 60 dB below full scale is used).
Power-supply rejection ratio (PSRR)	The ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
Total harmonic distortion plus noise (THD+N)	The ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth relative to the RMS amplitude of the fundamental (i.e., test frequency) output.

Note: Unless specified otherwise, all performance measurements are for a 10 Hz to 20 kHz bandwidth.

Table 3-2. Recommended Operating Conditions

Test conditions (unless specified otherwise): Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Analog supply [1]	VDD_A1, VDD_A2	3.13	3.47	V
	Digital I/O supply	VDD_IO1, VDD_IO2	1.71	3.63	V
Supply ramp up/down (all supplies)		t_{PWR-UD}	0.01	10	ms
Ambient temperature	Commercial Grade	T_A	–40	85	ºC

Note: The device is fully functional and meets all parametric specifications in this section if operated within the specified conditions. Functionality and parametric performance is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

Table 3-3. Absolute Maximum Ratings

Test conditions (unless specified otherwise): Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Analog supply [1]	VDD_A1, VDD_A2	–0.3	4.32	V
	Digital I/O supply	VDD_IO1, VDD_IO2	–0.3	4.32	V
External voltage applied to digital input/output	VDD_IO1 logic pins VDD_IO2 logic pins	V_{INDI}	–0.3 –0.3	VDD_IO1 + 0.3 VDD_IO2 + 0.3	V V
External voltage applied to analog inputs		V_{INAI}	–0.3	VDD_A + 0.3	V
Input current	digital input/output analog inputs	I_{IN}	— —	±10 ±10	mA mA
Ambient operating temperature		T_A	–40	+115	°C
Junction operating temperature		T_J	–40	+125	°C
Storage temperature		T_{STG}	–65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

Table 3-4. ADC Path Characteristics

Test conditions (unless specified otherwise): External components as shown in Fig. 2-1 incorporating the typical output circuit illustrated in Fig. 5-1; VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data, MCLK = 24.576 MHz.

Parameter		Min	Typ	Max	Units
Input impedance (INn)	internal analog gain = 0 dB	—	12	—	kΩ
	internal analog gain = 6 dB	—	6	—	kΩ
	internal analog gain = 12 dB	—	3	—	kΩ
Full-scale input signal level (INn) [1]	0 dBFS output	—	1.0	—	V_{RMS}
SNR	A-weighted	107	110	—	dB
	unweighted	104	107	—	dB
Dynamic range [2]	A-weighted	—	110	—	dB
	unweighted	—	107	—	dB
THD+N	–1 dBFS output	—	–100	–94	dB
	–20 dBFS output	—	–87	—	dB
	–60 dBFS output	—	–47	—	dB
Input-referred noise (A-weighted)	internal analog gain = 0 dB	—	3.16	4.43	μV_{RMS}
	internal analog gain = 6 dB	—	2.24	3.13	μV_{RMS}
	internal analog gain = 12 dB	—	1.58	2.22	μV_{RMS}
Channel separation		—	110	—	dB
Interchannel phase deviation		—	0.03	—	degree
Interchannel gain deviation		—	0.1	—	dB
Gain drift		—	±100	—	ppm/°C
DC offset error	HPF enabled	—	0	—	µV
	HPF disabled	—	100	—	µV
PSRR (VDD_A)	100 mV (peak-peak) 1 kHz sine wave	—	65	—	dB

1. The full-scale input signal level is also the maximum analog input level, before clipping occurs. A sinusoidal input signal is assumed. Full-scale input signal level scales with VDD_A.
2. Dynamic range is derived by measuring the performance including the input buffer, and then deducting the contribution from the input buffer.

Table 3-5. ADC Filter Characteristics

Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal, 32-bit audio data.

Parameter			Min	Typ	Max	Units
Fs = 16 kHz	Passband	to –3 dB corner	—	—	0.47	Fs
	Passband ripple	f ≤ 0.45 Fs	–0.092	—	0.092	dB
	Stopband attenuation	f ≥ 0.55 Fs	98	—	—	dB
	Group delay [1]		—	20.5/Fs	—	s
Fs = 32 kHz	Passband	to –3 dB corner	—	—	0.47	Fs
	Passband ripple	f ≤ 0.45 Fs	–0.092	—	0.092	dB
	Stopband attenuation	f ≥ 0.55 Fs	98	—	—	dB
	Group delay [1]		—	20.5/Fs	—	s
Fs = 44.1 kHz or 48 kHz	Passband	to –3 dB corner	—	—	0.46	Fs
	Passband ripple	f ≤ 0.42 Fs	–0.099	—	0.099	dB
	Stopband attenuation	f ≥ 0.58 Fs	96	—	—	dB
	Group delay [1]		—	3.9/Fs	—	s
Fs = 88.2 kHz or 96 kHz	Passband	to –3 dB corner	—	—	0.43	Fs
	Passband ripple	f ≤ 0.27 Fs	–0.011	—	0.011	dB
	Stopband attenuation	f ≥ 0.77 Fs	103	—	—	dB
	Group delay [1]		—	4.1/Fs	—	s
Fs = 176.4 kHz or 192 kHz	Passband	to –3 dB corner	—	—	0.29	Fs
	Passband ripple	f ≤ 0.12 Fs	–0.010	—	0.010	dB
	Stopband attenuation	f ≥ 0.67 Fs	99	—	—	dB
	Group delay [1]		—	4.2/Fs	—	s
Fs = 352.8 kHz or 384 kHz	Passband	to –3 dB corner	—	—	0.34	Fs
	Passband ripple	f ≤ 0.12 Fs	–0.010	—	0.010	dB
	Stopband attenuation	f ≥ 0.67 Fs	129	—	—	dB
	Group delay [1]		—	4.7/Fs	—	s

1. Group delay is measured from the time at which a signal is presented on the input pins (INn) to the time of the first data bit of the corresponding FSYNC frame being output on the ASP_DOUT pin.

Table 3-6. ADC High-Pass Filter (HPF)

Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter		Min	Typ	Max	Units
Passband	–0.01 dB corner	—	19	—	Hz
	–3 dB corner	—	1	—	Hz
Phase deviation	f = 20 Hz	—	0.001	—	degree
Filter settling time		—	0.4	—	s

Table 3-7. Device Power Consumption

Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Use Configuration		Typical Current (mA)			Total Power (mW)
		I_{VDD_A}	I_{VDD_IO1}	I_{VDD_IO2}	
Reset	$\overline{\text{RESET}}$ = Logic 0	0.70	0.04	0.04	2.574

Table 3-8. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise): Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC.

Parameter		Symbol	Minimum	Maximum	Unit
Input leakage current (per pin)		I_{IN}	—	±10	µA
Input capacitance (per pin)		C_{IN}	—	5	pF
Digital I/O (VDD_IO1 logic pins; see Section 1)[1]	High-level output	V_{OH}	0.9×VDD_IO1	—	V
	Low-level output	V_{OL}	—	0.1×VDD_IO1	V
	High-level input	V_{IH}	0.7×VDD_IO1	—	V
	Low-level input	V_{IL}	—	0.3×VDD_IO1	V
Digital I/O (VDD_IO2 logic pins; see Section 1)[1]	High-level output	V_{OH}	0.9×VDD_IO2	—	V
	Low-level output	V_{OL}	—	0.1×VDD_IO2	V
	High-level input	V_{IH}	0.7×VDD_IO2	—	V
	Low-level input	V_{IL}	—	0.3×VDD_IO2	V

1.If the system clock is not supplied by the crystal oscillator, the XTAL_IN and XTAL_OUT pins are used to support virtual PAD (see Section 4.5.6).

Table 3-9. DC Characteristics

Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC.

Parameter			Minimum	Typical	Maximum	Unit
LDO_VD_FILT	Nominal voltage		—	1.2	—	V
VQn	Nominal voltage		—	1.65	—	V
ADC_FILT [1]	Nominal voltage		—	3.3	—	V
	Maximum output current		—	0.01	—	mA
ADC_VMID [2]	Nominal voltage		—	1.65	—	V
	Maximum output current		—	0.01	—	mA
VDD_A power-on reset (POR) threshold (V_{POR})		VDD_A rising VDD_A falling	2.0 2.0	— —	2.8 2.8	V V
VDD_IO1 power-on reset (POR) threshold (V_{POR})		VDD_IO1 rising VDD_IO1 falling	1.08 0.99	— —	1.58 1.43	V V
VDD_IO2 power-on reset (POR) threshold (V_{POR})		VDD_IO2 rising VDD_IO2 falling	0.45 0.45	— —	0.75 0.74	V V

1.ADC_FILT characteristics are measured between ADC_FILT_P and ADC_FILT_N, and are provided as a guide for external component selection. The output current (arising from capacitor leakage) must be less than the maximum output current of the ADC_FILT_x pin.

2. The output current (arising from capacitor leakage and the input-buffer circuit) must be less than the maximum output current of the ADC_VMID pin. If a larger current is required, an external ADC_VMID buffer should be used. A buffer can be provided using a standard op-amp (noise voltage < 5 nV/√Hz, input current < 10 µA), an example circuit is as follows.

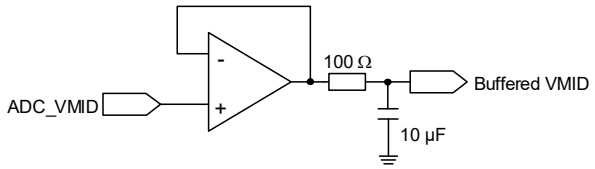


Table 3-10. Switching Specifications—Reset and Clock References

Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC.

Parameter		Symbol	Minimum	Typical	Maximum	Unit
Reset	$\overline{\text{RESET}}$ low (logic 0) pulse width	t_{RLPW}	1	—	—	ms
	$\overline{\text{RESET}}$ rising edge to control port active	t_{IRS}	—	—	5	ms
MCLK input	MCLK frequency	f_{MCLK}	— —	24.576 22.5792	— —	MHz MHz
	MCLK duty cycle	D_{MCLK}	45	—	55	%
	MCLK frequency tolerance	—	–1	—	1	%
MCLK output	MCLK frequency	f_{MCLK}	— —	24.576 22.5792	— —	MHz MHz
	MCLK duty cycle	D_{MCLK}	45	—	55	%
	MCLK frequency accuracy	—	–1	—	1	%
Crystal	Oscillator frequency	f_{XTAL}	— —	24.576 22.5792	— —	MHz MHz
	Interface transconductance VDD_IO2 = 3.3 V VDD_IO2 = 1.8 V	—	— —	26 43	— —	mS mS

Table 3-11. Switching Specifications—Audio Serial Port (ASP)

Test conditions (unless specified otherwise): VDD_A = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-8); T_A = 25°C.

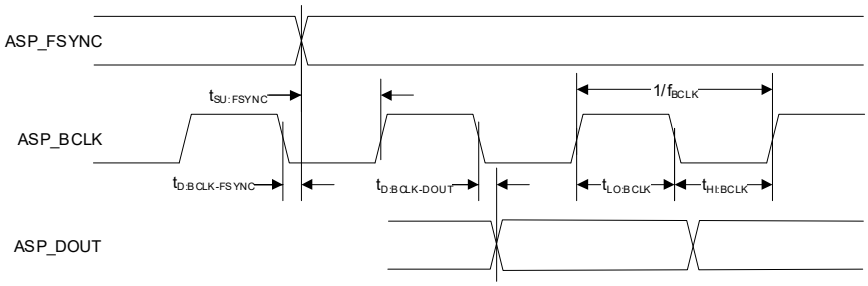
Parameter [1,2,3,4,5]			Symbol	Minimum	Maximum	Unit
Secondary Mode, VDD_IO1 = 3.3 V	ASP_FSYNC input sample/frame rate		Fs	16	384	kHz
	ASP_FSYNC pulse width		$t_{HI:FSYNC}$	$1/f_{ASP\_BCLK}$	—	ns
	ASP_BCLK frequency		f_{BCLK}	1.024	24.576	MHz
	ASP_BCLK high period		$t_{HI:BCLK}$	18	—	ns
	ASP_BCLK low period		$t_{LO:BCLK}$	18	—	ns
	ASP_FSYNC setup time before ASP_BCLK latching edge		$t_{SU:FSYNC}$	5	—	ns
	ASP_FSYNC hold time after ASP_BCLK latching edge		$t_{H:FSYNC}$	5	—	ns
	ASP_DOUT delay after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{D:BCLK–DOUT}$	0 0	10 12	ns ns
	ASP_DOUT Hi-Z delay after ASP_BCLK latching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:HiZ}$	0 0	9 9	ns ns
	ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:EN}$	0 10	10 28	ns ns
	ASP_DOUT load capacitance	ASP_DOUT	—	0	150	pF
Primary Mode, VDD_IO1 = 3.3 V	ASP_FSYNC output sample/frame rate		Fs	16	384	kHz
	ASP_BCLK frequency		f_{BCLK}	2.8224	24.576	MHz
	ASP_BCLK duty cycle		D_{BCLK}	45	55	%
	ASP_FSYNC delay time after ASP_BCLK launching edge		$t_{D:BCLK–FSYNC}$	0	20	ns
	ASP_DOUT delay after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{D:BCLK–DOUT}$	0 0	11 13	ns ns
	ASP_DOUT Hi-Z delay after ASP_BCLK latching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:HiZ}$	0 0	10 10	ns ns
	ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:EN}$	0 7	15 28	ns ns
	ASP_DOUT load capacitance	ASP_BCLK ASP_FSYNC ASP_DOUT	—	0 0 0	50 50 150	pF pF pF
Secondary Mode, VDD_IO1 = 1.8 V	ASP_FSYNC input sample/frame rate		Fs	16	384	kHz
	ASP_FSYNC pulse width		$t_{HI:FSYNC}$	$1/f_{ASP\_BCLK}$	—	ns
	ASP_BCLK frequency		f_{BCLK}	1.024	24.576	MHz
	ASP_BCLK high period		$t_{HI:BCLK}$	18	—	ns
	ASP_BCLK low period		$t_{LO:BCLK}$	18	—	ns
	ASP_FSYNC setup time before ASP_BCLK latching edge		$t_{SU:FSYNC}$	5	—	ns
	ASP_FSYNC hold time after ASP_BCLK latching edge		$t_{H:FSYNC}$	5	—	ns
	ASP_DOUT delay after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{D:BCLK–DOUT}$	0 0	15 17	ns ns
	ASP_DOUT Hi-Z delay after ASP_BCLK latching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:HiZ}$	0 0	12 12	ns ns
	ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:EN}$	0 11	15 33	ns ns
	ASP_DOUT load capacitance	ASP_DOUT	—	0	150	pF

Table 3-11. Switching Specifications—Audio Serial Port (ASP) *(Cont.)*

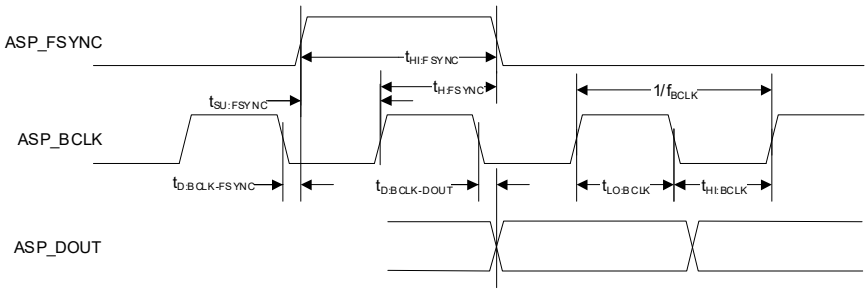
Test conditions (unless specified otherwise): VDD_A = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-8); T_A = 25°C.

Parameter [1,2,3,4,5]			Symbol	Minimum	Maximum	Unit
Primary Mode, VDD_IO1 = 1.8 V	ASP_FSYNC output sample/frame rate		Fs	16	384	kHz
	ASP_BCLK frequency		f_{BCLK}	2.8224	24.576	MHz
	ASP_BCLK duty cycle		D_{BCLK}	45	55	%
	ASP_FSYNC delay time after ASP_BCLK launching edge		$t_{D:BCLK–FSYNC}$	0	20	ns
	ASP_DOUT delay after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{D:BCLK–DOUT}$	0 0	16 18	ns ns
	ASP_DOUT Hi-Z delay after ASP_BCLK latching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:HiZ}$	0 0	13 13	ns ns
	ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge	half-cycle mode, load = 50 pF full-cycle mode, load = 150 pF	$t_{DLY:EN}$	0 7	15 34	ns ns
	ASP_DOUT load capacitance	ASP_BCLK ASP_FSYNC ASP_DOUT	—	0 0 0	50 50 150	pF pF pF

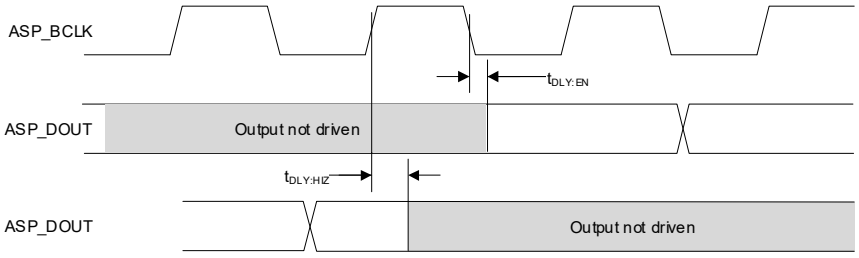
1. The ASP_BCLK launching edge is selectable. Half-cycle mode = ASP_BCLK launching edge is opposite to latching edge. Full-cycle mode = ASP_BCLK launching edge is same as latching edge.
2. ASP timing in I²S and Left-Justified Modes.
   ASP_BCLK can be inverted if required; the figure shows the default polarity in half-cycle mode.



3. ASP timing in TDM Mode.
   ASP_BCLK can be inverted if required; the figure shows the default polarity in half-cycle mode.



4. ASP_DOUT timing for multiple devices sharing the audio serial port bus—half-cycle mode.



5. ASP_DOUT timing for multiple devices sharing the audio serial port bus—full-cycle mode.

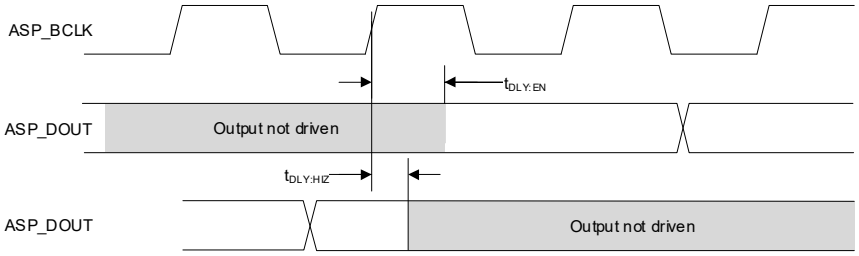
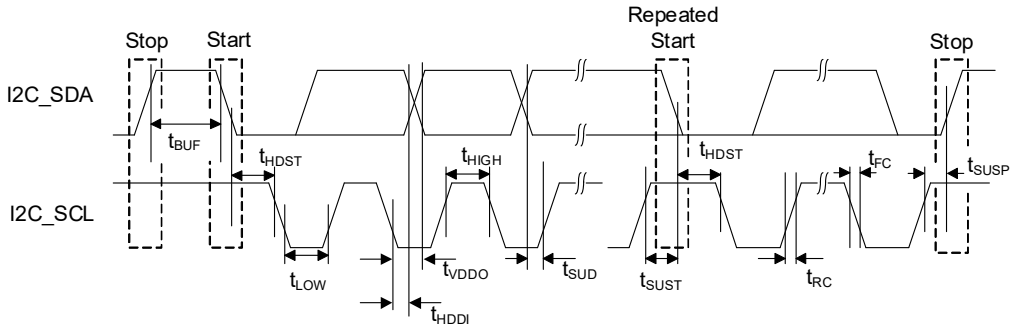


Table 3-12. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-8); T_A = 25°C.

Parameter [1,2]		Symbol	Minimum	Maximum	Unit
SCL clock frequency		f_{SCL}	—	1000	kHz
Clock low time		t_{LOW}	500	—	ns
Clock high time		t_{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)		t_{HDST}	260	—	ns
Setup time for repeated start		t_{SUST}	260	—	ns
Rise time of SCL and SDA	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{RC}	600 180 72	1000 300 120	ns ns ns
Fall time of SCL and SDA	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{FC}	6.5 6.5 6.5	300 300 120	ns ns ns
Rise time variation between SDA and SCL		—	—	1.67	ns
Fall time variation between SDA and SCL	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	—	— — —	100 100 75	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
SDA setup time to SCL rising		t_{SUD}	50	—	ns
SDA input hold time from SCL falling [3]		t_{HDDI}	0	—	ns
Output data valid (Data/ACK) [4]	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
SDA bus capacitance		C_B	—	550	pF
SCL/SDA pull-up resistance		R_P	500	—	Ω
Pulse width of spikes to be suppressed		t_{ps}	0	50	ns

1.All timing is relative to thresholds specified in Table 3-8, V_{IL} and V_{IH} for input signals, and V_{OL} and V_{OH} for output signals.
2.I²C control-port timing.



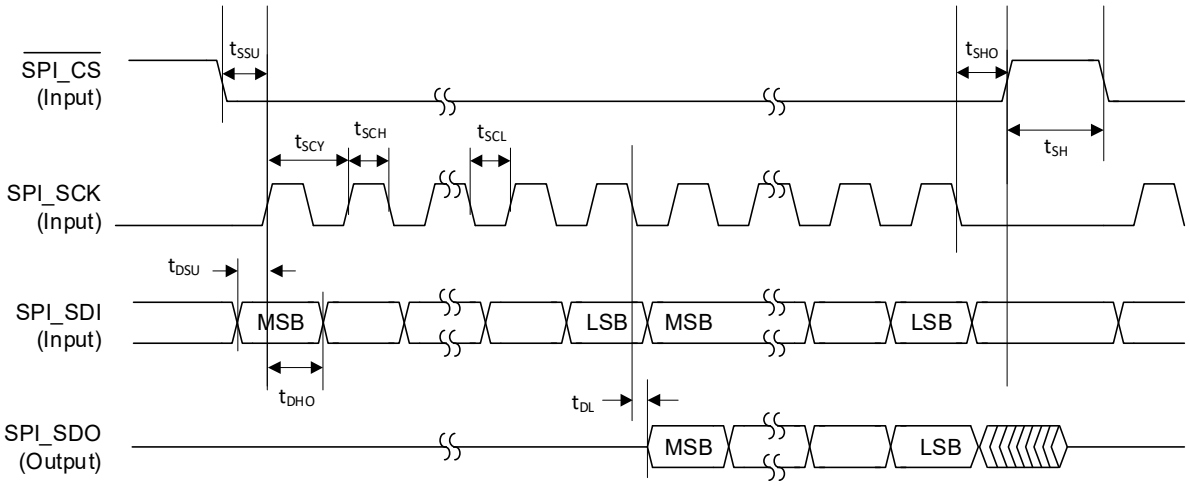
3.Data must be held long enough to bridge the transition time, t_{FC}, of SCL.
4.Time from falling edge of SCL until data output is valid.

Table 3-13. Switching Specifications—SPI Control Port

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; Ground = GND = GND_A = PAD = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-8); T_A = 25°C.

Parameter [1]	Symbol	Minimum	Maximum	Unit
SPI_SCK frequency	f_{SCY}	—	24	MHz
$\overline{\text{SPI\_CS}}$ falling edge to SPI_SCK rising edge	t_{SSU}	5	—	ns
SPI_SCK falling edge to $\overline{\text{SPI\_CS}}$ rising edge	t_{SHO}	0.5	—	ns
SPI_SCK pulse width low	t_{SCL}	18.5	—	ns
SPI_SCK pulse width high	t_{SCH}	18.5	—	ns
SPI_SDI to SPI_SCK setup time	t_{DSU}	5	—	ns
SPI_SDI to SPI_SCK hold time	t_{DHO}	2.5	—	ns
SPI_SCK falling edge to SPI_SDO transition	t_{DL}	0	15	ns
$\overline{\text{SPI\_CS}}$ rising edge to SPI_SDO output high-Z	—	0	15	ns
Bus free time between active $\overline{\text{SPI\_CS}}$	t_{SH}	20	—	ns

1.SPI control-port timing.



4 Functional Description

4.1 Device Power and Reset

The CS5312BSE is powered using VDD_A1, VDD_A2, VDD_IO1, and VDD_IO2 external supplies.

Notes: The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

VDD_IO1 and VDD_IO2 are independent power domains. VDD_IO1 supplies host-related interfaces (e.g., SPI control interface); VDD_IO2 supplies external interfaces (e.g., crystal oscillator connections). Integrated level shifters are included for direct interface to logic levels from 1.8 V to 3.3 V.

There are no power-sequencing requirements—supplies can be enabled in any order.

The CS5312BSE is in reset if the $\overline{\text{RESET}}$ pin is asserted (Logic 0), or if the VDD_A supply is below the respective reset threshold defined in Table 3-9.

All ground pins, including the ground paddle, must be tied to a common ground (GND) plane directly underneath the CS5312BSE.

4.2 Hardware Configuration

The CS5312BSE supports hardware and software control modes. In hardware mode, the device configuration is determined entirely by external resistors connected to the hardware-control pins. In software mode, the I²C/SPI control port is used to configure the device.

In hardware mode, the audio serial port (ASP) configuration is selected using the CONFIG1 and CONFIG2 pins as described in Table 4-1. See Section 4.4 for more details of the sample-rate selection and Section 4.6 for more details of the ASP operation.

Table 4-1. Hardware Control—ASP Configuration

Pin Name	Pin Configuration		Description
CONFIG1	Pull-up to VDD_IO1	0 Ω	Software control mode (I²C/SPI)
		4.7 kΩ	In I²C Mode, the pull-up resistor is used to select the device address—see Section 4.7.
		22 kΩ	In SPI Mode, it is recommended to use a 100 kΩ pull-up resistor.
		100 kΩ	
	Pull-down to GND_D	100 kΩ	ASP Primary Mode, 176.4 kHz, 192 kHz sample rate
		22 kΩ	ASP Primary Mode, 88.2 kHz, 96 kHz sample rate
		4.7 kΩ	ASP Primary Mode, 44.1 kHz, 48 kHz sample rate
		0 Ω	ASP Secondary Mode, autodetect sample rate
CONFIG2	Pull-up to VDD_IO1	0 Ω	ASP TDM Mode—minimum time slots [1], ASP_FSYNC_TYPE = pulse
		4.7 kΩ	ASP TDM Mode—maximum time slots [2], data output on BCLK falling edge (half-cycle mode) [3], ASP_FSYNC_TYPE = pulse
		22 kΩ	ASP TDM Mode—maximum time slots [2], data output on BCLK rising edge (full-cycle mode) [4], ASP_FSYNC_TYPE = pulse
		100 kΩ	ASP TDM Mode—minimum time slots [1], ASP_FSYNC_TYPE = square wave (50% duty cycle) [5]
	Pull-down to GND_D	100 kΩ	ASP TDM Mode—maximum time slots [2], data output on BCLK falling edge (half-cycle mode) [3], ASP_FSYNC_TYPE = square wave (50% duty cycle) [5]
		22 kΩ	ASP TDM Mode—maximum time slots [2], data output on BCLK rising edge (full-cycle mode) [4], ASP_FSYNC_TYPE = square wave (50% duty cycle) [5]
		4.7 kΩ	ASP Left-Justified Mode
		0 Ω	ASP I²S Mode

1. The ASP data format is configured to support two time slots; this is the minimum necessary for the CS5312BSE output.
2. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate, refer to Table 4-12.
3. Half-cycle mode = ASP_DOUT launching edge (BCLK falling) is opposite to the receiving-device latching edge (BCLK rising), refer to Table 3-11.
4. Full-cycle mode = ASP_DOUT launching edge (BCLK rising) is same as the receiving-device latching edge, refer to Table 3-11.
5. ASP_FSYNC_TYPE = square wave (50% duty cycle) is available in ASP Primary Mode only, as described in Section 4.6.

If the ASP is configured for TDM data format with maximum time slots, the TDM slot selection is determined using the CONFIG3 pin as described in Table 4-2. See Section 4.6 for more details of the ASP TDM modes.

Table 4-2. Hardware Control—TDM Slot Selection

Pin Name	Pin Configuration		Description
CONFIG3	Pull-up to VDD_IO1	0 Ω	Slots 14–15 [1]
		4.7 kΩ	Slots 12–13 [1]
		22 kΩ	Slots 10–11 [1]
		100 kΩ	Slots 8–9 [1]
	Pull-down to GND_D	100 kΩ	Slots 6–7 [2]
		22 kΩ	Slots 4–5 [2]
		4.7 kΩ	Slots 2–3
		0 Ω	Slots 0–1

1.Slots 8–15 are only valid in 16-slot TDM Mode.
2.Slots 4–7 are only valid in 8-slot or 16-slot TDM Mode.

The clock-reference and virtual PAD configurations are determined using the CONFIG4 pin as described in Table 4-3. See Section 4.4 for more details of the CS5312BSE clocking architecture, and Section 4.5.6 for more details of virtual PAD function.

Table 4-3. Hardware Control—Clocking Configuration

Pin Name	Pin Configuration		Clock Reference	Reference Clock Frequency (MHz) [1]	Virtual PAD
CONFIG4	Pull-up to VDD_IO1	0 Ω	—	—	Bypassed
		4.7 kΩ	XTAL	512 fs(base)	
		22 kΩ	—	—	
		100 kΩ	MCLK	512 fs(base)	
	Pull-down to GND_D	100 kΩ	—	—	Enabled - Level Detection
		22 kΩ	MCLK	512 fs(base)	
		4.7 kΩ	—	—	Enabled - Edge Detection
		0 Ω	MCLK	512 fs(base)	

1.fs(base) is the base sample rate. fs(base) = 48 kHz for 48 kHz-related sample rates; or 44.1 kHz for 44.1 kHz-related sample rates.

In hardware mode, the device configuration is latched when reset is released (either power-on reset or deassertion of the RESET pin). In hardware mode, the configuration cannot be changed while the device is operational. To update the device configuration, the RESET pin must be asserted (Logic 0), or the device power cycled, in order to read new settings on the CONFIGx pins.

If software mode is selected (i.e., CONFIG1 is pulled-up to VDD_IO1), the device configuration is controlled by register writes via the applicable control interface, as described in Section 4.7. Unused CONFIGx pins should be terminated as described in Section 1.3.

Note: In software mode, the CONFIG1 pin is used to select the I²C target address (see Section 4.7). If the SPI control interface is used, it is recommended to connect the CONFIG1 pin to VDD_IO1 via a 100 kΩ resistor.

4.3 Software Configuration

Software control mode is enabled if the CONFIG1 pin is pulled-up to VDD_IO1; note that RESET must remain asserted (i.e., Logic_0) until CONFIG_1/SPI_CS is deasserted (i.e., Logic_1). In software control mode, the CS5312BSE is configured by writing to control registers using the control port.

The control port supports I²C and SPI modes of operation; the applicable mode is detected automatically on the respective interface pins. In I²C mode, the target address is selectable using the CONFIG1 pin. See Section 4.7 for further details of the I²C/SPI control port.

In software control mode, GLOBAL_EN is used as the global control field for enabling/disabling the CS5312BSE functions. The device should be configured using the applicable control registers before setting GLOBAL_EN.

Note: The clocking (Section 4.4) and ASP (Section 4.6) control registers are only valid on the rising edge of GLOBAL_EN. Writing to these registers has no effect at any other time. It is recommended to select the disabled state (GLOBAL_EN = 0) before writing to these registers.

A reset of the CS5312BSE can be triggered by writing 0x5A to the SW_RESET field. A software reset disables all functions and sets the control registers to their default states.

4.4 System Clocking

Clocking for the CS5312BSE is provided using either the MCLK input or the crystal oscillator. In each case, the frequency must be 512 fs(base); where fs(base) = 48 kHz (for 48 kHz-related sample rates), or 44.1 kHz (for 44.1 kHz-related sample rates). The specifications for the clocking sources are described in Table 3-10.

In hardware mode, the clock source is configured using the CONFIG4 pin, as detailed in Table 4-3. In software mode, the clocking source is selected using SYSCLK_SRC.

The crystal oscillator uses an external crystal (XTAL) to generate the system clock. Load capacitors are connected to the crystal as shown in Fig. 4-1. A series resistor (R_S) may also be required to configure the drive level for the selected crystal.

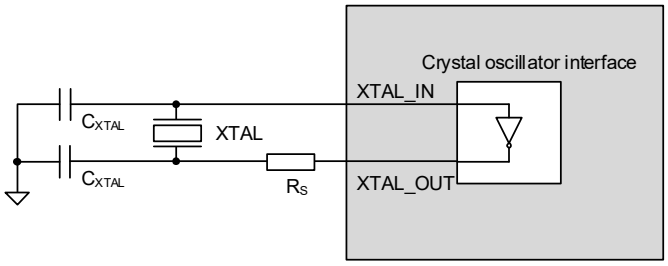


Figure 4-1. Crystal Oscillator Connection

Guidance on selecting a suitable crystal and associated components is provided in Section 5.2. The suitability of the external crystal is calculated as a function of the operating voltage (VDD_IO2) and the transconductance of the crystal interface, as defined in Table 3-10.

If clocking is provided using the crystal oscillator, the CS5312BSE outputs a clock on the MCLK pin. The frequency of the MCLK output clock matches the crystal oscillator frequency. The output clock can be used to drive other devices.

In ASP Secondary Mode, the ASP_FSYNC input is used to control the ADC-sample timing, enabling multiple CS5312BSE devices to operate synchronously (sample timing is phase aligned) in a system. The external clocks ASP_FSYNC and ASP_BCLK must be derived from a common clock source (i.e., the MCLK input, or the MCLK output when clocking is provided using the crystal oscillator). See Section 4.6 for more details of the ASP.

The clocking architecture is illustrated in Fig. 4-2.

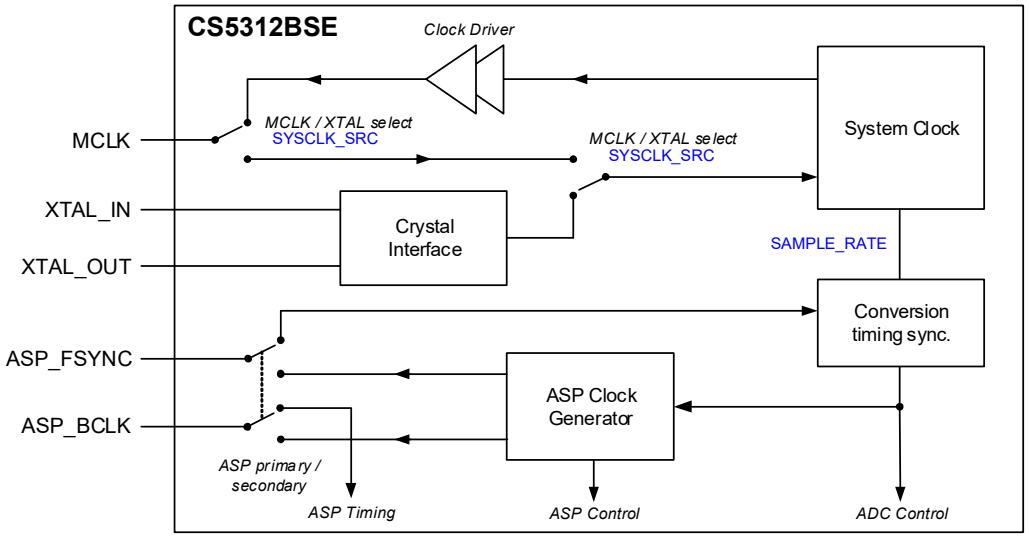


Figure 4-2. System Clocking

4.4.1 Hardware Control Mode

In hardware control mode, the system clock can be sourced from the MCLK pin or from the crystal oscillator. In each case, the frequency must be 512 fs(base); where fs(base) = 48 kHz (for 48 kHz-related sample rates), or 44.1 kHz (for 44.1 kHz-related sample rates). The clock source is configured using the CONFIG4 pin as described in Section 4.2.

The sample rate is selected using the CONFIG1 pin as described in Section 4.2. Sample rates 44.1 kHz–192 kHz can be configured, or else the autodetect option (sample rates 16 kHz–192 kHz) automatically configures the device according to the ASP interface clock signals. The autodetect sample-rate option is only valid if the ASP is operating in Secondary Mode (see Section 4.6).

The supported clocking configurations are summarized in Table 4-4.

Table 4-4. System Clock Configuration

Reference Source	Reference Frequency (MHz)	ASP Operating Conditions [1]
MCLK or XTAL	24.576	Primary or Secondary Mode, I²S, left-justified, or TDM data formats, sample rates 48, 96, and 192 kHz Primary Mode, or sample rates 16, 32, 48, 96, and 192 kHz in Secondary Mode (autodetect only).
MCLK or XTAL	22.5792	Primary or Secondary Mode, I²S, left-justified, or TDM data formats, sample rates 44.1, 88.2, 176.4 kHz in Primary Mode, or sample rates 44.1, 88.2, 176.4 kHz in Secondary Mode (autodetect only).

1. See Section 4.6 for details of the audio serial port (ASP).

The sample rate must be related to the system clock reference as described in Table 4-5.

Table 4-5. Hardware Control Mode Sample Rate Options

Reference Source	Reference Frequency (MHz)	MCLK Out (MHz)	Sample Rate (kHz)
MCLK	22.5792	—	44.1, 88.2, 176.4
	24.576		16, 32, 48, 96, 192
XTAL	22.5792	22.5792	44.1, 88.2, 176.4
	24.576	24.576	16, 32, 48, 96, 192

If the ASP is configured in ASP Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important. If clocking for the CS5312BSE is provided using the crystal oscillator, then the BCLK and FSYNC signals should be derived from the common clock source provided by the CS5312BSE MCLK output, see Section 4.6.

4.4.2 Software Control Mode

In software (I²C/SPI) control mode, the clocking configuration is selected using the following control fields:

- The sample rate is configured using SAMPLE_RATE. Sample rates 16 kHz–384 kHz can be configured, or else the autodetect option automatically configures the device according to the ASP interface signals. The sample-rate autodetect option is only valid for sample rates 16 kHz–192 kHz.
- The system clock source is selected using SYSCLK_SRC. The clock source can be either the crystal oscillator or MCLK.

The system clock frequency must be 512 fs(base); where fs(base) = 48 kHz (for 48 kHz-related sample rates), or 44.1 kHz (for 44.1 kHz-related sample rates). The sample rate must be related to the system clock reference as described in Table 4-6.

Table 4-6. Software Control Mode Sample Rate Options

Reference Source	Reference Frequency (MHz)	MCLK Out (MHz)	Sample Rate (kHz)
MCLK	22.5792	—	44.1, 88.2, 176.4, 352.8
	24.576		16, 32, 48, 96, 192, 384
XTAL	22.5792	22.5792	44.1, 88.2, 176.4, 352.8
	24.576	24.576	16, 32, 48, 96, 192, 384

The sample-rate autodetect option (16 kHz–192 kHz) is only valid if the ASP is operating in Secondary Mode (see Section 4.6).

If the ASP is configured in ASP Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important. If clocking for the CS5312BSE is provided using the crystal oscillator, then the BCLK and FSYNC signals should be derived from the common clock source provided by the CS5312BSE MCLK output, see Section 4.6.

4.5 ADC and Analog Input

The CS5312BSE supports two analog input channels, each incorporating a high-performance sigma-delta analog-to-digital converter (ADC) with integrated programmable analog gain. Digital volume and mute control is also provided on each input channel.

The analog gain, digital volume, and mute controls are supported in software (I2C/SPI) control mode only.

4.5.1 ADC Path Enable

The analog input and ADC paths are enabled using INx_ADC_EN (where x indicates the channel number 1–2).

Note: Both input paths (1–2) must always be configured in the same state (enabled or disabled). For example, input path 1 should not be enabled without also enabling input path 2.

The polarity of the ADC output can be inverted using INx_INV for the respective channel.

4.5.2 Signal-Activity Detection

The CS5312BSE incorporates a signal-activity detection function, enabling the host to control power-management circuits and related functions according to the status of the ADC input channels.The signal-activity detection function controls the CH_IDLE pin output. In a typical use case, CH_IDLE connects to an external PMIC, to control the power supply to the CS5312BSE input buffers. The Logic 0 output selects the fully operational condition; the Logic 1 output selects a low-power operating state.

The signal-activity detection function comprises two features:

- Idle detection: used to determine if the ADC channels are idle. A latching status bit is set if any of the input signals exceed a low-level threshold. The host clears this bit by writing 1. The idle status can be determined by the host on the basis that the status bit is not set for a required duration. Note that the CH_IDLE pin is not controlled by idle detection.
- Active detection: used to control the CH_IDLE pin. CH_IDLE is driven low (Logic 0) by default. If active detection is enabled, CH_IDLE is pulled high (Logic 1); if a high-level threshold is exceeded on any channel, CH_IDLE is driven low (Logic 0) and signal-activity detection (active and idle detection) is disabled. An external pull-up resistor, typically 10 kΩ, is required on CH_IDLE.

Idle detection is used to determine if all input channels are idle. In this event, the host enables active detection, which also selects the low-power PMIC operating state using the CH_IDLE output. If an active signal is detected on any channel, the CH_IDLE pin reverts to Logic 0 to select the fully operational PMIC condition, as illustrated in Fig. 4-3.

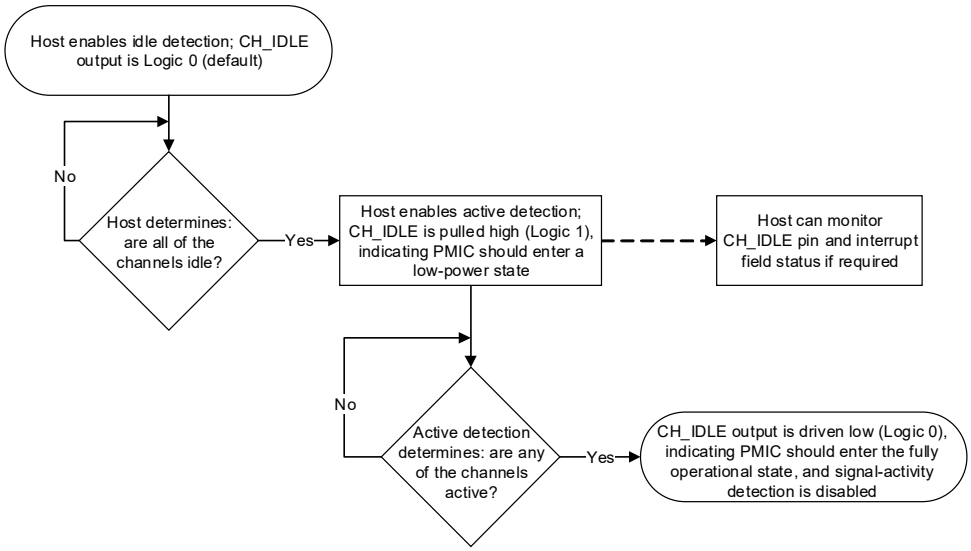


Figure 4-3. Signal Activity Detection Operation

Idle detection is enabled using IN_SIG_ACT_LOW_EN. The signal level is monitored against a low-level threshold; the threshold for each channel is configured using INx_SIG_ACT_LOW_THR(where x indicates the channel number 1–2). If any input channel exceeds the low-level threshold, INx_SIG_ACT_LOW_INT is set. In a typical application, the host polls INx_SIG_ACT_LOW_INT to determine if the input channels have been idle for a required duration, before selecting the low-power PMIC state.

Active detection is enabled using IN_SIG_ACT_HIGH_EN. The signal level is monitored against a high-level threshold; the high-level threshold for each channel is configured using INx_SIG_ACT_HIGH_THR. If any input channel exceeds the high-level threshold INx_SIG_ACT_HIGH_INT is set, the CH_IDLE pin is driven low (Logic 0), and signal-activity detection is disabled (IN_SIG_ACT_LOW_EN and IN_SIG_ACT_HIGH_EN are cleared).

Signal activity detection provides input to the interrupt controller, described in Section 4.8. INx_SIG_ACT_HIGH_INT and INx_SIG_ACT_LOW_INT are latching fields which, once set, remain set until a 1 is written to the respective bit; these bits can be polled at any time or in response to the interrupt being asserted.

Signal detection uses an averaged signal level. The averaged signal level is calculated using an exponential moving average (EMA) function; the time constant is configurable using IN_SIG_ACT_LD_TIME.

The CH_IDLE pin is an open-drain output, enabling multiple devices to drive the Logic 0 condition in a Wired-OR configuration. The host can monitor the CH_IDLE status to determine status of the ADC input channels.

Typical connections are shown in Fig. 4-4.

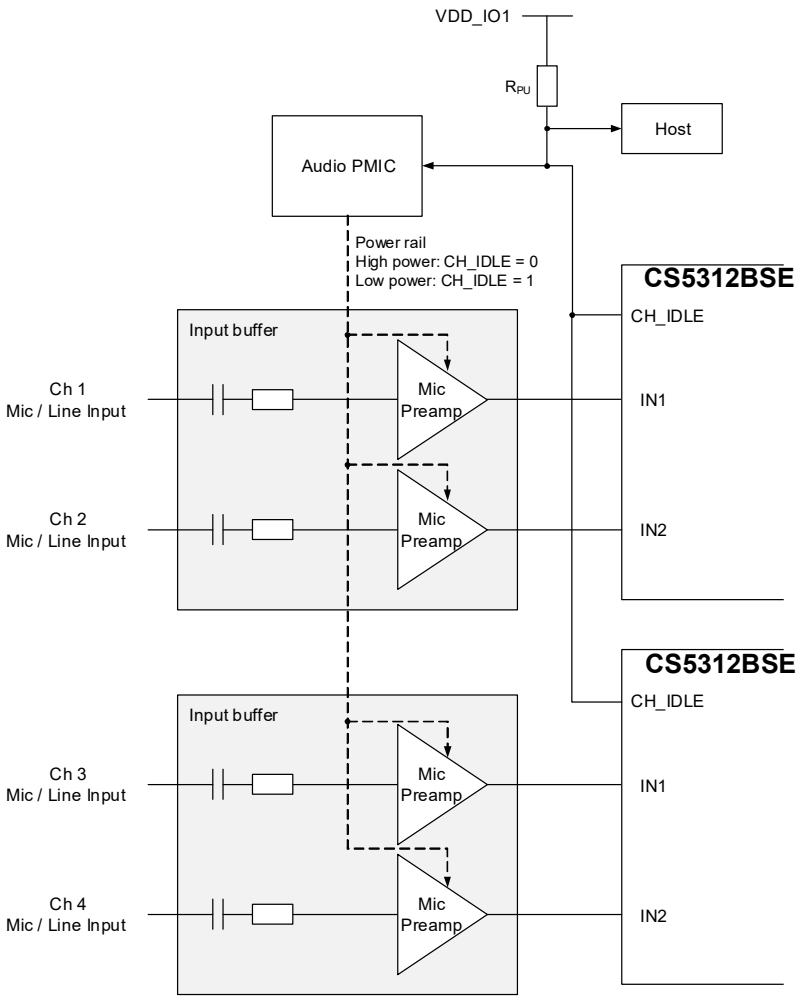


Figure 4-4. Signal Activity Detection

4.5.3 ADC Digital Volume and Mute

The ADC signal path incorporates a digital volume control, supporting a gain range of –127.5 dB to +30 dB in 0.5 dB steps. Volume ramping and digital mute is also supported.

The digital volume is configured using INx_VOL for the respective input channel. The digital mute is enabled by setting INx_MUTE.

Writing to the volume or mute fields has no effect on the signal path until a 1 is written to IN_VU. Writing 1 to IN_VU causes the volume and mute settings to be updated on all input paths simultaneously.

When the volume or mute is changed, the digital gain of the affected signal paths is ramped up or down to the new setting. For increasing gain, the rate is controlled by IN_RAMP_RATE_INC; for decreasing gain, the rate is controlled by IN_RAMP_RATE_DEC.

Note: The IN_RAMP_RATE_INC and IN_RAMP_RATE_DEC fields should not be changed while a volume ramp is in progress.

4.5.4 Input Path Analog and Digital Gain

The ADC signal path incorporates analog gain, minimizing external component requirements. The analog gain enhances overall system efficiency and performance by delivering superior input-referred noise and maintaining signal integrity between different applications.

The analog gain is configurable to 0 dB, 6 dB, or 12 dB. The maximum input signal level at each gain setting is shown in Table 4-7.

Table 4-7. Maximum Input Signal Level per Internal Analog Gain Setting

Internal Analog Gain (dB)	Maximum Input Signal Level (V_{RMS})
0	1
6	0.5
12	0.25

The ADC path incorporates digital gain, supporting a range of –32 dB to +31.875 dB in 0.125 dB steps. The digital gain provides fine adjustment of the overall input path gain, optimizing the dynamic range of the signal path across a wide range of signal levels.

4.5.4.1 Gain Control

Zero-cross detection is used to synchronize the analog and digital gain changes, avoiding audible gain-change transients.

The analog gain is configured for each channel using the respective INx_INT_ANA_GAIN bit (where x indicates the channel number 1–2). By default, both channels are enabled with 0 dB gain.

The digital gain is configured for each channel using INx_INT_DIG_GAIN.

The gain changes are applied upon register write using INx_UPDATE.

Note: The digital volume and digital gain are configured separately. The total digital gain of the input path is the sum of the digital volume and digital gain. Digital volume is described in Section 4.5.3.

4.5.5 Input Clip Warning

The CS5312BSE provides a clip-warning function on the ADC input paths; this can be used to provide a warning of large or clipped signal levels.

The clip-warning threshold level is configured using IN_CLIP_THRESH. The selected level applies to both input channels.

Clip warning provides input to the interrupt controller (see Section 4.8). If an input signal exceeds the clip-warning threshold, the INx_CLIP_WARN_INT bit is set (where *x* indicates the channel number 1–2). These bits are latching fields which, once set, remain set until a 1 is written to the respective bits; these bits can be polled at any time or in response to the logic output signal being asserted.

4.5.6 Virtual PAD

The CS5312BSE includes a virtual PAD function that emulates a conventional PAD with minimal impact on the noise floor; this reduces external component requirements, leading to a more compact and efficient design.

If virtual PAD is used, an external preamplifier attenuates the input signal, emulating a PAD-on status. To emulate a PAD-off status, corresponding gain is applied to compensate for the external attenuation. This architecture ensures a consistent anti-aliasing filter response in either state.

A logic input to a GPIO pin can be used to select PAD-on/off status. In software mode, the PAD-on/off status can also be selected by writing to control registers via the applicable control interface.

If a logic input to a GPIO pin is used to select PAD-on/off status, edge or level detection is supported.

- If edge detection is selected, a rising-edge input on a GPIO pin toggles the PAD-on/off status for each channel. The PAD-on/off status for each channel is provided as a logic output on a GPIO pin; this can be used, for example, to control LEDs for visual indication. The Logic 1 output indicates the PAD-off status; the Logic 0 output indicates the PAD_on status.
- If level detection is selected, a Logic 1 input on a GPIO pin selects PAD-off status and a Logic 0 input selects PAD-on status; a logic output is not provided. The logic levels are described in Table 3-8.

Note: The GPIO logic levels are referenced to the VDD_IO2 domain; level shifting may be required if connecting to a host interface operating at a different level (see Table 3-8 for details).

Virtual PAD is supported in hardware and software modes.

4.5.6.1 Hardware Mode

In hardware mode, the virtual PAD function supports a fixed external attenuation of 20 dB. The CS5312BSE analog and digital gains are configured to provide +20 dB gain if PAD-off status is selected and 0 dB gain if PAD-on status is selected.

Note: Virtual PAD is only supported in hardware mode if the system clock is sourced from MCLK.

Edge or level detection is configured using the CONFIG 4 pin, as shown in Table 4-3.

If edge detection is selected, the GPIO pins as assigned as described in Table 4-8.

Table 4-8. Virtual PAD Edge Detection GPIO Configuration

Pin Number	Pin Name	Function
14	GPIO1	Channel 1 output
15	GPIO2	Channel 2 output
17	GPIO3	Channel 1 input
18	GPIO4	Channel 2 input

If level detection is selected, the GPIO pins are assigned as described in Table 4-9.

Table 4-9. Virtual PAD Level Detection GPIO Configuration

Pin Number	Pin Name	Function
14	GPIO1	—
15	GPIO2	—
17	GPIO3	Channel 1 input
18	GPIO4	Channel 2 input

4.5.6.2 Software Mode

In software mode, the virtual PAD function supports a range of fixed external preamplifier gains; for PAD-on, a maximum attenuation of 20 dB is supported.

- To emulate PAD-off status, the internal analog and digital gains are configured for each channel using INx_HIGH_INT_ANA_GAIN and INx_HIGH_INT_DIG_GAIN respectively (where *x* indicates the channel number 1–2).
- To emulate PAD-on status, the internal analog and digital gains are configured using INx_LOW_INT_ANA_GAIN and INx_LOW_INT_DIG_GAIN respectively.

The gain configuration settings do not take effect until the PAD-on/off status is selected. PAD-off status can be selected by writing 1 to INx_HIGH_UPDATE; PAD-on status can be selected by writing 1 to INx_LOW_UPDATE.

PAD-on/off selection provides input to the interrupt controller, described in Section 4.8. If INx_HIGH_UPDATE and INx_LOW_UPDATE are set concurrently (i.e., PAD-on status and PAD-off status are both selected simultaneously), an interrupt event is indicated using GAIN_CONFLICT_INT. This is a latching bit which, once set, remains set until a 1 is written. This bit can be polled at any time or in response to the interrupt being asserted.

The PAD-on/off status can be selected by a logic input to a GPIO pin; the pin is selected using the respective INx_GPI_SEL bits. Edge or level detection (described in Section 4.5.6) is configured using SW_TYPE.

- If edge detection is selected, the debounce time is configurable using DB_TIME.
- If level detection is selected, a Logic 1 input selects PAD-off status and a Logic 0 input selects PAD-on status; the input polarity can be inverted for each channel using the respective INx_GPI_POL bits.

The PAD-on/off status for each channel can be configured as a logic output on a GPIO pin; the pin is selected using the respective INx_GPO1_SEL to INx_GPO4_SEL bits. For PAD on status, the GPIO output level (i.e. Logic 0 or Logic 1) status is configured using INx_LOW_GPO1 to INx_LOW_GPO4; for PAD off status, the GPIO output level is configured using INx_HIGH_GPO1 to INx_HIGH_GPO4.

Notes: Pins GPIO3 and GPIO4 are not available if the system clock is sourced from the crystal oscillator.

The GPIO logic levels are referenced to the VDD_IO2 domain; level shifting may be required if connecting to a host interface operating at a different level (see Table 3-8 for details).

The current status for each GPIO pin is indicated using GPI_STS and GPO_STS. If the input polarity is inverted (i.e., the INx_GPI_POL bits are set), the GPI_STS bits indicate the opposite logic level to the GPIO pin status.

4.5.6.3 Automatic PAD Response

In software mode, the virtual PAD function incorporates a level detector on the ADC input channels to selectively determine whether the PAD should be turned on. This can be used to prevent clipping of large signals at the ASP output without requiring host intervention. The level detector is enabled on each audio channel using the respective INx_PAD_LD_EN bit (where x indicates the channel number 1–2).

The high and low thresholds associated with the virtual PAD level detector are configured using INx_PAD_HIGH_THR and INx_PAD_LOW_THR respectively.

Signal detection for the high-level threshold uses either the instantaneous or averaged signal level; this is selected using IN_PAD_LD_AVG. Signal detection for the low-level threshold uses the averaged signal level. The averaged signal level is calculated using an exponential moving average (EMA) function; the time constant is configurable using IN_PAD_LD_TIME.

If the input signal exceeds the high-level threshold, the CS5312BSE can automatically select PAD-on status. Automatic PAD response is enabled using INx_PAD_AUTO_EN Note that PAD-on status remains selected until PAD-off is selected by a Logic 1 input to a GPIO pin or by writing 1 to INx_HIGH_UPDATE.

Automatic PAD response provides input to the interrupt controller, described in Section 4.8. If the input signal exceeds the low-level threshold, the INx_PAD_LOW_INT bit is set. If the input signal exceeds the high-level threshold, the INx_PAD_HIGH_INT bit is set. These bits are latching fields which, once set, remains set until a 1 is written. These bits can be polled at any time or in response the interrupt being asserted; the host can use these bits to determine whether to turn the PAD-on, or to turn the PAD-off (including after an automatic response).

4.6 Audio Serial Port (ASP)

The multichannel ASP supports the output of digital audio samples from the CS5312BSE. The ASP can be configured as a primary or secondary interface, and supports I²S, left-justified, and TDM data formats.

Timing specifications for the ASP are described in Table 3-11. An option is supported to drive the output data (DOUT) on the rising or falling BCLK edge; driving on the rising edge (assuming noninverted BCLK polarity) can be used to support a larger load capacitance by increasing the time between the launching edge from the CS5312BSE and the sampling edge at the receiving device.

In hardware control mode, the ASP data format is determined by the CONFIG1 and CONFIG2 pins (see Section 4.2). In software (I²C/SPI) control mode, the ASP data format is configured using register fields.

In hardware mode, sample rates 16 kHz–192 kHz are supported (sample rates 16 kHz and 32 kHz are supported using autodetect in ASP Secondary Mode only). In software mode, sample rates 16 kHz–384 kHz are supported; sample rate 384 kHz is not supported by autodetect. The supported sample rates in ASP Primary Mode and ASP Secondary Mode are summarized in Table 4-10.

Table 4-10. Supported Sample Rates in ASP Primary Mode and ASP Secondary Mode

	ASP Primary Mode		ASP Secondary Mode	
Sample Rate (kHz)	**Hardware Control Mode**	**Software Control Mode**	**Hardware Control Mode**	**Software Control Mode**
16–32	—	Configurable using SAMPLE_RATE	Determined using autodetect only	Configurable using SAMPLE_RATE (autodetect available)
44.1–192	Determined by CONFIG1 pin			
352.8, 384	—		—	Configurable using SAMPLE_RATE (autodetect not available)

4.6.1 Primary and Secondary Operation

The ASP interface can operate as a primary or secondary interface. In the primary configuration, the BCLK and FSYNC signals are generated by the CS5312BSE. In the secondary configuration, the BCLK and FSYNC pins are inputs, allowing another device to drive the respective signals.

In ASP Secondary Mode, the external clocks (MCLK, BLCK, and FSYNC) must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important.

If clocking is provided by the crystal oscillator and the CS5312BSE is operating in ASP Secondary Mode, then the FSYNC and the BCLK signals should be derived from the common clock source provided by the CS5312BSE MCLK output.

In hardware control mode, the ASP is configured as a primary or secondary interface using the CONFIG1 pin (see Section 4.2). In software control mode, the ASP primary/secondary configuration is selected using ASP_PRIMARY.

The ASP operation as a primary or secondary interface with MCLK as the clocking source is illustrated in Fig. 4-5 and Fig. 4-6.

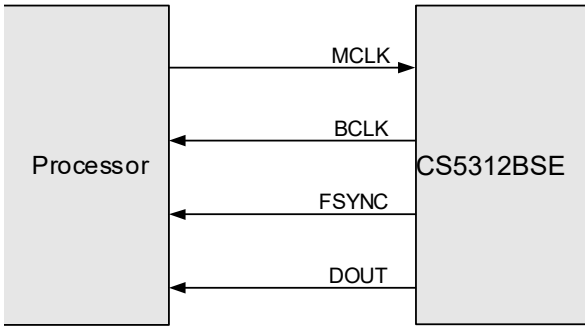


Figure 4-5. Primary Mode, MCLK Clocking Source

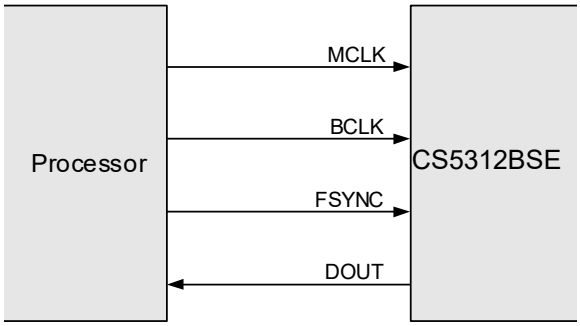


Figure 4-6. Secondary Mode, MCLK Clocking Source

The ASP operation as a primary or secondary interface with a crystal as the clocking source is illustrated in Fig. 4-7 and Fig. 4-8.

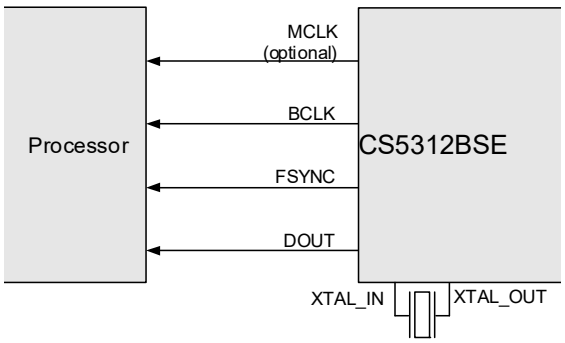


Figure 4-7. Primary Mode, XTAL Clocking Source

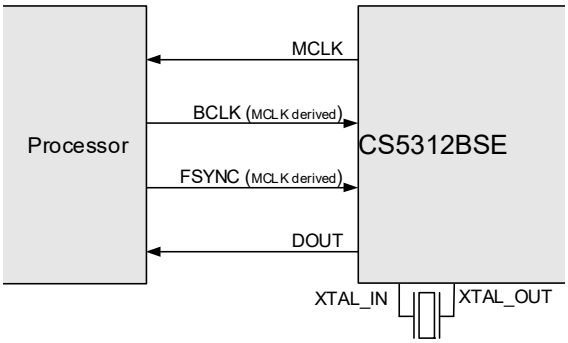


Figure 4-8. Secondary Mode, XTAL Clocking Source

4.6.2 ASP Data Formats

The ASP interface can be configured to operate in I²S, left-justified, or TDM data formats as illustrated in Fig. 4-9 through Fig. 4-11. The data-bit order is MSB first in each case; data words are encoded in 2's complement (signed, fixed-point) format. Each audio sample is allocated a time slot within the FSYNC frame.

- In I²S Mode, the MSB is valid on the second BCLK rising edge following an FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  I²S Mode data format is shown in Fig. 4-9.

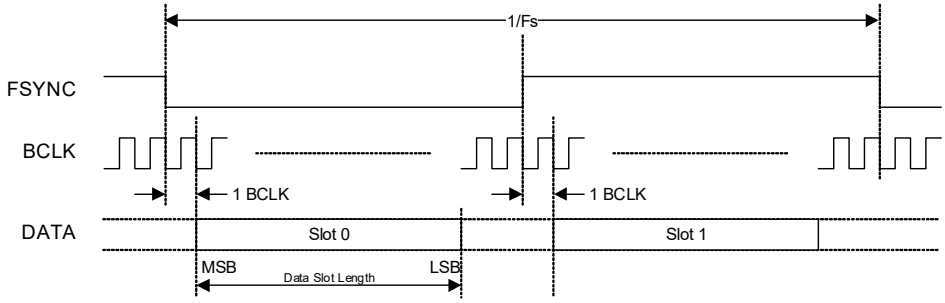


Figure 4-9. I²S Data Format

- In Left-Justified Mode, the MSB is valid on the first BCLK rising edge following an FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  Left-Justified Mode data format is shown in Fig. 4-10.

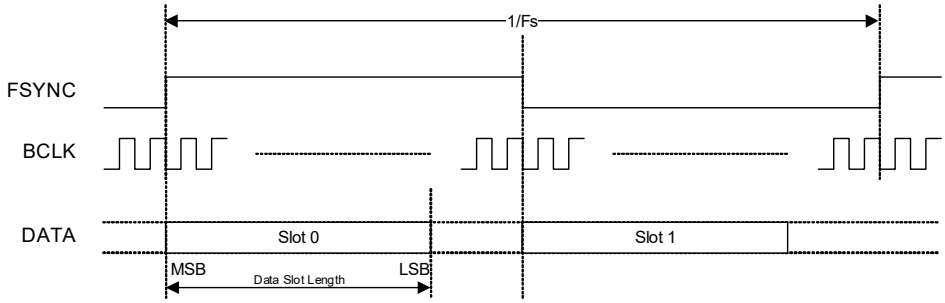


Figure 4-10. Left-Justified Data Format

- In TDM Mode, if the ASP is configured in Secondary Mode, the MSB of the first channel is valid on the second BCLK rising edge following a rising FSYNC edge. The other bits up to the LSB are valid on each successive BCLK cycle.

  If the ASP is configured in Primary Mode, the FSYNC signal can be configured as a pulse (default) or a square wave (with a 50% duty cycle). If the FSYNC signal is configured as a pulse, the MSB of the first channel is valid on the second BCLK rising edge following a rising FSYNC edge. The other bits up to the LSB are valid on each successive BCLK cycle.

  In ASP Secondary Mode and in ASP Primary Mode with the FSYNC signal configured as a pulse, the subsequent channels follow immediately after the first channel. The pulse duration can be anything less than 1/Fs, provided the falling edge of the frame pulse occurs at least one BCLK period before the rising edge of the next frame pulse. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  TDM Mode data format in ASP Secondary Mode and ASP Primary Mode with FSYNC configured as a pulse is shown in Fig. 4-11.

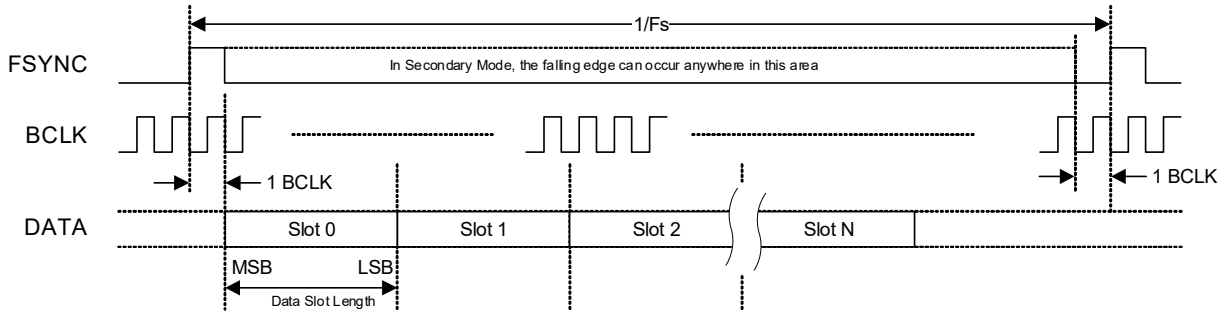


Figure 4-11. TDM Data Format Primary Mode (FSYNC = Pulse) and Secondary Mode

  In ASP Primary Mode with the FSYNC signal configured as a square wave, the slots are aligned with both rising and falling edges of FSYNC and half of the available slots occur within each phase of the FSYNC cycle. The total number of available slots is determined by the sample rate, as described in Table 4-12.

- The MSB of the first channel in each phase of the FSYNC cycle is valid on the second BCLK rising edge following the rising and falling FSYNC edge respectively. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, sample rate, and number of available slots, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  TDM Mode data format in ASP Primary Mode with FSYNC configured as a square wave is shown in Fig. 4-12.

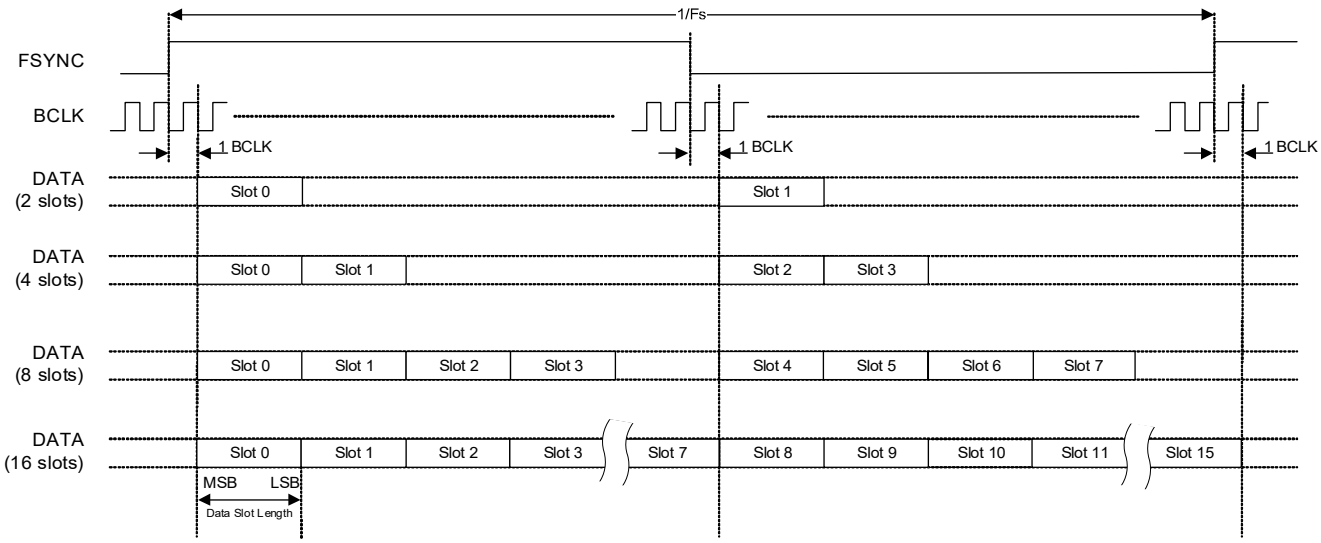


Figure 4-12. TDM Data Format Primary Mode (FSYNC = Square Wave)

4.6.3 ASP Configuration

In hardware control mode, the ASP data format is determined by the CONFIG1 and CONFIG2 pins (see Section 4.2).

In software control mode, the ASP data format is configured using SAMPLE_RATE, and ASP_FORMAT. If ASP Primary Mode is selected (see Section 4.6.1), the BCLK frequency is configured using ASP_BCLK_FREQ and the FSYNC waveform type (pulse or square wave) is configured using ASP_FSYNC_TYPE.

In software control mode, the BCLK polarity is selected using ASP_BCLK_INV. The polarity selection is valid in Primary and Secondary Modes, and determines whether the data is valid for sampling on the rising edge or the falling edge.

The BCLK polarity is illustrated in Fig. 4-13 and Fig. 4-14. In hardware control mode, the BCLK polarity is assumed to be noninverted.

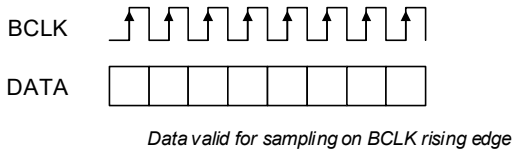


Figure 4-13. Noninverted BCLK

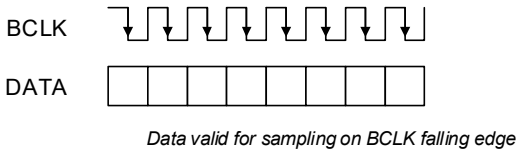


Figure 4-14. Inverted BCLK

In TDM Mode, the two data-format options are supported as follows:

- TDM Mode—minimum slots. The ASP data format is configured to support two slots. This mode allows the BCLK rate to be as low as possible, equating to a minimum of 128 BCLK cycles per audio sample at a minimum sample rate of 64 Fs.
- TDM Mode—maximum time slots. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate. The mode is designed for the maximum BCLK rate (22.5792 MHz for 44.1 kHz-related sample rates, or 24.576 MHz for 48 kHz-related sample rates), enabling the maximum possible bandwidth on the ASP data bus to be shared with other devices.

If the ASP is configured for TDM Mode with maximum time slots, the output data (DOUT) can be driven either on the rising or falling BCLK edge. Driving on the rising edge (assuming noninverted BCLK polarity) can be used to support a larger load capacitance by increasing the time between the launching edge from the CS5312BSE and the sampling edge at the receiving device.

Note that the ASP timing options are dependent on the behavior of the receiving device. It is assumed, for noninverted BCLK, the data is sampled on the rising BCLK edge. Similarly, for inverted BCLK, it is assumed the data is sampled on the falling BCLK edge.

The DOUT drive options for half-cycle and full-cycle mode are described in Table 4-11. In full-cycle mode, the output data is driven on the same BCLK edge as it is sampled (i.e., one full BCLK cycle before the sampling edge). In half-cycle mode, the output data is driven on the opposite BCLK edge as it is sampled (i.e. one half BCLK cycle before the sampling edge), this is also illustrated in Table 3-11.

Table 4-11. TDM Mode (Maximum Time Slots)—DOUT Drive Timing

TDM Mode [1]	BCLK Polarity [2]	DOUT Launching (Drive) Edge	DOUT Latching (Sampling) Edge
Half-cycle	Noninverted	BCLK falling	BCLK rising
	Inverted	BCLK rising	BCLK falling
Full-cycle	Noninverted	BCLK rising	BCLK rising
	Inverted	BCLK falling	BCLK falling

1. The TDM variant is selected using the CONFIG2 pin (in hardware control mode) or ASP_FORMAT (in software control mode).
2. The BCLK polarity is selected using ASP_BCLK_INV in software control mode. In hardware control mode, the polarity is assumed noninverted.

The ASP configuration depends on the sample rate and the selected data format as described in Table 4-12.

Table 4-12. ASP Data Format

ASP Format [1]	ASP Sample Rate [2,3]	Time Slots per Frame [4]	BCLK Rate[5,6]
I²S, Left-Justified	16 kHz	2	BCLK ≥ 64×Fs[7]
	32 kHz		BCLK ≥ 64×Fs[8]
	44.1 kHz, 48 kHz		BCLK ≥ 64×Fs
	88.2 kHz, 96 kHz		BCLK ≥ 64×Fs
	176.4 kHz, 192 kHz		BCLK ≥ 64×Fs
	352.8 kHz, 384 kHz		BCLK ≥ 64×Fs
	Autodetect (16 kHz–192 kHz)		BCLK ≥ 64×Fs
TDM—minimum time slots	16 kHz		BCLK ≥ 64×Fs[7]
	32 kHz		BCLK ≥ 64×Fs[8]
	44.1 kHz, 48 kHz		BCLK ≥ 64×Fs
	88.2 kHz, 96 kHz		BCLK ≥ 64×Fs
	176.4 kHz, 192 kHz		BCLK ≥ 64×Fs
	352.8 kHz, 384 kHz		BCLK ≥ 64×Fs
	Autodetect (16 kHz–192 kHz)		BCLK ≥ 64×Fs
TDM—maximum time slots	16 kHz	16	BCLK ≥ 512×Fs[7]
	32 kHz		BCLK ≥ 512×Fs[8]
	44.1 kHz, 48 kHz		BCLK = 512×Fs
	88.2 kHz, 96 kHz	8	BCLK = 256×Fs
	176.4 kHz, 192 kHz	4	BCLK = 128×Fs
	352.8 kHz, 384 kHz	2	BCLK = 64×Fs
	Autodetect (16 kHz–192 kHz)	4	BCLK ≥ 128×Fs

1. The ASP format is selected using the CONFIG2 pin (in hardware control mode) or ASP_FORMAT (in software control mode).
2. The sample rate is selected using the CONFIG1 pin (in hardware control mode) or SAMPLE_RATE (in software control mode).
3. Sample rates 16 kHz–192 kHz are supported in hardware and software control modes; sample rate 384 kHz is supported in software control mode only.
4. Time slots per frame is the number of data-sample time slots supported on the DOUT pin.
5. The BCLK rate must be a constant integer multiple of the sample rate (Fs).
6. In ASP Primary Mode (hardware control), the BCLK frequency is the minimum specified rate. In ASP Primary Mode (software control), the BCLK frequency is configured using ASP_BCLK_FREQ.
7. In ASP Primary Mode, the specified minimum BCLK frequency for 16 kHz sample rate is not supported. The available options correspond to 192×Fs, 384×Fs, 768×Fs, or 1536×Fs
8. In ASP Primary Mode, the specified minimum BCLK frequency for 32 kHz sample rate is not supported. The available options correspond to 96×Fs, 192×Fs, 384×Fs, or 768×Fs.

The ASP data format in I²S, Left-Justified, and TDM interface modes as illustrated in Fig. 4-15 through Fig. 4-18. Refer to Table 4-12 for the applicable definition.

- If I²S data format is selected, the ASP supports audio channels 1–2 as shown in Fig. 4-15. The minimum BCLK rate is 64×Fs (where Fs is the sample rate). In ASP Primary Mode, the minimum BCLK rate of 64×Fs is not supported for sample rates of 16 kHz or 32 kHz. A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

  The output data is provided on ASP_DOUT.

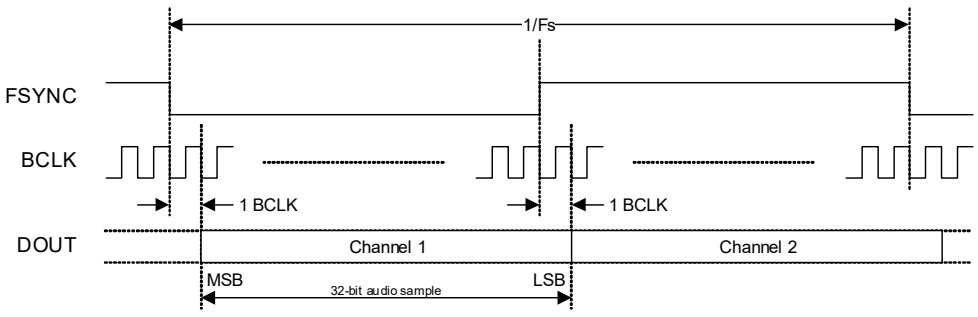


Figure 4-15. I²S Data Format

- If Left-Justified data format is selected, the ASP supports audio channels 1–2 as shown in Fig. 4-16. The minimum BCLK rate is 64×Fs (where Fs is the sample rate). In ASP Primary Mode, the minimum BCLK rate of 64×Fs is not supported for sample rates of 16 kHz or 32 kHz. A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

  The output data is provided on ASP_DOUT.

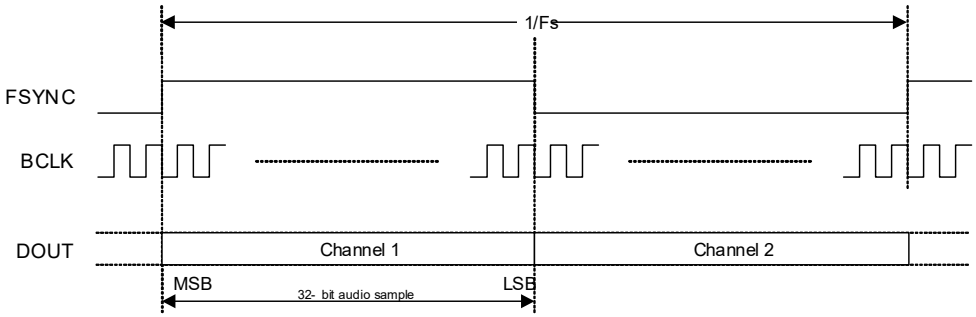


Figure 4-16. Left-Justified Data Format

- In TDM Mode, the FSYNC frame is configured for 2, 4, 8, or 16 slots as specified in Table 4-12.

  In 4-, 8-, and 16-slot modes, the slot assignment for audio channels 1–2 is selected using the CONFIG3 pin (in hardware control mode—see Section 4.2) or else using ASP_TDM_SLOT (in software control mode). In 2-slot modes, the default slot assignment (slots 0–1) should be selected.

  The BCLK rate is related to the sample rate (Fs) as described in Table 4-12. Where applicable, the BCLK rate can be higher than the stated minimum, resulting in additional unused BCLK cycles between the last slot in the frame and the start of the next frame.

  The ASP_DOUT pin is high impedance if the CS5312BSE is not transmitting data, allowing other devices on the bus to transmit data during any unused time slots.

  The output data is provided on ASP_DOUT.

  An example of the 4-slot TDM format in ASP Secondary Mode and in ASP Primary Mode with the FSYNC signal configured as a pulse is shown in Fig. 4-17. In this example, audio channels 1–2 occupy TDM slots 0–1 respectively.

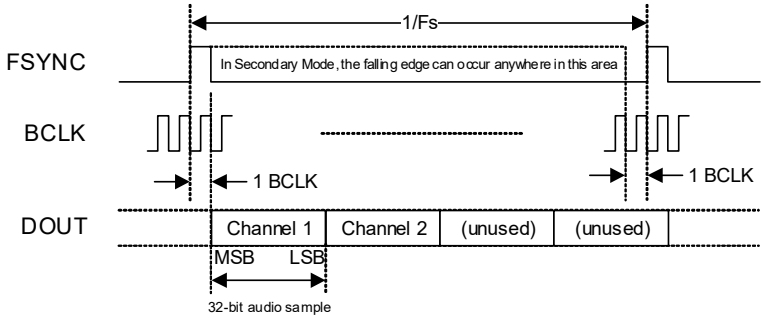


Figure 4-17. TDM Data Format, 4-Slot Example (FSYNC = Pulse)

An example of the 4-slot TDM format in ASP Primary Mode with the FSYNC signal configured as a square wave is shown in Fig. 4-18. In this example, audio channels 0 and 1 occupy TDM slots 0 and 1 in the high (Logic 1) phase of the FSYNC signal, TDM slot 0 and 1 in the low (Logic 1) phase of the FSYNC signal are unused.

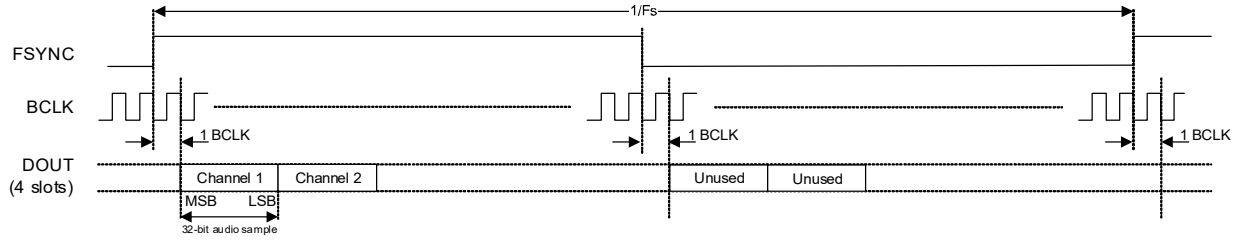


Figure 4-18. TDM Data Format, 4-Slot Example (FSYNC = Square Wave)

4.7 I²C/SPI Control Port

The CS5312BSE incorporates a control port, supporting I²C or SPI modes of operation; this is selected using CONFIG1, as described in Table 4-1. If the SPI control interface is required, it is recommended to use a pull-up resistor of 100 kΩ. In software control mode, the CS5312BSE is configured by writing to control registers using the control port.

The control port is automatically configured in I²C mode or SPI mode following the first valid I²C/SPI activity detected after power-on or hardware reset.

4.7.1 I²C Control Port

The I²C control port is supported using the following pins, which must be configured for the I²C function if required:

- CONFIG2/SPI_SDI/I2C_SDA
- CONFIG3/SPI_SDO/I2C_SCL

The CS5312BSE is a target device on the I²C bus—SCL is a clock input, while SDA is a bidirectional data pin. To allow arbitration of multiple targets (and/or multiple controllers) on the same interface, the CS5312BSE transmits Logic 1 by tristating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the Logic 1 can be recognized by the controller.

In order to allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit device address (this is not the same as the address of each register in the CS5312BSE). The LSB of the device address is the read/write bit; this bit is set to Logic 1 for read and Logic 0 for write.

The I²C device address is configured using the CONFIG1 pin as described in Table 4-13.

Table 4-13. I2C Address Selection—CONFIG1 pin

Pin Configuration		I2C Address
Pull-up to VDD_IO1	0 kΩ	0x26 (write), 0x27 (read)
	4.7 kΩ	0x24 (write), 0x25 (read)
	22 kΩ	0x22 (write), 0x23 (read)
	100 kΩ	0x20 (write), 0x21 (read)

The host device indicates the start of data transfer with a high-to-low transition on SDA while SCL remains high. This indicates that a device address and subsequent address/data bytes follow. The CS5312BSE responds to the start condition and shifts in the next 8 bits on SDA (8-bit device address, including read/write bit, MSB first). If the device address received matches the device address of the CS5312BSE, the CS5312BSE responds by pulling SDA low on the next clock pulse (ACK). If the device address is not recognized or the R/W bit is set incorrectly, the CS5312BSE returns to the idle condition and waits for a new start condition.

If the device address matches the device address of the CS5312BSE, the data transfer continues. The controller indicates the end of data transfer with a low-to-high transition on SDA while SCL remains high. After receiving a complete address and data sequence the CS5312BSE returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e., SDA changes while SCL is high), the device returns to the idle condition.

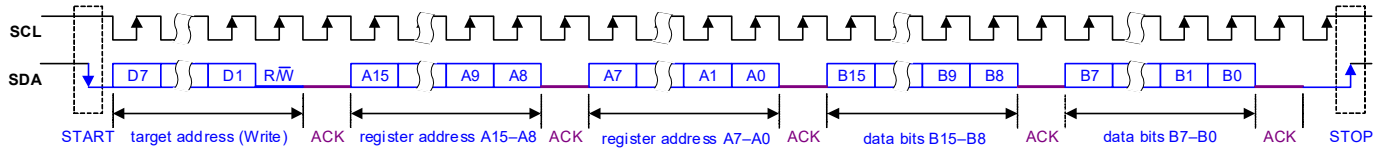
The I²C interface uses a 16-bit register address and 16-bit data words. The register address must be aligned to a 16-bit word boundary (i.e., the LSB must be 0). The full I²C message protocol also includes a device address, a read/write bit, and other signaling bits (see Fig. 4-19 and Fig. 4-20).

The CS5312BSE supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. In these modes, the CS5312BSE automatically increments the register address after each data word. Successive data words can be input/output every two data bytes.

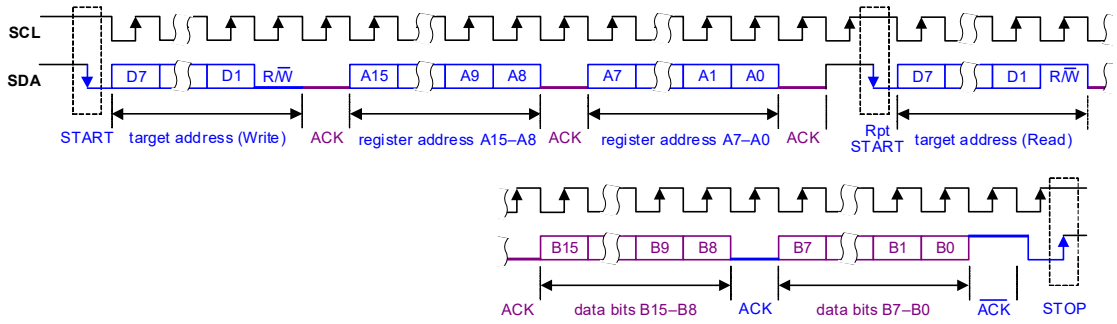
The I²C protocol for a single, 16-bit register write operation is shown in Fig. 4-19.



Note: The SDA pin is used as input for the control register address and data; SDA is pulled low by the receiving device to provide the acknowledge (ACK) response

Figure 4-19. Control Interface I²C Register Write

The I²C protocol for a single, 16-bit register read operation is shown in Fig. 4-20.



Note: The SDA pin is driven by both the controller and target devices in turn to transfer target address, register address, data and ACK responses

Figure 4-20. Control Interface I²C Register Read

The control interface also supports other register operations; the interface protocol for these operations is shown in Fig. 4-21 through Fig. 4-24. The terminology used in the following figures is detailed in Table 4-14.

Table 4-14. Control Interface (I2C) Terminology

Terminology	Description
S	Start condition
Sr	Repeated start
A	Acknowledge (SDA low)
$\overline{A}$	No Acknowledge (SDA high)
P	Stop condition
R/$\overline{W}$	Read/not Write: 0 = Write, 1 = Read
[White field]	Data flow from bus controller to CS5312BSE
[Gray field]	Data from CS5312BSE to bus controller

Fig. 4-21 shows a single register write to a specified address.

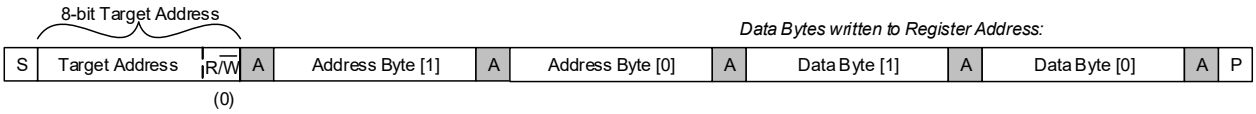


Figure 4-21. Single-Register Write to Specified Address

Fig. 4-22 shows a single register read from a specified address.

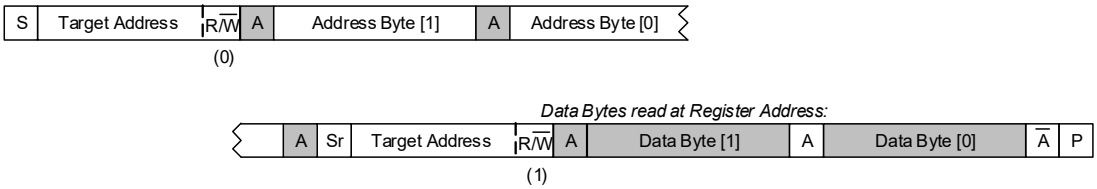


Figure 4-22. Single-Register Read from Specified Address

Fig. 4-23 shows a multiple register write to a specified address.

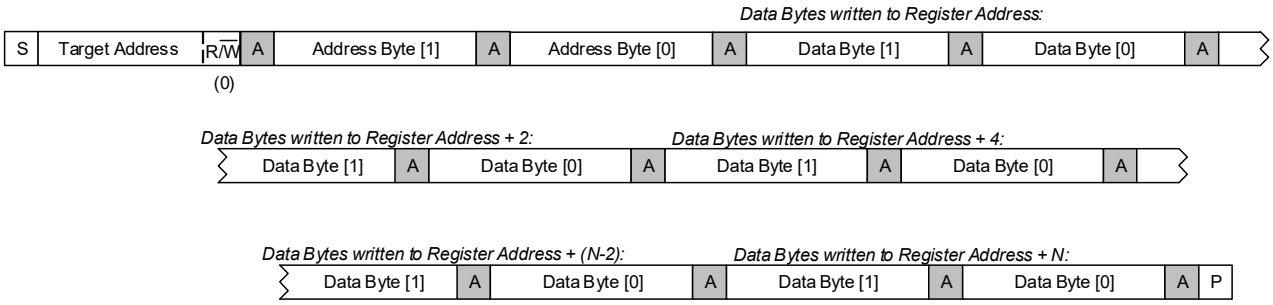


Figure 4-23. Multiple-Register Write to Specified Address

Fig. 4-24 shows a multiple register read from a specified address.

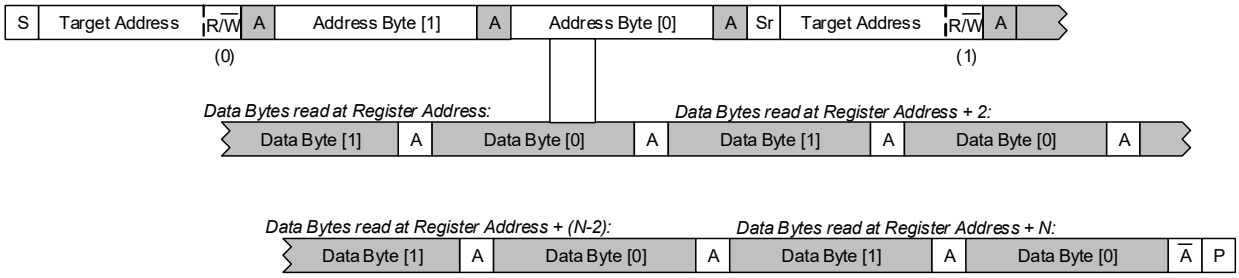


Figure 4-24. Multiple-Register Read from Specified Address

4.7.2 SPI Interface

The SPI interface is supported using the following pins, which must be configured for the SPI function if required:

- CONFIG1/SPI_CS
- CONFIG2/SPI_SDI/I2C_SDA
- CONFIG3/SPI_SDO/I2C_SCL
- SPI_SCK

To ensure that the control port is inactive prior to use, SPI_CS must be deasserted (i.e., Logic 1) during device startup; RESET must remain asserted (i.e., Logic_0) until SPI_CS is deasserted (i.e., Logic_1), timing information is provided in Table 3-10.

The SDI (data-input) pin supports the following behavior:

- In write operations (R/W = 0), the SDI pin input is driven by the controlling device.
- In read operations (R/W = 1), the SDI pin is ignored following receipt of the valid register address.

The SDO (data-output) pin supports the following behavior:

- If CS is asserted (Logic 0), the SDO output is actively driven when outputting data and is high impedance at other times. If CS is not asserted, the SDO output is high impedance.
- The high-impedance state of the SDO output allows the pin to be shared with other peripheral devices.
- The output (SDO) data bit is available to the host device at the rising edge of SCK. See Table 3-13 for timing information.

The SPI interface uses a 15-bit register address and 16-bit data words. The full SPI message protocol also includes a read/write bit and a 16-bit padding phase (see Fig. 4-25 and Fig. 4-26).

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS5312BSE automatically increments the register address at the end of each data word, for as long as CS is held low and SCK is toggled. Successive data words can be input/output every 16 clock cycles.

The SPI protocol is shown in Fig. 4-25 and Fig. 4-26.

Fig. 4-25 shows a single register write to a specified address.

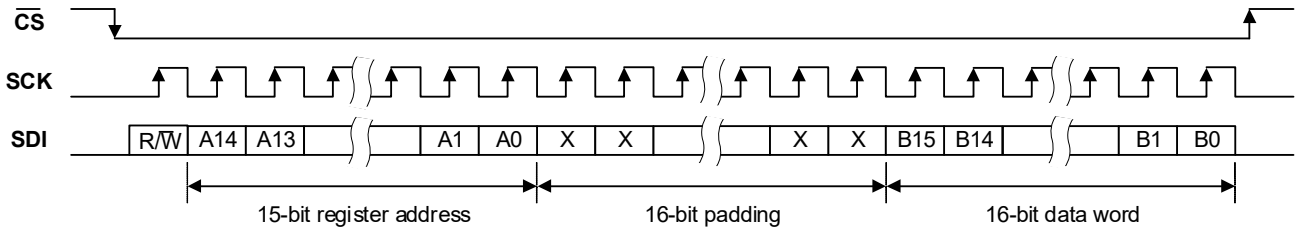


Figure 4-25. Control Interface SPI Register Write

Fig. 4-26 shows a single register read from a specified address.

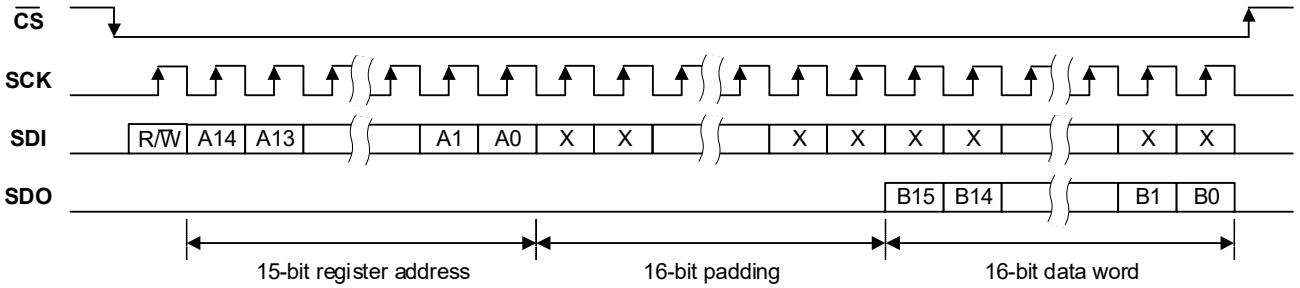


Figure 4-26. Control Interface SPI Register Read

Fig. 4-27 shows a multiple register write to a specified address.

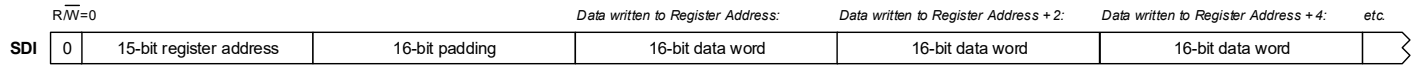


Figure 4-27. Multiple-Register Write to Specified Address

Fig. 4-28 shows a multiple register read from a specified address.

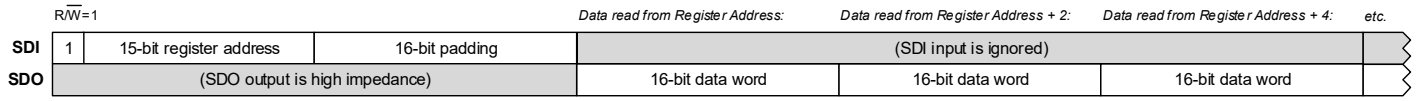


Figure 4-28. Multiple-Register Read from Specified Address

4.8 Interrupts

The CS5312BSE incorporates an interrupt controller for monitoring event conditions. Inputs to the interrupt controller include signal activity detection, clip warning, and virtual PAD warning/error conditions.

Any of these input conditions can be used to assert the IRQ output signal. The IRQ signal can be configured as an output on different pins as described in Table 4-15.

Table 4-15. IRQ Event Logic Output Pins

Pin Name	Power Supply	Control Field	Notes
GPIO1 [1]	VDD_IO2	GPIO1_IRQ_EN	IRQ not supported if GPIO1 is configured for virtual PAD
GPIO2 [1]	VDD_IO2	GPIO2_IRQ_EN	
CONFIG4/CH_IDLE	VDD_IO1	CONFIG4_IRQ_EN	IRQ not supported if pin is configured for signal activity detection.
SPI_SCK	VDD_IO1	SPI_SCK_IRQ_EN	IRQ not supported if SPI control interface is used.

1. The GPIO logic levels are referenced to the VDD_IO2 domain; level shifting may be required if connecting to a host interface operating at a different level (see Table 3-8 for details).

An interrupt register bit, x_INT, is associated with each interrupt input, indicating that the respective event has been detected. The interrupt bits are latching fields which, once set, remain set until a 1 is written to the respective bits. The interrupt register bits can be polled at any time or in response to the IRQ output signal being asserted.

A status bit, x_STS, is provided to indicate the current status of the signal activity detection, clip warning, and virtual PAD inputs.

Mask bits, x_MASK, are provided for each input condition, to enable or disable the respective functions from contributing to the interrupt logic output. The interrupt register bits (x_INT) remain valid—even if masked—but the masked interrupts do not cause the interrupt logic output to be asserted.

The output can be either CMOS driven or open drain; this is selected using IRQ_OP_CFG.

- If the output is configured as CMOS driven, the IRQ output signal is active high, i.e., Logic 1 if one or more unmasked interrupt is asserted.
- If the output is configured as open drain, the IRQ output signal is active low, i.e., Logic 0 if one or more unmasked interrupt is asserted.

The IRQ signal represents the logical OR of the unmasked interrupt registers. The IRQ output remains asserted until all of the associated interrupts have been either masked or reset.

The IRQ status is indicated using IRQ_STS; this bit is set if one or more unmasked interrupt is asserted.

4.9 Device ID

The device ID, and other associated data, can be read from the control fields listed in Table 4-16.

Table 4-16. Device ID

Label	Description
DEVID_0	Lower bytes of the Device ID
DEVID_1	Upper bytes of the Device ID
AREVID	All-layer device revision
MTLREVID	Metal-layer device revision

5 Applications

5.1 Input Buffer Circuit

The analog input channels are supported using external buffer circuits. A typical buffer circuit comprising a high-pass filter and anti-alias filter is shown in Fig. 5-1. The typical buffer circuit shown produces a full-scale (0 dBFS) output from a 1 V_{RMS} single-ended input.

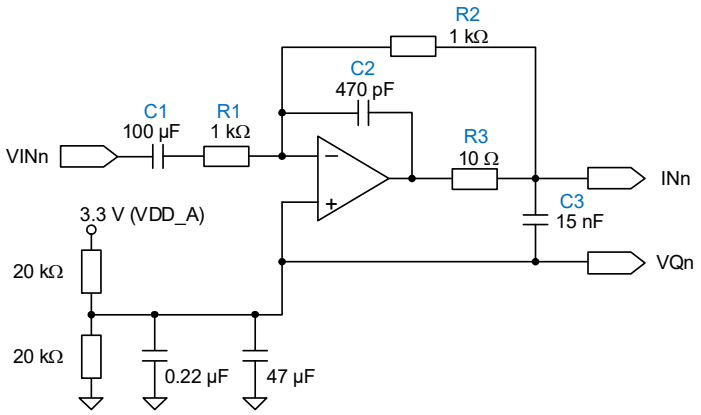


Figure 5-1. Single-Ended Input Buffer

The high-pass filter is provided by the AC-coupling capacitor, C_1 and series resistor, R_1. Using the values shown, the -3 dB cut-off frequency (F_C) can be calculated using the following equation:

$$F_C = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 1000 \times (100 \times 10^{-6})} = 1.59 \text{ Hz}$$

The anti-alias filter is provided by the operational amplifier and associated feedback components. The objective is to provide a flat passband for the audio input bandwidth, and sufficient attenuation at the ADC-modulator sample frequency. The low output impedance of the circuit minimizes the distortion of the signal path.

The typical filter shown provides an approximated –3 dB cut-off frequency of 424 kHz, suitable for the highest CS5312BSE sample rate of 384 kHz. The attenuation slope of –12 dB/octave results in 42 dB attenuation at the ADC-modulator sample frequency of 6.144 MHz.

The –3 dB cut-off frequency is approximated by the following equation:

$$F_C = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 2C_3}} = \frac{1}{2\pi\sqrt{1000 \times 10 \times 470 \times 10^{-12} \times 2 \times 15 \times 10^{-9}}} = 424 \text{ kHz}$$

The gain of the input buffer is set by R_1 and R_2. The gain should be configured to provide a full-scale signal of 1 V_{RMS} at the input to the CS5312BSE. The values shown in Fig. 5-1 provide a ratio of 1; in this configuration, the buffer supports a full-scale input of 1 V_{RMS}.

5.1.1 Unused Input Pins

The recommended input buffer circuit (see Fig. 5-1) provides a single-ended connection to the input pins INn. If one, or more, input channel is not used (disabled), the respective unused input and reference pin INn and VQn should be floating (no connection).

5.1.2 Recommended Components

To achieve the specified performance characteristics, the choice of external components should observe the following recommendations:

- Capacitors should be stable dielectric types, such as C0G (NP0) or electrolytic.
- Resistors should be low value where possible, to minimize thermal noise.
- Low-noise operational amplifiers should be used, such as Texas Instruments OPA1656. The operational amplifiers should meet the minimum performance requirements noted in Table 5-1.

Table 5-1. Op-Amp Specification

Parameter	Specification
Input noise	<5 nV/√Hz
Unity gain bandwidth	>15 MHz
Slew rate	5 V/µs
Total harmonic distortion plus noise (THD+N)	<-128 dB

5.2 Crystal Component Selection

The crystal oscillator (see Section 4.4) uses an external crystal to generate the timing reference. Load capacitors are connected to the crystal as shown in Fig. 5-2. A series resistor (R_S) may also be required to configure the drive level for the selected crystal.

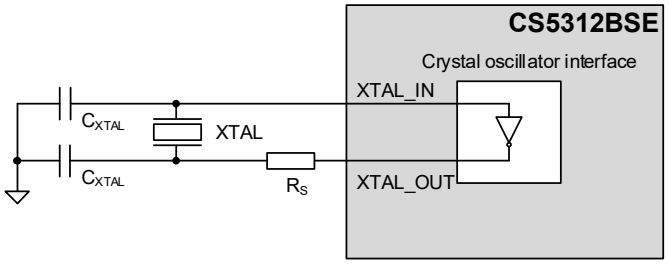


Figure 5-2. Crystal Oscillator Connection

The suitability of the selected crystal is determined by whether the gain margin and drive level are within the valid operating limits of the crystal. The gain margin and drive level can be calculated as a function of the transconductance of the crystal interface.

The transconductance of the crystal interface is dependent on the VDD_IO2 operating voltage as described in Table 3-10.

The recommended sequence for crystal component selection is as follows:

1. **Crystal selection.** The CS5312BSE is compatible with a wide variety of crystal components, including the KC3225Z series of oscillators.
2. **Capacitor selection.** Capacitors should be selected according to the crystal manufacturer's specification for load capacitance (C_L). The recommended value for each C_{XTAL} capacitor is 2 × C_L.
3. **Series resistor.** In the first instance, assume the series resistor Rs is not required (0 Ω).
4. **Gain margin calculation.** The gain margin can be calculated from the transconductance of the crystal interface and the series resistor R_S, together with the crystal characteristics. If the required gain margin is less than 5, a different crystal selection must be made (Step 1).

   The gain margin is calculated as follows: $$\text{Gain Margin} = \frac{\text{Transconductance}}{4 \times (\text{ESR} + R_S) \times (2\pi \times f_{XTAL})^2 \times (C_0 + C_L)^2}$$

   where:

   Transconductance = transconductance of the crystal interface (S)

   ESR = equivalent series resistance (ESR) of the crystal (Ω)

   R_S = series resistance (Ω)

   f_{XTAL} = resonant frequency of the crystal (Hz)

   C_L = load capacitance of the crystal (F)

   C_0 = shunt capacitance of the crystal (F)

5. **Drive level calculation.** The drive level can be calculated using the crystal characteristics and the operating voltage. The operating voltage (peak voltage across the crystal) can be determined using measurement or else by simulation. If the drive level exceeds the maximum level for the crystal, adjust the series resistor R_S to meet the required specification. Increasing R_S results in a lower voltage across the crystal and a decrease in drive level.

   If the series resistor is adjusted, the gain margin must now be recalculated (Step 4). It is recommended to find the minimum series resistance that meets the required gain margin and drive level.

   The drive level (W) is calculated as follows: $\text{Drive Level} = 2 \times \text{ESR} \times (\pi \times f_{XTAL} \times V \times (C_L + C_0))^2$

   where:

   ESR = equivalent series resistance (ESR) of the crystal (Ω)

   f_{XTAL} = resonant frequency of the crystal (Hz)

   V = Peak voltage across the crystal (V)

   C_L = load capacitance of the crystal (F)

   C_0 = shunt capacitance of the crystal (F)

The sequence for crystal component selection is illustrated in Fig. 5-3

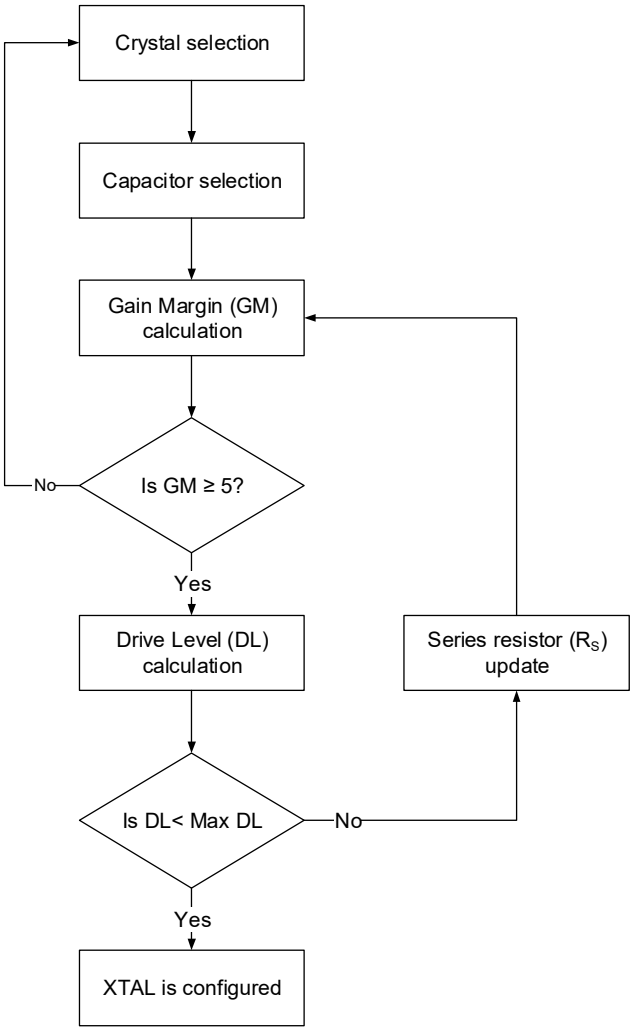


Figure 5-3. Crystal Oscillator Component Selection

6 Register Quick Reference

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

This register view is for the CS5312BSE.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

Table 6-1. Block Base Addresses

Base Address	Block Name	Register Quick Reference	Register Description Reference
0x0000 0000	**DEVID**	Section 6.1	Section 7.1
0x0000 0040	**CONFIG**	Section 6.2	Section 7.2
0x0000 0080	**INPUT_PATH**	Section 6.3	Section 7.3
0x0000 2000	**IN_SIG_CTRL**	Section 6.4	Section 7.4
0x0000 3D00	**PIN_CONFIG**	Section 6.5	Section 7.5
0x0000 3E00	**IRQ_CONFIG**	Section 6.6	Section 7.6

6.1 DEVID

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0000	DEVID_0	DEVID_0															
p. 46		0	0	1	1	0	0	0	1	0	0	1	0	0	0	0	1
0x0000 0002	DEVID_1	DEVID_1															
p. 46		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
0x0000 0004	REVID	—								AREVID				MTLREVID			
p. 46		0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
0x0000 0022	SW_RESET	SW_RESET								—							
p. 47		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.2 CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0040	CLK_CFG		—		SYSCLK_SRC						—						
p. 47		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0042	SAMPLE_RATE							—							SAMPLE_RATE		
p. 47		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x0000 0044	CHIP_ENABLE								—								GLOBAL_EN
p. 47		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0048	ASP_CFG					—					ASP_BCLK_INV	ASP_PRIMARY		—		ASP_BCLK_FREQ	
p. 48		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0050	SIGNAL_PATH_CFG					—					ASP_FSYNC_TYPE	ASP_TDM_SLOT			ASP_FORMAT		
p. 48		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.3 INPUT_PATH

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0080	IN_ENABLES	—														IN2_ADC_EN	IN1_ADC_EN
p. 48		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0082	IN_RAMP_SUM	—				IN_CLIP_THRESH				—	IN_RAMP_RATE_DEC			—	IN_RAMP_RATE_INC		
p. 49		0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
0x0000 008A	IN_INV	—														IN2_INV	IN1_INV
p. 49		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0090	IN1_VOL_CTRL	IN1_MUTE	—						IN1_VOL								
p. 49		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0092	IN2_VOL_CTRL	IN2_MUTE	—						IN2_VOL								
p. 50		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00A0	IN_VOL_UPDATE	—															IN_VU
p. 50		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.4 IN_SIG_CTRL

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 200C	IO_CTRL	—					DB_TIME			—		SW_TYPE	—				
p. 50		0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0
0x0000 2010	GPIO_STS	—				GPO_STS				—				GPI_STS			
p. 51		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2110	IN_SIG_ACT_CTRL	—			IN_SIG_ACT_LD_TIME					—							
p. 51		0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
0x0000 2140	IN_PAD_CFG	—						IN2_PAD_LD_EN	IN1_PAD_LD_EN	—						IN2_PAD_AUTO_EN	IN1_PAD_AUTO_EN
p. 51		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2142	IN_PAD_SIGNAL	IN_PAD_LD_AVG	—										IN_PAD_LD_TIME				
p. 51		0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
0x0000 2146	IN1_PAD_THR	—				IN1_PAD_LOW_THR				—			IN1_PAD_HIGH_THR				
p. 52		0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	0
0x0000 214A	IN2_PAD_THR	—				IN2_PAD_LOW_THR				—			IN2_PAD_HIGH_THR				
p. 52		0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	0
0x0000 2170	IN_SIG_ACT_EN	—														IN_SIG_ACT_HIGH_EN	IN_SIG_ACT_LOW_EN
p. 52		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2176	IN1_SIG_ACT_THR	—				IN1_SIG_ACT_HIGH_THR				—				IN1_SIG_ACT_LOW_THR			
p. 53		0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	1
0x0000 217A	IN2_SIG_ACT_THR	—				IN2_SIG_ACT_HIGH_THR				—				IN2_SIG_ACT_LOW_THR			
p. 53		0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	1
0x0000 2202	IN1_CFG_GPIO	—			IN1_GPI_POL	—	IN1_GPI_SEL			—				IN1_GPO4_SEL	IN1_GPO3_SEL	IN1_GPO2_SEL	IN1_GPO1_SEL
p. 53		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2206	IN2_CFG_GPIO	—			IN2_GPI_POL	—	IN2_GPI_SEL			—				IN2_GPO4_SEL	IN2_GPO3_SEL	IN2_GPO2_SEL	IN2_GPO1_SEL
p. 54		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2226	IN1_INT_GAIN	IN1_UPDATE	—	IN1_INT_ANA_GAIN		—			IN1_INT_DIG_GAIN								
p. 54		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 222E	IN2_INT_GAIN	IN2_UPDATE	—	IN2_INT_ANA_GAIN		—			IN2_INT_DIG_GAIN								
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2262	IN1_LOW_GPO	IN1_LOW_GPO4	IN1_LOW_GPO3	IN1_LOW_GPO2	IN1_LOW_GPO1	—											
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2266	IN1_LOW_INT_GAIN	IN1_LOW_UPDATE	—	IN1_LOW_INT_ANA_GAIN		—			IN1_LOW_INT_DIG_GAIN								
p. 55		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 226A	IN2_LOW_GPO	IN2_LOW_GPO4	IN2_LOW_GPO3	IN2_LOW_GPO2	IN2_LOW_GPO1	—											
p. 56		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 226E	IN2_LOW_INT_GAIN	IN2_LOW_UPDATE	—	IN2_LOW_INT_ANA_GAIN		—			IN2_LOW_INT_DIG_GAIN								
p. 56		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 22C2	IN1_HIGH_GPO	IN1_HIGH_GPO4	IN1_HIGH_GPO3	IN1_HIGH_GPO2	IN1_HIGH_GPO1	—											
p. 57		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 22C6	IN1_HIGH_INT_GAIN	IN1_HIGH_UPDATE	—	IN1_HIGH_INT_ANA_GAIN		—			IN1_HIGH_INT_DIG_GAIN								
p. 57		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 22CA	IN2_HIGH_GPO	IN2_HIGH_GPO4	IN2_HIGH_GPO3	IN2_HIGH_GPO2	IN2_HIGH_GPO1	—											
p. 57		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 22CE	IN2_HIGH_INT_GAIN	IN2_HIGH_UPDATE	—	IN2_HIGH_INT_ANA_GAIN		—			IN2_HIGH_INT_DIG_GAIN								
p. 58		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.5 PIN_CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 3D1C	PAD_IRQ_CFG	IRQ_OP_CFG	—						GPIO1_IRQ_EN	GPIO2_IRQ_EN	—		CONFIG4_IRQ_EN	SPI_SCK_IRQ_EN	—		
p. 58		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.6 IRQ_CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 3E04	IRQ_STS	—															IRQ_STS
p. 59		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 3E1C	IRQ_ADC_EVENT_INT	IN2_SIG_ACT_LOW_INT	IN1_SIG_ACT_LOW_INT	IN2_SIG_ACT_HIGH_INT	IN1_SIG_ACT_HIGH_INT	IN2_PAD_LOW_INT	IN1_PAD_LOW_INT	IN2_PAD_HIGH_INT	IN1_PAD_HIGH_INT	GAIN_CONFLICT_INT	—				IN2_CLIP_WARN_INT	IN1_CLIP_WARN_INT	—
p. 59		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 3E2C	IRQ_ADC_EVENT_MASK	IN2_SIG_ACT_LOW_MASK	IN1_SIG_ACT_LOW_MASK	IN2_SIG_ACT_HIGH_MASK	IN1_SIG_ACT_HIGH_MASK	IN2_PAD_LOW_MASK	IN1_PAD_LOW_MASK	IN2_PAD_HIGH_MASK	IN1_PAD_HIGH_MASK	GAIN_CONFLICT_MASK	—				IN2_CLIP_WARN_MASK	IN1_CLIP_WARN_MASK	—
p. 60		1	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0
0x0000 3E5C	IRQ_ADC_EVENT_STS	IN2_SIG_ACT_LOW_STS	IN1_SIG_ACT_LOW_STS	IN2_SIG_ACT_HIGH_STS	IN1_SIG_ACT_HIGH_STS	IN2_PAD_LOW_STS	IN1_PAD_LOW_STS	IN2_PAD_HIGH_STS	IN1_PAD_HIGH_STS			—			IN2_CLIP_WARN_STS	IN1_CLIP_WARN_STS	—
p. 60		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7 Register Descriptions

This section describes each of the control port registers.

This register view is for the CS5312BSE.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

7.1 DEVID

7.1.1 DEVID_0

Address: 0x0000 0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	DEVID_0															
Default	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0	1

Bits	Name	Description
15:0	DEVID_0	This register indicates the lower bytes of Device ID CS5312BSE 0x0000–0x3120 = Reserved 0x3122–0xFFFF = Reserved 0x3121 = (Default) CS5312BSE

7.1.2 DEVID_1

Address: 0x0000 0002

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	DEVID_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Name	Description
15:0	DEVID_1	This register indicates the upper bytes of Device ID CS5312BSE 0x0000–0x0004 = Reserved 0x0006–0xFFFF = Reserved 0x0005 = (Default) CS5312BSE

7.1.3 REVID

Address: 0x0000 0004

	15…8	7	6	5	4	3	2	1	0
RO	—	AREVID				MTLREVID			
Default	0x00	1	0	1	0	0	0	0	0

Bits	Name	Description
15:8	—	Reserved
7:4	AREVID	This field indicates the all-layer device revision. 0x0–0x9 = Reserved 0xB–0xF = Reserved 0xA = (Default) Revision Ax
3:0	MTLREVID	This field indicates the metal-layer device revision. 0x0 = (Default) Revision x0 0x1–0xF = Reserved

7.1.4 SW_RESET

Address: 0x0000 0022

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO	SW_RESET								—							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	SW_RESET	Software Reset. Writing 0x5A triggers a reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved
7:0	—	Reserved

7.2 CONFIG

7.2.1 CLK_CFG

Address: 0x0000 0040

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—			SYSCLK_SRC	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12	SYSCLK_SRC	System clock source. If XTAL is selected, the MCLK is the output clock. 0 = (Default) MCLK input 1 = XTAL input
11:0	—	Reserved

7.2.2 SAMPLE_RATE

Address: 0x0000 0042

	15…8	7	6	5	4	3	2	1	0
RW	—	—						SAMPLE_RATE	
Default	0x00	0	0	0	0	0	0	0	1

Bits	Name	Description
15:3	—	Reserved
2:0	SAMPLE_RATE	Audio sample frequency. Note the sample rate must be integer-related to the system clock frequency. Auto-detect is only valid if sample rate = 16-192 kHz, and the ASP is in Secondary Mode. 000 = 32 kHz 001 = (Default) 48/44.1 kHz 010 = 96/88.2 kHz 011 = 192/176.4 kHz 100 = 384/356.8 kHz 101 = Reserved 110 = Auto-detect 111 = 16 kHz

7.2.3 CHIP_ENABLE

Address: 0x0000 0044

	15…8	7	6	5	4	3	2	1	0
RW	—	—							GLOBAL_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	GLOBAL_EN	Global enable. Set to 1 to configure and enable all functions. Clear to 0 to disable. Note the clocking and ASP control registers are only valid on the rising edge of GLOBAL_EN. It is recommended to select the disabled state (GLOBAL_EN=0) before writing to these registers.

7.2.4 ASP_CFG

Address: 0x0000 0048

RW	15…8	7	6	5	4	3	2	1	0
	—	—	ASP_BCLK_INV	ASP_PRIMARY	—			ASP_BCLK_FREQ	
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6	ASP_BCLK_INV	ASP BCLK polarity. Selects the valid BCLK edge for data sampling. In non-inverted mode, DOUT data is driven on BCLK falling edge (TDM half-cycle mode) or rising edge (TDM full-cycle mode). In inverted mode, DOUT data is driven on BCLK rising edge (TDM half-cycle mode) or falling edge (TDM full-cycle mode). 0 = (Default) Non-inverted 1 = Inverted
5	ASP_PRIMARY	ASP Primary/Secondary Mode select. In ASP Primary Mode, BCLK and FSYNC are outputs. In ASP Secondary Mode, BCLK and FSYNC are inputs. 0 = (Default) Secondary Mode 1 = Primary Mode
4:2	—	Reserved
1:0	ASP_BCLK_FREQ	ASP BCLK frequency. The BCLK frequency must be high enough to support the required number of data bits at the selected sample rate. Only valid in ASP Primary Mode. Note the BCLK frequency is integer-related to the system clock frequency i.e., multiples of 3.072 MHz for 24.576 MHz system clock, or multiples of 2.8224 MHz for 22.5792 MHz system clock. 00 = (Default) 3.072/2.8224 MHz 01 = 6.144/5.6448 MHz 10 = 12.288/11.2896 MHz 11 = 24.576/22.5792 MHz

7.2.5 SIGNAL_PATH_CFG

Address: 0x0000 0050

RW	15…8	7	6	5	4	3	2	1	0
	—	—	ASP_FSYNC_TYPE	ASP_TDM_SLOT				ASP_FORMAT	
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6	ASP_FSYNC_TYPE	Configure ASP_FSYNC as pulse or square wave (50% duty cycle) in TDM mode. Only applicable when ASP is in Primary Mode. 0 = (Default) FSYNC Pulse 1 = FSYNC Square Wave
5:3	ASP_TDM_SLOT	TDM slot select. Configures which TDM slots are used in TDM maximum-time-slots mode. 000 = (Default) Slots 0-1 001 = Slots 2-3 010 = Slots 4-5 011 = Slots 6-7 100 = Slots 8-9 101 = Slots 10-11 110 = Slots 12-13 111 = Slots 14-15
2:0	ASP_FORMAT	ASP data format. Selects how the audio samples are arranged within the FSYNC frame. 000 = (Default) I2S Mode 001 = Left-Justified Mode 010–100 = Reserved 101 = TDM Mode maximum time slots, full cycle 110 = TDM Mode maximum time slots, half cycle 111 = TDM Mode minimum time slots

7.3 INPUT_PATH

7.3.1 IN_ENABLES

Address: 0x0000 0080

RW	15…8	7	6	5	4	3	2	1	0
	—	—						IN2_ADC_EN	IN1_ADC_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved

Bits	Name	Description
1	IN2_ADC_EN	Channel 2 input enable. Note that Channels 1-2 should always be enabled/disabled as a pair. 0 = (Default) Disabled 1 = Enabled
0	IN1_ADC_EN	Channel 1 input enable. Note that Channels 1-2 should always be enabled/disabled as a pair. 0 = (Default) Disabled 1 = Enabled

7.3.2 IN_RAMP_SUM

Address: 0x0000 0082

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				IN_CLIP_THRESH				—	IN_RAMP_RATE_DEC			—	IN_RAMP_RATE_INC		
Default	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Bits	Name	Description
15:12	—	Reserved
11:8	IN_CLIP_THRESH	Input clip-warning threshold. 0x0 = (Default) 0.0 dBFS 0x1 = –0.125 dBFS 0x2 = –0.25 dBFS 0x3 = –0.5 dBFS 0x4 = –1.0 dBFS 0x5 = –3.0 dBFS 0x6 = –6.0 dBFS 0x7–0xF = Reserved
7	—	Reserved
6:4	IN_RAMP_RATE_DEC	ADC input volume Decrease Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms
3	—	Reserved
2:0	IN_RAMP_RATE_INC	ADC input volume Increase Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms

7.3.3 IN_INV

Address: 0x0000 008A

RW	15…8	7	6	5	4	3	2	1	0
	—	—						IN2_INV	IN1_INV
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved
1	IN2_INV	Channel 2 ADC invert. 0 = (Default) No inversion 1 = ADC data invert
0	IN1_INV	Channel 1 ADC invert. 0 = (Default) No inversion 1 = ADC data invert

7.3.4 IN1_VOL_CTRL

Address: 0x0000 0090

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN1_MUTE	—							IN1_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN1_MUTE	Channel 1 input mute. 0 = Unmute 1 = (Default) Mute

Bits	Name	Description
14:9	—	Reserved
8:0	IN1_VOL	Channel 1 input digital volume, –127.5 dB to +30 dB in 0.5 dB steps. 0x000 = (Default) 0.0 dB 0x001 = –0.5 dB … 0x0FF = –127.5 dB 0x100 = Reserved 0x101 = 0.5 dB 0x102 = 1.0 dB … 0x13C = 30.0 dB 0x13D–0x1FF = Reserved

7.3.5 IN2_VOL_CTRL

Address: 0x0000 0092

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_MUTE	—							IN2_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_MUTE	Channel 2 input mute. 0 = Unmute 1 = (Default) Mute
14:9	—	Reserved
8:0	IN2_VOL	Channel 2 input digital volume, –127.5 dB to +30 dB in 0.5 dB steps. 0x000 = (Default) 0.0 dB 0x001 = –0.5 dB … 0x0FF = –127.5 dB 0x100 = Reserved 0x101 = 0.5 dB 0x102 = 1.0 dB … 0x13C = 30.0 dB 0x13D–0x1FF = Reserved

7.3.6 IN_VOL_UPDATE

Address: 0x0000 00A0

WO	15…8	7	6	5	4	3	2	1	0
	—	—							IN_VU
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	IN_VU	Global ADC input volume update trigger. 0 = (Default) No action 1 = Write 1 to trigger an update of all input volume/mute registers

7.4 IN_SIG_CTRL

7.4.1 IO_CTRL

Address: 0x0000 200C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				DB_TIME				—		SW_TYPE		—			
Default	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0

Bits	Name	Description
15:11	—	Reserved
10:8	DB_TIME	GPI debounce time, base 32 kHz. 000 = 124 us 001 = 2 ms 010 = 4 ms 011 = (Default) 8 ms 100 = 16 ms 101 = 32 ms 110 = 64 ms 111 = 128 ms
7:6	—	Reserved
5	SW_TYPE	GPI type selection. Select toggle switch for rising-edge detection or latching switch for level detection. 0 = Toggle switch 1 = (Default) Latching switch
4:0	—	Reserved

7.4.2 GPIO_STS

Address: 0x0000 2010

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	—				GPO_STS				—				GPI_STS			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:12	—	Reserved
11:8	GPO_STS	GPO read back status.
7:4	—	Reserved
3:0	GPI_STS	GPI read back status.

7.4.3 IN_SIG_ACT_CTRL

Address: 0x0000 2110

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—			IN_SIG_ACT_LD_TIME					—							
Default	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12:8	IN_SIG_ACT_LD_TIME	Signal activity detection level-detect time constant. The time constant is defined in audio sample (1/fs) units. 0x00–0x09 = Reserved 0x0A = 1024 samples 0x0B = 2048 samples 0x0C = (Default) 4096 samples 0x0D = 8192 samples 0x0E = 16384 samples 0x0F = 32768 samples 0x10 = 65536 samples 0x11–0x1F = Reserved
7:0	—	Reserved

7.4.4 IN_PAD_CFG

Address: 0x0000 2140

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—						IN2_PAD_LD_EN	IN1_PAD_LD_EN	—						IN2_PAD_AUTO_EN	IN1_PAD_AUTO_EN
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:10	—	Reserved
9	IN2_PAD_LD_EN	PAD level detector (LD) enable for Channel 2. 0 = (Default) Disabled 1 = Enabled
8	IN1_PAD_LD_EN	PAD level detector (LD) enable for Channel 1. 0 = (Default) Disabled 1 = Enabled
7:2	—	Reserved
1	IN2_PAD_AUTO_EN	Channel 2 PAD automatic response enable. 0 = (Default) Disabled 1 = Enabled
0	IN1_PAD_AUTO_EN	Channel 1 PAD automatic response enable. 0 = (Default) Disabled 1 = Enabled

7.4.5 IN_PAD_SIGNAL

Address: 0x0000 2142

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	IN_PAD_LD_AVG	—											IN_PAD_LD_TIME			
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Name	Description
15	IN_PAD_LD_AVG	Selects averaged or instantaneous input signal for PAD high-level threshold level detection (LD). 0 = (Default) Averaged signal 1 = Instantaneous signal

Bits	Name	Description
14:5	—	Reserved
4:0	IN_PAD_LD_TIME	PAD level-detect time constant. The time constant is defined in audio sample (1/fs) units. 0x00–0x09 = Reserved 0x0A = 1024 samples 0x0B = 2048 samples 0x0C = (Default) 4096 samples 0x0D = 8192 samples 0x0E = 16384 samples 0x0F = 32768 samples 0x10 = 65536 samples 0x11–0x1F = Reserved

7.4.6 IN1_PAD_THR

Address: 0x0000 2146

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				IN1_PAD_LOW_THR				—				IN1_PAD_HIGH_THR			
Default	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	0

Bits	Name	Description
15:12	—	Reserved
11:8	IN1_PAD_LOW_THR	Channel 1 PAD level detector (LD) low-level threshold. 0x0–0x2 = Reserved 0x3 = –38.0 dBFS … 0x9 = –74.0 dBFS 0xA = (Default) –80.0 dBFS 0xB–0xE = Reserved 0xF = mute
7:5	—	Reserved
4:0	IN1_PAD_HIGH_THR	Channel 1 PAD level detector (LD) high-level threshold. 0x00 = –1 dBFS 0x01 = –2 dBFS … 0x06 = (Default) –7 dBFS … 0x1E = –31 dBFS 0x1F = –32 dBFS

7.4.7 IN2_PAD_THR

Address: 0x0000 214A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				IN2_PAD_LOW_THR				—				IN2_PAD_HIGH_THR			
Default	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	0

Bits	Name	Description
15:12	—	Reserved
11:8	IN2_PAD_LOW_THR	Channel 2 PAD level detector (LD) low-level threshold. 0x0–0x2 = Reserved 0x3 = –38 dBFS … 0x9 = –74 dBFS 0xA = (Default) –80 dBFS 0xB–0xE = Reserved 0xF = mute
7:5	—	Reserved
4:0	IN2_PAD_HIGH_THR	Channel 2 PAD level detector (LD) high-level threshold. 0x00 = –1 dBFS 0x01 = –2 dBFS … 0x06 = (Default) –7 dBFS … 0x1E = –31 dBFS 0x1F = –32 dBFS

7.4.8 IN_SIG_ACT_EN

Address: 0x0000 2170

RW	15…8	7	6	5	4	3	2	1	0
	—	—						IN_SIG_ACT_HIGH_EN	IN_SIG_ACT_LOW_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved
1	IN_SIG_ACT_HIGH_EN	Signal-activity detection, active-detection enable. 0 = (Default) Disabled 1 = Enabled
0	IN_SIG_ACT_LOW_EN	Signal-activity detection, idle-detection enable. 0 = (Default) Disabled 1 = Enabled

7.4.9 IN1_SIG_ACT_THR

Address: 0x0000 2176

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				IN1_SIG_ACT_HIGH_THR				—				IN1_SIG_ACT_LOW_THR			
Default	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	1

Bits	Name	Description
15:12	—	Reserved
11:8	IN1_SIG_ACT_HIGH_THR	Channel 1 signal-activity detection, high-level threshold. 0x0–0x2 = Reserved 0x3 = –38 dBFS … 0xA = (Default) –80 dBFS 0xB–0xE = Reserved 0xF = mute
7:4	—	Reserved
3:0	IN1_SIG_ACT_LOW_THR	Channel 1 signal-activity detection, low-level threshold. 0x0–0x2 = Reserved 0x3 = –80 dBFS … 0x7 = (Default) –104 dBFS 0x8–0xE = Reserved 0xF = mute

7.4.10 IN2_SIG_ACT_THR

Address: 0x0000 217A

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				IN2_SIG_ACT_HIGH_THR				—				IN2_SIG_ACT_LOW_THR			
Default	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	1

Bits	Name	Description
15:12	—	Reserved
11:8	IN2_SIG_ACT_HIGH_THR	Channel 2 signal-activity detection high-level threshold. 0x0–0x2 = Reserved 0x3 = –38 dBFS … 0xA = (Default) –80 dBFS 0xB–0xE = Reserved 0xF = mute
7:4	—	Reserved
3:0	IN2_SIG_ACT_LOW_THR	Channel 2 signal-activity detection low-level threshold. 0x0–0x2 = Reserved 0x3 = –80 dBFS … 0x7 = (Default) –104 dBFS 0x8–0xE = Reserved 0xF = mute

7.4.11 IN1_CFG_GPIO

Address: 0x0000 2202

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			IN1_GPI_POL	—	IN1_GPI_SEL			—				IN1_GPO4_SEL	IN1_GPO3_SEL	IN1_GPO2_SEL	IN1_GPO1_SEL
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12	IN1_GPI_POL	GPI polarity for Input Channel 1. 0 = (Default) GPI not inverted 1 = GPI inverted
11	—	Reserved
10:8	IN1_GPI_SEL	Select GPIO pin as GPI for Input Channel 1. 000 = (Default) Select GPI disabled 001 = Select GPIO1 010 = Select GPIO2 011 = Select GPIO3 100 = Select GPIO4 101–111 = Reserved
7:4	—	Reserved
3	IN1_GPO4_SEL	Input Channel 1 GPO4 configuration. 0 = (Default) Disabled 1 = Enabled
2	IN1_GPO3_SEL	Input Channel 1 GPO3 configuration. 0 = (Default) Disabled 1 = Enabled

Bits	Name	Description
1	IN1_GPO2_SEL	Input Channel 1 GPO2 configuration. 0 = (Default) Disabled 1 = Enabled
0	IN1_GPO1_SEL	Input Channel 1 GPO1 configuration. 0 = (Default) Disabled 1 = Enabled

7.4.12 IN2_CFG_GPIO

Address: 0x0000 2206

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			IN2_GPI_POL	—	IN2_GPI_SEL			—				IN2_GPO4_SEL	IN2_GPO3_SEL	IN2_GPO2_SEL	IN2_GPO1_SEL
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12	IN2_GPI_POL	GPI polarity for Input Channel 2. 0 = (Default) GPI not inverted 1 = GPI inverted
11	—	Reserved
10:8	IN2_GPI_SEL	Select GPIO pin as GPI for Input Channel 2. 000 = (Default) Select GPI disabled 001 = Select GPIO1 010 = Select GPIO2 011 = Select GPIO3 100 = Select GPIO4 101–111 = Reserved
7:4	—	Reserved
3	IN2_GPO4_SEL	Input Channel 2 GPO4 configuration 0 = (Default) Disabled 1 = Enabled
2	IN2_GPO3_SEL	Input Channel 2 GPO3 configuration 0 = (Default) Disabled 1 = Enabled
1	IN2_GPO2_SEL	Input Channel 2 GPO2 configuration. 0 = (Default) Disabled 1 = Enabled
0	IN2_GPO1_SEL	Input Channel 2 GPO1 configuration. 0 = (Default) Disabled 1 = Enabled

7.4.13 IN1_INT_GAIN

Address: 0x0000 2226

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN1_UPDATE	—	IN1_INT_ANA_GAIN		—				IN1_INT_DIG_GAIN							
Access	WO	—	RW		—				RW							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN1_UPDATE	Channel 1 gain update. Write 1 to apply the Channel 1 gain selection. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14	—	Reserved
13:12	IN1_INT_ANA_GAIN	Channel 1 internal analog gain. 00 = (Default) 0 dB 01 = 6 dB 10 = Reserved 11 = 12 dB
11:9	—	Reserved
8:0	IN1_INT_DIG_GAIN	Channel 1 digital gain. Note the signal level is also controlled by the digital volume. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB … 0x0FF = 31.875 dB 0x100 = –32.000 dB … 0x1FF = –0.125 dB

7.4.14 IN2_INT_GAIN

Address: 0x0000 222E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_UPDATE	—	IN2_INT_ANA_GAIN		—				IN2_INT_DIG_GAIN							
Access	WO	—	RW		—				RW							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_UPDATE	Input Channel 2 gain update. Write 1 to apply the Channel 2 gain selection. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14	—	Reserved
13:12	IN2_INT_ANA_GAIN	Input Channel 2 internal analog gain. 00 = (Default) 0 dB 01 = 6 dB 10 = Reserved 11 = 12 dB
11:9	—	Reserved
8:0	IN2_INT_DIG_GAIN	Input Channel 2 digital gain. Note that the signal level is also controlled by the digital volume. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB … 0x0FF = 31.875 dB 0x100 = –32.000 dB … 0x1FF = –0.125 dB

7.4.15 IN1_LOW_GPO

Address: 0x0000 2262

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN1_LOW_GPO4	IN1_LOW_GPO3	IN1_LOW_GPO2	IN1_LOW_GPO1	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN1_LOW_GPO4	Channel 1 low gain GPO4 logic output. 0 = (Default) GPO4 logic low 1 = GPO4 logic high
14	IN1_LOW_GPO3	Channel 1 low gain GPO3 logic output. 0 = (Default) GPO3 logic low 1 = GPO3 logic high
13	IN1_LOW_GPO2	Channel 1 low gain GPO2 logic output. 0 = (Default) GPO2 logic low 1 = GPO2 logic high
12	IN1_LOW_GPO1	Channel 1 low gain GPO1 logic output. 0 = (Default) GPO1 logic low 1 = GPO1 logic high
11:0	—	Reserved

7.4.16 IN1_LOW_INT_GAIN

Address: 0x0000 2266

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN1_LOW_UPDATE	—	IN1_LOW_INT_ANA_GAIN		—				IN1_LOW_INT_DIG_GAIN							
Access	WO	—	RW		—				RW							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN1_LOW_UPDATE	Input Channel 1 gain update. Write 1 to apply the Channel 1 gain selection. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14	—	Reserved
13:12	IN1_LOW_INT_ANA_GAIN	Input Channel 1 internal analog gain. 00 = (Default) 0 dB 01 = 6 dB 10 = Reserved 11 = 12 dB

Bits	Name	Description
11:9	—	Reserved
8:0	IN1_LOW_INT_DIG_GAIN	Input Channel 1 digital gain. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB … 0x0FF = 31.875 dB 0x100 = –32.000 dB … 0x1FF = –0.125 dB

7.4.17 IN2_LOW_GPO

Address: 0x0000 226A

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	IN2_LOW_GPO4	IN2_LOW_GPO3	IN2_LOW_GPO2	IN2_LOW_GPO1	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_LOW_GPO4	Channel 2 low gain GPO4 logic output 0 = (Default) GPO4 logic low 1 = GPO4 logic high
14	IN2_LOW_GPO3	Channel 2 low gain GPO3 logic output 0 = (Default) GPO3 logic low 1 = GPO3 logic high
13	IN2_LOW_GPO2	Channel 2 low gain GPO2 logic output 0 = (Default) GPO2 logic low 1 = GPO2 logic high
12	IN2_LOW_GPO1	Channel 2 low gain GPO1 logic output 0 = (Default) GPO1 logic low 1 = GPO1 logic high
11:0	—	Reserved

7.4.18 IN2_LOW_INT_GAIN

Address: 0x0000 226E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_LOW_UPDATE	—	IN2_LOW_INT_ANA_GAIN		—			IN2_LOW_INT_DIG_GAIN								
Access	WO	—	RW		—			RW								
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_LOW_UPDATE	Input Channel 2 gain update. Write 1 to apply Channel 2 gain selection. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14	—	Reserved
13:12	IN2_LOW_INT_ANA_GAIN	Input Channel 2 internal analog gain. 00 = (Default) 0 dB 01 = 6 dB 10 = Reserved 11 = 12 dB
11:9	—	Reserved
8:0	IN2_LOW_INT_DIG_GAIN	Input Channel 2 digital gain. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB … 0x0FF = 31.875 dB 0x100 = –32.000 dB … 0x1FF = –0.125 dB

7.4.19 IN1_HIGH_GPO

Address: 0x0000 22C2

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN1_HIGH_GPO4	IN1_HIGH_GPO3	IN1_HIGH_GPO2	IN1_HIGH_GPO1	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN1_HIGH_GPO4	Channel 1 high gain GPO4 logic output. 0 = (Default) GPO4 logic low 1 = GPO4 logic high
14	IN1_HIGH_GPO3	Channel 1 high gain GPO3 logic output. 0 = (Default) GPO3 logic low 1 = GPO3 logic high
13	IN1_HIGH_GPO2	Channel 1 high gain GPO2 logic output. 0 = (Default) GPO2 logic low 1 = GPO2 logic high
12	IN1_HIGH_GPO1	Channel 1 high gain GPO1 logic output. 0 = (Default) GPO1 logic low 1 = GPO1 logic high
11:0	—	Reserved

7.4.20 IN1_HIGH_INT_GAIN

Address: 0x0000 22C6

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN1_HIGH_UPDATE	—	IN1_HIGH_INT_ANA_GAIN		—				IN1_HIGH_INT_DIG_GAIN							
Access	WO	—	RW		—				RW							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN1_HIGH_UPDATE	Input Channel 1 gain update. Write 1 to apply the Channel 1 gain selection. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14	—	Reserved
13:12	IN1_HIGH_INT_ANA_GAIN	Input Channel 1 internal analog gain. 00 = (Default) 0 dB 01 = 6 dB 10 = Reserved 11 = 12 dB
11:9	—	Reserved
8:0	IN1_HIGH_INT_DIG_GAIN	Input Channel 1 digital gain. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB … 0x0FF = 31.875 dB 0x100 = –32.000 dB … 0x1FF = –0.125 dB

7.4.21 IN2_HIGH_GPO

Address: 0x0000 22CA

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_HIGH_GPO4	IN2_HIGH_GPO3	IN2_HIGH_GPO2	IN2_HIGH_GPO1	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_HIGH_GPO4	Channel 2 high gain GPO4 logic output. 0 = (Default) GPO4 logic low 1 = GPO4 logic high
14	IN2_HIGH_GPO3	Channel 2 high gain GPO3 logic output. 0 = (Default) GPO3 logic low 1 = GPO3 logic high
13	IN2_HIGH_GPO2	Channel 2 high gain GPO2 logic output. 0 = (Default) GPO2 logic low 1 = GPO2 logic high

Bits	Name	Description
12	IN2_HIGH_GPO1	Channel 2 high gain GPO1 logic output. 0 = (Default) GPO1 logic low 1 = GPO1 logic high
11:0	—	Reserved

7.4.22 IN2_HIGH_INT_GAIN

Address: 0x0000 22CE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_HIGH_UPDATE	—	IN2_HIGH_INT_ANA_GAIN		—				IN2_HIGH_INT_DIG_GAIN							
Access	WO	—	RW		—				RW							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_HIGH_UPDATE	Input Channel 2 gain update. Write 1 to apply the Channel 2 gain selection. The gain update is applied at the next scheduling opportunity, zero-cross aligned.
14	—	Reserved
13:12	IN2_HIGH_INT_ANA_GAIN	Input Channel 2 internal analog gain. 00 = (Default) 0 dB 01 = 6 dB 10 = Reserved 11 = 12 dB
11:9	—	Reserved
8:0	IN2_HIGH_INT_DIG_GAIN	Input Channel 2 digital gain. 0x000 = (Default) 0.000 dB 0x001 = 0.125 dB … 0x0FF = 31.875 dB 0x100 = –32.000 dB … 0x1FF = –0.125 dB

7.5 PIN_CONFIG

7.5.1 PAD_IRQ_CFG

Address: 0x0000 3D1C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ_OP_CFG	—						GPIO1_IRQ_EN	GPIO2_IRQ_EN	—		CONFIG4_IRQ_EN	SPI_SCK_IRQ_EN	—		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IRQ_OP_CFG	IRQ output configuration 0 = (Default) CMOS 1 = Open drain
14:9	—	Reserved
8	GPIO1_IRQ_EN	IRQ output to GPIO1 0 = (Default) GPIO1 1 = IRQ output
7	GPIO2_IRQ_EN	IRQ output to GPIO2 0 = (Default) GPIO2 1 = IRQ output
6:5	—	Reserved
4	CONFIG4_IRQ_EN	CONFIG4 pin function select 0 = (Default) HW config/CH_IDLE 1 = IRQ output
3	SPI_SCK_IRQ_EN	IRQ output to SPI_SCK 0 = (Default) SPI_SCK 1 = IRQ output
2:0	—	Reserved

7.6 IRQ_CONFIG

7.6.1 IRQ_STS

Address: 0x0000 3E04

	15…8	7	6	5	4	3	2	1	0
RO	—	—							IRQ_STS
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	IRQ_STS	IRQ status. Logical OR of all unmasked x_INT interrupts. 0 = (Default) Not asserted 1 = Asserted

7.6.2 IRQ_ADC_EVENT_INT

Address: 0x0000 3E1C

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	IN2_SIG_ACT_LOW_INT	IN1_SIG_ACT_LOW_INT	IN2_SIG_ACT_HIGH_INT	IN1_SIG_ACT_HIGH_INT	IN2_PAD_LOW_INT	IN1_PAD_LOW_INT	IN2_PAD_HIGH_INT	IN1_PAD_HIGH_INT	GAIN_CONFLICT_INT	—				IN2_CLIP_WARN_INT	IN1_CLIP_WARN_INT	—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_SIG_ACT_LOW_INT	ADC Channel 2 signal-activity detection, input signal exceeds low-level threshold interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Exceed LOW Th
14	IN1_SIG_ACT_LOW_INT	ADC Channel 1 signal-activity detection, input signal exceeds low-level threshold interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Exceed LOW Th
13	IN2_SIG_ACT_HIGH_INT	ADC Channel 2 signal-activity detection, input signal exceeds high-level threshold interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Exceed High Th
12	IN1_SIG_ACT_HIGH_INT	ADC Channel 1 signal-activity detection, input signal exceeds high-level threshold interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Exceed High Th
11	IN2_PAD_LOW_INT	ADC Channel 2 PAD LD, input signal exceeds low-level threshold interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Exceeds Low Th
10	IN1_PAD_LOW_INT	ADC Channel 1 PAD LD, input signal exceeds low-level threshold interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Exceeds Low Th
9	IN2_PAD_HIGH_INT	ADC Channel 2 PAD LD, input signal exceeds high-level threshold interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Exceed High Th
8	IN1_PAD_HIGH_INT	ADC Channel 1 PAD LD, input signal exceeds high-level threshold interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Exceed High Th
7	GAIN_CONFLICT_INT	Gain updates both high gain and low gain concurrently interrupt. Write 1 to clear. 0 = (Default) Normal 1 = Update conflict
6:3	—	Reserved
2	IN2_CLIP_WARN_INT	Channel 2 clip-detect warning interrupt, rising-edge triggered. Write 1 to clear. 0 = (Default) Normal 1 = Clip detect
1	IN1_CLIP_WARN_INT	Channel 1 clip-detect warning interrupt, rising-edge triggered. Write 1 to clear. 0 = (Default) Normal 1 = Clip detect
0	—	Reserved

7.6.3 IRQ_ADC_EVENT_MASK

Address: 0x0000 3E2C

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_SIG_ACT_LOW_MASK	IN1_SIG_ACT_LOW_MASK	IN2_SIG_ACT_HIGH_MASK	IN1_SIG_ACT_HIGH_MASK	IN2_PAD_LOW_MASK	IN1_PAD_LOW_MASK	IN2_PAD_HIGH_MASK	IN1_PAD_HIGH_MASK	GAIN_CONFLICT_MASK	—				IN2_CLIP_WARN_MASK	IN1_CLIP_WARN_MASK	—
Default	1	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_SIG_ACT_LOW_MASK	ADC Channel 2 signal-activity detection, input signal level exceeds low-level threshold interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
14	IN1_SIG_ACT_LOW_MASK	ADC Channel 1 signal-activity detection, input signal level exceeds low-level threshold interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
13	IN2_SIG_ACT_HIGH_MASK	ADC Channel 2 signal-activity detection, input signal level exceeds high-level threshold interrupt mask. 0 = (Default) Do Not Mask 1 = Mask Interrupt
12	IN1_SIG_ACT_HIGH_MASK	ADC Channel 1 signal-activity detection, input signal level exceeds high-level threshold interrupt mask. 0 = (Default) Do Not Mask 1 = Mask Interrupt
11	IN2_PAD_LOW_MASK	ADC Channel 2 PAD LD, input signal exceeds low-level threshold interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
10	IN1_PAD_LOW_MASK	ADC Channel 1 PAD LD, input signal exceeds low-level threshold interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
9	IN2_PAD_HIGH_MASK	ADC Channel 2 PAD LD, input signal exceeds high-level threshold interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
8	IN1_PAD_HIGH_MASK	ADC Channel 1 PAD LD, input signal exceeds high-level threshold interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
7	GAIN_CONFLICT_MASK	Gain updates both high gain and low gain interrupt mask. 0 = Do Not Mask 1 = (Default) Mask Interrupt
6:3	—	Reserved
2	IN2_CLIP_WARN_MASK	ADC Channel 2 clip-detect warning interrupt mask. 0 = (Default) Do Not Mask 1 = Mask Interrupt
1	IN1_CLIP_WARN_MASK	ADC Channel 1 clip-detect warning interrupt mask. 0 = (Default) Do Not Mask 1 = Mask Interrupt
0	—	Reserved

7.6.4 IRQ_ADC_EVENT_STS

Address: 0x0000 3E5C

RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IN2_SIG_ACT_LOW_STS	IN1_SIG_ACT_LOW_STS	IN2_SIG_ACT_HIGH_STS	IN1_SIG_ACT_HIGH_STS	IN2_PAD_LOW_STS	IN1_PAD_LOW_STS	IN2_PAD_HIGH_STS	IN1_PAD_HIGH_STS	—					IN2_CLIP_WARN_STS	IN1_CLIP_WARN_STS	—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	IN2_SIG_ACT_LOW_STS	ADC Channel 2 signal-activity detection, input signal exceeds low-level threshold status. 0 = (Default) Not asserted 1 = Asserted
14	IN1_SIG_ACT_LOW_STS	ADC Channel 1 signal-activity detection, input signal exceeds low-level threshold status. 0 = (Default) Not asserted 1 = Asserted

Bits	Name	Description
13	IN2_SIG_ACT_HIGH_STS	ADC Channel 2 signal-activity detection, input signal exceeds high-level threshold status. 0 = (Default) Not asserted 1 = Asserted
12	IN1_SIG_ACT_HIGH_STS	ADC Channel 1 signal-activity detection, input signal exceeds high-level threshold status. 0 = (Default) Not asserted 1 = Asserted
11	IN2_PAD_LOW_STS	ADC Channel 2 PAD LD, input signal exceeds low-level threshold status. 0 = (Default) Not asserted 1 = Asserted
10	IN1_PAD_LOW_STS	ADC Channel 1 PAD LD, input signal exceeds low-level threshold status. 0 = (Default) Not asserted 1 = Asserted
9	IN2_PAD_HIGH_STS	ADC Channel 2 PAD LD, input signal exceeds high-level threshold status. 0 = (Default) Not asserted 1 = Asserted
8	IN1_PAD_HIGH_STS	ADC Channel 1 PAD LD, input signal exceeds high-level threshold status. 0 = (Default) Not asserted 1 = Asserted
7:3	—	Reserved
2	IN2_CLIP_WARN_STS	ADC Channel 1 clip warning status. 0 = (Default) Not asserted 1 = Asserted
1	IN1_CLIP_WARN_STS	ADC Channel 1 clip warning status. 0 = (Default) Not asserted 1 = Asserted
0	—	Reserved

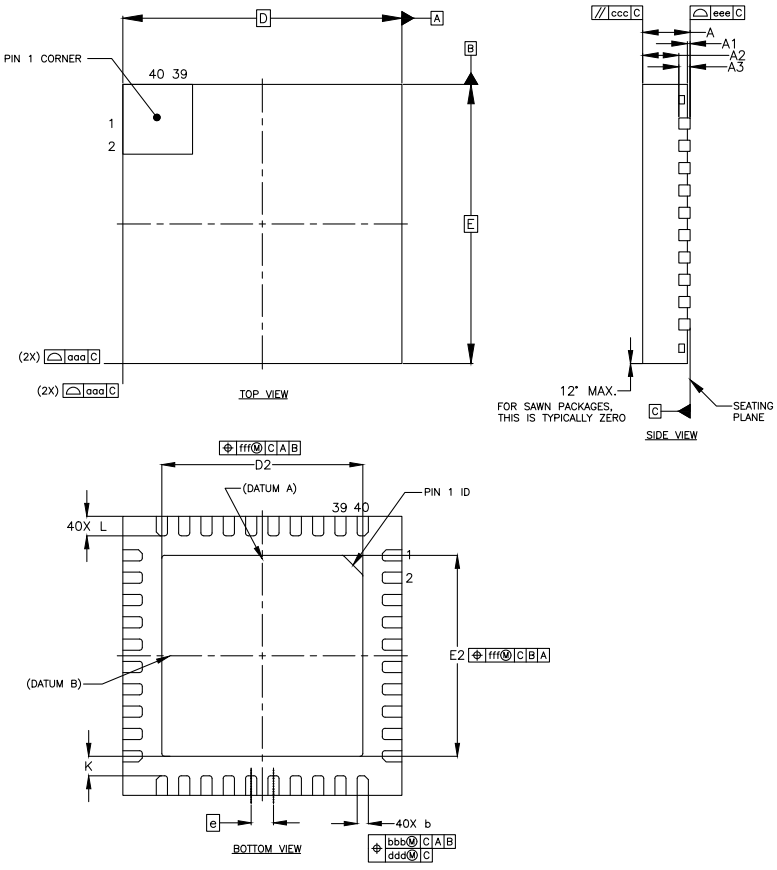
8 Thermal Characteristic

Table 8-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	QFN	Units
Junction-to-ambient thermal resistance	θ_{JA}	29.62	°C/W
Junction-to-board thermal resistance	θ_{JB}	16.37	°C/W
Junction-to-case (top) thermal resistance	θ_{JC}	54.85	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	15.21	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	2.38	°C/W

Notes:
- Natural convection at the maximum recommended operating temperature T_A (see Table 3-2)
- Four-layer, 2s2p PCB as specified by JESD51–9 and JESD51–11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51–12

9 Package Dimensions

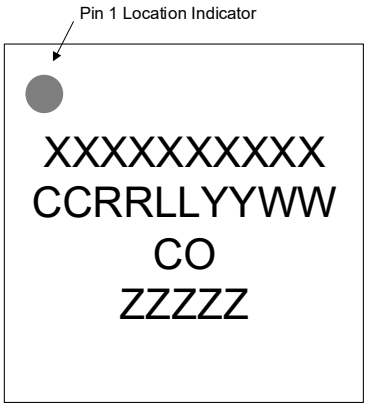


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	–	0.65	–
L/F THICKNESS		A3		0.20 REF.	
LEAD WIDTH		b	0.15	0.20	0.25
BODY SIZE	X	D		5.0 BSC	
	Y	E		5.0 BSC	
LEAD PITCH		e		0.40 BSC	
EP SIZE	X	D2	3.50	3.60	3.70
	Y	E2	3.50	3.60	3.70
LEAD LENGTH		L	0.30	0.35	0.40
LEAD TO EP CLEARANCE		K		0.35 REF.	
PACKAGE EDGE TOLERANCE		aaa		0.10	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	
MOLD FLATNESS		ccc		0.10	
COPLANARITY		eee		0.08	
EXPOSED PAD OFFSET		fff		0.10	

Figure 9-1. QFN Package Drawing

10 Package Marking

Figure 10-1. Package Marking



Top Side Brand
Line 1: Part number
Line 2: Package mark
Line 3: Country of origin (CO)
Line 4: Encoded wafer/device ID

Package Mark Fields
CC = Cirrus Logic Index Code
RR = Device revision code
LL = Lot sequence code
YY = Year of manufacture
WW = Work week of manufacture

11 Ordering Information

Table 11-1. Ordering Information

Product	Description	Package	Environmental Certifications	Grade	Temperature Range	Container	Orderable Part Number
CS5312BSE	High Performance Two-Channel Audio ADC	40-pin QFN	RoHS Compliant	Commercial	–40 to +85°C	Tray	CS5312BSE-DN
						Tape and Reel	CS5312BSE-DNR

12 References

- NXP Semiconductors, UM10204 Rev. 7, October 2021, *I2C-Bus Specification and User Manual*, http://www.nxp.com

13 Revision History

Important: Please check www.cirrus.com or with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Table 13-1. Revision History

Revision	Change
A2 MAY 2026	• Released for public distribution
A1 NOV 2025	• Initial version

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.