CS82L41

Imaging AFE with CMOS Data Output

Features

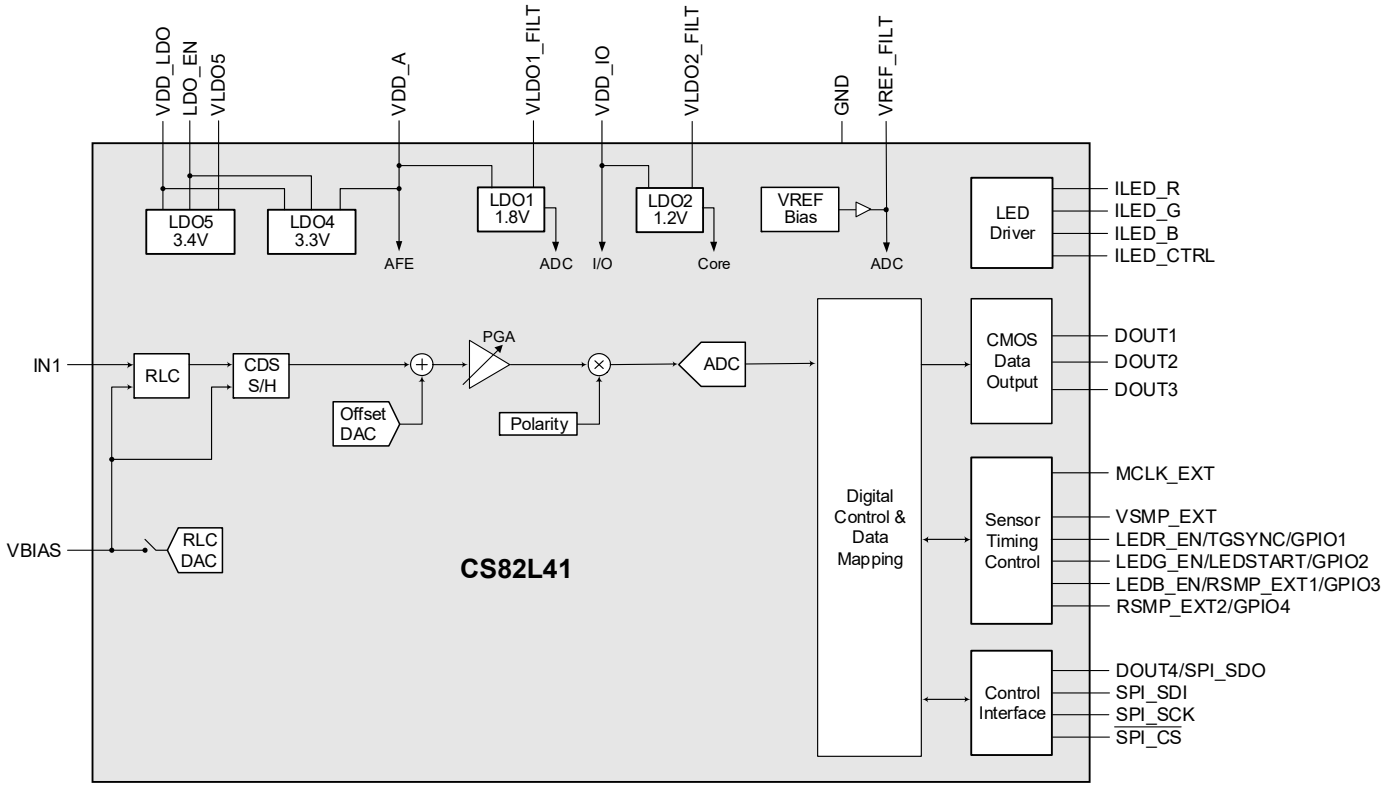
- Analog front end (AFE) for imaging applications
- Correlated double sampling
- Tolerant of spread-spectrum clock reference
- RGB LED current drive and timing control
- Internally generated reference voltages
- 3.3 V power regulation for CIS sensor
- SPI control interface
- 28-pin QFN package

Specifications

- 16-bit data output
- 24 MSPS conversion rate
- 12-bit programmable gain
- 9-bit programmable offset adjust
- 5-bit programmable clamp voltage
- 8-bit LED drive resolution

Applications

- Flatbed and sheet-feed scanners
- USB-compatible scanners
- Multifunction peripherals



General Description

The CS82L41 is a front-end device for CCD and CIS sensors. The CS82L41 processes and digitizes the analog sensor signal at pixel conversion rates of up to 24 MSPS.

The signal processing includes reset level clamping (RLC), correlated double sampling (CDS), and programmable polarity, gain and offset adjustment. Voltage references may be generated by an internal DAC or else provided externally.

The output data is available in a variety of CMOS digital formats.

The CS82L41 incorporates an RGB LED driver with programmable current sinks and timing control. White LEDs are also supported.

The 3.3 V supply may be provided directly, or else generated using an on-chip LDO. An additional LDO provides a 3.4 V supply for an external sensor.

The CS82L41 is available in a commercial-grade 0.4 mm pitch, 28-pin QFN package for operation from –40 °C to +85 °C.

See Section 11 for ordering information.

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1 Pin Assignments and Descriptions

1.1 QFN 28-Pin (Top View, Through-Package)

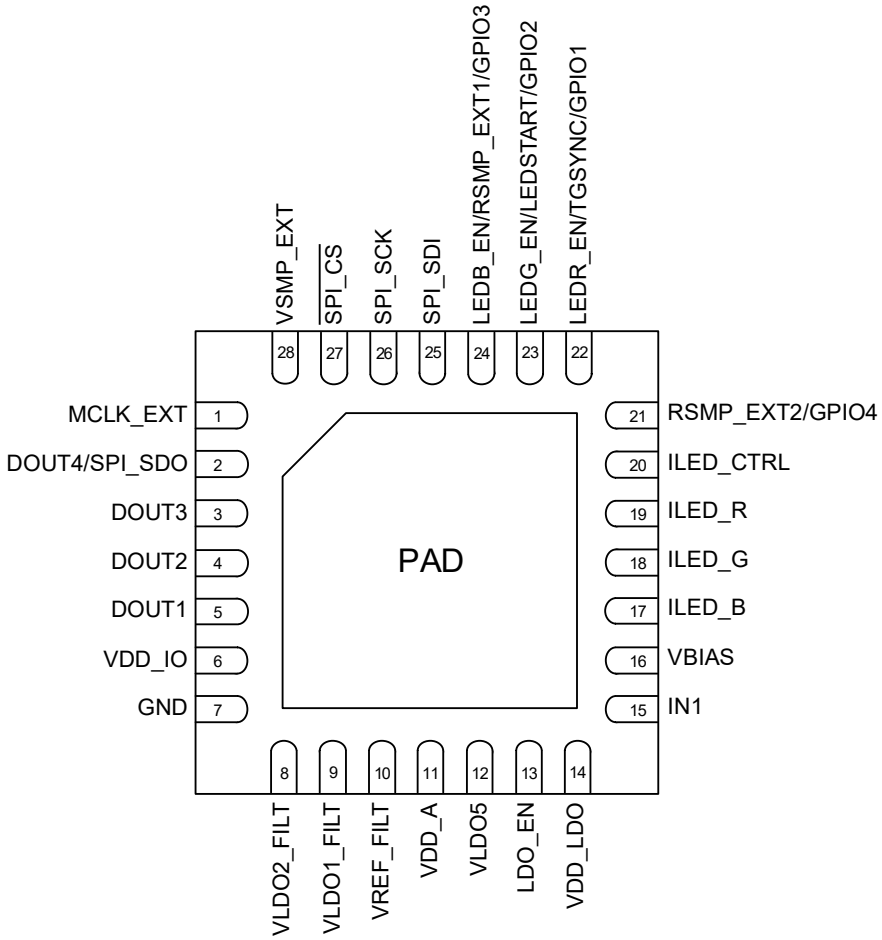


Figure 1-1. QFN 28-pin diagram (Top View, Through Package)

1.2 QFN Pin Descriptions

Table 1-1. QFN Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description	State at Reset
			Digital I/O		
DOUT1	5	VDD_IO	O	CMOS data output 1	Disabled o/p, pull-down
DOUT2	4	VDD_IO	O	CMOS data output 2	Disabled o/p, pull-down
DOUT3	3	VDD_IO	O	CMOS data output 3	Disabled o/p, pull-down
DOUT4/SPI_SDO	2	VDD_IO	O	CMOS data output 4/SPI data output	Disabled o/p, pull-down
LEDR_EN/TGSYNC/GPIO1	22	VDD_IO	I/O	Red LED enable/ Timing generator control input/ General-Purpose Input/Output 1	TGSYNC input, pull-down

Table 1-1. QFN Pin Descriptions *(Cont.)*

Pin Name	Pin #	Power Supply	I/O	Description	State at Reset
LEDG_EN/LEDSTART/ GPIO2	23	VDD_IO	I/O	Green LED enable/ LED timing control input/ General-Purpose Input/Output 2	LEDSTART input, pull-down
LEDB_EN/RSMP_EXT1/ GPIO3	24	VDD_IO	I/O	Blue LED enable/ Reset sample control input/ General-Purpose Input/Output 3/ Clock monitor	RSMP_EXT input, pull-down
MCLK_EXT	1	VDD_IO	I	Reference clock input	Input, pull-down
RSMP_EXT2/GPIO4	21	VDD_IO	I/O	Reset sample control input/ General-Purpose Input/Output 4	Input, pull-down
SPI_SDI	25	VDD_IO	I	SPI data input	Input, pull-down
SPI_SCK	26	VDD_IO	I	SPI clock input	Input, pull-down
$\overline{\text{SPI\_CS}}$	27	VDD_IO	I	SPI peripheral select input	Input, pull-down
VSMP_EXT	28	VDD_IO	I	Video sample control input	Input, pull-down
				Analog I/O	
ILED_B	17	—	I	Blue LED current sink	—
ILED_G	18	—	I	Green LED current sink	—
ILED_R	19	—	I	Red LED current sink	—
ILED_CTRL	20	VDD_A	O	External resistor for LED current control	—
IN1	15	VDD_A	I	Analog input for ADC channel 1	—
LDO_EN	13	—	I	LDO regulator enable (LDO4, LDO5)	—
VBIAS	16	VDD_A	I/O	Reference voltage for AFE inputs	—
VLDO1_FILT	9	VDD_A	O	LDO1 output	—
VLDO2_FILT	8	VDD_IO	O	LDO2 output	—
VLDO5	12	VDD_LDO	O	LDO5 output	—
VREF_FILT	10	VDD_A	O	Voltage reference for internal circuits	—
				Power Supplies	
GND	7, PAD	—	—	Ground	—
VDD_A	11	—	—	Supply for LDO1 and analog circuits	—
VDD_IO	6	—	—	Supply for LDO2 and digital I/O	—
VDD_LDO	14	—	—	Supply for LDO4 and LDO5	—

- See Table 3-1 for recommended operating limits for all pins

1.3 Termination of Unused Pins

Table 1-2 shows the required termination for unused pins (i.e., if the functionality of the pin is not being used). Pins not listed must be connected as shown in the typical connection drawings (see Section 2).

Table 1-2. Termination of Unused Pins

Name	Termination if unused
DOUTx LEDR_EN/TGSYNC/GPIO1 LEDG_EN/LEDSTART/GPIO2 LEDB_EN/RSMP_EXT1/GPIO3 RSMP_EXT2/GPIO4 VSMP_EXT	Float
ILED_x ILED_CTRL	Connect to GND

1.4 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS82L41 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD protection standards.

2 Typical Connection Diagram

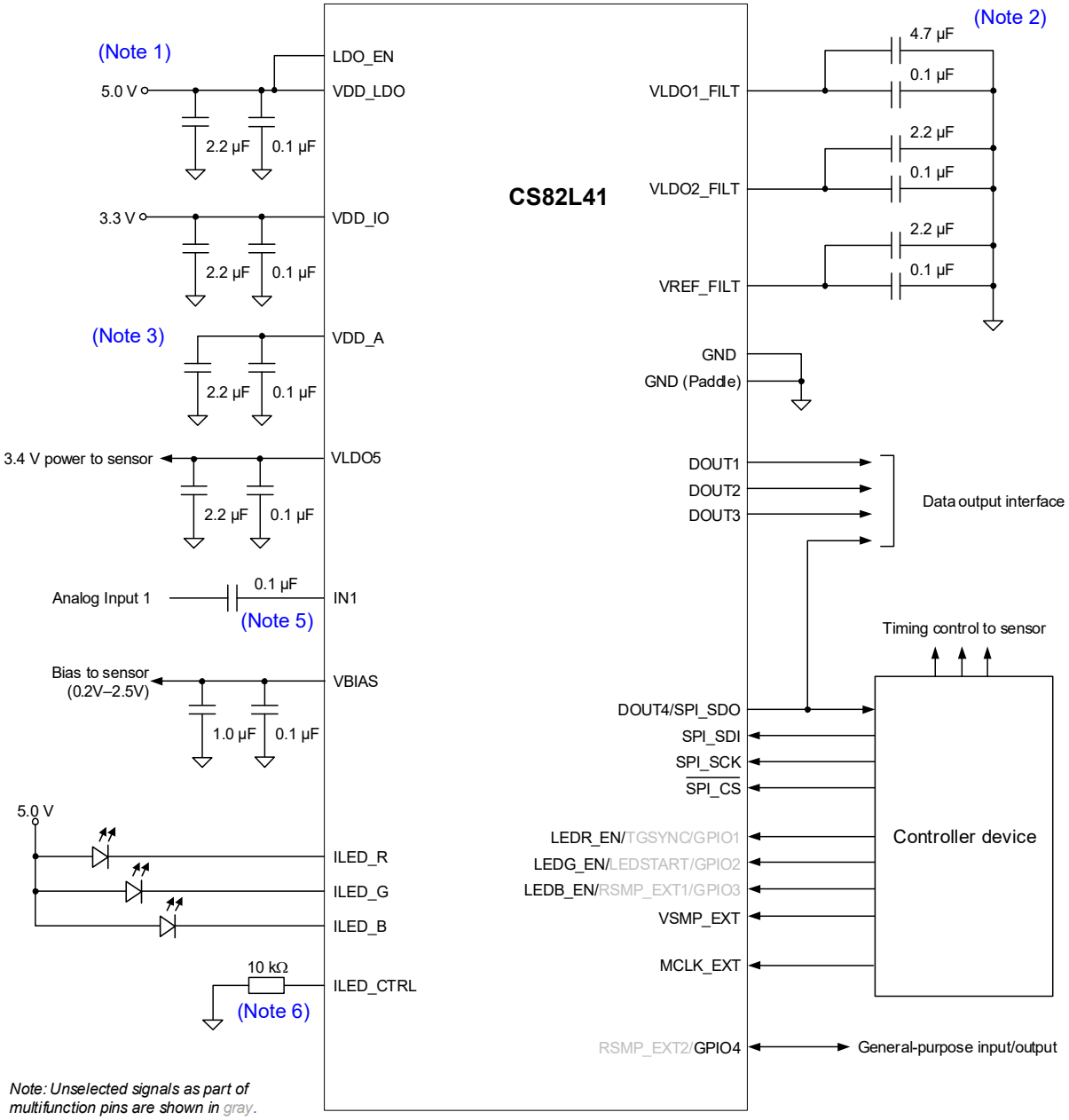


Figure 2-1. Typical Connections—Using LDO4/LDO5 Regulators

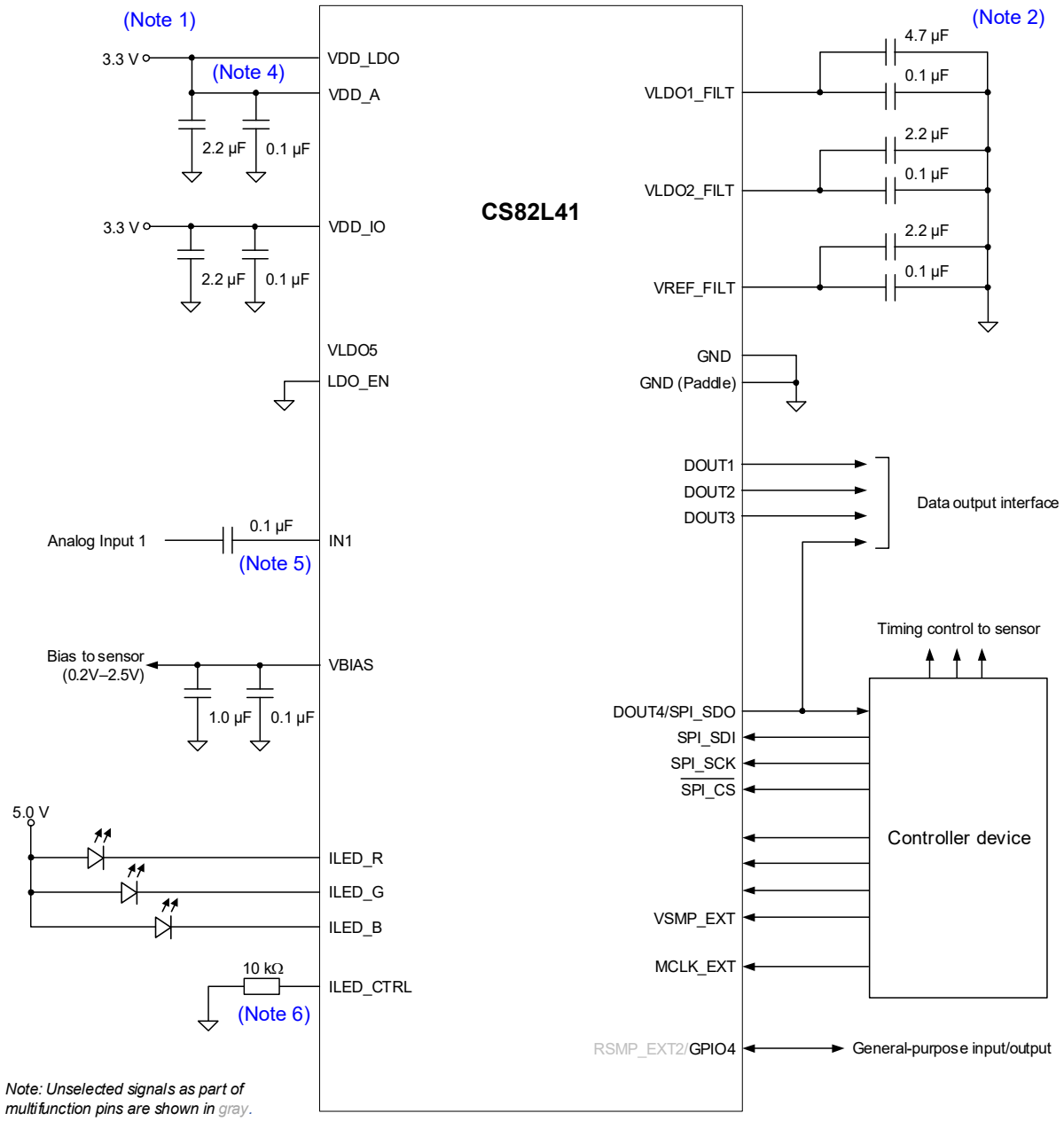


Figure 2-2. Typical Connections—LDO4/LDO5 Regulators Not Used

Notes referenced in the typical connection diagrams:

1. Power supply decoupling should be placed as close as possible to the CS82L41.
2. All capacitors are X7R, 20 % tolerance.
3. In the configuration shown, VDD_A is derived from the VDD_LDO supply, using the internal regulator.
4. In the configuration shown, the LDO4 and LDO5 internal regulators are not used. The VDD_LDO connection must be tied to VDD_A in this case.
5. Input capacitor is not required for DC-coupled analog input.
6. The LED current-control resistor must be within 1 % of the specified value.

3 Characteristics and Specifications

Note: The default register field configurations are used unless specified otherwise in the test conditions.

Table 3-1. Recommended Operating Conditions

Test conditions: Ground = 0 V; voltages are with respect to ground.

Parameter			Symbol	Minimum	Typical	Maximum	Unit
DC power supply	Digital input/output supply		VDD_IO	3.04	3.3	3.63	V
	Analog supply [1,2]		VDD_A	3.04	3.3	3.63	V
	LDO regulators supply [3]	LDO4 and LDO5 disabled	VDD_LDO	VDD_A	3.3	5.5	V
		LDO4 or LDO5 enabled		4.7	5.0	5.5	V
Supply ramp up/down (all supplies)			t_{PWR-UD}	0.001	—	0.1	V/µs
LED operating voltage		ILED_R, ILED_G, ILED_B	V_{ILED}	0.25	—	5.5	V
Ambient temperature		Functional	T_A	–40	25	85	°C
		Parametric performance		0	25	85	°C

Note: Functionality or parametric performance is not guaranteed or implied outside the limits in this table. Operation outside these limits may adversely affect device reliability.

1. The VDD_A supply can be generated by internal LDO4 (powered from VDD_LDO), or else provided externally.
2. The VDD_A supply is not required in the Idle and Sleep states (see Section 4.2); VDD_A can be disabled in these states to reduce power consumption. Note the sensor must also be powered down if VDD_A is disabled, to ensure the IN1 input voltage does not exceed VDD_A.
3. The VDD_LDO voltage must always be greater than or equal to VDD_A. If the LDO regulators are not used, VDD_LDO should be tied to VDD_A.

Table 3-2. Absolute Maximum Ratings

Test conditions: Ground = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
Analog and digital supplies		VDD_A, VDD_IO	–0.3	4.36	V
LDO regulators supply		VDD_LDO	VDD_A–0.3 [1]	6.6	V
External voltage at digital inputs/outputs		V_{INDI}	–0.3	VDD_IO + 0.3	V
External voltage at analog inputs	IN1, VBIAS	V_{INAI}	–0.3	VDD_A + 0.3	V
	LDO_EN		–0.3	5.5	V
	ILED_R, ILED_G, ILED_B		–0.3	6.6	V
Input current	digital input	I_{in}	—	±10	mA
Ambient operating temperature		T_A	–40	+85	°C
Junction operating temperature		T_J	–40	+125	°C
Storage temperature		T_{STG}	–65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-1 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. If VDD_A < 0 V, the minimum VDD_LDO rating is –0.3 V.

Table 3-3. Analog Input Path

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = VDD_LDO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25º C for typical specifications, T_A = 0 ºC to 85 ºC for min/max specifications.

Parameter		Minimum	Typical	Maximum	Unit
ADC sample rate		1	—	24	MHz
Maximum ADC output word length		—	16	—	Bits
Full-scale input voltage	Minimum gain Maximum gain	— —	2.4 0.25	— —	Vpk-pk Vpk-pk
Input capacitance	IN1 to ground	—	4	8	pF
Full-scale transition error	0 dB gain	—	55	—	mV
Zero-scale transition error	0 dB gain	—	33	—	mV
Differential nonlinearity	10 bit	–0.999	±0.5	+1.5	LSB
Integral nonlinearity	10 bit	—	±1	±4	LSB
Output noise	10 bit, 0 dB gain	—	0.5	1.5	LSB_{RMS}
PGA gain	minimum maximum step size (gain = 1–5 V/V) step size (gain = 5–9.75 V/V)	— — — —	1.0 9.75 0.125 0.25	— — — —	V/V V/V V V
Digital gain	minimum maximum resolution	— — —	0.5 1.99 12	— — —	V/V V/V bits
VBIAS input voltage		0.11	—	2.95	V
VBIAS short-circuit current	short to VDD_A short to GND	— —	42 2	— —	mA mA
VBIAS clamp-on resistance		—	50	—	Ω
VBIAS output resistance	VBIAS_ISEL = 10	—	2	—	Ω
VBIAS leakage current	0 < VBIAS < VDD_A	—	—	1	µA
RLC output voltage	minimum maximum step size	— — —	0.17 2.65 0.08	— — —	V V V
RLC differential nonlinearity		—	±0.5	—	LSB
RLC integral nonlinearity		—	±0.5	—	LSB
Offset voltage	minimum maximum step size	–400 250 —	–343 343 1.34	–250 400 —	mV mV mV
Offset voltage settling time [1]		—	2	—	samples
Offset differential nonlinearity		—	±0.5	±1	LSB
Offset integral nonlinearity		—	±0.5	±1	LSB
Offset temperature drift	T_A = 0 °C to 85 °C	–2.5	—	2.5	%

1. Measured when changing from the maximum output code to the minimum output code; settling time is defined from the end of the register write to the offset voltage being within 1.3 mV of the final level.

Table 3-4. LED Driver

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = VDD_LDO = 3.3 V; Ground = 0 V; voltages are with respect to ground; LED control resistor (ILED_CTRL to GND) = 10 kΩ; T_A = +25º C for typical specifications, T_A = 0 ºC to 85 ºC for min/max specifications.

Parameter		Minimum	Typical	Maximum	Unit
Coarse current control [1]	LEDx_COARSE = 00	28	33	38	mA
	LEDx_COARSE = 01	36	41	46	mA
	LEDx_COARSE = 10	44	49	54	mA
	LEDx_COARSE = 11	59	66	73	mA
Fine current control	minimum	—	0	—	mA
	maximum	—	Note [2]	—	mA
	resolution	—	8	—	bits
Fine current control DNL		–1	—	1	LSB
Fine current control INL		–1	—	1	LSB
Current control error	LEDx_COARSE = 00, LEDx_FINE > 0x26	—	—	18	%
	LEDx_COARSE = 01, LEDx_FINE > 0x20	—	—	15	%
	LEDx_COARSE = 10, LEDx_FINE > 0x1B	—	—	12	%
	LEDx_COARSE = 11, LEDx_FINE > 0x14	—	—	12	%
Maximum LED driver current (sum of all enabled channels)		—	135	—	mA
LED leakage current (LED output disabled)		—	20	—	µA
Maximum LED fault current [3]		—	90	—	mA
Load capacitance		—	—	10	pF

1.Assumes maximum fine-current selection (LEDx_FINE = 0xFF).
2.At the maximum fine-current selection, the LED current is equal to the applicable coarse control setting.
3.Fault conditions include ILED_CTRL resistor short circuit, ILED_CTRL resistor short to GND or supply, and internal driver faults.

Table 3-5. LDO5 Regulator

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V, VDD_LDO = 5.0 V; Ground = 0 V; voltages are with respect to ground; T_A = +25 ºC for typical specifications, T_A = 0 ºC to 85 ºC for min/max specifications.

Parameter		Minimum	Typical	Maximum	Unit
Programmable output voltage	minimum	—	3.016	—	V
	maximum	—	3.56	—	V
	step size	—	0.068	—	V
Output voltage accuracy	V_{OUT} = 3.4 V, I_{LOAD} = 200 mA	–3	—	3	%
Output load current		0	—	200	mA
Output load current limit [1]	V_{OUT} = 3.4 V	300	400	500	mA
Output load regulation	V_{OUT} = 3.4 V, I_{LOAD} = 1–200 mA	—	60	—	mV
PSRR	100 mV (peak-peak) 1 kHz sine wave	—	70	—	dB
Start-up time	from LDO_EN high to output within specification	—	—	5	ms
Input voltage to enable LDO5	LDO_EN pin	2	—	—	V
Input voltage to disable LDO5	LDO_EN pin	—	—	250	mV

1.Assumes default register conditions, LDO5_ILIMIT_CTRL = 000, LDO5_ILIMIT_VPC = 1.

Table 3-6. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = VDD_LDO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25 ºC for typical specifications, T_A = 0 ºC to 85 ºC for min/max specifications.

Parameter		Symbol	Minimum	Typical	Maximum	Unit
Input leakage current (per pin)		I_{IN}	—	—	±4	µA
Input capacitance (per pin)		—	—	—	10	pF
High-level output	I_{OH} = 1 mA	V_{OH}	0.9×VDD_IO	—	—	V
Low-level output	I_{OL} = –1 mA	V_{OL}	—	—	0.1×VDD_IO	V
High-level input		V_{IH}	0.7×VDD_IO	—	—	V
Low-level input		V_{IL}	—	—	0.3×VDD_IO	V
Internal weak pull-up/pull-down		—	1.2	1.4	1.6	MΩ
High-impedance output current	Pin grounded	I_{OZ}	—	—	1	µA

Table 3-7. DC Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = VDD_LDO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25 ºC for typical specifications, T_A = 0 ºC to 85 ºC for min/max specifications.

Parameter			Minimum	Typical	Maximum	Unit
Voltage reference (VREF_FILT)	Output voltage		—	1.2	—	V
Power-on reset	VDD_IO reset threshold	VDD_IO rising	1.97	—	2.89	V
		VDD_IO falling	1.80	—	2.67	V
	VDD_LDO reset threshold	VDD_LDO rising	1.92	—	2.89	V
		VDD_LDO falling	1.75	—	2.67	V

Table 3-8. System Clocking, Startup and Shutdown

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = VDD_LDO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25 ºC for typical specifications, T_A = 0 ºC to 85 ºC for min/max specifications.

Parameter			Minimum	Typical	Maximum	Unit
Reset	Power-on reset to control port active [1,2]		—	—	2	ms
	Software reset to control port active [2]		—	—	2	ms
	Power-on reset to Idle State		—	—	4	ms
	Software reset to Idle State		—	—	4	ms
Ready	Idle to Ready State		—	—	3	ms
Power-down	Ready to Idle State		—	—	10	ms
MCLK input	Input reference frequency (MCLK_EXT)		2	—	48	MHz
	Duty cycle		45	—	55	%
	Spread-spectrum modulation tolerance	Amplitude [3]	–3	—	3	%
		Frequency	—	—	60	kHz

1.Measured from VDD_IO above its reset threshold.
2.It is recommended to confirm the device has reached the Idle State before configuring the control registers.
3.Note the instantaneous frequency must always be within the specified input range.

Table 3-9. Temperature Monitoring and Protection Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V, VDD_LDO = 5.0 V; Ground = 0 V; voltages are with respect to ground.

Parameter	Minimum	Typical	Maximum	Unit
Overtemperature error threshold	—	155	—	°C
Overtemperature error threshold deviation [1]	–10	—	10	°C

1.The overtemperature error threshold deviation specifies the accuracy of the temperature-detection circuitry. This specification relates how many degrees above or below the threshold the overtemperature error circuitry may trigger.

Table 3-10. Device Power Consumption

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = VDD_LDO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25 ºC for typical specifications, T_A = 0 ºC to 85 ºC for min/max specifications.

Use Configuration			Typical	Maximum	Unit
Sleep State (MCLK stopped, oscillator disabled)	VDD_IO current	T_A = 25 ºC	58	100	µA
		T_A = 0 ºC to 85 ºC	—	250	µA
	VDD_LDO current	VDD_LDO = 5.0 V, LDO5 enabled [1]	—	400	µA
		VDD_LDO = 5.0 V, LDO5 disabled	—	50	µA
	VDD_A current		—	100	µA
Idle State (MCLK stopped, default register conditions)	VDD_IO current	T_A = 25 ºC	191	240	µA
		T_A = 0 ºC to 85 ºC	—	400	µA
	VDD_LDO current	VDD_LDO = 5.0 V, LDO5 enabled [1]	—	400	µA
		VDD_LDO = 5.0 V, LDO5 disabled	—	50	µA
	VDD_A current		—	100	µA
Active State CMOS input/output	Total power consumption MCLK = 12 MHz, sample rate = 6 MHz, 4 x DOUT, C_{DOUT} = 10 pF		43	—	mW
	Total power consumption MCLK = 48 MHz, sample rate = 24 MHz, 4 x DOUT, C_{DOUT} = 10 pF		47	—	mW
LED Drivers	Incremental power consumption LED current = 45 mA, fine current = full scale	1 LED enabled	1.8	—	mW
		2 LEDs enabled	3.2	—	mW
		3 LEDs enabled	4.4	—	mW

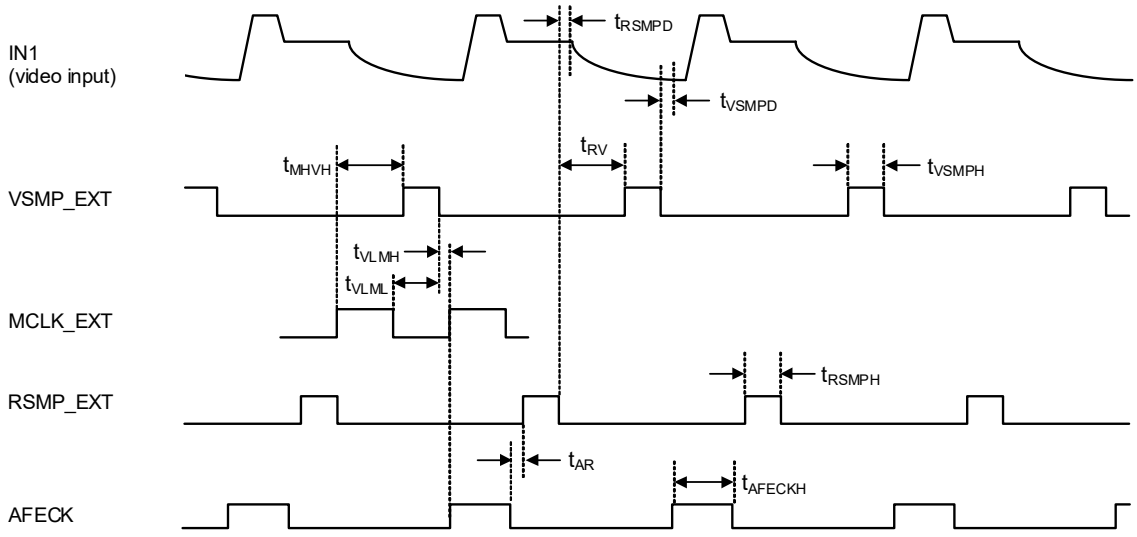
1.Assumes LDO4 is disabled; LDO5 is enabled under software control using the LDO5_EN bit.

Table 3-11. Switching Specifications—Video Sampling (Timing Mode 1)

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = VDD_LDO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

Parameter [1,2]		Symbol	Minimum	Typical	Maximum	Unit
Aperture delay from RSMP falling edge	CDS mode	t_{RSMPD}	—	8	—	ns
Aperture delay from VSMP falling edge		t_{VSMPD}	—	5	—	ns
RSMP high period	CDS mode	t_{RSMPH}	5	—	—	ns
VSMP high period		t_{VSMPH}	5	—	—	ns
AFECK high period		t_{AFECKH}	15.1	—	—	ns
RSMP falling edge to VSMP rising edge	CDS mode	t_{RV}	0	—	—	ns
AFECK falling edge to RSMP rising edge	CDS mode	t_{AR}	0	—	—	ns
AFECK falling edge to VSMP rising edge	non-CDS mode	t_{AV}	0	—	—	ns
MCLK rising edge to VSMP rising edge		t_{MHVH}	0	—	—	ns
MCLK falling edge to VSMP falling edge		t_{VLML}	0	—	—	ns
VSMP falling edge to MCLK rising edge		t_{VLMH}	2	—	—	ns

1.Video input timing—CDS mode. The VSMP and RSMP timing is controlled by external signals VSMP_EXT and RSMP_EXT.



2.Video input timing—non-CDS mode. The VSMP timing is controlled by external signal VSMP_EXT.

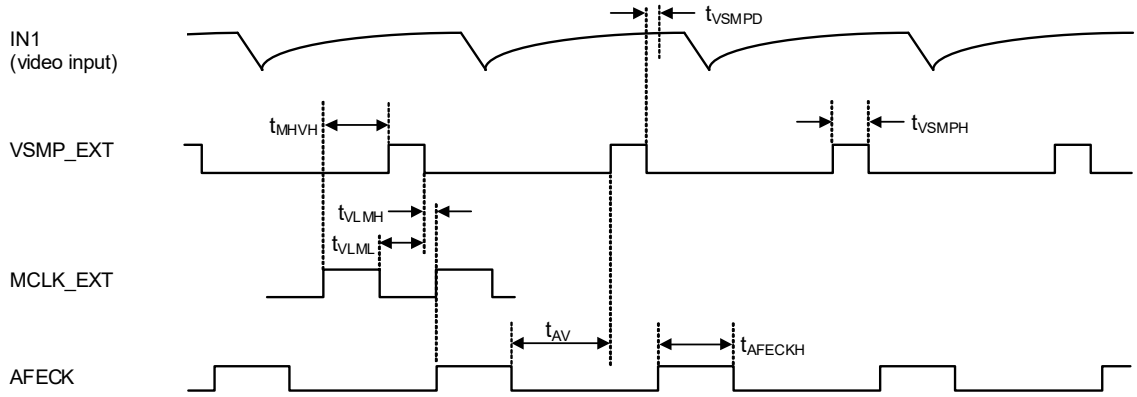
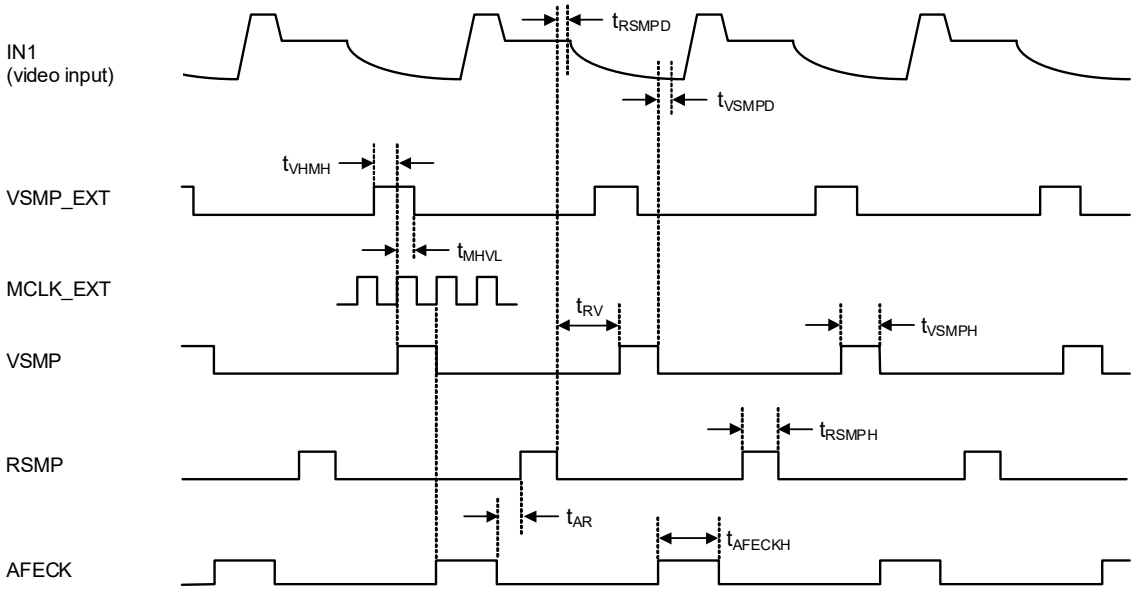


Table 3-12. Switching Specifications—Video Sampling (Timing Mode 2)

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = VDD_LDO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

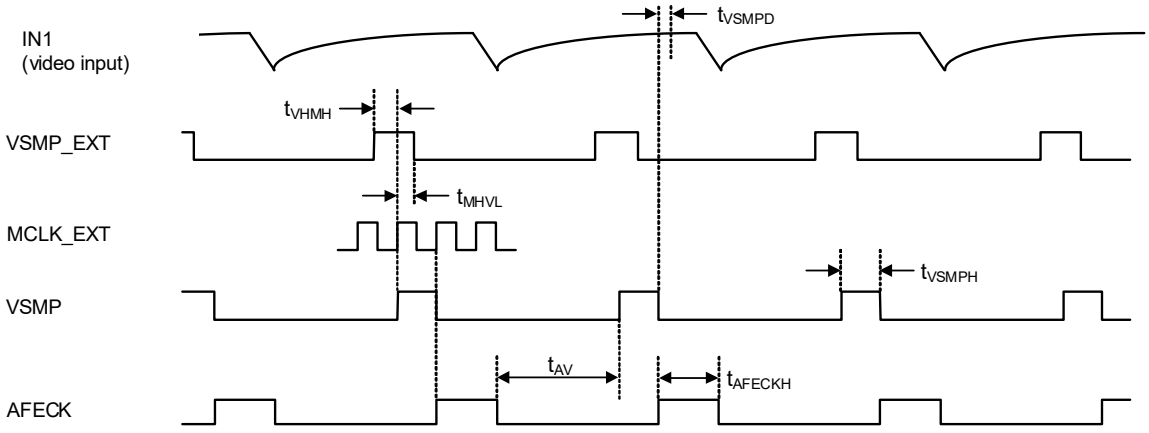
Parameter [1,2]		Symbol	Minimum	Typical	Maximum	Unit
Aperture delay from RSMP falling edge	CDS mode	t_{RSMPD}	—	8	—	ns
Aperture delay from VSMP falling edge		t_{VSMPD}	—	5	—	ns
RSMP high period	CDS mode	t_{RSMPH}	—	1	—	MCLK
VSMP high period		t_{VSMPH}	—	1	—	MCLK
AFECK high period		t_{AFECKH}	15.1	—	—	ns
RSMP falling edge to VSMP rising edge	CDS mode	t_{RV}	0	—	—	ns
AFECK falling edge to RSMP rising edge	CDS mode	t_{AR}	0	—	—	ns
AFECK falling edge to VSMP rising edge	non-CDS mode	t_{AV}	0	—	—	ns
VSMP_EXT rising edge to MCLK rising edge		t_{VHMH}	2.0	—	—	ns
MCLK rising edge to VSMP_EXT falling edge		t_{MHVL}	2.1	—	—	ns

1.Video input timing—CDS mode. The VSMP and RSMP timing is controlled by external signal VSMP_EXT, retimed to MCLK_EXT.



Note: Assumes VSMP_EXT_DLY = 0 (rising edge of VSMP on first MCLK edge)
Assumes VSMP_EXT_POL = 0 (VSMP_EXT rising is the active edge)

2.Video input timing—non-CDS mode. The VSMP timing is controlled by external signal VSMP_EXT, retimed to MCLK_EXT.



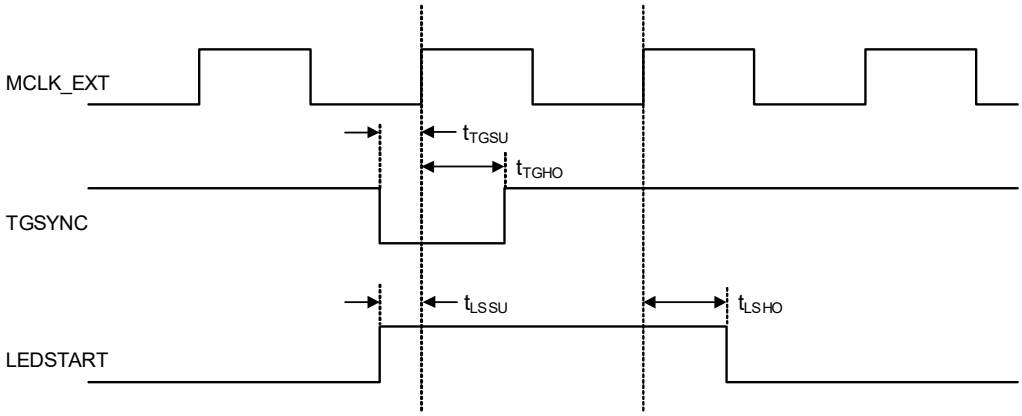
Note: Assumes VSMP_EXT_DLY = 0 (rising edge of VSMP on first MCLK edge)
Assumes VSMP_EXT_POL = 0 (VSMP_EXT rising is the active edge)

Table 3-13. Switching Specifications—TGSYNC/LEDSTART Timing

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = VDD_LDO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

Parameter [1,2,3,4]	Symbol	Minimum	Typical	Maximum	Unit
TGSYNC setup time to MCLK active edge	t_{TGSU}	4	—	—	ns
TGSYNC hold time from MCLK active edge	t_{TGHO}	2	—	—	ns
LEDSTART setup time to MCLK active edge	t_{LSSU}	4	—	—	ns
LEDSTART hold time from MCLK active edge	t_{LSHO}	2	—	—	ns

1.Assumes the TGSYNC filter is disabled. See Section 4.7.2.1 for use cases with TGSYNC filter enabled.
2.TGSYNC/LEDSTART timing—figure shows active-high TGSYNC and LEDSTART signals, timed with reference to rising active MCLK edge.



3.TGSYNC input is supported on two different pins—TGSYNC1 or LEDSTART.
4.LEDSTART input is only used if LEDSTART_SEQ_INIT is set.

Table 3-14. Switching Specifications—Data Output

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = VDD_LDO = 3.3 V; Ground = 0 V; voltages are with respect to ground; Load capacitance = 10 pF; T_A = 0–85ºC.

Parameter [1]	Symbol	Minimum	Typical	Maximum	Unit
Propagation delay	t_{PD}	6	—	12	ns

1.Output data timing.

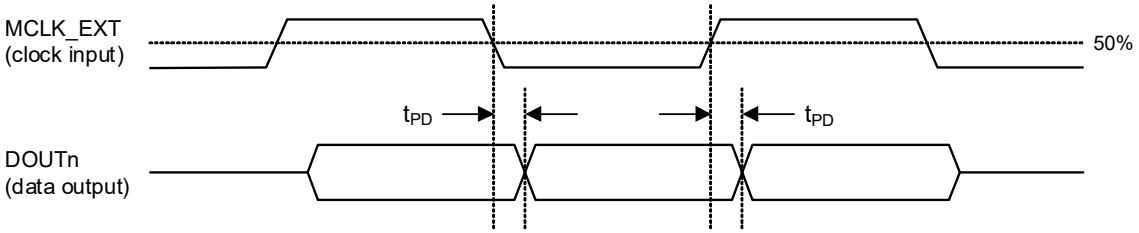


Table 3-15. Switching Specifications—Monitor Output

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = VDD_LDO = 3.3 V; Ground = 0 V; voltages are with respect to ground; Load capacitance = 10 pF; T_A = 0–85ºC.

Parameter [1]		Symbol	Minimum	Typical	Maximum	Unit
Propagation delay	VSMP, RSMP	t_{PD}	—	2.0	—	ns

1.Output data timing.

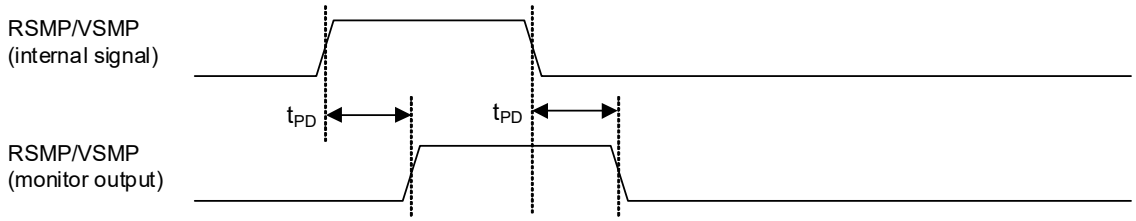
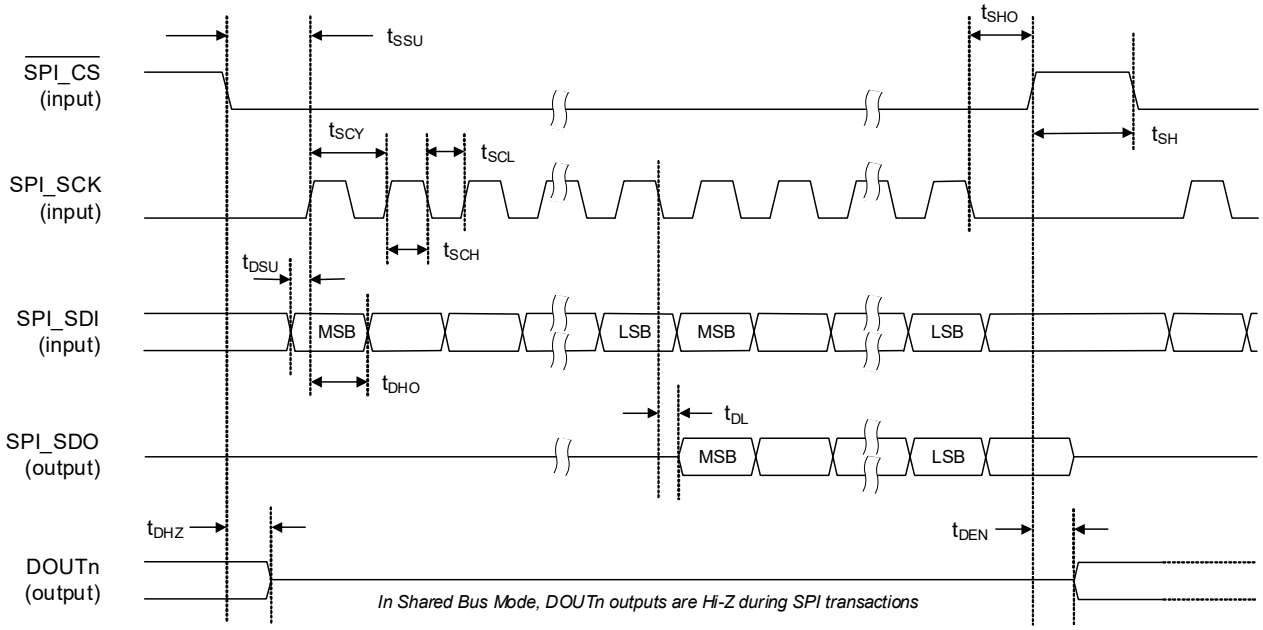


Table 3-16. Switching Specifications—SPI Port

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = VDD_LDO = 3.3 V; Ground = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for CMOS input/output (as specified in Table 3-6); T_A = 0–85ºC.

Parameter [1]		Symbol	Minimum	Maximum	Unit
SPI_SCK frequency		$1/t_{SCY}$	—	12	MHz
$\overline{\text{SPI\_CS}}$ falling edge to SPI_SCK rising edge		t_{SSU}	60	—	ns
SPI_SCK falling edge to $\overline{\text{SPI\_CS}}$ rising edge		t_{SHO}	20	—	ns
SPI_SCK pulse width low		t_{SCL}	33	—	ns
SPI_SCK pulse width high		t_{SCH}	33	—	ns
SPI_SDI to SPI_SCK setup time		t_{DSU}	20	—	ns
SPI_SDI to SPI_SCK hold time		t_{DHO}	20	—	ns
SPI_SCK falling edge to SPI_SDO transition		t_{DL}	0	33	ns
Bus free time between active $\overline{\text{SPI\_CS}}$		t_{SH}	417	—	ns
DOUT disable time from $\overline{\text{SPI\_CS}}$ falling edge [2]	Shared Bus Mode	t_{DHZ}	—	15	ns
DOUT enable time from $\overline{\text{SPI\_CS}}$ rising edge [2]	Shared Bus Mode	t_{DEN}	5	—	ns

1.SPI control-port timing.



2.In Shared Bus Mode, the DOUTn data outputs are disabled (Hi-Z) whenever $\overline{\text{SPI\_CS}}$ is asserted (see Section 4.9.1).

4 Functional Description

4.1 Power Supplies and Reset

The CS82L41 is powered using VDD_A, VDD_IO, and VDD_LDO external supplies.

- **VDD_A** is the supply rail for the analog circuits, including internal regulator LDO1. VDD_A can be powered directly from an external source, or can be generated from VDD_LDO using the internal regulator LDO4.

  The VDD_A supply is not required in the Idle and Sleep states; the VDD_A supply can be disabled in these states to reduce power consumption. Note the sensor must also be powered down if VDD_A is disabled, to ensure the IN1 input voltage does not exceed VDD_A.

  The VDD_A status is indicated using VDDA_STS. A valid VDD_A (internal or external) must be present when transitioning to the Ready or Active states. Sampling and conversion is not supported if VDD_A is not present.
- **VDD_IO** is the supply rail for digital input/output; it also powers other digital circuits via internal regulator LDO2. VDD_IO can be powered directly from an external source, or can be generated from VDD_LDO using the internal regulator LDO5.

  Note that, if the LDO5 regulator is used to generate the VDD_IO supply, an external connection is required between the VLDO5 and VDD_IO pins.
- **VDD_LDO** is the supply rail for internal regulators LDO4 and LDO5. The regulators can be used to generate the VDD_A and VDD_IO supplies, and also to provide power to an external sensor. See Section 4.1.1 and Section 4.1.2 to configure these regulators.

  The VDD_LDO voltage must always be greater than or equal to VDD_A. If VDD_A is powered externally, VDD_LDO must be enabled before VDD_A; the VDD_A supply must be disabled before VDD_LDO.

  If the LDO4/LDO5 regulators are not used, the VDD_LDO supply should be tied to VDD_A, or to a higher voltage such as a 5 V rail.

Note that all digital inputs should be held low until VDD_IO is within the recommended operating limits. Analog video input must not be applied until VDD_A is within recommended operating limits. See Table 3-2 for maximum ratings.

4.1.1 LDO4 Regulator

The LDO4 regulator can be used to generate a 3.3 V analog supply for VDD_A. The LDO4 regulator is enabled using the LDO_EN pin—connect to VDD_LDO to enable the LDO, or connect to GND to disable. The LDO can also be enabled by setting LDO4_EN.

The LDO_EN input pin controls LDO4 and LDO5. The LDO_EN control can be masked using LDO_EN_MASK. If this bit is set, the LDO_EN input has no effect on the regulators; this can be used to allow independent control of LDO4 and LDO5, even if the hardware input is asserted—see Section 4.1.3 for example control sequences.

The VDD_A supply is not required in the Idle and Sleep states; if VDD_A is powered from LDO4, the LDO can be disabled in these states to reduce power consumption. Note that the sensor must also be powered down in this case. After enabling the LDO4 regulator, a start-up delay of 1 ms should be allowed before transitioning to the Active State.

If the LDO4 regulator is under software control (i.e., the LDO_EN input is masked or deasserted), it can only be enabled or disabled in the Idle State. If LDO4_EN is written in any other state, the update does not take effect until the device returns to the Idle State. See Section 4.2 for details of the CS82L41 operational states.

If the LDO4 regulator is under software control, it is disabled by default, supporting external VDD_A supply. Note that the LDO must not be enabled if an external VDD_A supply is present.

The LDO4 output can configured in a high-impedance (Hi-Z) state using LDO4_HIZ. Note that setting this bit disables the LDO, regardless of the LDO4_EN bit or LDO_EN hardware control. If an external VDD_A supply is used, it is recommended to set LDO4_HIZ in order to reduce power dissipation through the discharge path.

4.1.2 LDO5 Regulator

The LDO5 regulator can be used to provide power to an external sensor; it can also be used to generate the VDD_IO supply. The output voltage is configured using LDO5_VOUT.

The LDO5 regulator is enabled using the LDO_EN pin—connect to VDD_LDO to enable the LDO, or connect to GND to disable. The LDO can also be enabled by setting LDO5_EN.

The LDO_EN input pin controls LDO4 and LDO5. The LDO_EN control can be masked using LDO_EN_MASK. If this bit is set, the LDO_EN input has no effect on the regulators; this can be used to allow independent control of LDO4 and LDO5, even if the hardware input is asserted—see Section 4.1.3 for example control sequences.

Notes: It is recommended that the LDO5 regulator should not be used to power an external sensor at the same time as providing the VDD_IO supply. Noise associated with the VDD_IO supply may be detrimental to the performance of an external sensor connected to the same node. If LDO5 is used to power an external sensor and VDD_IO, care should be taken to ensure VDD_IO noise is within acceptable range for the sensor.

If LDO5 is used to power the external sensor, the LDO5 regulator must not be enabled if VDD_A is disabled. In typical use cases, this means LDO5 must not be enabled if LDO4 is disabled.

If LDO5 is used to generate the VDD_IO supply, the LDO must be enabled using the LDO_EN pin. Care must be taken when controlling the LDOs to avoid interrupting the VDD_IO supply.

If the LDO_EN pin is used to control LDO5, care must be taken to ensure the switching edges are free of bounce/chatter. To avoid overshoot, the LDO output must be fully discharged before re-enabling the LDO.

The LDO5 regulator supports a configurable current limit, including a dynamic control that is proportional to the output voltage. Proportional control (VPC) is enabled by default and can be used to suppress inrush currents in the load. The current limit is configured using LDO5_ILIMIT_CTRL. Note that the valid selections vary depending on whether VPC is enabled. If VPC is enabled (LDO5_ILIMIT_VPC = 1), the limit is approximated by the following formula:

$$\text{Current Limit (mA)} = I_{LDO5\_ILIMIT\_CTRL} + (V_{LDO5} \times 60)$$

The output of the LDO regulator is provided on the VLDO5 pin. If LDO5 is used to generate the VDD_IO supply, an external connection is required between VLDO5 and VDD_IO.

4.1.3 Typical Power-Supply Configurations

Typical power-supply configurations for the CS82L41 are shown in Section 4.1.3.1 through Section 4.1.3.3.

4.1.3.1 Dual Supply (5 V, 3.3 V)

Fig. 4-1 shows the CS82L41 powered using 5 V and 3.3 V external supplies. The 5 V supply powers the external sensor (using LDO5) and the analog circuits (using LDO4). A separate 3.3 V supply powers the digital circuits.

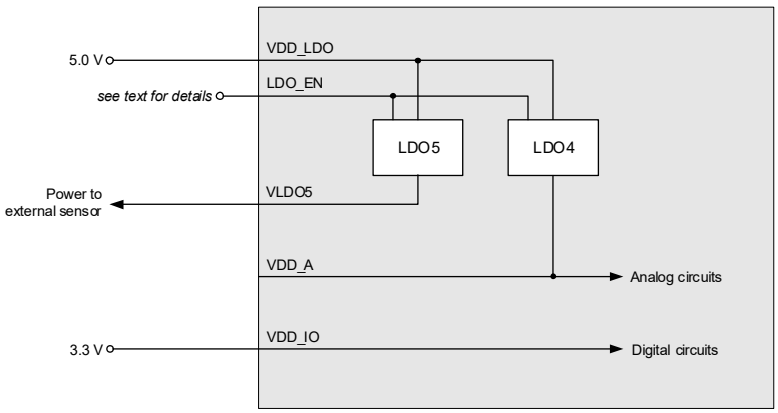


Figure 4-1. Dual Supply (5 V, 3.3 V)

In this configuration, the LDO4 and LDO5 can be controlled to suit the application requirements. The LDO_EN pin can be used in the following ways:

- **LDO_EN tied to GND.** LDOs are disabled by default and controlled in software using LDO4_EN and LDO5_EN.
- **LDO_EN tied to VDD_LDO.** LDOs are enabled by default.
- **LDO_EN controlled by host.** The LDOs are controlled by an external device driving the LDO_EN pin.

If both LDOs are enabled using the LDO_EN pin, the following control sequence can be used to disable the sensor (LDO5) while maintaining VDD_A.

1. Set LDO4_EN
2. Set LDO5_EN
3. Set LDO_EN_MASK
4. Clear LDO5_EN to disable LDO5

Note that LDO4 must not be disabled while LDO5 is enabled—this would result in an input voltage applied while VDD_A is disabled. Equivalently, LDO5 must not be enabled while LDO4 is disabled.

4.1.3.2 Single/Dual Supply (3.3 V)

Fig. 4-2 shows the CS82L41 powered using 3.3 V external supplies. The analog and digital power can be provided separately, or else from a single supply. Note the VDD_LDO connection must be tied to VDD_A in this case.

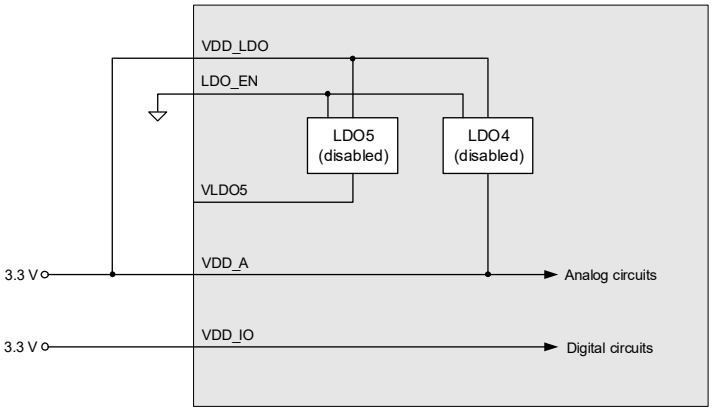


Figure 4-2. Single/Dual Supply (3.3 V)

In this configuration, the LDO regulators are not used. The regulators must remain disabled at all times.

4.1.3.3 Single Supply (5 V)

Fig. 4-3 shows the CS82L41 powered using a single 5 V external supply. The LDO5 regulator provides power to the external sensor, and to the digital circuits via VDD_IO. The LDO4 regulator powers the analog circuits.

Note that powering the external sensor and VDD_IO from a common supply can be detrimental to the performance of the sensor. In this configuration, care should be taken to provide adequate filtering to minimize noise associated with the VDD_IO supply reaching the sensor.

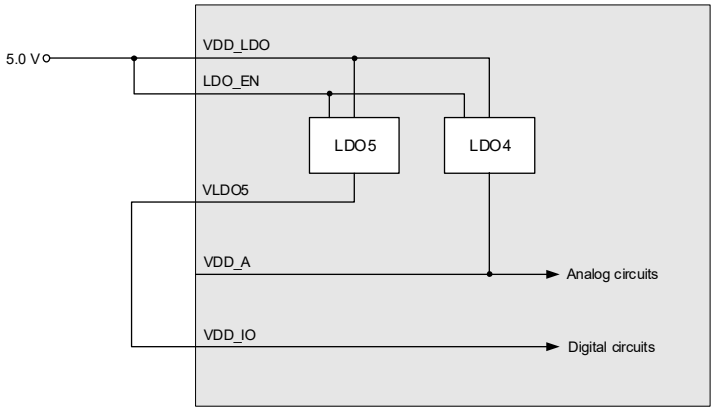


Figure 4-3. Single Supply (5 V)

In this configuration, the LDO regulators are enabled at power-up and must remain enabled at all times. Software control of the LDO enable/disable functions should not be used in this configuration.

4.1.4 Resets

The CS82L41 is in reset if the VDD_IO or VDD_LDO supply is below the respective reset threshold defined in Table 3-7. The POR sequence is scheduled on initial power-up, and following any interruption to VDD_IO or VDD_LDO that results in a drop below the reset threshold. The POR causes all of the CS82L41 control registers to be reset to their default states.

A software reset is triggered by writing 0x5A to the SFT_RESET field. A software reset causes all of the CS82L41 control registers to be reset to their default states.

On completion of the reset and associated start-up processes, the device transitions to the Idle State (see Section 4.2).

Note: The LDO4 and LDO5 regulators can be enabled without VDD_IO applied (i.e., while the device is in reset). If the LDO_EN pin is asserted and VDD_LDO is within valid operating conditions, the regulators are enabled. The default output voltage and current limit are applied if VDD_IO is not present.

4.2 Operational States

The CS82L41 behavior is defined according to its operational states as follows:

- **Start-Up.** This is the initial state following reset, in which the device performs necessary start-up processes. On successful completion of start-up, the device automatically transitions to the Idle State.
- **Idle.** This is a low-power state in which the device can be configured for the required operational behavior. Register access is supported on the SPI control interface. After configuring the device, the host can command the device to transition to the Ready State.
- **Ready.** In this state, the analog input path and internal control circuits are fully enabled. In this state, the host can select the Active State when required.
- **Active.** This is the fully operational state, supporting active sampling and data output.
- **Error.** This is the error state. See Section 4.2.1 for further details.
- **Sleep.** This is a dormant state with very low power consumption. Note that register access is not possible in this state, other than to wake the device to the Idle State.

The operational state transitions are shown in Fig. 4-4.

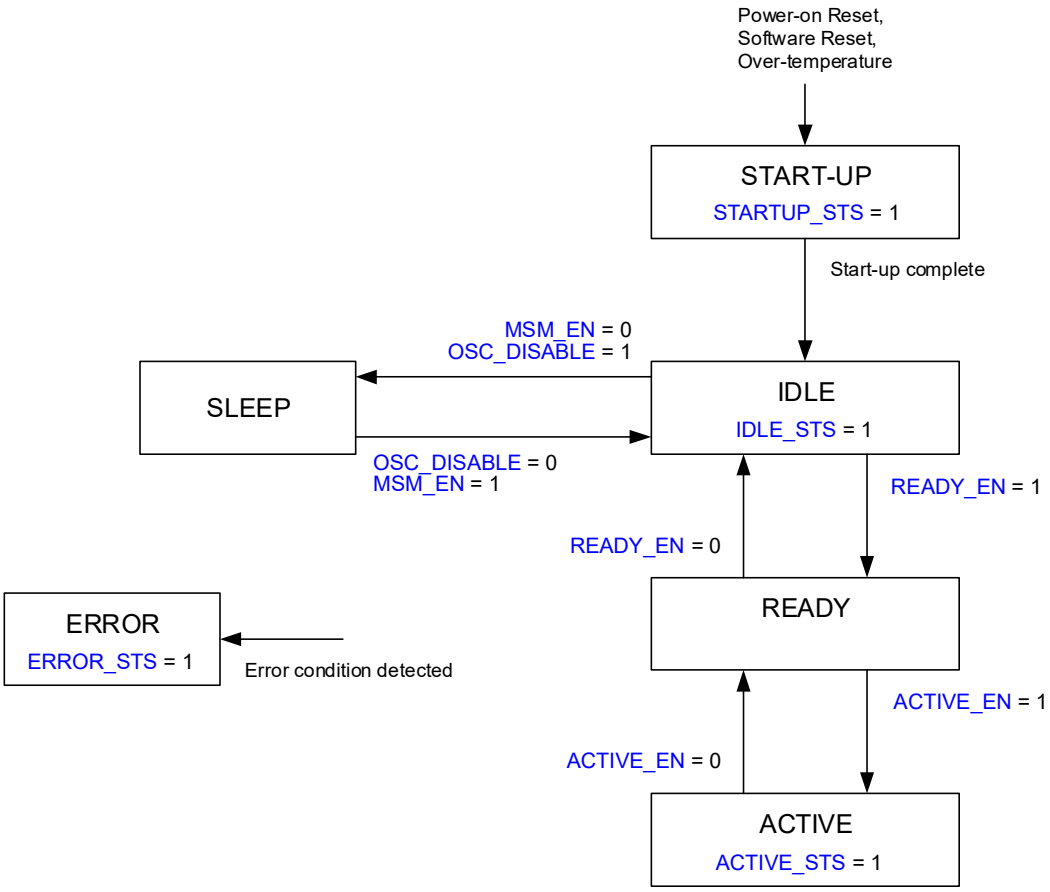


Figure 4-4. Operational States

The Start-Up State is indicated using STARTUP_STS. On successful completion of start-up, the device automatically transitions to the Idle State.

The Idle State is indicated using IDLE_STS. The CS82L41 is configured in the Idle State using the control interface (see Section 4.9). The transition from the Idle State to the Ready State is selected by setting READY_EN.

The Ready State is indicated using READY_STS. The transition from the Ready State to the Active State is selected by setting ACTIVE_EN.

The Active State is indicated using ACTIVE_STS. The transition from the Active State to the Ready State is selected by clearing ACTIVE_EN.

In the Ready State, the transition to the Idle State is selected by clearing READY_EN.

The Error State is selected if an error condition is detected; this is indicated using ERROR_STS. See Section 4.2.1 for further details.

The Sleep State is selected by clearing MSM_EN, then setting OSC_DISABLE. To exit the Sleep State, the host must clear OSC_DISABLE, then set MSM_EN. On exiting the Sleep State, the device transitions to the Idle State.

Note: The Sleep State should only be selected from the Idle State.

4.2.1 Error Conditions

If an error condition is detected, the error state is indicated using ERROR_STS. A more specific indication of the error is provided using the following fields.

- TEMP_ERROR_STS—Indicates an overtemperature error. In this event, an automatic reset shuts down all functions. The host must set TEMP_ERROR_CLR to return to the Idle State (provided the error has cleared). After returning to the Idle State, the host should then clear TEMP_ERROR_CLR.

  If TEMP_ERROR_RST_MASK is set, there is no reset following a temperature error; instead, there is a controlled shutdown of the analog path. The host must set TEMP_ERROR_CLR to return to the Idle State (provided the error has cleared). The host must also clear ACTIVE_EN and READY_EN. After returning to the Idle State, the host should then clear TEMP_ERROR_CLR.
- ACTIVE_ERROR_STS—Indicates an error in the Active or Ready state. The errors include clocking, AVDD absent, LDO error, and LED driver errors. The host must clear ACTIVE_EN and READY_EN to return to the Idle State (provided the error has cleared).
- STARTUP_ERROR_STS—Indicates a start-up error. This error can only be cleared by resetting the device.
- BOOT_ERROR_STS—Indicates a boot error. This error can only be cleared by resetting the device.
- MCLK_ERROR_STS—Indicates an invalid or absent MCLK in the Idle State. No corrective action is required by the host—the Ready State can be selected as usual, provided a valid MCLK has resumed.

4.3 MCLK Input

Clocking for the CS82L41 is provided using the MCLK_EXT input. The MCLK frequency must be a valid multiple of the pixel-sample rate; the supported frequency ratios are dependent on the selected output data format (see Section 4.5).

The supported frequency range for MCLK_EXT is described in Table 3-9.

4.4 Analog Input Path

The analog input path supports video input from an external sensor. The input path can be optimized to support a wide range of CIS and CCD sensors. A voltage reference (VBIAS) for the sensor can be generated internally on the CS82L41, or else can be provided from an external source.

The CS82L41 supports CDS and non-CDS sampling modes. For non-CDS operation, the video signal is sampled once per pixel. For CDS processing, two samples per pixel are used (reset level and video level); the correlated processing of these samples enables common-mode noise to be suppressed.

The clamp circuit allows the device to support video signals that exceed the maximum DC input voltage, and to align the video input to the VBIAS reference. Clamping can be applied during the reset portion of active scan pixels (pixel clamping) or else during black pixels outside the active scan periods (line clamping).

The input path can be optimized for different sensors using configurable offset, gain, and signal inversion. Different parameter values can be configured for different sequence states, allowing cyclic configuration for different phases of the scan pattern.

An overview of the analog input path is shown in Fig. 4-5.

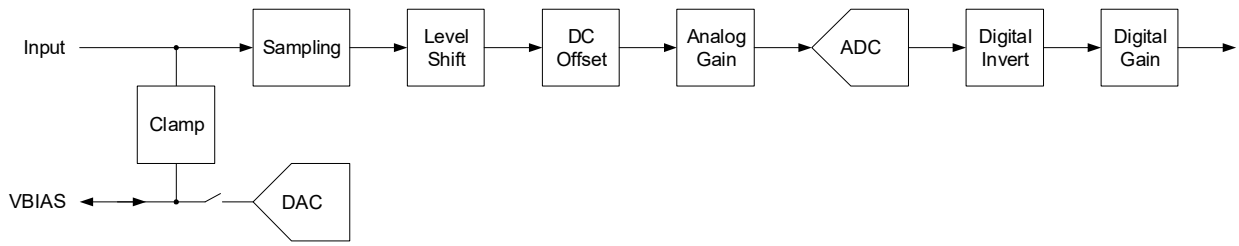


Figure 4-5. Analog Input Path

4.4.1 Input Sampling Mode

The CS82L41 supports a wide range of video input signals. Typical CIS and CCD sensor waveforms are shown in Fig. 4-6.

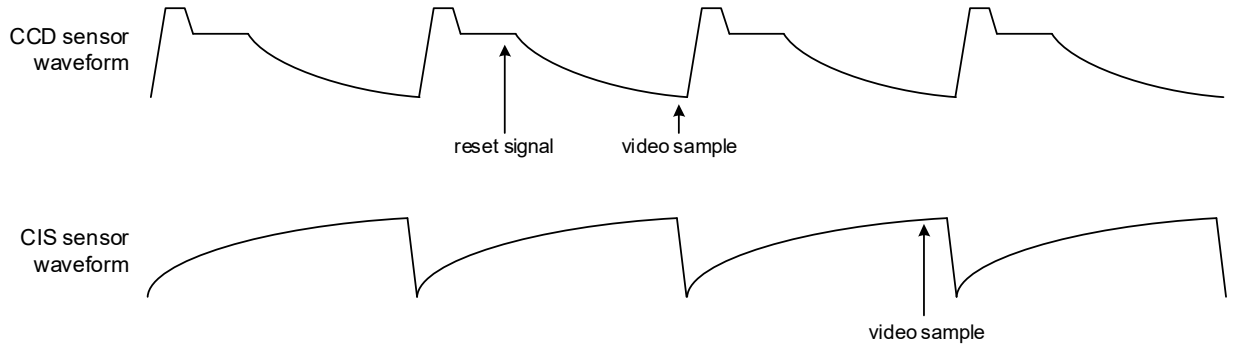


Figure 4-6. Typical CIS/CCD Waveforms

The analog input path can be configured in CDS or non-CDS sampling modes as follows:

- In CDS mode (CDS_EN = 1), the reset level and the video level are sampled for each pixel. This is typically used with CCD sensors, where the video waveform includes a reset level for each pixel. In CDS sampling mode, each video sample is measured relative to the reset level in the same pixel frame.
- In non-CDS mode (CDS_EN = 0), a single video-level sample is used for each pixel. This is typically used with CIS sensors, where the video waveform does not provide a reset level for each pixel. In this case, the video sample is measured relative to the VBIAS reference (see Section 4.4.2).

Note that both sampling modes (CDS or non-CDS) may be used with either type of sensor (CIS or CCD). The suitability of either sampling mode must be determined by the specific waveforms and timing constraints of the target application.

The analog input path can be configured for low-power operation, enabling power savings under suitable operating conditions. The default, high-performance configuration is recommended for pixel sample rates of 10 MHz and above. For slower sample rates, power consumption can be optimized using CH1_AFE_POWER.

4.4.2 Bias Voltage (VBIAS)

The CS82L41 provides a configurable voltage reference on the VBIAS pin; this is used as an input to the external sensor and as a reference for the analog input path. The VBIAS reference is required during active sampling. In non-CDS sampling mode, the bias voltage provides the reference level for the input-signal measurement. When the input clamp is active (see Section 4.4.3), the video input is clamped to the VBIAS reference.

The VBIAS reference is configured using the reset-level clamp (RLC) DAC. The bias is enabled using VBIAS_EN; the output voltage is configured using VBIAS_LVL.

The bias voltage should be configured within the operating conditions of the sensor. If input clamping is enabled, the bias should be set at the desired reset level, ensuring that both the reset level and the full-scale level are within the measurement range of the CS82L41 (see Section 4.4.3 for further details).

The drive strength of the bias is configurable using VBIAS_ISEL and VBIAS_ISEL_BOOST. The internal source for the bias reference is selected using VBIAS_REF; the VREF source is recommended in all cases.

Note: The bias voltage can also be provided externally. The RLC DAC must be disabled if an external reference source is connected to the VBIAS pin.

4.4.3 Clamp Control

The clamp provides a short circuit between the input signal and the VBIAS reference. The clamp is used with AC-coupled input to align the video signal within the measurable range of the CS82L41. The clamp enables video signals that exceed the full-scale input level to be accommodated; it can also be used to protect the input circuit from transient voltages that may arise during sensor start-up.

The full-scale input voltage is defined in Table 3-3. If the input signal (at the reset- or video-sample points) exceeds the full-scale level, the clamp must be used to offset the signal level within the permitted limit.

Note: The output from a CCD sensor typically includes transients that do not represent either the reset level or the video sample level; these transients do not need to lie within the measurable range. However, the absolute maximum rating of the input pins (see Table 3-2) must be observed at all times.

If the clamp is used, the input must be AC-coupled using a capacitor on the input pin as shown in Section 2. If the clamp is not used, the DC-coupled configuration is recommended (i.e., without a capacitor).

The clamp operation must be timed to coincide with the input reset signal, in order to align the reset (black) level with the VBIAS reference. To ensure correct behavior, the input voltage must be a constant level while the clamp is active.

- In CDS mode, the clamp can be applied during the reset portion of active scan pixels (pixel clamping).
- In non-CDS mode, the clamp is typically used during black pixels outside the active scan periods (line clamping).

The clamp circuit is illustrated in Fig. 4-7. The clamp is used with the VBIAS reference to adjust the video signal level within the operating limits of the CS82L41.

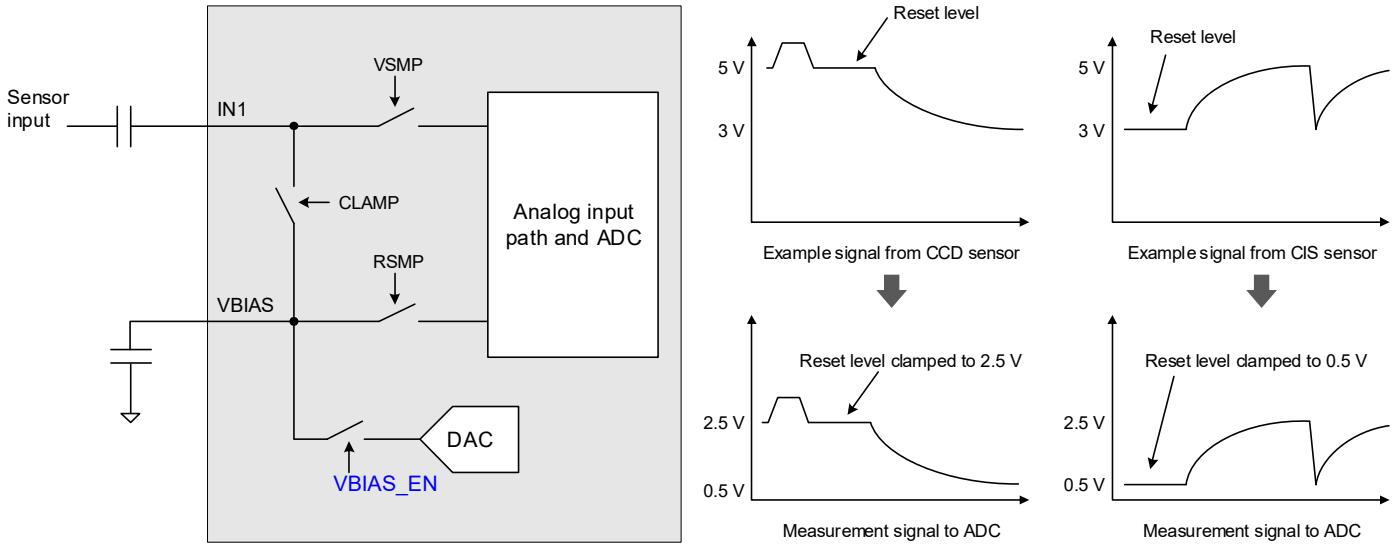


Figure 4-7. Input Clamp

The clamp function is enabled by setting CLAMP_EN. The CLAMP_MODE field is used to select when clamping is applied.

- If CLAMP_MODE = 0, clamping is enabled for all pixels.
- If CLAMP_MODE = 1, clamping is enabled if RSMP_EXT is asserted (Logic 1). The RSMP_EXT function is supported on two different multifunction pins—RSMP_EXT1 or RSMP_EXT2. The applicable pin must be configured for the RSMP input as described in Section 4.10.

  Note this option is not valid if CDS sampling is enabled in Timing Mode 1 (see Section 4.6).

During pixels where clamping is enabled (and the applicable CLAMP_MODE condition is met), the clamp is applied for a portion of the respective pixel frames. In CDS mode, the clamp is applied while RSMP is asserted; in non-CDS mode, the clamp is applied while VSMP is not asserted. See Section 4.6 for further details of the VSMP and RSMP signals.

The clamp timing in CDS mode is illustrated in Fig. 4-8.

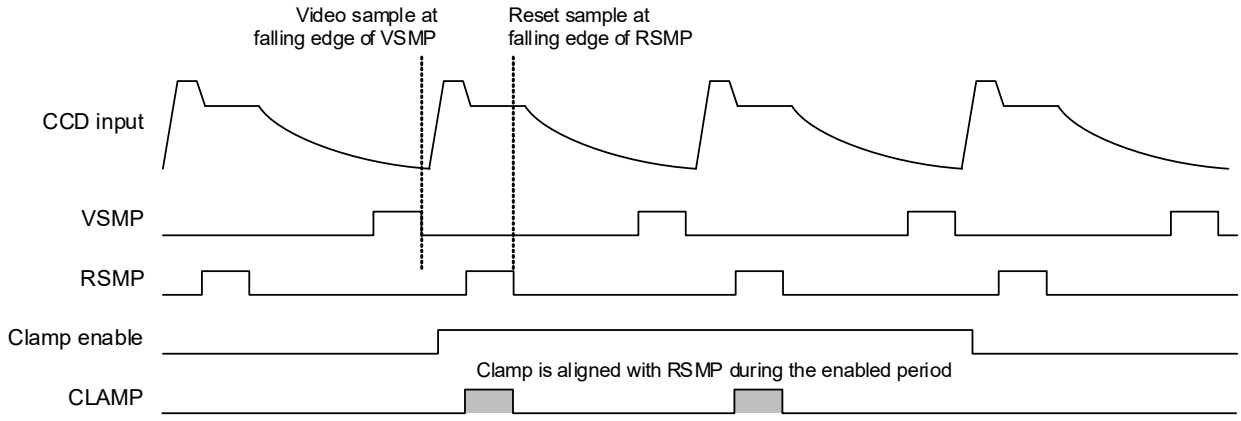


Figure 4-8. Clamp Timing (CDS Mode)

The clamp timing in non-CDS mode is illustrated in Fig. 4-9.

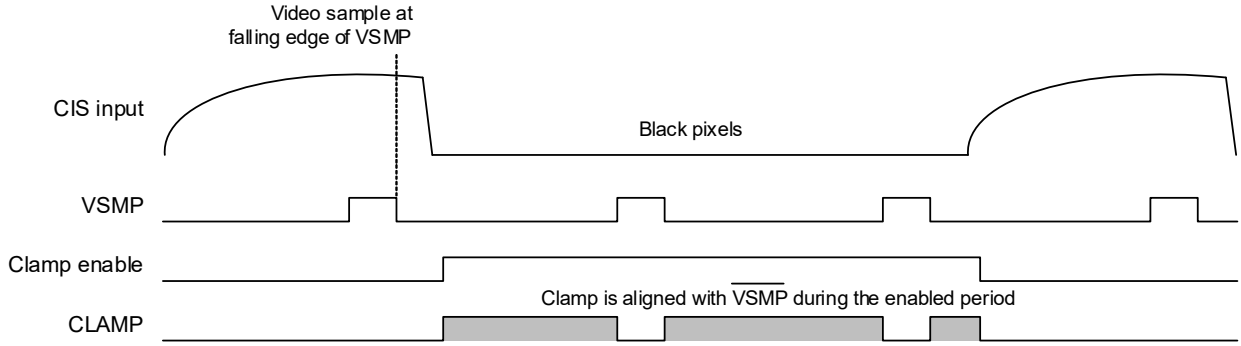


Figure 4-9. Clamp Timing (Non-CDS Mode)

The clamp can also be enabled using CLAMP_OVRD. If this bit is set, the input clamp is enabled continuously until the bit is cleared. This can be used to protect the input circuits from transient voltages that may arise during sensor start-up.

4.4.4 Polarity Select

The analog input path provides selectable polarity control; this can be used to accommodate different types of sensor waveform. The polarity of the sensor waveforms are defined as follows:

- For a CCD-type waveform, the reset level is higher than the video sample level; this is inverted polarity.
- For a CIS-type waveform, the reset level is lower than the video sample level; this is non-inverted polarity.

The full-scale signal level for the input path is 2.4 V pk-pk (see Table 3-3). The input signal is measured relative to the VBIAS/reset level, as described in Section 4.4.1.

The analog input path must be configured for the polarity of the input waveform. If inverted polarity is selected, the waveform is level-shifted so the reset-level signal is measured around 2.4 V. If non-inverted polarity is selected, there is no level shift, and the reset-level is measured around 0 V.

Note: The level shift can be combined with additional DC offset as described in Section 4.4.5.

The polarity selection is illustrated in Fig. 4-10 for typical CCD and CIS sensor waveforms. The inverted CCD waveform is level-shifted to the 2.4 V level. The non-inverted CIS waveform is unaffected.

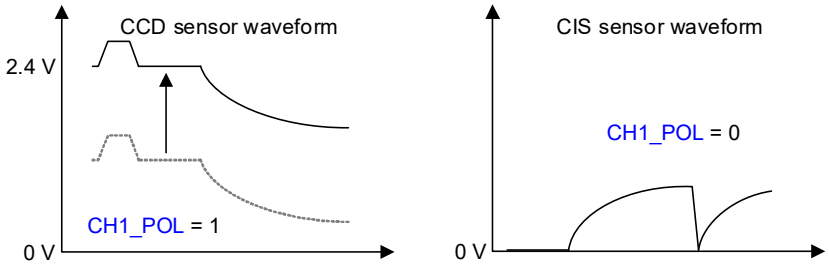


Figure 4-10. Polarity Select

The polarity is configured using CH1_POL.

4.4.5 Offset Control

The offset provides DC adjustment to the analog input signal. The offset can be either positive or negative, and can be used to optimize the input path for the video signal.

The offset is illustrated in Fig. 4-11 for typical CCD and CIS sensor waveforms.

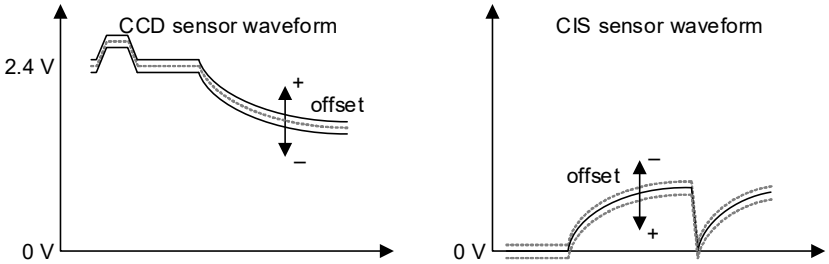


Figure 4-11. Offset Control

The offset can be set in the range –333 mV to +333 mV. The offset is applied differently depending on whether the signal path is inverted (see Section 4.4.4):

- If the signal path is inverted (CH1_POL = 1), the offset is added to signal voltage—a positive offset increases the output voltage, and a negative offset decreases the output voltage.
- If the signal path is not inverted (CH1_POL = 0), the offset is subtracted from the signal voltage—a positive offset decreases the output voltage, and a negative offset increases the output voltage.

The offset is associated with the sequence state, allowing different offsets to be applied automatically according to the current state (see Section 4.7.1 for details of the sequence state).

The offset is configured using CH1_SEQn_OFFSET (where *n* is 0–3 for the respective sequence state).

The auto-cycle function is enabled using ACYC_EN. If auto-cycle is enabled, the offset is determined by the current sequence state. If auto-cycle is disabled, IN_SEQ_SEL is used to select which sequence-state offset should be applied.

4.4.6 Analog Gain Control

The analog gain provides control of the input signal amplitude. The analog gain can be used to optimize the input signal to match the measurable range of the ADC.

The analog gain is illustrated in Fig. 4-12 for typical CCD and CIS sensor waveforms.

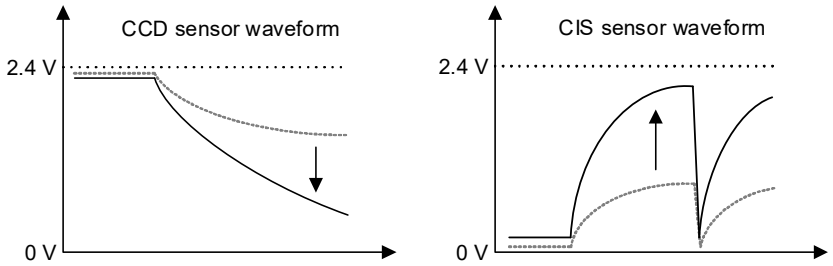


Figure 4-12. Analog Gain

The analog gain is associated with the sequence state, allowing different gain settings to be applied automatically according to the current state.

The analog gain is configured using CH1_SEQn_AGAIN (where *n* is 0–3 for the respective sequence state).

The auto-cycle function is enabled using ACYC_EN. If auto-cycle is enabled, the gain is determined by the current sequence state. If auto-cycle is disabled, IN_SEQ_SEL is used to select which sequence-state gain should be applied.

4.4.7 Analog to Digital Converter (ADC)

The input path incorporates a high-performance analog-to-digital converter (ADC). The ADC is configured automatically and does not require any user configuration.

4.4.8 Digital Invert

The input path accommodates sensor waveforms of inverted or non-inverted polarity, as described in Section 4.4.4. The digital invert is used to ensure the ADC output is a standardized polarity for all signal types, i.e., the reset (black) signal level is a lower numerical value than the full-scale (white) signal level.

The digital invert is configured automatically to align with the selected polarity of the analog input.

The digital invert is illustrated in Fig. 4-13 for typical CCD and CIS sensor waveforms. The inverted CCD waveform is adjusted so the reset (black) signal level is towards the zero end of the digital range. The non-inverted CIS waveform is unaffected.

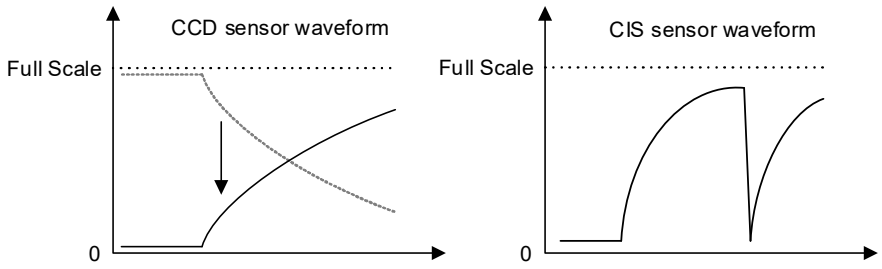


Figure 4-13. Digital Invert

4.4.9 Digital Gain Control

The digital gain provides control of the digital output scaling. In typical applications, the digital gain is configured to set the highest signal level close to the full-scale digital level.

The digital gain is illustrated in Fig. 4-14 for typical CCD and CIS sensor waveforms.

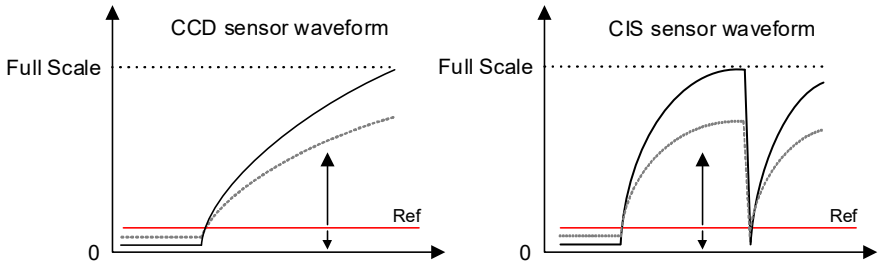


Figure 4-14. Digital Gain

The digital gain is associated with the sequence state, allowing different gain settings to be applied automatically according to the current state.

The digital gain is configured using CH1_SEQn_DGAIN (where *n* is 0–3 for the respective sequence state). The output data is scaled according to the selected gain. The output is scaled relative to the reference level CH1_SEQn_DGAIN_REF as shown in Fig. 4-14; this can be used to reduce the reset-level offset while also maximizing the signal amplitude.

The auto-cycle function is enabled using ACYC_EN. If auto-cycle is enabled, the gain is determined by the current sequence state. If auto-cycle is disabled, IN_SEQ_SEL is used to select which sequence-state gain should be applied.

4.4.10 Test Pattern Generator

The CS82L41 incorporates a test pattern generator, which can be used for debug purposes. The test pattern allows the digital output to be verified without any analog input required.

If the test pattern is enabled, the analog input path is bypassed. Note that other required functions must be configured as for normal operation, including the external clock reference and VSMP/RSMP timing signals.

The test pattern is enabled using TEST_PATT_EN. If the test pattern is enabled, the output data ramps continually through the full 16-bit range of digital output codes. The data is incremented/decremented for each pixel. The ramp direction is selectable using TEST_PATT_DIR.

The pattern should be configured and enabled while in the Idle State. The digital output is generated after transitioning to the Active State. The Idle State should be selected before disabling or reconfiguring the pattern.

4.5 Digital Output Format

The CS82L41 provides single-ended data output, over a maximum of four data lines, DOUTn. Signal timing is referenced to the external clock input (on the MCLK_EXT pin). The data output is supported in single- or double-rate formats:

- In single-data-rate (SDR) formats, the data bit rate is equal to the MCLK rate
- In double-data-rate (DDR) formats, the data bit rate is 2 × MCLK rate

The data output format is illustrated in Fig. 4-15. See Table 3-18 for timing specifications.

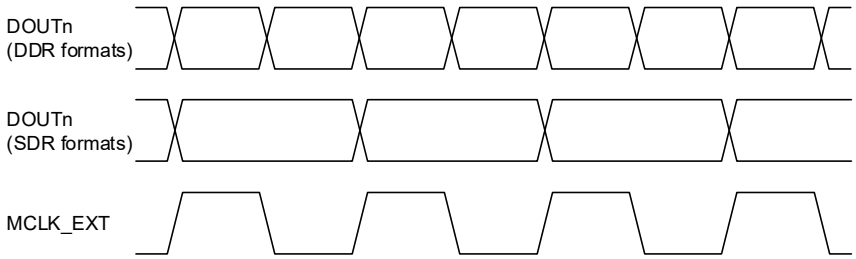


Figure 4-15. Data Output Format

The data output can be supported on four data lines (DOUT1–DOUT4) or two data lines (DOUT1–DOUT2); the number of data lines is selected using DOUT_CONFIG. The data output is configured in SDR or DDR format using DOUT_DDR.

The format is configurable using DOUT_PHASE, allowing the data output to be referenced to either the rising or falling edge of the MCLK input.

The latency of the output data from the VSMP_EXT trigger signal is described in Section 4.6.1 and Section 4.6.2. Additional delay can be configured using DOUT_DLY.

The MCLK frequency is a multiple of the pixel-sample rate; the frequency ratio can be chosen according to the selected output format and the required number of data bits per sample. Valid MCLK ratios for different use cases are noted in Table 4-1.

Table 4-1. MCLK Frequency Ratio

Number of Data Lines	Data Rate	Minimum MCLK Ratio		
		16-bit	12-bit	8-bit
Four	Single	4	3	2
	Double	2	—	—
Two	Single	8	6	4
	Double	4	3	2

The data output formats are illustrated in Fig. 4-16 through Fig. 4-19. The examples show 16-bit data, referenced to the rising MCLK edge. If the MCLK frequency ratio is reduced, the data samples are truncated as described in Table 4-1. If the ratio is increased, the LSBs of each sample are maintained through the additional MCLK cycles.

The four-line SDR data output is illustrated in Fig. 4-16.

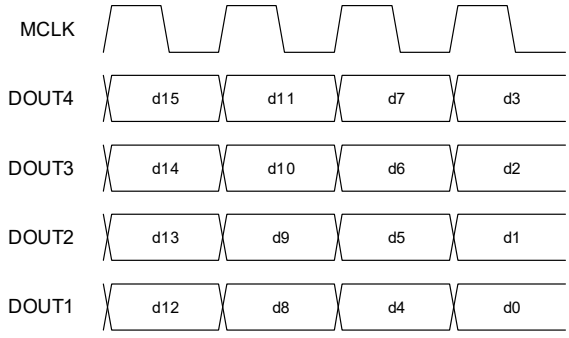


Figure 4-16. Four-line SDR Data Output

The four-line DDR data output is illustrated in Fig. 4-17.

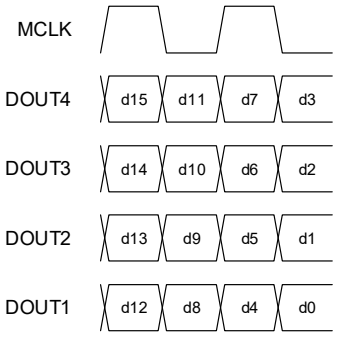


Figure 4-17. Four-line DDR Data Output

The two-line SDR data output is illustrated in Fig. 4-18.

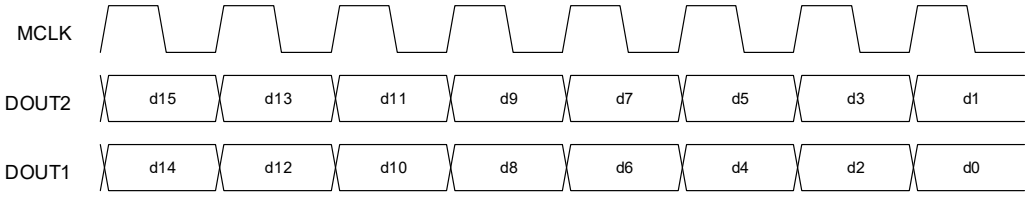


Figure 4-18. Two-line SDR Data Output

The two-line DDR data output is illustrated in Fig. 4-19.

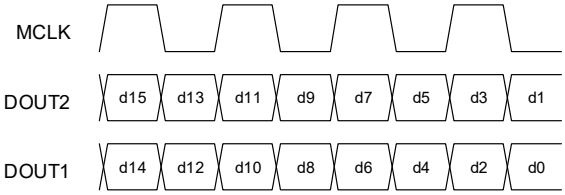


Figure 4-19. Two-line DDR Data Output

4.6 Sample Timing Control

The CS82L41 supports CDS and non-CDS sampling modes. CDS refers to correlated double-sampling—in CDS mode, the reset level and the video level are sampled for each pixel; in non-CDS mode, a single video-level sample is used for each pixel. The sampling mode is configured using CDS_EN.

The sample timing is controlled by the internal VSMP and RSMP signals—the video level is sampled on the falling edge of VSMP; the reset level is sampled on the falling edge of RSMP.

Note: The RSMP signal is used in CDS sampling mode only. RSMP is not used in non-CDS sampling mode.

The ADC sample/conversion timing is controlled by the AFECK signal. The rising edge of AFECK occurs after the falling edge of VSMP. The AFECK signal must be optimized according to the application requirements, to ensure correct sequencing of the associated functions.

Sample timing is controlled using external hardware inputs. The external signals can be configured to trigger the internal VSMP and RSMP signals directly, or can be retimed to align with the MCLK reference input. The AFECK timing is configured with reference to the MCLK input.

To assist in debug and timing set-up, the VSMP, RSMP, and AFECK signals can be monitored externally as described in Section 4.11.

The CDS timing for a typical CCD-sensor video signal is shown in Fig. 4-20.

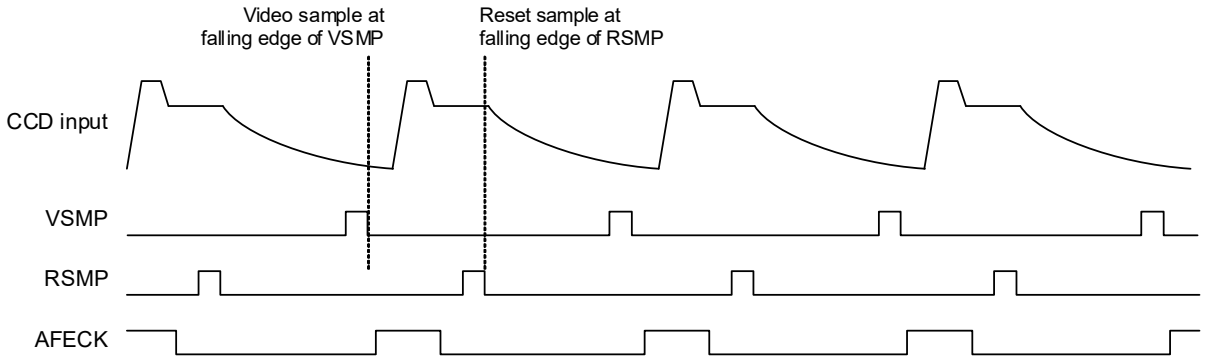


Figure 4-20. Sample Timing Control (CDS Mode)

The non-CDS timing for a typical CIS-sensor video signal is shown in Fig. 4-21.

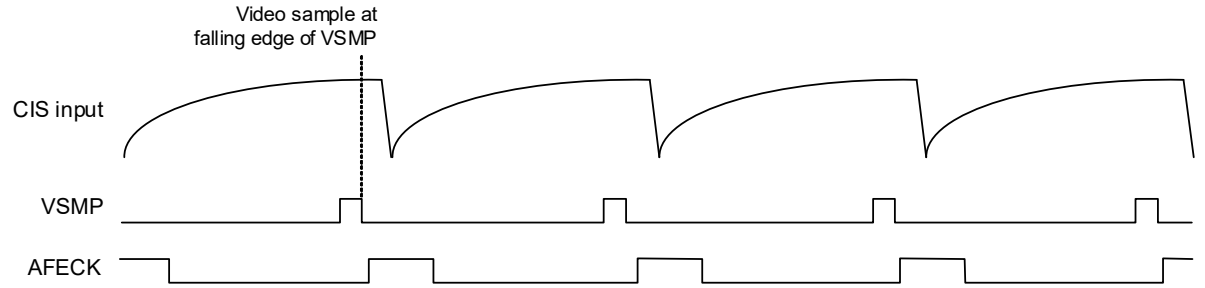


Figure 4-21. Sample Timing Control (non-CDS Mode)

4.6.1 Direct Pin Trigger (Timing Mode 1)

In Timing Mode 1, the VSMP and RSMP signals are controlled directly using external hardware inputs. The video sample is triggered on the falling edge of VSMP_EXT; the reset-level sample is triggered on the falling edge of RSMP_EXT.

Timing Mode 1 is selected if TIMING_MODE = 0.

The rising edge of AFECK occurs on the first MCLK rising edge after the VSMP falling edge. The falling edge of AFECK is configured using AFECK_DUR to define the duration of the AFECK pulse.

The timing constraints in Table 3-11 must be observed when controlling VSMP and RSMP directly from the external pins. A minimum pulse duration is specified for each signal; it is recommended to configure the shortest possible AFECK pulse within the defined limits. The VSMP, RSMP, and AFECK pulses must not overlap.

Note: The RSMP signal is used in CDS sampling mode only. If CDS_EN = 0, the RSMP timing constraints do not apply.

The RSMP_EXT function is supported on two different multifunction pins—RSMP_EXT1 or RSMP_EXT2. The applicable pin must be configured for the RSMP input as described in Section 4.10.

The direct-pin trigger is illustrated in Fig. 4-22.

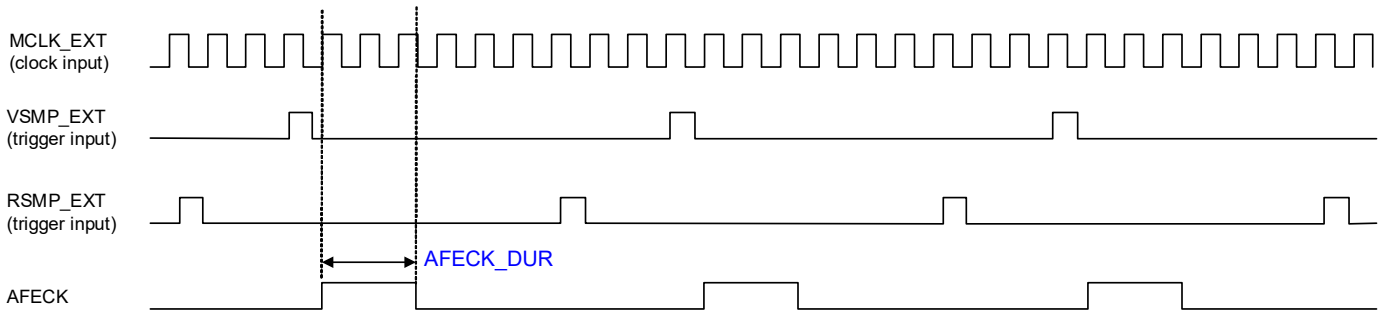


Figure 4-22. Direct-Pin Trigger (Timing Mode 1)

The data output is formatted as described in Section 4.5. The latency of the output (measured in MCLK cycles) is defined in Table 4-2, according to the selected data format.

Table 4-2. Data Output Latency

Leading Edge [1]	Data Rate [2]	Output Latency [3,4]
Positive	Single	((7 + *Delay*) x *MCLK cycles per pixel*) + 2
	Double	((7 + *Delay*) x *MCLK cycles per pixel*) + 2
Negative	Single	((7 + *Delay*) x *MCLK cycles per pixel*) + 1.5
	Double	((7 + *Delay*) x *MCLK cycles per pixel*) + 2.5

1. The leading edge is configured using DOUT_PHASE.
2. The data rate is configured using DOUT_DDR.
3. *Delay* is configured in the range 0–3 using DOUT_DLY.
4. *MCLK cycles per pixel* is the ratio of the MCLK frequency to the VSMP rate.

The latency is defined from the rising edge of AFECK (i.e., the first MCLK rising edge after the VSMP falling edge), as shown in Fig. 4-23.

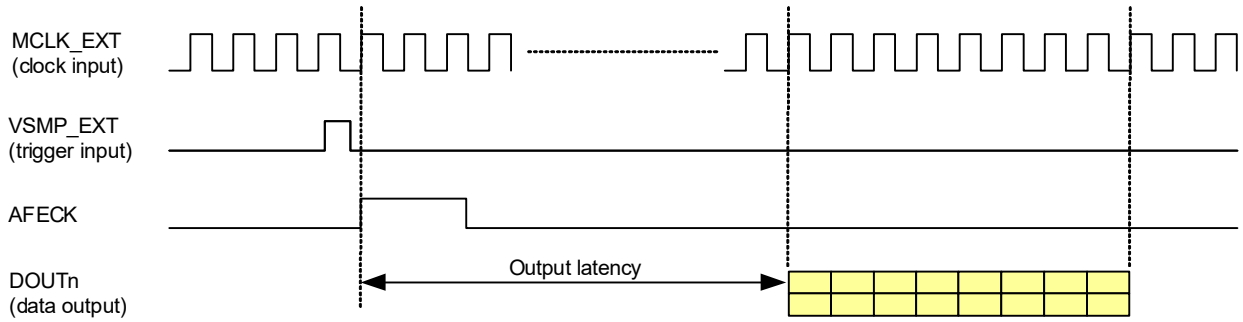


Figure 4-23. Data Output Latency (Timing Mode 1)

4.6.2 MCLK-Aligned Trigger (Timing Mode 2)

In Timing Mode 2, the VSMP, RSMP, and AFECK signals are controlled using the VSMP_EXT pin as the trigger. The active edge of the trigger (rising or falling) is selectable. The internal signals are retimed to align with the MCLK input; this can be used to ensure the internal pulses do not exceed a minimum duration, regardless of the external trigger.

Timing Mode 2 is selected if TIMING_MODE = 1.

The active edge of the VSMP_EXT trigger (rising or falling) is configured using VSMP_EXT_POL.

The MCLK-aligned signals are configured as follows:

- The VSMP timing is controlled using VSMP_EXT_DLY to select the number of MCLK cycles between the active VSMP_EXT edge and the rising edge of VSMP. The falling edge of VSMP is one MCLK cycle after the rising edge.
- The RSMP timing is controlled using RSMP_EXT_DLY to select the number of MCLK cycles between rising edge of VSMP and the rising edge of RSMP. The falling edge of RSMP is one MCLK cycle after the rising edge.
- The rising edge of AFECK occurs at the same time as the VSMP falling edge. The falling edge of AFECK is configured using AFECK_DUR to define the duration of the AFECK pulse.

The rising edge of VSMP is configured as described above. The rising edge is delayed by a number of MCLK cycles—if a delay of n cycles is selected, the rising edge of VSMP occurs on the n-th rising edge of MCLK after the rising edge of the VSMP_EXT signal.

The timing constraints in Table 3-12 must be observed when configuring the phase offset of VSMP, RSMP, and AFECK. It is recommended to configure the shortest possible AFECK pulse within the defined limits. The VSMP, RSMP, and AFECK pulses must not overlap.

Note: The RSMP signal is used in CDS sampling mode only. If CDS_EN = 0, there is no requirement to configure RSMP, and the associated timing constraints do not apply.

The MCLK-aligned trigger is illustrated in Fig. 4-24.

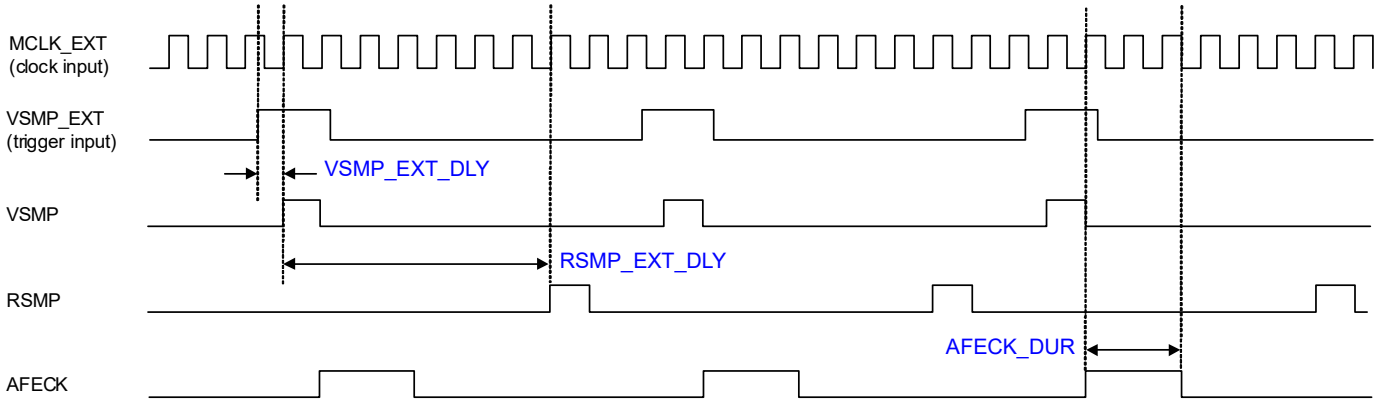


Figure 4-24. MCLK-Aligned Trigger (Timing Mode 2)

The data output is formatted as described in Section 4.5. The latency of the output (measured in MCLK cycles) is defined in Table 4-3, according to the selected data format.

Table 4-3. Data Output Latency

Leading Edge [1]	Data Rate [2]	Output Latency [3,4]
Positive	Single	((7 + *Delay*) x *MCLK cycles per pixel*) + 2
	Double	((7 + *Delay*) x *MCLK cycles per pixel*) + 2
Negative	Single	((7 + *Delay*) x *MCLK cycles per pixel*) + 1.5
	Double	((7 + *Delay*) x *MCLK cycles per pixel*) + 2.5

1. The leading edge is configured using DOUT_PHASE.
2. The data rate is configured using DOUT_DDR.
3. *Delay* is configured in the range 0–3 using DOUT_DLY.
4. *MCLK cycles per pixel* is the ratio of the MCLK frequency to the VSMP rate

The latency is defined from the rising edge of AFECK (i.e., the internal VSMP falling edge), as shown in Fig. 4-25.

Note the latency is defined from the internal VSMP/AFECK signals. The additional latency from the active VSMP_EXT edge to the internal VSMP pulse is configurable using VSMP_EXT_DLY.

The data output latency is illustrated in Fig. 4-25.

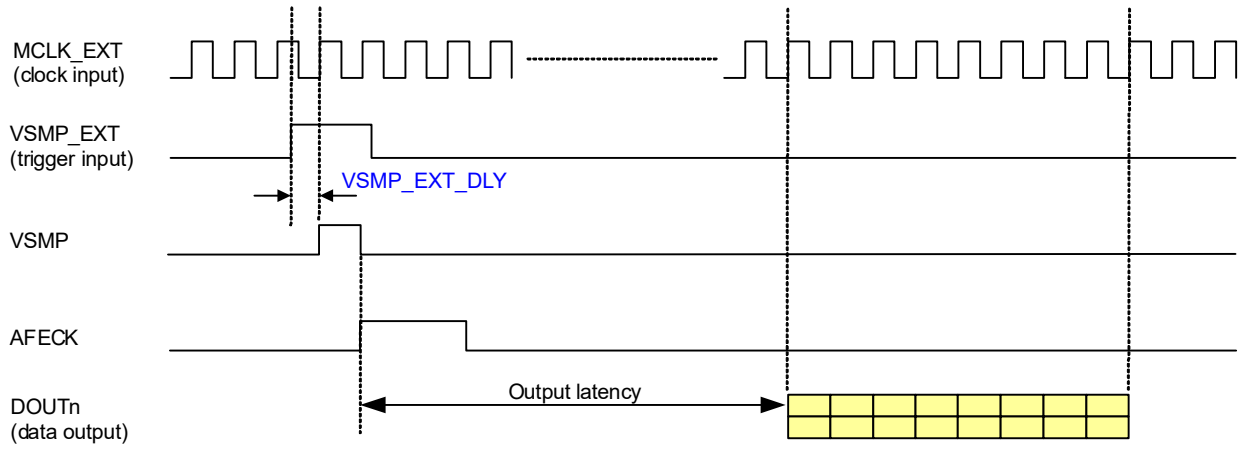


Figure 4-25. Data Output Latency (Timing Mode 2)

4.7 TG Sync and Sequence State Control

The video input signal is sampled on the falling edge of VSMP, as described in Section 4.6. In typical applications, the samples represent pixels within a scan pattern; blocks of samples represent successive lines, or different scan colors, within the scan pattern.

The scan pattern can be referenced to a sequence-state parameter, supporting a maximum of four sequential states. Each state represents a different portion of the scan pattern; this can be used to reconfigure the input path for different scan colors, or other functions, for the respective portions of the scan.

The TG Sync input is used to control the sequence state. The sync signal may indicate the start of each scan line, or may signal intermediate stages within a scan line. The LEDSTART input may also be used, in conjunction with TG Sync signal.

4.7.1 Sequence State

The number of sequence states is configured using NUM_SEQ_STATES. A maximum of four states is supported.

The current sequence state is indicated in SEQ_STATE_STS.

The input-path configuration (PGA gain, DC offset, digital gain) can be defined for each sequence state as described in Section 4.4. The LED drivers can be configured for each sequence state as described in Section 4.8.1.

4.7.2 TG Sync Control

The TG Sync input is used to trigger the sequence-state transitions. Optionally, this can be used in conjunction with the LEDSTART signal to provide additional control of the sequence states.

The TGSYNC_SINGLE_SEQ bit selects whether the TG Sync triggers a cycle of multiple state transitions (Multiple Mode) or triggers a single state transition only (Single Mode).

- In Multiple Mode (TGSYNC_SINGLE_SEQ = 0), the TG Sync indicates the start of State 0. The transition to the next sequence state occurs automatically after the required number of pulse cycles for the current state (configured using LED_SEQn_END—see Section 4.8.1). At the end of the configured number of sequence states, the current state is maintained until TG Sync signal indicates the start of the next cycle (i.e., State 0).

  If TG Sync is asserted before the end of the configured number of sequence states, the device behavior depends on TGSYNC_SEQ_RST. If this bit is clear, the ‘early’ TG Sync is ignored. If this bit is set, the TG Sync resets the sequence to the start of the next cycle (i.e., State 0).

- In Single Mode (TGSYNC_SINGLE_SEQ = 1), the TG Sync indicates the start of each sequence state. The transition to the next sequence state occurs when a valid TG Sync pulse is detected. At the end of the configured number of sequence states, the next TG Sync indicates the start of the next cycle (i.e., State 0).

  The state transition occurs at each TG Sync pulse, regardless of the number of pulse cycles configured for the LED drivers (see Section 4.8.1). Note there is no option to suppress an 'early' TG Sync as in Multiple Mode.

The LEDSTART_SEQ_INIT bit selects whether the LEDSTART signal is used (in conjunction with TG Sync) to indicate the start of State 0. If this bit is clear, the sequence-state transitions are controlled using only the TG Sync input. If this bit is set, the LEDSTART and TG Sync signals must both be asserted to restart the sequence in State 0.

The TG Sync input is supported on two different pins—TGSYNC or LEDSTART. The applicable input is selected using TGSYNC_IN_SRC. The polarity of the selected input is configured using TGSYNC_IN_POL. The TG Sync input is timed with reference to the MCLK signal as shown in Table 3-13; the active MCLK edge is selected using MCLK_SYNC_POL.

A filter can be applied to the selected TG Sync input, to avoid erroneous triggers. The filter is enabled using TGSYNC_FILT_EN. The external signal is sampled at the pixel rate, and decimated at a rate selected by TGSYNC_FILT_DECM. The decimated input is tested for a valid transition using the TGSYNC_FILT_STAGE field; for example, if a 6-stage filter is selected, a valid rising edge is detected if a 0–0–0–1–1–1 sequence is detected in the decimated input signal. See Section 4.7.2.1 for additional timing requirements if the filter is enabled.

If LEDSTART_SEQ_INIT is set, LEDSTART indicates the start of State 0. In this configuration, the polarity of the LEDSTART input is selected using LEDSTART_POL. The LEDSTART input is timed with reference to the MCLK signal as shown in Table 3-13; the active MCLK edge is selected using MCLK_SYNC_POL.

The TG Sync and LEDSTART functions are supported on multifunction pins, which must be configured for the required functions as described in Section 4.10.

Multiple-cycle operation with four sequence states is illustrated in Fig. 4-26. The TG Sync pulse triggers the cycle of four sequence states. The sequence state is initialized in State 0 on each TG Sync pulse.

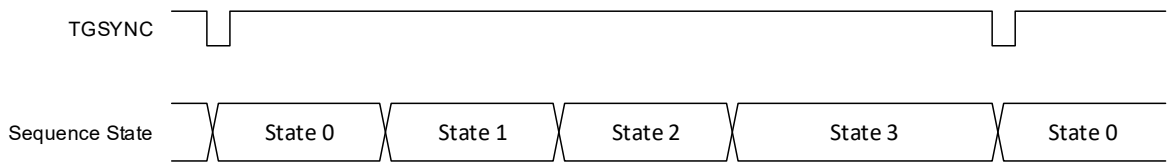


Figure 4-26. Multiple Cycle, TGSYNC Trigger

Single-cycle operation with four sequence states is illustrated in Fig. 4-27. The TG Sync pulse is used to control each sequence-state transition. At the end of the last state, the sequence state returns to State 0.

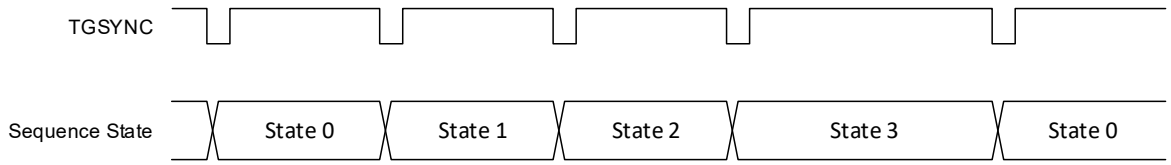


Figure 4-27. Single Cycle, TGSYNC Trigger

Multiple-cycle operation with four sequence states is illustrated in Fig. 4-28. The LEDSTART and TG Sync pulses (together) trigger the cycle of four sequence states. The sequence state is initialized in State 0 on each trigger event.

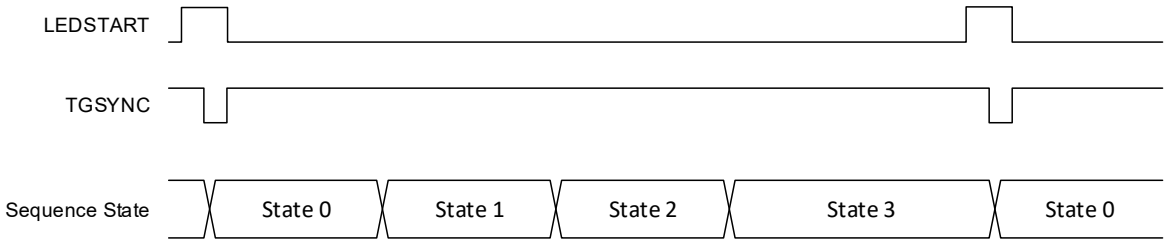


Figure 4-28. Multiple Cycle, LEDSTART + TGSYNC Trigger

Single-cycle operation with four sequence states is illustrated in Fig. 4-29. The TG Sync pulse is used to control each sequence-state transition. The sequence state is initialized in State 0 using LEDSTART and TG Sync together.

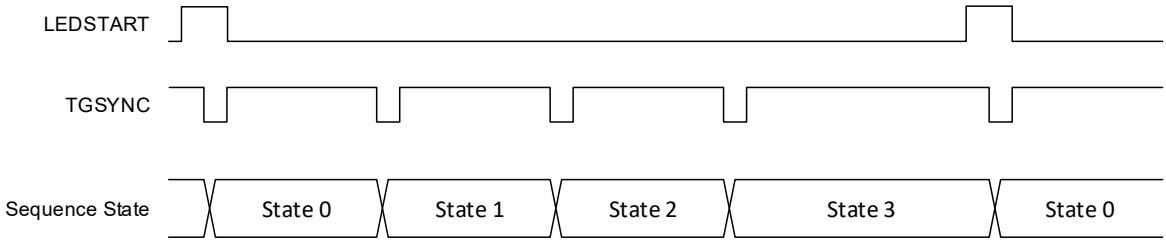


Figure 4-29. Single Cycle, LEDSTART + TGSYNC Trigger

4.7.2.1 TGSYNC and LEDSTART Signal Timing

The TGSYNC signal is used to trigger the sequence-state transitions. Optionally, LEDSTART can be used to control the transition that restarts the sequence in State 0. The signals must conform to the applicable timing requirements.

- The TGSYNC and LEDSTART timing requirements are defined in Table 3-13. Note these requirements assume the TGSYNC filter is disabled.
- If the TGSYNC filter is enabled (TGSYNC_FILT_EN = 1), the TGSYNC minimum pulse width is defined by the following equation:

  $$(Filter\ Stages \times Decimation\ Ratio / 2) \quad \text{MCLK cycles}$$

  where *Filter Stages* is the number of filter stages selected by TGSYNC_FILT_STAGE and *Decimation Ratio* is the ratio selected by TGSYNC_FILT_DECM.

  If the LEDSTART input is used (LEDSTART_SEQ_INIT = 1), the LEDSTART pulse duration must be larger than the TGSYNC pulse, as illustrated in Fig. 4-30.

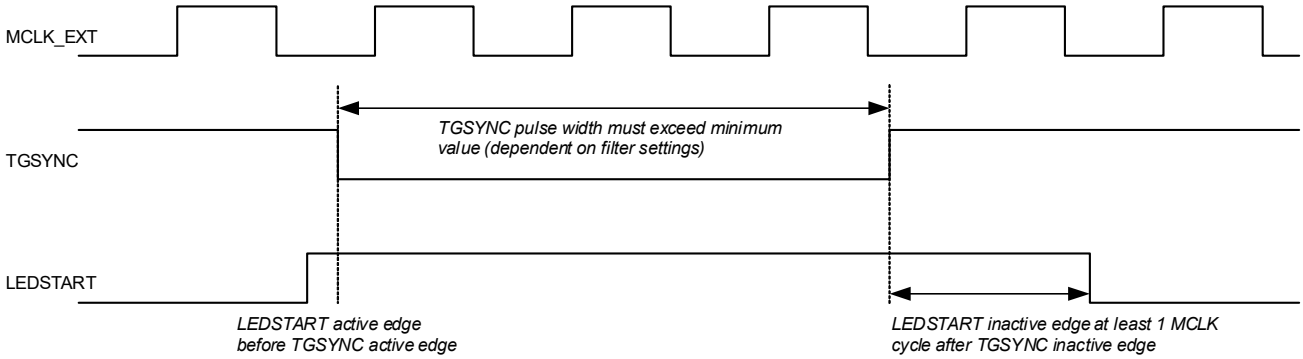


Figure 4-30. TGSYNC/LEDSTART Timing—TGSYNC Filter Enabled

4.8 LED Driver Control

Three current-sink LED drivers are provided, supporting independently programmable control. The three-channel controller is typically used to drive red, green, and blue LED outputs. White LEDs can also be supported. The LED drivers can be enabled using dedicated hardware pins, or else using an internal pulse waveform derived from a clock counter and the sequence state.

Note: The LED drivers are only supported if a valid VSMP signal is present. See Section 4.6 for further details of VSMP.

The LED control functions are enabled using LEDR_EN, LEDG_EN, and LEDB_EN for the red, green, and blue channels respectively.

The control source for the LED drivers is selected using LED_CTRL_SRC. The selection applies to all LED channels.

- If the hardware pin is selected, the LED is enabled if the respective pin is asserted high (Logic 1). The switching edges are synchronized to the MCLK_EXT clock input in order to reduce asynchronous noise in the system.

  The LED control inputs are supported on multifunction pins, which must be configured for the respective function as described in Section 4.10.
- If internal control is selected, the LED is enabled using the LED_CLK pulse waveform. The LED_CLK signal is configurable for different sequence-state conditions as described in Section 4.8.1.

The external connections for the LED drivers are illustrated in Fig. 4-31. An external resistor, connected to ILED_CTRL, is used to calibrate the output current of the LED drivers.

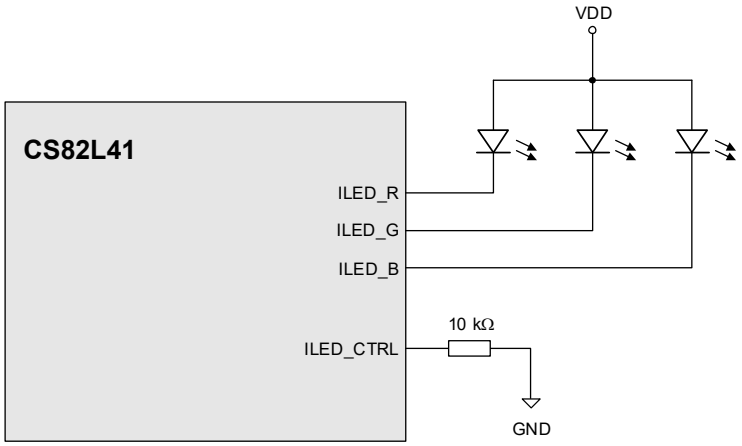


Figure 4-31. LED Output Drivers

4.8.1 Internal Timing Control (LED_CLK)

If the internal control source is selected, the LED drivers are enabled using the LED_CLK pulse waveform. The LEDs are enabled for a selected number of pulse cycles in each sequence state; different duty cycle and timing patterns can be configured according to the current sequence state.

The LED_CLK signal is derived using a division of the MCLK frequency, configured using LED_CLK_DIV. The divided MCLK controls the resolution (or step size) of the LED_CLK period and duty-cycle parameters.

The LED_CLK period is configured for each sequence state using LED_SEQn_PERIOD (where *n* is 0–3 for the respective sequence state). The LED_CLK duty cycle is configured using LED_SEQn_DUTY.

The LED drivers are enabled for selected pulse cycles in each sequence state. The LED_SEQn_START field selects the first pulse cycle in which the LED driver is enabled for the respective state; the LED_SEQn_END field configures the last pulse cycle in which the LED driver is enabled.

The LED drivers can be selectively enabled for individual sequence states using LEDx_SEQ_SEL. Each bit within these fields enables the LED driver in the corresponding state.

The LED_CLK signal and LED timing are illustrated in Fig. 4-32.

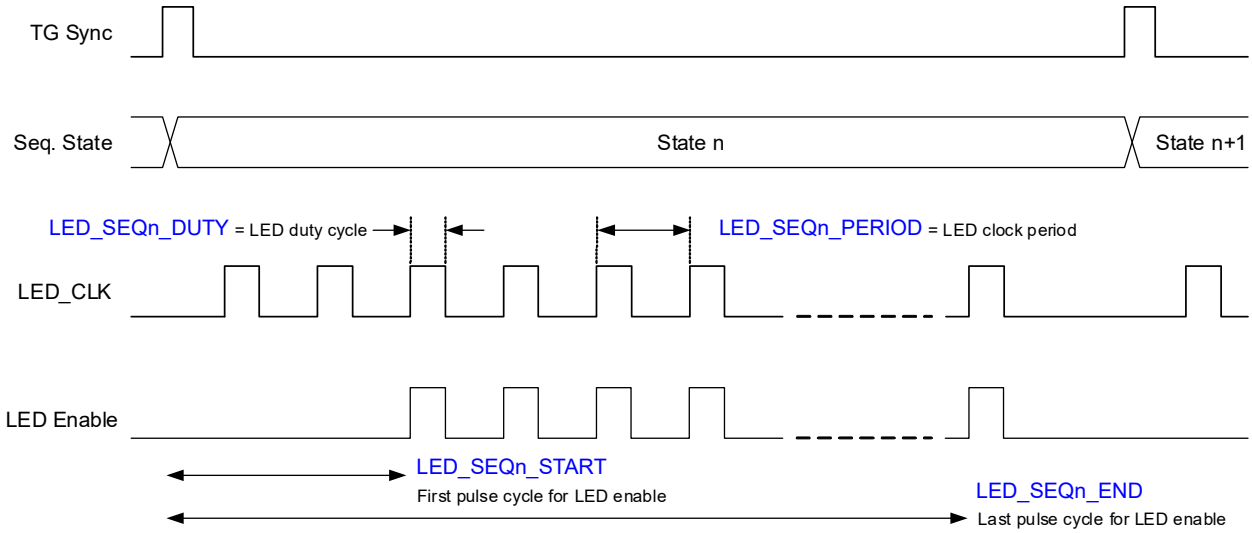


Figure 4-32. LED_CLK Timing Control

4.8.2 Current Control

The output current of each LED driver is configured using coarse and fine controls. The maximum available output current is configured using the coarse control, LEDx_COARSE. The output current is selected—from zero to the configured maximum—using the fine control, LEDx_FINE. The fine control provides an 8-bit resolution to set the output current between zero and the configured maximum (coarse) level.

Notes: If the sum of the coarse current selections in the enabled channels exceed the maximum limit (123 mA in typical combinations), the current levels are automatically restricted to a maximum of 41 mA; the maximum current limit is assured, but the accuracy may be outside the specified tolerance (see Table 3-4).

The LED drivers must be disabled before changing the coarse current control. The host should confirm the CS82L41 is in the Idle State (see Section 4.2) before changing the coarse current control.

When an LED driver is enabled/disabled, or the fine current level is changed, the respective current sink ramps up/down to the configured level. The ramp rate is configurable using LED_RAMP_TIME. If the fine current level is changed while a ramp is in progress, the current sink ramps up/down to the new level.

The ramp rate can be modified using LED_RAMP_BOOST, allowing slew rates 2x or 4x faster than the LED_RAMP_TIME rate. Some restrictions are applicable on these faster rates, as noted in the register-field description.

The current ramp uses the MCLK_EXT input as a timing reference. The MCLK_FREQ field must be configured according to the frequency of MCLK_EXT input.

4.8.3 Fault Detection

The LED drivers are protected in case of fault conditions. Error conditions are indicated using the following control bits:

- LED_MAX_CURRENT_ERR—indicates sum of the coarse current levels (in the enabled channels) exceeds the maximum limit. If this bit is set, the fine current levels are automatically restricted to a maximum of 41 mA.
- LED_CTRL_SHORT_ERR—indicates a short circuit on the external ILED_CTRL resistor.

If a short circuit is detected, the LED drivers are shut down and the CS82L41 enters the Error State. See Section 4.2.1 for further details.

Note there is no specific indication of an open circuit on the external ILED_CTRL resistor, but the LED drivers are protected and disabled in this event.

If an LED output pin is shorted to a supply rail, the driver maintains the selected current through the pin, resulting in increased voltage drop across the internal circuits. The current drawn from the supply is protected, but thermal dissipation in the CS82L41 is increased.

4.9 Control Interface

The CS82L41 incorporates a SPI control port, using the $\overline{\text{SPI\_CS}}$, SPI_SCK, SPI_SDI, and SPI_SDO pins.

The $\overline{\text{SPI\_CS}}$ pin provides the chip-select input (active low). Clocking for the input/output data is supported using SPI_SCK.

The SDI (data-input) pin supports the following behavior:

- In write operations (R/W = 0), the SDI pin input is driven by the controlling device.
- In read operations (R/W = 1), the SDI pin is ignored following receipt of the valid register address.

The SDO (data-output) pin is multiplexed with DOUT4 and supports the following behavior:

- If $\overline{\text{CS}}$ is deasserted (Logic 1), the pin function is DOUT4, supporting sample-data output. See Section 4.5 for details of the output data formats.
- If $\overline{\text{CS}}$ is asserted (Logic 0), the pin function is SDO, supporting control-port operations. The output is actively driven when outputting control data and is high impedance at other times. Note that sample-data output is interrupted during any SPI control port transaction.
- The high-impedance state of the SDO output allows the pin to be shared with other peripheral devices.
- The output (SDO) data bit is available to the host device at the rising edge of SCK. See Table 3-16 for timing information.

The SPI interface uses a 7-bit register address and 8-bit data words. A read/write bit is also used to select the transaction type.

The register map is arranged in 8 banks, each containing 128 registers. By selecting different banks, all of the CS82L41 control registers can be accessed using the 7-bit register address.

The current bank is configured using BANK. This field is supported at register address 0x00 in all banks, and can therefore be accessed in the same way regardless of which bank is currently selected.

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS82L41 automatically increments the register address at the end of each data word, for as long as $\overline{\text{CS}}$ is held low and SCK is toggled. Successive data words can be input/output every 8 clock cycles.

Fig. 4-33 shows a single register write to a specified address.

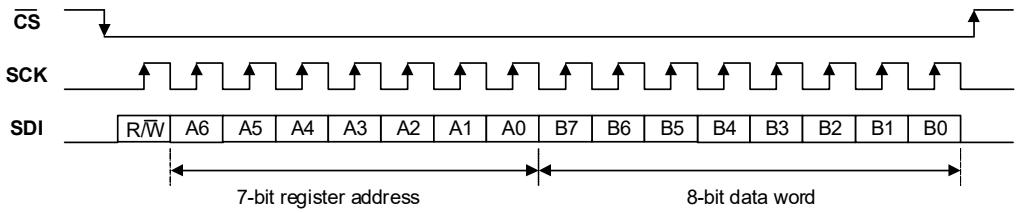


Figure 4-33. Control Interface SPI Register Write

Fig. 4-34 shows a single register read from a specified address.

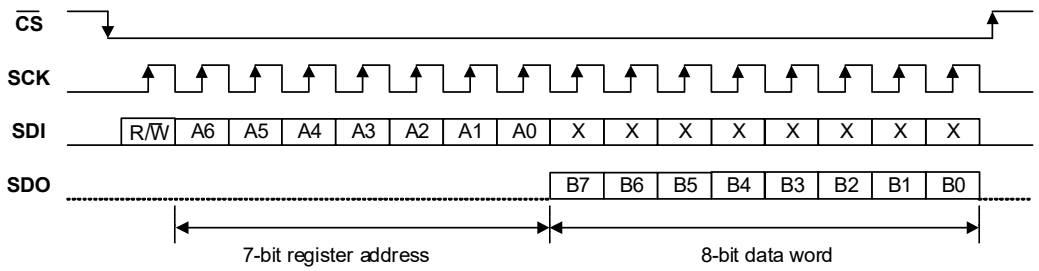


Figure 4-34. Control Interface SPI Register Read

4.9.1 Shared Bus Mode

The CS82L41 can be configured in Shared Bus Mode, where the SPI control interface and the digital data output are supported on shared pins. This can be used to reduce the number of I/O connections to the host interface.

In Shared Bus Mode, the DOUT1–DOUT3 outputs are disabled (Hi-Z) whenever $\overline{\text{SPI\_CS}}$ is asserted. This allows the two interfaces to be connected together and used in turn.

Note: The DOUT4 output is also disabled (HiZ) whenever $\overline{\text{SPI\_CS}}$ is asserted; this is the default behavior for the shared DOUT4/SPI_SDO pin, as described in Section 4.9.

Typical connections for Shared Bus Mode are shown in Fig. 4-35.

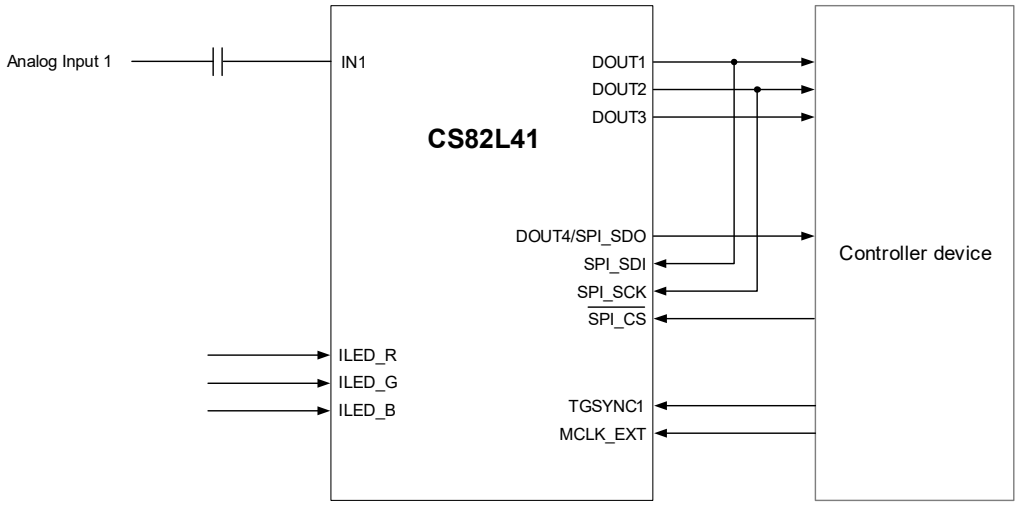


Figure 4-35. Shared Bus Mode

Shared Bus Mode is enabled using SHARED_BUS_MODE. If this bit is set, the DOUTn pins are controlled to allow these pins to be shared with the SPI control interface. The DOUTn pins are Hi-Z when $\overline{\text{SPI\_CS}}$ is asserted (Logic 0), allowing the host to access the control registers using the SPI interface.

In a typical application, the host configures the device in the Idle State (see Section 4.2). When the host selects the Active State, the data output commences after $\overline{\text{SPI\_CS}}$ is deasserted high. The data output ceases when $\overline{\text{SPI\_CS}}$ is asserted low.

Note: The DOUTn output pins are enabled in the Ready State (the data bits are held at 0). If the SPI and DOUT pins are connected on the PCB, the Shared Bus Mode must be enabled prior to selecting the Ready State in order to avoid bus contention.

The DOUT1–DOUT3 pins can be shared with the SPI_SDI and SPI_SCK pins in any configuration; the connections shown in Fig. 4-35 are an example configuration only.

4.10 Pin Configuration and General-Purpose Input/Output

Many of the digital input/output functions are supported on multifunction pins. These pins are used for sample/frame timing control and LED control inputs. General-purpose input/output is also supported.

4.10.1 Pin Function Select

The multifunction pins are configured for the required function using the control fields described in Table 4-4.

Table 4-4. Pin Function Select

Pin Name	Control Field	Selection	Reference
LEDR_EN/TGSYNC/ GPIO1	LEDR_EN_FN	00 = Red LED control input 01 = TGSYNC input 10 = General-purpose input/output 1 11 = Reserved	Section 4.8 Section 4.7.2 Section 4.10.2 —
LEDG_EN/LEDSTART/ GPIO2	LEDG_EN_FN	00 = Green LED control input 01 = LEDSTART 10 = General-purpose input/output 2 11 = Reserved	Section 4.8 Section 4.7.2 Section 4.10.2 —
LEDB_EN/RSMP_EXT1/ GPIO3	LEDB_EN_FN	00 = Blue LED control input 01 = RSMP input 1 [1] 10 = General-purpose input/output 3 11 = Monitor/test input	Section 4.8 Section 4.6.1 Section 4.10.2 Section 4.11
RSMP_EXT2/GPIO4	RSMP_EXT2_FN	0 = General-purpose input/output 4 1 = RSMP input 2 [1,2]	Section 4.10.2 Section 4.6.1

1. The RSMP input can also be used to control the input clamp, as described in Section 4.4.3.
2. Not supported if LEDB_EN_FN = 01; in this case, the GPIO4 function applies.

4.10.2 General Purpose Input/Output

The CS82L41 supports general-purpose (GP) input/output on selected digital I/O pins. The input function can be used to allow readback of hardware signals from other devices. The output function can be used to control other devices.

The general-purpose inputs are multiplexed with other pin functions. Each pin is configured for GP input/output using the respective x_FN field as noted in Table 4-4.

The general-purpose I/O functions are configured as input by default. The output function is enabled by setting the respective GPx_DIR bit.

- If a pin is configured for GP input, the logic level is indicated using GPx_IN_STS.
- If a pin is configured for GP output, the output level is controlled using GPx_OUT_LVL.

4.10.3 Digital I/O Pin Configuration

The digital I/O pins are configurable to support flexible integration with other devices. Configurable options are provided for all of the digital I/O listed in Table 1-1—this includes MCLK input, data output, and the multifunction pins listed in Table 4-4.

Integrated pull-up and pull-down resistors are configured and enabled using the respective x_PULL fields. A bus-keeper function can also be enabled using the x_PULL fields; the bus-keeper holds the logic level unchanged whenever the pin is undriven (e.g., if the signal is tristated).

The drive strength for CMOS digital output is configured using x_DRV_STR.

The input function on each pin is enabled using x_IE. This bit must be set to support input functions on the respective pin.

The pins can be configured in a high-impedance state using x_HIZ_EN. Note that, to configure the high-impedance state, the pull-up and pull-down resistors must also be disabled using x_PULL.

4.11 Debug Monitor Output

The MON output allows internal clock signals to be monitored externally for timing set-up and debug purposes. The MON function is supported on a multifunction pin, which must be configured for monitor output as described in Section 4.10.

The MON output is configured using MON_SEL. The following output signals are supported:

- VSMP—video sample control
- RSMP—reset sample control
- AFECK—ADC sample/conversion control

If using the monitor output to configure the signal timing for an application, it is recommended to take account of the propagation delay from the internal signal to the monitor output. The propagation delay is defined in Table 3-15.

4.12 Device ID

The device ID, and other associated data, can be read from the control fields listed in Table 4-5.

Table 4-5. Device ID

Label	Description
DEVID	Device ID
AREVID	All-layer device revision
MTLREVID	Metal-layer device revision
RELID	Software device revision
DESCRIM	Device identifier (readback value 0xC)

5 Applications

5.1 Output Code Calculation

The digital output code associated with a given analog input voltage is dependent on how the analog input path is configured (see Section 4.4), and on the selected data-output format (see Section 4.5). This section describes a calculation that can be used to predict the digital output code for a given configuration.

The digital output code can be derived as follows:

1. Calculate V_{OFFSET} = (V_{REF} / 3.6) × ((2 × CH1_SEQn_OFFSET / 511) – 1)
   where V_{REF} = internal reference voltage (1.2 V)
2. Calculate V_{PGA_INPUT} according to the applicable sampling mode:
   - In CDS Mode (CDS_EN = 1), V_{PGA_INPUT} = V_{VSMP} – V_{RSMP}
     where V_{VSMP} = video sample level, and V_{RSMP} = reset sample level
   - In non-CDS Mode (CDS_EN = 0), V_{PGA_INPUT} = V_{VSMP} – V_{BIAS}
     where V_{VSMP} = video sample level, and V_{BIAS} = bias voltage
     if the internal bias is enabled, the bias voltage is configured using VBIAS_LVL
3. Calculate V_{PGA_OUTPUT} = GAIN × ((V_{PGA_INPUT} × (1 – (2 × CH1_POL))) – V_{OFFSET})
   where GAIN = PGA gain represented by CH1_SEQn_AGAIN
4. Calculate the ADC output code:

$$\text{ADC output code} = \max\left(\min\left(\frac{(V_{PGA\_OUTPUT} - V_{REF}) \times 2^{RES-1}}{V_{REF}} + 2^{RES-1}, 2^{RES} - 1\right), 0\right)$$

   where RES = number of data bits in selected output format

Note: The calculation assumes default digital gain of 1 V/V (CH1_SEQn_DGAIN = 0x800)

5.1.1 Example Calculation—CDS Mode

Using example data, the digital output code can be calculated as follows:

- V_{REF} = 1.2 V
- V_{VSMP} = 1.0 V
- V_{RSMP} = 2.5 V
- Offset code (CH1_SEQn_OFFSET) = 256
- PGA gain (CH1_SEQn_AGAIN) = 1 V/V
- Polarity (CH1_POL) = 1
- Output data resolution = 16 bits

Calculate V_{OFFSET} = (1.2 / 3.6) × ((2 × 256 / 511) – 1) = 0.000652 V

Calculate V_{PGA_INPUT} = 1.0 – 2.5 = –1.5 V

Calculate V_{PGA_OUTPUT} = 1 × ((–1.5 × (1 – (2 × 1))) – 0.000652 V) = 1.499348 V

Calculate the ADC output code:

$$\text{ADC output code} = \max\left(\min\left(\frac{(1.499348 - 1.2) \times 2^{15}}{1.2} + 2^{15}, 2^{16} - 1\right), 0\right) = \max(\min(40942, 65535), 0) = 40942$$

5.1.2 Example Calculation—Non-CDS Mode

Using example data, the digital output code can be calculated as follows:

- V_{IN} = 2.3 V
- V_{REF} = 1.2 V
- V_{BIAS} = 1.0 V
- Offset code (CH1_SEQn_OFFSET) = 256
- PGA gain (CH1_SEQn_AGAIN) = 1 V/V
- Polarity (CH1_POL) = 0
- Output data resolution = 16 bits

Calculate V_{OFFSET} = (1.2 / 3.6) × ((2 × 256 / 511) – 1) = 0.000652 V

Calculate V_{PGA_INPUT} = 2.3 – 1.0 = 1.3 V

Calculate V_{PGA_OUTPUT} = 1 × ((1.3 × (1 – (2 × 0))) – 0.000652) = 1.299348 V

Calculate the ADC output code:

$$\text{ADC output code} = \max\left(\min\left(\frac{(1.299348 - 1.2) \times 2^{15}}{1.2} + 2^{15}, 2^{16} - 1\right), 0\right) = \max(\min(35481, 65535), 0) = 35481$$

6 Register Quick Reference

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

- This register view is for the CS82L41 imaging AFE/ADC, using the banked host-interface configuration.
- The register field default values are established on power-up and after soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 8 bits wide.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

Table 6-1. Bank Overview

Block Name	Register Quick Reference	Register Description Reference
BANK0—Hardware ID, Clocking, MSM, Output Format, Control Keys, Pad I/O, Control Interface	Section 6.1	Section 7.1
BANK1—DAC, PGA, DGAIN, SARADC, LED Control	Section 6.2	Section 7.2
BANK2—MSM	Section 6.3	Section 7.3
BANK3—MSM	Section 6.4	Section 7.4

6.1 BANK0—Hardware ID, Clocking, MSM, Output Format, Control Keys, Pad I/O, Control Interface

Address	Register	7	6	5	4	3	2	1	0
0x00	BANK	DESCRIM				—	BANK		
p. 51		1	1	0	0	0	0	0	0
0x04	ASYNC0_0	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	—	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
p. 51		0	0	0	0	0	0	0	0
0x05	ASYNC0_1	—							OSC_DISABLE
p. 52		0	0	0	0	0	0	0	0
0x08	SFT_RESET	SFT_RESET							
p. 52		0	0	0	0	0	0	0	0
0x0C	DEVID_0	DEVID_0							
p. 52		X	X	X	X	X	X	X	X
0x0D	DEVID_1	DEVID_1							
p. 52		X	X	X	X	X	X	X	X
0x0E	DEVID_2	DEVID_2							
p. 52		X	X	X	X	X	X	X	X
0x10	REVID	AREVID				MTLREVID			
p. 52		1	0	1	0	0	0	0	0
0x14	RELID	RELID							
p. 53		0	0	0	0	0	0	0	0
0x20	CCM_AFECLK_CFG_0	—			TIMING_MODE	CLAMP_OVRD	CLAMP_EN	CLAMP_MODE	CDS_EN
p. 53		0	0	0	0	0	0	0	0
0x21	CCM_AFECLK_CFG_1	—					AFECK_DUR		
p. 53		0	0	0	0	0	0	0	1
0x22	CCM_AFECLK_CFG_2	RSMP_EXT_DLY			VSMP_EXT_DLY				VSMP_EXT_POL
p. 53		0	0	1	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x28	DEVICE_CTRL_0	LDO4_EN	SHARED_BUS_MODE	—			ACTIVE_EN	READY_EN	MSM_EN
p. 54		0	0	0	0	0	0	0	1
0x29	DEVICE_CTRL_1	TEMP_ERROR_RST_MASK	—	TEMP_ERROR_CLR	—				
p. 54		0	0	0	0	0	0	0	0
0x2A	DEVICE_CTRL_2	LDO4_HIZ	—	LDO_EN_MASK	LDO5_EN	LDO5_ILIMIT_VPC	LDO5_ILIMIT_CTRL		
p. 55		0	0	0	0	1	0	0	0
0x2B	DEVICE_CTRL_3	—			LDO5_VOUT				
p. 55		0	0	0	0	0	0	0	0
0x2C	RLCDAC_CTRL_0	—							VBIAS_EN
p. 55		0	0	0	0	0	0	0	0
0x2D	RLCDAC_CTRL_1	—			VBIAS_LVL				
p. 56		0	0	0	0	0	0	0	0
0x2E	RLCDAC_CTRL_2	—				VBIAS_ISEL_BOOST	VBIAS_ISEL		VBIAS_REF
p. 56		0	0	0	0	0	0	0	1
0x30	OP_FORMAT_CFG1_0	—			DOUT_CONFIG	DOUT_PHASE	DOUT_DLY		DOUT_DDR
p. 56		0	0	0	1	1	0	0	1
0x31	OP_FORMAT_CFG1_1	—						TEST_PATT_DIR	TEST_PATT_EN
p. 56		0	0	0	0	0	0	0	0
0x40	LED_EN_SEL_0	RSMP_EXT2_FN	—	LEDB_EN_FN		LEDG_EN_FN		LEDR_EN_FN	
p. 57		0	0	0	1	0	1	0	1
0x42	LED_EN_SEL_2	—			MON_SEL			—	
p. 57		0	0	0	0	0	0	0	0
0x44	GPI_VAL_0	—			GP4_IN_STS	GP3_IN_STS	GP2_IN_STS	GP1_IN_STS	—
p. 57		0	0	0	X	X	X	X	0
0x46	GPI_VAL_2	—			GP4_DIR	GP3_DIR	GP2_DIR	GP1_DIR	—
p. 58		0	0	0	0	0	0	0	0
0x47	GPI_VAL_3	—			GP4_OUT_LVL	GP3_OUT_LVL	GP2_OUT_LVL	GP1_OUT_LVL	—
p. 58		0	0	0	0	0	0	0	0
0x48	CMOS_CFG_0	—	DOUT4_SPI_SDO_DRV_STR			DOUT4_SPI_SDO_PULL		DOUT4_SPI_SDO_HIZ_EN	DOUT4_SPI_SDO_IE
p. 59		0	0	0	1	1	0	0	1
0x49	CMOS_CFG_1	—	SPI_SDI_DRV_STR			SPI_SDI_PULL		SPI_SDI_HIZ_EN	SPI_SDI_IE
p. 59		0	0	0	1	1	0	0	1
0x4A	CMOS_CFG_2	—				SPI_SCK_PULL		—	SPI_SCK_IE
p. 59		0	0	0	1	1	0	0	1
0x4B	CMOS_CFG_3	—				SPI_CS_PULL		—	SPI_CS_IE
p. 60		0	0	0	1	1	0	0	1
0x4D	MCLK_CFG	—				MCLK_PULL		MCLK_HIZ_EN	MCLK_IE
p. 60		0	0	0	1	1	0	0	1
0x50	LED_EN_CFG_0	—	LEDR_EN_TGSYNC_GPIO1_DRV_STR			LEDR_EN_TGSYNC_GPIO1_PULL		LEDR_EN_TGSYNC_GPIO1_HIZ_EN	LEDR_EN_TGSYNC_GPIO1_IE
p. 60		0	0	0	1	1	0	0	1
0x51	LED_EN_CFG_1	—	LEDG_EN_LEDSTART_GPIO2_DRV_STR			LEDG_EN_LEDSTART_GPIO2_PULL		LEDG_EN_LEDSTART_GPIO2_HIZ_EN	LEDG_EN_LEDSTART_GPIO2_IE
p. 61		0	0	0	1	1	0	0	1
0x52	LED_EN_CFG_2	—	LEDB_EN_MON_RSMP_EXT_GPIO3_DRV_STR			LEDB_EN_MON_RSMP_EXT_GPIO3_PULL		LEDB_EN_MON_RSMP_EXT_GPIO3_HIZ_EN	LEDB_EN_MON_RSMP_EXT_GPIO3_IE
p. 61		0	0	0	1	1	0	0	1

Address	Register	7	6	5	4	3	2	1	0
0x53	LED_EN_CFG_3	—	RSMP_GPIO4_DRV_STR			RSMP_GPIO4_PULL		RSMP_GPIO4_HIZ_EN	RSMP_GPIO4_IE
p. 61		0	0	0	1	1	0	0	1
0x54	VSMP_EXT_CFG	—	VSMP_EXT_DRV_STR			VSMP_EXT_PULL		VSMP_EXT_HIZ_EN	VSMP_EXT_IE
p. 62		0	0	0	1	1	0	0	1
0x58	DOUT_CFG_0	—	DOUT1_DRV_STR			DOUT1_PULL		DOUT1_HIZ_EN	DOUT1_IE
p. 62		0	0	0	1	1	0	0	0
0x59	DOUT_CFG_1	—	DOUT2_DRV_STR			DOUT2_PULL		DOUT2_HIZ_EN	DOUT2_IE
p. 63		0	0	0	1	1	0	0	0
0x5A	DOUT_CFG_2	—	DOUT3_DRV_STR			DOUT3_PULL		DOUT3_HIZ_EN	DOUT3_IE
p. 63		0	0	0	1	1	0	0	0

6.2 BANK1—DAC, PGA, DGAIN, SARADC, LED Control

Address	Register	7	6	5	4	3	2	1	0
0x00	BANK	DESCRIM				—	BANK		
p. 63		1	1	0	0	0	0	0	0
0x04	ASYNC0_0	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	—	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
p. 64		0	0	0	0	0	0	0	0
0x05	ASYNC0_1	—							OSC_DISABLE
p. 64		0	0	0	0	0	0	0	0
0x08	SFT_RESET	SFT_RESET							
p. 64		0	0	0	0	0	0	0	0
0x10	DAC_CTRL_OFS01_CH1_0	CH1_SEQ0_OFFSET_0							
p. 65		0	0	0	0	0	0	0	0
0x11	DAC_CTRL_OFS01_CH1_1	—							CH1_SEQ0_OFFSET_1
p. 65		0	0	0	0	0	0	0	1
0x12	DAC_CTRL_OFS01_CH1_2	CH1_SEQ1_OFFSET_0							
p. 65		0	0	0	0	0	0	0	0
0x13	DAC_CTRL_OFS01_CH1_3	—							CH1_SEQ1_OFFSET_1
p. 65		0	0	0	0	0	0	0	1
0x14	DAC_CTRL_OFS23_CH1_0	CH1_SEQ2_OFFSET_0							
p. 66		0	0	0	0	0	0	0	0
0x15	DAC_CTRL_OFS23_CH1_1	—							CH1_SEQ2_OFFSET_1
p. 66		0	0	0	0	0	0	0	1
0x16	DAC_CTRL_OFS23_CH1_2	CH1_SEQ3_OFFSET_0							
p. 66		0	0	0	0	0	0	0	0
0x17	DAC_CTRL_OFS23_CH1_3	—							CH1_SEQ3_OFFSET_1
p. 66		0	0	0	0	0	0	0	1
0x1C	PGA_CTRL_AGAIN_CH1_0	—		CH1_SEQ0_AGAIN					
p. 67		0	0	0	0	0	0	0	0
0x1D	PGA_CTRL_AGAIN_CH1_1	—		CH1_SEQ1_AGAIN					
p. 67		0	0	0	0	0	0	0	0
0x1E	PGA_CTRL_AGAIN_CH1_2	—		CH1_SEQ2_AGAIN					
p. 67		0	0	0	0	0	0	0	0
0x1F	PGA_CTRL_AGAIN_CH1_3	—		CH1_SEQ3_AGAIN					
p. 67		0	0	0	0	0	0	0	0
0x20	DGAIN_SEQ01_CH1_0	CH1_SEQ0_DGAIN_0							
p. 68		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x21	DGAIN_SEQ01_CH1_1	—				CH1_SEQ0_DGAIN_1			
p. 68		0	0	0	0	1	0	0	0
0x22	DGAIN_SEQ01_CH1_2	CH1_SEQ1_DGAIN_0							
p. 68		0	0	0	0	0	0	0	0
0x23	DGAIN_SEQ01_CH1_3	—				CH1_SEQ1_DGAIN_1			
p. 68		0	0	0	0	1	0	0	0
0x24	DGAIN_SEQ23_CH1_0	CH1_SEQ2_DGAIN_0							
p. 69		0	0	0	0	0	0	0	0
0x25	DGAIN_SEQ23_CH1_1	—				CH1_SEQ2_DGAIN_1			
p. 69		0	0	0	0	1	0	0	0
0x26	DGAIN_SEQ23_CH1_2	CH1_SEQ3_DGAIN_0							
p. 69		0	0	0	0	0	0	0	0
0x27	DGAIN_SEQ23_CH1_3	—				CH1_SEQ3_DGAIN_1			
p. 69		0	0	0	0	1	0	0	0
0x28	DGAIN_REF_CH1_0	CH1_SEQ0_DGAIN_REF							
p. 70		0	0	0	0	0	0	0	0
0x29	DGAIN_REF_CH1_1	CH1_SEQ1_DGAIN_REF							
p. 70		0	0	0	0	0	0	0	0
0x2A	DGAIN_REF_CH1_2	CH1_SEQ2_DGAIN_REF							
p. 70		0	0	0	0	0	0	0	0
0x2B	DGAIN_REF_CH1_3	CH1_SEQ3_DGAIN_REF							
p. 70		0	0	0	0	0	0	0	0
0x2D	SAR1_CTRL_1	—					CH1_POL	—	
p. 70		0	0	0	0	0	0	0	0
0x2F	SAR1_CTRL_3	—						CH1_AFE_POWER	
p. 71		0	0	0	0	0	0	1	1
0x40	LED_CTRL_CONFIG_0	—				LED_CTRL_SRC	LEDB_EN	LEDG_EN	LEDR_EN
p. 71		0	0	0	0	0	0	0	0
0x41	LED_CTRL_CONFIG_1	—				LED_RAMP_TIME			
p. 71		0	0	0	0	0	0	0	0
0x42	LED_CTRL_CONFIG_2	LED_RAMP_BOOST		LEDB_COARSE		LEDG_COARSE		LEDR_COARSE	
p. 71		0	0	0	0	0	0	0	0
0x43	LED_CTRL_CONFIG_3	MCLK_FREQ							
p. 72		0	0	0	0	1	0	1	0
0x44	LEDX_FINE_0	LEDR_FINE							
p. 72		0	0	0	0	0	0	0	0
0x45	LEDX_FINE_1	LEDG_FINE							
p. 72		0	0	0	0	0	0	0	0
0x46	LEDX_FINE_2	LEDB_FINE							
p. 72		0	0	0	0	0	0	0	0
0x48	TG_FILT_CONFIG_0	—			LEDSTART_POL	—	TGSYNC_IN_POL	TGSYNC_IN_SRC	
p. 72		0	0	0	0	0	1	0	0
0x49	TG_FILT_CONFIG_1	MCLK_SYNC_POL	TGSYNC_FILT_STAGE			TGSYNC_FILT_DECM			TGSYNC_FILT_EN
p. 73		0	1	0	0	0	1	1	0
0x4C	PWM_CONFIG_0	LED_CLK_DIV				—		NUM_SEQ_STATES	
p. 73		0	0	0	0	0	0	0	0
0x4D	PWM_CONFIG_1	LEDG_SEQ_SEL				LEDR_SEQ_SEL			
p. 74		0	0	0	0	0	0	0	0
0x4E	PWM_CONFIG_2	—				LEDB_SEQ_SEL			
p. 74		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x4F	PWM_CONFIG_3	—		TGSYNC_SEQ_RST	TGSYNC_SINGLE_SEQ	LEDSTART_SEQ_INIT	IN_SEQ_SEL		ACYC_EN
p. 74		0	0	0	0	0	0	0	1
0x50	PWM_S0_CFG_0	LED_SEQ0_PERIOD_0							
p. 75		0	0	0	0	0	0	0	0
0x51	PWM_S0_CFG_1	—	LED_SEQ0_PERIOD_1						
p. 75		0	0	0	0	0	0	0	0
0x52	PWM_S0_CFG_2	LED_SEQ0_DUTY_0							
p. 75		0	0	0	0	0	0	0	0
0x53	PWM_S0_CFG_3	—	LED_SEQ0_DUTY_1						
p. 75		0	0	0	0	0	0	0	0
0x54	PWM_S1_CFG_0	LED_SEQ1_PERIOD_0							
p. 75		0	0	0	0	0	0	0	0
0x55	PWM_S1_CFG_1	—	LED_SEQ1_PERIOD_1						
p. 76		0	0	0	0	0	0	0	0
0x56	PWM_S1_CFG_2	LED_SEQ1_DUTY_0							
p. 76		0	0	0	0	0	0	0	0
0x57	PWM_S1_CFG_3	—	LED_SEQ1_DUTY_1						
p. 76		0	0	0	0	0	0	0	0
0x58	PWM_S2_CFG_0	LED_SEQ2_PERIOD_0							
p. 76		0	0	0	0	0	0	0	0
0x59	PWM_S2_CFG_1	—	LED_SEQ2_PERIOD_1						
p. 76		0	0	0	0	0	0	0	0
0x5A	PWM_S2_CFG_2	LED_SEQ2_DUTY_0							
p. 77		0	0	0	0	0	0	0	0
0x5B	PWM_S2_CFG_3	—	LED_SEQ2_DUTY_1						
p. 77		0	0	0	0	0	0	0	0
0x5C	PWM_S3_CFG_0	LED_SEQ3_PERIOD_0							
p. 77		0	0	0	0	0	0	0	0
0x5D	PWM_S3_CFG_1	—	LED_SEQ3_PERIOD_1						
p. 77		0	0	0	0	0	0	0	0
0x5E	PWM_S3_CFG_2	LED_SEQ3_DUTY_0							
p. 77		0	0	0	0	0	0	0	0
0x5F	PWM_S3_CFG_3	—	LED_SEQ3_DUTY_1						
p. 78		0	0	0	0	0	0	0	0
0x60	LED_START_STOP1_0	—	LED_SEQ0_START						
p. 78		0	0	0	0	0	0	0	0
0x61	LED_START_STOP1_1	—	LED_SEQ0_END						
p. 78		0	0	0	0	0	0	0	0
0x62	LED_START_STOP1_2	—	LED_SEQ1_START						
p. 78		0	0	0	0	0	0	0	0
0x63	LED_START_STOP1_3	—	LED_SEQ1_END						
p. 79		0	0	0	0	0	0	0	0
0x64	LED_START_STOP2_0	—	LED_SEQ2_START						
p. 79		0	0	0	0	0	0	0	0
0x65	LED_START_STOP2_1	—	LED_SEQ2_END						
p. 79		0	0	0	0	0	0	0	0
0x66	LED_START_STOP2_2	—	LED_SEQ3_START						
p. 79		0	0	0	0	0	0	0	0
0x67	LED_START_STOP2_3	—	LED_SEQ3_END						
p. 80		0	0	0	0	0	0	0	0
0x68	LED_CTRL_STATUS	—	SEQ_STATE_STS		LED_MAX_CURRENT_ERR	LED_CTRL_SHORT_ERR		—	
p. 80		0	0	0	0	0	0	0	0

6.3 BANK2—MSM

Address	Register	7	6	5	4	3	2	1	0
0x00	BANK	DESCRIM				—		BANK	
p. 80		1	1	0	0	0	0	0	0
0x04	ASYNC0_0	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	—	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
p. 81		0	0	0	0	0	0	0	0
0x05	ASYNC0_1	—							OSC_DISABLE
p. 81		0	0	0	0	0	0	0	0
0x08	SFT_RESET	SFT_RESET							
p. 81		0	0	0	0	0	0	0	0
0x10	DEVICE_STATUS_0	ERROR_STS	—	ACTIVE_STS	READY_STS	—		IDLE_STS	STARTUP_STS
p. 81		0	0	0	0	0	0	0	0
0x12	DEVICE_STATUS_2	VDDA_STS	—						
p. 82		0	0	0	0	0	1	0	0

6.4 BANK3—MSM

Address	Register	7	6	5	4	3	2	1	0
0x00	BANK	DESCRIM				—		BANK	
p. 82		1	1	0	0	0	0	0	0
0x04	ASYNC0_0	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	—	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
p. 82		0	0	0	0	0	0	0	0
0x05	ASYNC0_1	—							OSC_DISABLE
p. 83		0	0	0	0	0	0	0	0
0x08	SFT_RESET	SFT_RESET							
p. 83		0	0	0	0	0	0	0	0

7 Register Descriptions

This section describes each of the control port registers.

- This register view is for the CS82L41 imaging AFE/ADC, using the banked host-interface configuration.
- The register field default values are established on power-up and after soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 8 bits wide.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

7.1 BANK0—Hardware ID, Clocking, MSM, Output Format, Control Keys, Pad I/O, Control Interface

7.1.1 BANK

BANKn (n = 0–7) Address: 0x00

	7	6	5	4	3	2	1	0
	DESCRIM				—	BANK		
Access	RO				—	RW		
Default	1	1	0	0	0	0	0	0

Bits	Name	Description
7:4	DESCRIM	Read-only device identifier field. Readback value is 0xC.
3	—	Reserved
2:0	BANK	Selects the active bank for SPI access. 000 = (Default) Bank 0 001 = Bank 1 010 = Bank 2 011 = Bank 3 100 = Bank 4 101 = Bank 5 110 = Bank 6 111 = Bank 7

7.1.2 ASYNC0_0

BANKn (n = 0–7) Address: 0x04

RO	7	6	5	4	3	2	1	0
	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	—	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	ACTIVE_ERROR_STS	Path error status. Indicates an error condition in the Active or Ready states. 0 = (Default) Normal 1 = Error
4	TEMP_ERROR_STS	Temperature error status. Indicates an overtemperature condition has been detected. 0 = (Default) Normal 1 = Error
3	—	Reserved
2	MCLK_ERROR_STS	MCLK error status. Indicates MCLK is invalid or absent in the Idle State. 0 = (Default) Normal 1 = Error
1	STARTUP_ERROR_STS	Start up error status. Indicates an error detected during start-up. 0 = (Default) Normal 1 = Error
0	BOOT_ERROR_STS	Boot error status. Indicates an error detected during boot. 0 = (Default) Normal 1 = Error

7.1.3 ASYNC0_1

BANKn (n = 0–7) Address: 0x05

	7	6	5	4	3	2	1	0
RW	—							OSC_DISABLE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	OSC_DISABLE	Oscillator disable. Setting this bit places the device in a low-power Sleep State. Note that the host must return the device to the Idle State before writing to any other control registers. 0 = (Default) RCO enabled 1 = RCO disabled

7.1.4 SFT_RESET

BANKn (n = 0–7) Address: 0x08

	7	6	5	4	3	2	1	0
WO	SFT_RESET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	SFT_RESET	Software reset. Write 0x5A to execute a software reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved

7.1.5 DEVID_0

BANK0 Address: 0x0C

	7	6	5	4	3	2	1	0
RO	DEVID_0							
Default	X	X	X	X	X	X	X	X

Bits	Name	Description
7:0	DEVID_0	Device ID (Byte 0). A value of 0x41 indicates the device is a CS82L41.

7.1.6 DEVID_1

BANK0 Address: 0x0D

	7	6	5	4	3	2	1	0
RO	DEVID_1							
Default	X	X	X	X	X	X	X	X

Bits	Name	Description
7:0	DEVID_1	Device ID (Byte 1). Readback value is 0x2A.

7.1.7 DEVID_2

BANK0 Address: 0x0E

	7	6	5	4	3	2	1	0
RO	DEVID_2							
Default	X	X	X	X	X	X	X	X

Bits	Name	Description
7:0	DEVID_2	Device ID (Byte 2). Readback value is 0x08.

7.1.8 REVID

BANK0 Address: 0x10

	7	6	5	4	3	2	1	0
RO	AREVID				MTLREVID			
Default	1	0	1	0	0	0	0	0

Bits	Name	Description
7:4	AREVID	All-layer device revision. This field is incremented for every all-layer revision of the device.
3:0	MTLREVID	Metal-layer device revision. This field is incremented for every metal-layer revision of the device.

7.1.9 RELID

BANK0 Address: 0x14

	7	6	5	4	3	2	1	0
RO	RELID							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	RELID	Software device revision. This field is incremented if software-driver compatibility or software feature support is changed.

7.1.10 CCM_AFECLK_CFG_0

BANK0 Address: 0x20

	7	6	5	4	3	2	1	0
RW	—			TIMING_MODE	CLAMP_OVRD	CLAMP_EN	CLAMP_MODE	CDS_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4	TIMING_MODE	Sample Timing Mode select In Timing Mode 1, VSMP/RSMP are controlled directly from the hardware pins. In Timing Mode 2, VSMP/RSMP are generated internally from external VSMP_EXT. 0 = (Default) Timing Mode 1 1 = Timing Mode 2
3	CLAMP_OVRD	AFE clamp override switch control 0 = (Default) Disabled 1 = Enabled
2	CLAMP_EN	AFE clamp enable 0 = (Default) Disable Clamp 1 = Enable Clamp
1	CLAMP_MODE	AFE clamp operation mode select 0 = (Default) Enabled for all pixels 1 = Controlled by external RSMP
0	CDS_EN	AFE cds mode enable 0 = (Default) non CDS Sampling 1 = CDS Sampling

7.1.11 CCM_AFECLK_CFG_1

BANK0 Address: 0x21

	7	6	5	4	3	2	1	0
RW	—					AFECK_DUR		
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:3	—	Reserved
2:0	AFECK_DUR	AFECK pulse duration 000 = 0.5 cycle 001 = (Default) 1.0 cycle 010 = 1.5 cycle 011 = 2.0 cycle 100 = 2.5 cycle 101 = 3.0 cycle 110 = 3.5 cycle 111 = 4.0 cycle

7.1.12 CCM_AFECLK_CFG_2

BANK0 Address: 0x22

	7	6	5	4	3	2	1	0
RW	RSMP_EXT_DLY			VSMP_EXT_DLY				VSMP_EXT_POL
Default	0	0	1	0	0	0	0	0

Bits	Name	Description
7:5	RSMP_EXT_DLY	Timing Mode 2, internal RSMP latency from internal VSMP 000 = 2 clocks 001 = (Default) 3 clocks … 111 = 9 clocks

Bits	Name	Description
4:1	VSMP_EXT_DLY	Timing Mode 2, internal VSMP latency from VSMP_EXT input 0x0 = (Default) 1 clocks … 0xF = 16 clocks 0x1 = 2 clocks
0	VSMP_EXT_POL	Timing Mode 2, VSMP polarity 0 = (Default) VSMP is detected at rising edge of input pad 1 = VSMP is detected at falling edge of input pad

7.1.13 DEVICE_CTRL_0

BANK0 Address: 0x28

RW	7	6	5	4	3	2	1	0
	LDO4_EN	SHARED_BUS_MODE	—			ACTIVE_EN	READY_EN	MSM_EN
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7	LDO4_EN	LDO4 Enable. Generates 3.3 V supply to VDD_A. Note that LDO4 can also be enabled using the LDO_EN input pin. 0 = (Default) Disabled 1 = Enabled
6	SHARED_BUS_MODE	Enables SPI control interface to be shared with CMOS data outputs. If this bit is set, the DOUTn pins are configured HiZ during SPI access (while $\overline{\text{SPI\_CS}}$ is low), allowing the DOUTn pins to be shared with the SPI control interface. If SPI and DOUT pins are connected on the PCB, this bit MUST be set before setting READY_EN=1 in order to avoid bus contention. 0 = (Default) Disabled. Bus sharing of the SPI/DOUT pins is not supported. 1 = Enabled. DOUTn are HiZ during SPI access, allowing bus sharing of the SPI/DOUT pins.
5:3	—	Reserved
2	ACTIVE_EN	Selects the ACTIVE state. This bit causes a transition from READY to the ACTIVE state. Note the READY_EN bit must also be set. 0 = (Default) No action 1 = Select ACTIVE state
1	READY_EN	Selects READY state. After the device has been configured, this bit causes a transition from IDLE to the READY state. 0 = (Default) No action 1 = Select READY state
0	MSM_EN	Enables the main state machine (MSM) control. This bit must be set to support any operational control. 0 = Disabled. Operational control not supported. 1 = (Default) Enabled. Operational control is enabled.

7.1.14 DEVICE_CTRL_1

BANK0 Address: 0x29

RW	7	6	5	4	3	2	1	0
	TEMP_ERROR_RST_MASK	—	TEMP_ERROR_CLR			—		
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	TEMP_ERROR_RST_MASK	Selects whether an overtemperature error causes a system reset. 0 = (Default) Disabled. Device reset is triggered on overtemperature. 1 = Enabled. Device shuts down on overtemperature, but does not trigger a reset.
6	—	Reserved
5	TEMP_ERROR_CLR	Following an overtemperature error, this bit enables a transition to the IDLE state (provided the error has cleared). This bit should be cleared by the host after the device has entered the IDLE state. 0 = (Default) No action 1 = Clear the overtemperature error and move to IDLE state
4:0	—	Reserved

7.1.15 DEVICE_CTRL_2

BANK0 Address: 0x2A

RW	7	6	5	4	3	2	1	0
	LDO4_HIZ	—	LDO_EN_MASK	LDO5_EN	LDO5_ILIMIT_VPC	LDO5_ILIMIT_CTRL		
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7	LDO4_HIZ	Configures the LDO4 output floating (HiZ). 0 = (Default) LDO4 discharged when disabled 1 = LDO4 output HiZ
6	—	Reserved
5	LDO_EN_MASK	Masks the LDO_EN control input. If masked, the LDO_EN pin has no effect on the LDO4/LDO5 regulators. 0 = (Default) Unmasked. LDO4/LDO5 enabled if LDO_EN is asserted 1 = Masked. LDO_EN pin has no control over LDO4/LDO5
4	LDO5_EN	LDO5 Enable. Generates power for external sensor or VDD_IO. Note that LDO5 can also be enabled using the LDO_EN input pin. 0 = (Default) Disabled 1 = Enabled
3	LDO5_ILIMIT_VPC	Enables voltage-proportional control (VPC) for LDO5 current limit 0 = Disabled. Current limit set by LDO5_ILIMIT_CTRL 1 = (Default) Enabled. Current limit scales with output voltage
2:0	LDO5_ILIMIT_CTRL	LDO5 current limit (assumes VPC proportional control is disabled). If VPC is enabled (LDO5_ILIMIT_VPC=1), the current limit scales with output voltage. If VPC is enabled, the selected current limit must not exceed 260 mA. 000 = (Default) 195 mA 001 = 130 mA 010 = 65 mA 011 = Reserved 100 = 455 mA (Do not use if VPC is enabled) 101 = 390 mA (Do not use if VPC is enabled) 110 = 325 mA (Do not use if VPC is enabled) 111 = 260 mA

7.1.16 DEVICE_CTRL_3

BANK0 Address: 0x2B

RW	7	6	5	4	3	2	1	0
	—			LDO5_VOUT				
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4:0	LDO5_VOUT	LDO5 output voltage 0x00 = (Default) 3.424 V 0x01 = 3.492 V 0x02 = 3.56 V 0x03–0x19 = Reserved 0x1A = 3.016 V 0x1B = 3.084 V 0x1C = 3.152 V 0x1D = 3.22 V 0x1E = 3.288 V 0x1F = 3.356 V

7.1.17 RLCDAC_CTRL_0

BANK0 Address: 0x2C

RW	7	6	5	4	3	2	1	0
	—							VBIAS_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	VBIAS_EN	Enables VBIAS in the ACTIVE state 0 = (Default) VBIAS not enabled during conversions 1 = VBIAS enabled during conversions

7.1.18 RLCDAC_CTRL_1

BANK0 Address: 0x2D

RW	7	6	5	4	3	2	1	0
	—				VBIAS_LVL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4:0	VBIAS_LVL	VBIAS output level 0x00 = (Default) 0.17 V 0x01 = 0.25 V … 0x1F = 2.65 V

7.1.19 RLCDAC_CTRL_2

BANK0 Address: 0x2E

RW	7	6	5	4	3	2	1	0
	—				VBIAS_ISEL_BOOST	VBIAS_ISEL		VBIAS_REF
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:4	—	Reserved
3	VBIAS_ISEL_BOOST	VBIAS output drive strength doubler 0 = (Default) No doubling of current reference 1 = Double current reference
2:1	VBIAS_ISEL	VBIAS output drive strength. Note the drive strength is doubled if VBIAS_ISEL_BOOST is set. 00 = (Default) 2 mA 01 = 3 mA 10 = 4 mA 11 = Reserved
0	VBIAS_REF	VBIAS reference select 0 = Reference is VDDA 1 = (Default) Reference is VREF

7.1.20 OP_FORMAT_CFG1_0

BANK0 Address: 0x30

RW	7	6	5	4	3	2	1	0
	—			DOUT_CONFIG	DOUT_PHASE	DOUT_DLY		DOUT_DDR
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7:5	—	Reserved
4	DOUT_CONFIG	Selects data-output configuration 0 = Two pin output (DOUT1-DOUT2) 1 = (Default) Four pin output (DOUT1-DOUT4)
3	DOUT_PHASE	Selects data-output phase timing 0 = Aligned to rising MCLK edge 1 = (Default) Aligned to falling MCLK edge
2:1	DOUT_DLY	Selects additional delay in data-output latency 00 = (Default) 0 sample periods 01 = 1 sample periods 10 = 2 sample periods 11 = 3 sample periods
0	DOUT_DDR	Selects data-output format 0 = Single data rate (SDR) 1 = (Default) Double data rate (DDR)

7.1.21 OP_FORMAT_CFG1_1

BANK0 Address: 0x31

RW	7	6	5	4	3	2	1	0
	—						TEST_PATT_DIR	TEST_PATT_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved

Bits	Name	Description
1	TEST_PATT_DIR	Test pattern ramp direction 0 = (Default) Ramp up 1 = Ramp down
0	TEST_PATT_EN	Enable test pattern 0 = (Default) Disabled 1 = Enabled

7.1.22 LED_EN_SEL_0

BANK0 Address: 0x40

RW	7	6	5	4	3	2	1	0
	RSMP_EXT2_FN	—	LEDB_EN_FN		LEDG_EN_FN		LEDR_EN_FN	
Default	0	0	0	1	0	1	0	1

Bits	Name	Description
7	RSMP_EXT2_FN	RSMP_EXT2 pin function select 0 = (Default) General purpose input/output (GPIO4) 1 = RSMP input for reset sampling
6	—	Reserved
5:4	LEDB_EN_FN	LEDB_EN/RSMP_EXT1 pin function select 00 = Blue LED control input 01 = (Default) RSMP input for reset sampling 10 = General purpose input/output (GPIO3) 11 = Monitor
3:2	LEDG_EN_FN	LEDG_EN/LED_START pin function select 00 = Green LED control input 01 = (Default) External LED Start input 10 = General purpose input/output (GPIO2) 11 = Reserved
1:0	LEDR_EN_FN	LEDR_EN/TGSYNC pin function select 00 = Red LED control input 01 = (Default) External TGSYNC input 10 = General purpose input/output (GPIO1) 11 = Reserved

7.1.23 LED_EN_SEL_2

BANK0 Address: 0x42

RW	7	6	5	4	3	2	1	0
	—			MON_SEL			—	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4:2	MON_SEL	MON pin function select 000 = (Default) VSMP output 001 = RSMP output 010 = AFECK output 011–111 = Reserved
1:0	—	Reserved

7.1.24 GPI_VAL_0

BANK0 Address: 0x44

RO	7	6	5	4	3	2	1	0
	—			GP4_IN_STS	GP3_IN_STS	GP2_IN_STS	GP1_IN_STS	—
Default	0	0	0	X	X	X	X	0

Bits	Name	Description
7:5	—	Reserved
4	GP4_IN_STS	GP4 input status 0 = Low 1 = High
3	GP3_IN_STS	GP3 input status 0 = Low 1 = High
2	GP2_IN_STS	GP2 input status 0 = Low 1 = High

Bits	Name	Description
1	GP1_IN_STS	GP1 input status 0 = Low 1 = High
0	—	Reserved

7.1.25 GPI_VAL_2

BANK0 Address: 0x46

RW	7	6	5	4	3	2	1	0
	—			GP4_DIR	GP3_DIR	GP2_DIR	GP1_DIR	—
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4	GP4_DIR	GPIO4 pin direction 0 = (Default) Input 1 = Output
3	GP3_DIR	GPIO3 pin direction 0 = (Default) Input 1 = Output
2	GP2_DIR	GPIO2 pin direction 0 = (Default) Input 1 = Output
1	GP1_DIR	GPIO1 pin direction 0 = (Default) Input 1 = Output
0	—	Reserved

7.1.26 GPI_VAL_3

BANK0 Address: 0x47

RW	7	6	5	4	3	2	1	0
	—			GP4_OUT_LVL	GP3_OUT_LVL	GP2_OUT_LVL	GP1_OUT_LVL	—
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4	GP4_OUT_LVL	GP4 output level 0 = (Default) Low 1 = High
3	GP3_OUT_LVL	GP3 output level 0 = (Default) Low 1 = High
2	GP2_OUT_LVL	GP2 output level 0 = (Default) Low 1 = High
1	GP1_OUT_LVL	GP1 output level 0 = (Default) Low 1 = High
0	—	Reserved

7.1.27 CMOS_CFG_0

BANK0 Address: 0x48

RW	7	6	5	4	3	2	1	0
	—	DOUT4_SPI_SDO_DRV_STR			DOUT4_SPI_SDO_PULL		DOUT4_SPI_SDO_HIZ_EN	DOUT4_SPI_SDO_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	DOUT4_SPI_SDO_DRV_STR	DOUT4/SPI_SDO output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DOUT4_SPI_SDO_PULL	DOUT4/SPI_SDO pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DOUT4_SPI_SDO_HIZ_EN	DOUT4/SPI_SDO High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT4_SPI_SDO_IE	SPI_SDO input enable 0 = Disabled 1 = (Default) Enabled

7.1.28 CMOS_CFG_1

BANK0 Address: 0x49

RW	7	6	5	4	3	2	1	0
	—	SPI_SDI_DRV_STR			SPI_SDI_PULL		SPI_SDI_HIZ_EN	SPI_SDI_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	SPI_SDI_DRV_STR	SPI_SDI output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	SPI_SDI_PULL	SPI_SDI pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	SPI_SDI_HIZ_EN	SPI_SDI High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	SPI_SDI_IE	SPI_SDI input enable 0 = Disabled 1 = (Default) Enabled

7.1.29 CMOS_CFG_2

BANK0 Address: 0x4A

RW	7	6	5	4	3	2	1	0
	—				SPI_SCK_PULL		—	SPI_SCK_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7:4	—	Reserved
3:2	SPI_SCK_PULL	SPI_SCK pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	—	Reserved
0	SPI_SCK_IE	SPI_SCK input enable 0 = Disabled 1 = (Default) Enabled

7.1.30 CMOS_CFG_3

BANK0 Address: 0x4B

RW	7	6	5	4	3	2	1	0
	—				SPI_CS_PULL		—	SPI_CS_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7:4	—	Reserved
3:2	SPI_CS_PULL	$\overline{\text{SPI\_CS}}$ pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	—	Reserved
0	SPI_CS_IE	$\overline{\text{SPI\_CS}}$ input enable 0 = Disabled 1 = (Default) Enabled

7.1.31 MCLK_CFG

BANK0 Address: 0x4D

RW	7	6	5	4	3	2	1	0
	—				MCLK_PULL		MCLK_HIZ_EN	MCLK_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7:4	—	Reserved
3:2	MCLK_PULL	MCLK_EXT pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	MCLK_HIZ_EN	MCLK_EXT High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	MCLK_IE	MCLK_EXT input enable 0 = Disabled 1 = (Default) Enabled

7.1.32 LED_EN_CFG_0

BANK0 Address: 0x50

RW	7	6	5	4	3	2	1	0
	—	LEDR_EN_TGSYNC_GPIO1_DRV_STR			LEDR_EN_TGSYNC_GPIO1_PULL		LEDR_EN_TGSYNC_GPIO1_HIZ_EN	LEDR_EN_TGSYNC_GPIO1_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	LEDR_EN_TGSYNC_GPIO1_DRV_STR	LEDR_EN/TGSYNC/GPIO1 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	LEDR_EN_TGSYNC_GPIO1_PULL	LEDR_EN/TGSYNC/GPIO1 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	LEDR_EN_TGSYNC_GPIO1_HIZ_EN	LEDR_EN/TGSYNC/GPIO1 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	LEDR_EN_TGSYNC_GPIO1_IE	LEDR_EN/TGSYNC/GPIO1 input enable 0 = Disabled 1 = (Default) Enabled

7.1.33 LED_EN_CFG_1

BANK0 Address: 0x51

RW	7	6	5	4	3	2	1	0
	—	LEDG_EN_LEDSTART_GPIO2_DRV_STR			LEDG_EN_LEDSTART_GPIO2_PULL		LEDG_EN_LEDSTART_GPIO2_HIZ_EN	LEDG_EN_LEDSTART_GPIO2_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	LEDG_EN_LEDSTART_GPIO2_DRV_STR	LEDG_EN/LED_START/GPIO2 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	LEDG_EN_LEDSTART_GPIO2_PULL	LEDG_EN/LED_START/GPIO2 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	LEDG_EN_LEDSTART_GPIO2_HIZ_EN	LEDG_EN/LED_START/GPIO2 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	LEDG_EN_LEDSTART_GPIO2_IE	LEDG_EN/LED_START/GPIO2 input enable 0 = Disabled 1 = (Default) Enabled

7.1.34 LED_EN_CFG_2

BANK0 Address: 0x52

RW	7	6	5	4	3	2	1	0
	—	LEDB_EN_MON_RSMP_EXT_GPIO3_DRV_STR			LEDB_EN_MON_RSMP_EXT_GPIO3_PULL		LEDB_EN_MON_RSMP_EXT_GPIO3_HIZ_EN	LEDB_EN_MON_RSMP_EXT_GPIO3_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	LEDB_EN_MON_RSMP_EXT_GPIO3_DRV_STR	LEDB_EN/MON/RSMP_EXT1/GPIO3 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	LEDB_EN_MON_RSMP_EXT_GPIO3_PULL	LEDB_EN/MON/RSMP_EXT1/GPIO3 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	LEDB_EN_MON_RSMP_EXT_GPIO3_HIZ_EN	LEDB_EN/MON/RSMP_EXT1/GPIO3 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	LEDB_EN_MON_RSMP_EXT_GPIO3_IE	LEDB_EN/MON/RSMP_EXT1/GPIO3 input enable 0 = Disabled 1 = (Default) Enabled

7.1.35 LED_EN_CFG_3

BANK0 Address: 0x53

RW	7	6	5	4	3	2	1	0
	—	RSMP_GPIO4_DRV_STR			RSMP_GPIO4_PULL		RSMP_GPIO4_HIZ_EN	RSMP_GPIO4_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	RSMP_GPIO4_DRV_STR	RSMP_EXT2/GPIO4 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	RSMP_GPIO4_PULL	RSMP_EXT2/GPIO4 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper

Bits	Name	Description
1	RSMP_GPIO4_HIZ_EN	RSMP_EXT2/GPIO4 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	RSMP_GPIO4_IE	RSMP_EXT2/GPIO4 input enable 0 = Disabled 1 = (Default) Enabled

7.1.36 VSMP_EXT_CFG

BANK0 Address: 0x54

RW	7	6	5	4	3	2	1	0
	—	VSMP_EXT_DRV_STR			VSMP_EXT_PULL		VSMP_EXT_HIZ_EN	VSMP_EXT_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	VSMP_EXT_DRV_STR	VSMP_EXT output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	VSMP_EXT_PULL	VSMP_EXT pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	VSMP_EXT_HIZ_EN	VSMP_EXT High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	VSMP_EXT_IE	VSMP_EXT input enable 0 = Disabled 1 = (Default) Enabled

7.1.37 DOUT_CFG_0

BANK0 Address: 0x58

RW	7	6	5	4	3	2	1	0
	—	DOUT1_DRV_STR			DOUT1_PULL		DOUT1_HIZ_EN	DOUT1_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DOUT1_DRV_STR	DOUT1 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DOUT1_PULL	DOUT1 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DOUT1_HIZ_EN	DOUT1 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT1_IE	DOUT1 input enable 0 = (Default) Disabled 1 = Enabled

7.1.38 DOUT_CFG_1

BANK0 Address: 0x59

RW	7	6	5	4	3	2	1	0
	—	DOUT2_DRV_STR			DOUT2_PULL		DOUT2_HIZ_EN	DOUT2_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DOUT2_DRV_STR	DOUT2 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DOUT2_PULL	DOUT2 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DOUT2_HIZ_EN	DOUT2 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT2_IE	DOUT2 input enable 0 = (Default) Disabled 1 = Enabled

7.1.39 DOUT_CFG_2

BANK0 Address: 0x5A

RW	7	6	5	4	3	2	1	0
	—	DOUT3_DRV_STR			DOUT3_PULL		DOUT3_HIZ_EN	DOUT3_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DOUT3_DRV_STR	DOUT3 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DOUT3_PULL	DOUT3 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DOUT3_HIZ_EN	DOUT3 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT3_IE	DOUT3 input enable 0 = (Default) Disabled 1 = Enabled

7.2 BANK1—DAC, PGA, DGAIN, SARADC, LED Control

7.2.1 BANK

BANKn (n = 0–7) Address: 0x00

	7	6	5	4	3	2	1	0
	DESCRIM				—	BANK		
Access	RO				—	RW		
Default	1	1	0	0	0	0	0	0

Bits	Name	Description
7:4	DESCRIM	Read-only device identifier field. Readback value is 0xC.
3	—	Reserved
2:0	BANK	Selects the active bank for SPI access. 000 = (Default) Bank 0 001 = Bank 1 010 = Bank 2 011 = Bank 3 100 = Bank 4 101 = Bank 5 110 = Bank 6 111 = Bank 7

7.2.2 ASYNC0_0

BANKn (n = 0–7) Address: 0x04

RO	7	6	5	4	3	2	1	0
	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	—	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	ACTIVE_ERROR_STS	Path error status. Indicates an error condition in the Active or Ready states. 0 = (Default) Normal 1 = Error
4	TEMP_ERROR_STS	Temperature error status. Indicates an overtemperature condition has been detected. 0 = (Default) Normal 1 = Error
3	—	Reserved
2	MCLK_ERROR_STS	MCLK error status. Indicates MCLK is invalid or absent in the Idle State. 0 = (Default) Normal 1 = Error
1	STARTUP_ERROR_STS	Start up error status. Indicates an error detected during start-up. 0 = (Default) Normal 1 = Error
0	BOOT_ERROR_STS	Boot error status. Indicates an error detected during boot. 0 = (Default) Normal 1 = Error

7.2.3 ASYNC0_1

BANKn (n = 0–7) Address: 0x05

RW	7	6	5	4	3	2	1	0
	—							OSC_DISABLE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	OSC_DISABLE	Oscillator disable. Setting this bit places the device in a low-power Sleep State. Note that the host must return the device to the Idle State before writing to any other control registers. 0 = (Default) RCO enabled 1 = RCO disabled

7.2.4 SFT_RESET

BANKn (n = 0–7) Address: 0x08

WO	7	6	5	4	3	2	1	0
	SFT_RESET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	SFT_RESET	Software reset. Write 0x5A to execute a software reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved

7.2.5 DAC_CTRL_OFS01_CH1_0

BANK1 Address: 0x10

	7	6	5	4	3	2	1	0
RW	CH1_SEQ0_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ0_ OFFSET_0	DAC offset for Channel 1, State 0 This field contains bits [7:0] of the 9-bit code. Note the effective offset on the signal path is only 2/3 of this value, i.e., –333.3 mV to 331.998 mV. 0 = –500 mV 256 = 0 mV 511 = 498.05 mV

7.2.6 DAC_CTRL_OFS01_CH1_1

BANK1 Address: 0x11

	7	6	5	4	3	2	1	0
RW	—							CH1_SEQ0_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH1_SEQ0_ OFFSET_1	DAC offset for Channel 1, State 0 This field contains bit [8] of the 9-bit code. Note the effective offset on the signal path is only 2/3 of this value, i.e., –333.3 mV to 331.998 mV. 0 = –500 mV 256 = 0 mV 511 = 498.05 mV

7.2.7 DAC_CTRL_OFS01_CH1_2

BANK1 Address: 0x12

	7	6	5	4	3	2	1	0
RW	CH1_SEQ1_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ1_ OFFSET_0	DAC offset for Channel 1, State 1 This field contains bits [7:0] of the 9-bit code. Note the effective offset on the signal path is only 2/3 of this value, i.e., –333.3 mV to 331.998 mV. 0 = –500 mV 256 = 0 mV 511 = 498.05 mV

7.2.8 DAC_CTRL_OFS01_CH1_3

BANK1 Address: 0x13

	7	6	5	4	3	2	1	0
RW	—							CH1_SEQ1_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH1_SEQ1_ OFFSET_1	DAC offset for Channel 1, State 1 This field contains bit [8] of the 9-bit code. Note the effective offset on the signal path is only 2/3 of this value, i.e., –333.3 mV to 331.998 mV. 0 = –500 mV 256 = 0 mV 511 = 498.05 mV

7.2.9 DAC_CTRL_OFS23_CH1_0

BANK1 Address: 0x14

	7	6	5	4	3	2	1	0
RW	CH1_SEQ2_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ2_ OFFSET_0	DAC offset for Channel 1, State 2 This field contains bits [7:0] of the 9-bit code. Note the effective offset on the signal path is only 2/3 of this value, i.e., –333.3 mV to 331.998 mV. 0 = –500 mV 256 = 0 mV 511 = 498.05 mV

7.2.10 DAC_CTRL_OFS23_CH1_1

BANK1 Address: 0x15

	7	6	5	4	3	2	1	0
RW	—							CH1_SEQ2_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH1_SEQ2_ OFFSET_1	DAC offset for Channel 1, State 2 This field contains bit [8] of the 9-bit code. Note the effective offset on the signal path is only 2/3 of this value, i.e., –333.3 mV to 331.998 mV. 0 = –500 mV 256 = 0 mV 511 = 498.05 mV

7.2.11 DAC_CTRL_OFS23_CH1_2

BANK1 Address: 0x16

	7	6	5	4	3	2	1	0
RW	CH1_SEQ3_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ3_ OFFSET_0	DAC offset for Channel 1, State 3 This field contains bits [7:0] of the 9-bit code. Note the effective offset on the signal path is only 2/3 of this value, i.e., –333.3 mV to 331.998 mV. 0 = –500 mV 256 = 0 mV 511 = 498.05 mV

7.2.12 DAC_CTRL_OFS23_CH1_3

BANK1 Address: 0x17

	7	6	5	4	3	2	1	0
RW	—							CH1_SEQ3_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH1_SEQ3_ OFFSET_1	DAC offset for Channel 1, State 3 This field contains bit [8] of the 9-bit code. Note the effective offset on the signal path is only 2/3 of this value, i.e., –333.3 mV to 331.998 mV. 0 = –500 mV 256 = 0 mV 511 = 498.05 mV

7.2.13 PGA_CTRL_AGAIN_CH1_0

BANK1 Address: 0x1C

RW	7	6	5	4	3	2	1	0
	—				CH1_SEQ0_AGAIN			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH1_SEQ0_AGAIN	Analog gain for Channel 1, State 0 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

7.2.14 PGA_CTRL_AGAIN_CH1_1

BANK1 Address: 0x1D

RW	7	6	5	4	3	2	1	0
	—				CH1_SEQ1_AGAIN			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH1_SEQ1_AGAIN	Analog gain for Channel 1, State 1 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

7.2.15 PGA_CTRL_AGAIN_CH1_2

BANK1 Address: 0x1E

RW	7	6	5	4	3	2	1	0
	—				CH1_SEQ2_AGAIN			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH1_SEQ2_AGAIN	Analog gain for Channel 1, State 2 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

7.2.16 PGA_CTRL_AGAIN_CH1_3

BANK1 Address: 0x1F

RW	7	6	5	4	3	2	1	0
	—				CH1_SEQ3_AGAIN			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH1_SEQ3_AGAIN	Analog gain for Channel 1, State 3 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

7.2.17 DGAIN_SEQ01_CH1_0

BANK1 Address: 0x20

RW	7	6	5	4	3	2	1	0
	CH1_SEQ0_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ0_DGAIN_0	Digital gain for Channel 1, State 0 Gain = [DGAIN/2048]. Valid from 1024 to 4095. This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

7.2.18 DGAIN_SEQ01_CH1_1

BANK1 Address: 0x21

RW	7	6	5	4	3	2	1	0
	—				CH1_SEQ0_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH1_SEQ0_DGAIN_1	Digital gain for Channel 1, State 0 Gain = [DGAIN/2048]. Valid from 1024 to 4095. This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

7.2.19 DGAIN_SEQ01_CH1_2

BANK1 Address: 0x22

RW	7	6	5	4	3	2	1	0
	CH1_SEQ1_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ1_DGAIN_0	Digital gain for Channel 1, State 1 Gain = [DGAIN/2048]. Valid from 1024 to 4095. This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

7.2.20 DGAIN_SEQ01_CH1_3

BANK1 Address: 0x23

RW	7	6	5	4	3	2	1	0
	—				CH1_SEQ1_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH1_SEQ1_DGAIN_1	Digital gain for Channel 1, State 1 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

7.2.21 DGAIN_SEQ23_CH1_0

BANK1 Address: 0x24

	7	6	5	4	3	2	1	0
RW	CH1_SEQ2_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ2_DGAIN_0	Digital gain for Channel 1, State 2 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

7.2.22 DGAIN_SEQ23_CH1_1

BANK1 Address: 0x25

	7	6	5	4	3	2	1	0
RW	—				CH1_SEQ2_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH1_SEQ2_DGAIN_1	Digital gain for Channel 1, State 2 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

7.2.23 DGAIN_SEQ23_CH1_2

BANK1 Address: 0x26

	7	6	5	4	3	2	1	0
RW	CH1_SEQ3_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ3_DGAIN_0	Digital gain for Channel 1, State 3 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

7.2.24 DGAIN_SEQ23_CH1_3

BANK1 Address: 0x27

	7	6	5	4	3	2	1	0
RW	—				CH1_SEQ3_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH1_SEQ3_DGAIN_1	Digital gain for Channel 1, State 3 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

7.2.25 DGAIN_REF_CH1_0

BANK1 Address: 0x28

	7	6	5	4	3	2	1	0
RW	CH1_SEQ0_DGAIN_REF							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ0_DGAIN_REF	Digital gain reference level for Channel 1, State 0 The digital gain is applied relative to the reference level. 0x00 = (Default) 0 0x01 = 16 0x02 = 32 0x03 = 48 … 0xFF = 4,080

7.2.26 DGAIN_REF_CH1_1

BANK1 Address: 0x29

	7	6	5	4	3	2	1	0
RW	CH1_SEQ1_DGAIN_REF							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ1_DGAIN_REF	Digital gain reference level for Channel 1, State 1 The digital gain is applied relative to the reference level. 0x00 = (Default) 0 0x01 = 16 0x02 = 32 0x03 = 48 … 0xFF = 4,080

7.2.27 DGAIN_REF_CH1_2

BANK1 Address: 0x2A

	7	6	5	4	3	2	1	0
RW	CH1_SEQ2_DGAIN_REF							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ2_DGAIN_REF	Digital gain reference level for Channel 1, State 2 The digital gain is applied relative to the reference level. 0x00 = (Default) 0 0x01 = 16 0x02 = 32 0x03 = 48 … 0xFF = 4,080

7.2.28 DGAIN_REF_CH1_3

BANK1 Address: 0x2B

	7	6	5	4	3	2	1	0
RW	CH1_SEQ3_DGAIN_REF							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ3_DGAIN_REF	Digital gain reference level for Channel 1, State 3 The digital gain is applied relative to the reference level. 0x00 = (Default) 0 0x01 = 16 0x02 = 32 0x03 = 48 … 0xFF = 4,080

7.2.29 SAR1_CTRL_1

BANK1 Address: 0x2D

	7	6	5	4	3	2	1	0
RW	—					CH1_POL	—	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	CH1_POL	Signal polarity selection 0 = (Default) Positive signalling (CIS waveform) 1 = Negative signalling (CCD waveform)
1:0	—	Reserved

7.2.30 SAR1_CTRL_3

BANK1 Address: 0x2F

RW	7	6	5	4	3	2	1	0
	—						CH1_AFE_POWER	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1:0	CH1_AFE_POWER	AFE power mode selection. 00 = Low Power 01–10 = Reserved 11 = (Default) High Performance

7.2.31 LED_CTRL_CONFIG_0

BANK1 Address: 0x40

RW	7	6	5	4	3	2	1	0
	—				LED_CTRL_SRC	LEDB_EN	LEDG_EN	LEDR_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3	LED_CTRL_SRC	Select control source for LED drivers 0 = (Default) Internal 1 = External
2	LEDB_EN	LEDB driver control 0 = (Default) Disabled 1 = Enabled
1	LEDG_EN	LEDG driver control 0 = (Default) Disabled 1 = Enabled
0	LEDR_EN	LEDR driver control 0 = (Default) Disabled 1 = Enabled

7.2.32 LED_CTRL_CONFIG_1

BANK1 Address: 0x41

RW	7	6	5	4	3	2	1	0
	—				LED_RAMP_TIME			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	LED_RAMP_TIME	LED ramp time. Time taken to ramp fine current (LEDn_FINE) from 0-255. 0x0–0x7 = (Default) 8 us 0x8 = 9 us 0x9 = 10 us … 0xF = 16 us

7.2.33 LED_CTRL_CONFIG_2

BANK1 Address: 0x42

RW	7	6	5	4	3	2	1	0
	LED_RAMP_BOOST		LEDB_COARSE		LEDG_COARSE		LEDR_COARSE	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	LED_RAMP_BOOST	LED ramp boost. Shortens the ramp time by a factor of 2 or 4. Boost by 2 is only valid if MCLK rate >= 4 MHz. Boost by 4 is only valid if MCLK rate >= 12 MHz and LED_RAMP_TIME >= 0xB. If an invalid selection is made, the boost is disabled and the unmodified LED_RAMP_TIME is used. 00 = (Default) No boost 01 = Boost by 2 10 = Boost by 4 11 = Reserved
5:4	LEDB_COARSE	LEDB coarse current control. This is the output current if LEDB_FINE=255. 00 = (Default) 33 mA 01 = 41 mA 10 = 49 mA 11 = 66 mA

Bits	Name	Description
3:2	LEDG_COARSE	LEDG coarse current control. This is the output current if LEDG_FINE=255. 00 = (Default) 33 mA 01 = 41 mA 10 = 49 mA 11 = 66 mA
1:0	LEDR_COARSE	LEDR coarse current control. This is the output current if LEDR_FINE=255. 00 = (Default) 33 mA 01 = 41 mA 10 = 49 mA 11 = 66 mA

7.2.34 LED_CTRL_CONFIG_3

BANK1 Address: 0x43

	7	6	5	4	3	2	1	0
RW	MCLK_FREQ							
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:0	MCLK_FREQ	MCLK frequency. This field must be set to the frequency closest to that of the MCLK_EXT input. 0x00–0x01 = Reserved 0x02 = 2 MHz 0x03 = 3 MHz … 0x0A = (Default) 10 MHz … 0x30 = 48 MHz 0x31–0xFF = Reserved

7.2.35 LEDX_FINE_0

BANK1 Address: 0x44

	7	6	5	4	3	2	1	0
RW	LEDR_FINE							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LEDR_FINE	LEDR fine current control. Selects the output current from 0 to LEDR_COARSE. If the LEDR output is enabled, the current ramps to (LEDR_FINE/255 * LEDR_COARSE)

7.2.36 LEDX_FINE_1

BANK1 Address: 0x45

	7	6	5	4	3	2	1	0
RW	LEDG_FINE							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LEDG_FINE	LEDG fine current control. Selects the output current from 0 to LEDG_COARSE. If the LEDG output is enabled, the current ramps to (LEDG_FINE/255 * LEDG_COARSE)

7.2.37 LEDX_FINE_2

BANK1 Address: 0x46

	7	6	5	4	3	2	1	0
RW	LEDB_FINE							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LEDB_FINE	LEDB fine current control. Selects the output current from 0 to LEDB_COARSE. If the LEDB output is enabled, the current ramps to (LEDB_FINE/255 * LEDB_COARSE)

7.2.38 TG_FILT_CONFIG_0

BANK1 Address: 0x48

	7	6	5	4	3	2	1	0
RW	—			LEDSTART_POL	—	TGSYNC_IN_POL	TGSYNC_IN_SRC	
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7:5	—	Reserved
4	LEDSTART_POL	LEDSTART input polarity. 0 = (Default) Active high 1 = Active low
3	—	Reserved

Bits	Name	Description
2	TGSYNC_IN_POL	TGSYNC input polarity. 0 = Active high 1 = (Default) Active low
1:0	TGSYNC_IN_SRC	TGSYNC input source selection 00 = (Default) TGSYNC 01 = Reserved 10 = LEDSTART 11 = Reserved

7.2.39 TG_FILT_CONFIG_1

BANK1 Address: 0x49

RW	7	6	5	4	3	2	1	0
	MCLK_SYNC_POL	TGSYNC_FILT_STAGE			TGSYNC_FILT_DECM			TGSYNC_FILT_EN
Default	0	1	0	0	0	1	1	0

Bits	Name	Description
7	MCLK_SYNC_POL	Selects the active edge of the MCLK input, for TGSYNC/LEDSTART timing. 0 = (Default) Falling 1 = Rising
6:4	TGSYNC_FILT_STAGE	TGSYNC filter stage selection 000 = 2 stage 001 = 4 stage 010 = 6 stage 011 = 8 stage 100 = (Default) 10 stage 101–111 = Reserved
3:1	TGSYNC_FILT_DECM	TGSYNC filter decimation frequency division ratio 000 = 1 divs 001 = 2 divs … 011 = (Default) 4 divs … 111 = 8 divs
0	TGSYNC_FILT_EN	TGSYNC input filter enable 0 = (Default) Disabled 1 = Enabled

7.2.40 PWM_CONFIG_0

BANK1 Address: 0x4C

RW	7	6	5	4	3	2	1	0
	LED_CLK_DIV				—		NUM_SEQ_STATES	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	LED_CLK_DIV	Configures the MCLK division for the LED_CLK pulse waveform. The divided MCLK controls the resolution (step-size) of the LED_CLK period/duty-cycle parameters. 0x0 = (Default) 1 clocks 0x1 = 2 clocks … 0xF = 16 clocks
3:2	—	Reserved
1:0	NUM_SEQ_STATES	Number of sequence states 00 = (Default) 1 state 01 = 2 state 10 = 3 state 11 = 4 state

7.2.41 PWM_CONFIG_1

BANK1 Address: 0x4D

RW	7	6	5	4	3	2	1	0
	LEDG_SEQ_SEL				LEDR_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	LEDG_SEQ_SEL	LEDG sequence state select Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3
3:0	LEDR_SEQ_SEL	LEDR sequence state select Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

7.2.42 PWM_CONFIG_2

BANK1 Address: 0x4E

RW	7	6	5	4	3	2	1	0
	—				LEDB_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	LEDB_SEQ_SEL	LEDB sequence state select Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

7.2.43 PWM_CONFIG_3

BANK1 Address: 0x4F

RW	7	6	5	4	3	2	1	0
	—		TGSYNC_SEQ_RST	TGSYNC_SINGLE_SEQ	LEDSTART_SEQ_INIT	IN_SEQ_SEL		ACYC_EN
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:6	—	Reserved
5	TGSYNC_SEQ_RST	Selects what action is taken if TGSYNC is asserted before the configured length of the state sequence. Valid for Multi Cycle mode only. 0 = (Default) TGSYNC is ignored 1 = TGSYNC restarts sequence
4	TGSYNC_SINGLE_SEQ	Cycle mode selection Multi Cycle: one TGSYNC pulse triggers a full cycle of the configured number of states Single Cycle: a TGSYNC pulse is required for each state transition 0 = (Default) Multi Cycle 1 = Single Cycle
3	LEDSTART_SEQ_INIT	Sequence start condition selection If this bit is set, the TG sequence can only be initiated using the TGSYNC and LEDSTART signals together. 0 = (Default) TGSYNC 1 = TGSYNC and LEDSTART
2:1	IN_SEQ_SEL	Sequence-state select for PGA gain, DC offset, and digital gain. Only valid if auto-cycle is disabled. 00 = (Default) State 0 01 = State 1 10 = State 2 11 = State 3
0	ACYC_EN	Enables auto-cycle of gain/offset configuration 0 = Disabled 1 = (Default) Enabled

7.2.44 PWM_S0_CFG_0

BANK1 Address: 0x50

	7	6	5	4	3	2	1	0
RW	LED_SEQ0_PERIOD_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LED_SEQ0_ PERIOD_0	LED_CLK period in State 0. This field contains bits [7:0] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.45 PWM_S0_CFG_1

BANK1 Address: 0x51

	7	6	5	4	3	2	1	0
RW	—	LED_SEQ0_PERIOD_1						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ0_ PERIOD_1	LED_CLK period in State 0. This field contains bits [14:8] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.46 PWM_S0_CFG_2

BANK1 Address: 0x52

	7	6	5	4	3	2	1	0
RW	LED_SEQ0_DUTY_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LED_SEQ0_DUTY_0	LED_CLK duty cycle in State 0. This field contains bits [7:0] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.47 PWM_S0_CFG_3

BANK1 Address: 0x53

	7	6	5	4	3	2	1	0
RW	—	LED_SEQ0_DUTY_1						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ0_DUTY_1	LED_CLK duty cycle in State 0. This field contains bits [14:8] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.48 PWM_S1_CFG_0

BANK1 Address: 0x54

	7	6	5	4	3	2	1	0
RW	LED_SEQ1_PERIOD_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LED_SEQ1_ PERIOD_0	LED_CLK period in State 1. This field contains bits [7:0] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.49 PWM_S1_CFG_1

BANK1 Address: 0x55

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ1_PERIOD_1						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ1_PERIOD_1	LED_CLK period in State 1. This field contains bits [14:8] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.50 PWM_S1_CFG_2

BANK1 Address: 0x56

RW	7	6	5	4	3	2	1	0
	LED_SEQ1_DUTY_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LED_SEQ1_DUTY_0	LED_CLK duty cycle in State 1. This field contains bits [7:0] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.51 PWM_S1_CFG_3

BANK1 Address: 0x57

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ1_DUTY_1						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ1_DUTY_1	LED_CLK duty cycle in State 1. This field contains bits [14:8] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.52 PWM_S2_CFG_0

BANK1 Address: 0x58

RW	7	6	5	4	3	2	1	0
	LED_SEQ2_PERIOD_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LED_SEQ2_PERIOD_0	LED_CLK period in State 2. This field contains bits [7:0] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.53 PWM_S2_CFG_1

BANK1 Address: 0x59

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ2_PERIOD_1						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ2_PERIOD_1	LED_CLK period in State 2. This field contains bits [14:8] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.54 PWM_S2_CFG_2

BANK1 Address: 0x5A

RW	7	6	5	4	3	2	1	0
	LED_SEQ2_DUTY_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LED_SEQ2_DUTY_0	LED_CLK duty cycle in State 2. This field contains bits [7:0] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.55 PWM_S2_CFG_3

BANK1 Address: 0x5B

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ2_DUTY_1						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ2_DUTY_1	LED_CLK duty cycle in State 2. This field contains bits [14:8] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.56 PWM_S3_CFG_0

BANK1 Address: 0x5C

RW	7	6	5	4	3	2	1	0
	LED_SEQ3_PERIOD_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LED_SEQ3_PERIOD_0	LED_CLK period in State 3. This field contains bits [7:0] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.57 PWM_S3_CFG_1

BANK1 Address: 0x5D

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ3_PERIOD_1						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ3_PERIOD_1	LED_CLK period in State 3. This field contains bits [14:8] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.58 PWM_S3_CFG_2

BANK1 Address: 0x5E

RW	7	6	5	4	3	2	1	0
	LED_SEQ3_DUTY_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LED_SEQ3_DUTY_0	LED_CLK duty cycle in State 3. This field contains bits [7:0] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.59 PWM_S3_CFG_3

BANK1 Address: 0x5F

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ3_DUTY_1						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ3_DUTY_1	LED_CLK duty cycle in State 3. This field contains bits [14:8] of the 15-bit code, valid from 0-32767. The LSB units are equal to the divided MCLK period set by LED_CLK_DIV.

7.2.60 LED_START_STOP1_0

BANK1 Address: 0x60

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ0_START						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ0_START	Selects the first pulse cycle in State 0 in which the LED driver is enabled. The LED driver is enabled in pulse cycles from LED_SEQ0_START through LED_SEQ0_END. 0x00 = (Default) 0 cycles 0x01 = 1 cycles … 0x0F = 15 cycles 0x10–0x7F = Reserved

7.2.61 LED_START_STOP1_1

BANK1 Address: 0x61

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ0_END						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ0_END	Selects the last pulse cycle in State 0 in which the LED driver is enabled. The LED driver is enabled in pulse cycles from LED_SEQ0_START through LED_SEQ0_END. 0x00 = (Default) 0 cycles 0x01 = 1 cycles … 0x0F = 15 cycles 0x10–0x7F = Reserved

7.2.62 LED_START_STOP1_2

BANK1 Address: 0x62

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ1_START						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ1_START	Selects the first pulse cycle in State 1 in which the LED driver is enabled. The LED driver is enabled in pulse cycles from LED_SEQ1_START through LED_SEQ1_END. 0x00 = (Default) 0 cycles 0x01 = 1 cycles … 0x0F = 15 cycles 0x10–0x7F = Reserved

7.2.63 LED_START_STOP1_3

BANK1 Address: 0x63

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ1_END						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ1_END	Selects the last pulse cycle in State 1 in which the LED driver is enabled. The LED driver is enabled in pulse cycles from LED_SEQ1_START through LED_SEQ1_END. 0x00 = (Default) 0 cycles 0x01 = 1 cycles … 0x0F = 15 cycles 0x10–0x7F = Reserved

7.2.64 LED_START_STOP2_0

BANK1 Address: 0x64

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ2_START						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ2_START	Selects the first pulse cycle in State 2 in which the LED driver is enabled. The LED driver is enabled in pulse cycles from LED_SEQ2_START through LED_SEQ2_END. 0x00 = (Default) 0 cycles 0x01 = 1 cycles … 0x0F = 15 cycles 0x10–0x7F = Reserved

7.2.65 LED_START_STOP2_1

BANK1 Address: 0x65

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ2_END						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ2_END	Selects the last pulse cycle in State 2 in which the LED driver is enabled. The LED driver is enabled in pulse cycles from LED_SEQ2_START through LED_SEQ2_END. 0x00 = (Default) 0 cycles 0x01 = 1 cycles … 0x0F = 15 cycles 0x10–0x7F = Reserved

7.2.66 LED_START_STOP2_2

BANK1 Address: 0x66

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ3_START						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ3_START	Selects the first pulse cycle in State 3 in which the LED driver is enabled. The LED driver is enabled in pulse cycles from LED_SEQ3_START through LED_SEQ3_END. 0x00 = (Default) 0 cycles 0x01 = 1 cycles … 0x0F = 15 cycles 0x10–0x7F = Reserved

7.2.67 LED_START_STOP2_3

BANK1 Address: 0x67

RW	7	6	5	4	3	2	1	0
	—	LED_SEQ3_END						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	LED_SEQ3_END	Selects the last pulse cycle in State 3 in which the LED driver is enabled. The LED driver is enabled in pulse cycles from LED_SEQ3_START through LED_SEQ3_END. 0x00 = (Default) 0 cycles 0x01 = 1 cycles … 0x0F = 15 cycles 0x10–0x7F = Reserved

7.2.68 LED_CTRL_STATUS

BANK1 Address: 0x68

RO	7	6	5	4	3	2	1	0
	—	SEQ_STATE_STS		LED_MAX_CURRENT_ERR	LED_CTRL_SHORT_ERR	—		
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:5	SEQ_STATE_STS	Current sequence state 00 = (Default) State 0 01 = State 1 10 = State 2 11 = State 3
4	LED_MAX_CURRENT_ERR	Maximum current error. Indicates the sum of LEDR_COARSE, LEDG_COARSE, and LEDB_COARSE for the active LED channels exceeds 0b11. Only applies to active channels (enabled using LEDx_EN and by an asserted hardware pin or LED_CLK pulse waveform). If this bit is set, the fine current selections are restricted to a maximum of 45 mA. In most configurations, the error indicates a sum exceeding 135 mA. The combination of 33mA + 49mA + 49mA (total 131 mA) also triggers the maximum-current response. 0 = (Default) Normal 1 = Max current error
3	LED_CTRL_SHORT_ERR	Short circuit detection on LED control resistor. Indicates a short circuit in the ILED_CTRL external resistor. 0 = (Default) Normal 1 = Short detected
2:0	—	Reserved

7.3 BANK2—MSM

7.3.1 BANK

BANKn (n = 0–7) Address: 0x00

	7	6	5	4	3	2	1	0
	DESCRIM				—	BANK		
Access	RO				—	RW		
Default	1	1	0	0	0	0	0	0

Bits	Name	Description
7:4	DESCRIM	Read-only device identifier field. Readback value is 0xC.
3	—	Reserved
2:0	BANK	Selects the active bank for SPI access. 000 = (Default) Bank 0 001 = Bank 1 010 = Bank 2 011 = Bank 3 100 = Bank 4 101 = Bank 5 110 = Bank 6 111 = Bank 7

7.3.2 ASYNC0_0

BANKn (n = 0–7) Address: 0x04

	7	6	5	4	3	2	1	0
RO	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	—	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	ACTIVE_ERROR_STS	Path error status. Indicates an error condition in the Active or Ready states. 0 = (Default) Normal 1 = Error
4	TEMP_ERROR_STS	Temperature error status. Indicates an overtemperature condition has been detected. 0 = (Default) Normal 1 = Error
3	—	Reserved
2	MCLK_ERROR_STS	MCLK error status. Indicates MCLK is invalid or absent in the Idle State. 0 = (Default) Normal 1 = Error
1	STARTUP_ERROR_STS	Start up error status. Indicates an error detected during start-up. 0 = (Default) Normal 1 = Error
0	BOOT_ERROR_STS	Boot error status. Indicates an error detected during boot. 0 = (Default) Normal 1 = Error

7.3.3 ASYNC0_1

BANKn (n = 0–7) Address: 0x05

	7	6	5	4	3	2	1	0
RW	—							OSC_DISABLE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	OSC_DISABLE	Oscillator disable. Setting this bit places the device in a low-power Sleep State. Note that the host must return the device to the Idle State before writing to any other control registers. 0 = (Default) RCO enabled 1 = RCO disabled

7.3.4 SFT_RESET

BANKn (n = 0–7) Address: 0x08

	7	6	5	4	3	2	1	0
WO	SFT_RESET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	SFT_RESET	Software reset. Write 0x5A to execute a software reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved

7.3.5 DEVICE_STATUS_0

BANK2 Address: 0x10

	7	6	5	4	3	2	1	0
RO	ERROR_STS	—	ACTIVE_STS	READY_STS	—		IDLE_STS	STARTUP_STS
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	ERROR_STS	Indicates the device is in the ERROR state. 0 = (Default) Not in ERROR state 1 = ERROR state
6	—	Reserved

Bits	Name	Description
5	ACTIVE_STS	Indicates the device is in the ACTIVE state. This is the fully operational state, supporting active sampling and data output. 0 = (Default) Not in ACTIVE state 1 = ACTIVE state
4	READY_STS	Indicates the device is in the READY state. The analog input path and internal clocking circuits are fully enabled. The data-output interface is enabled (Logic 0 output), ready to support sample data in the configured format. 0 = (Default) Not in READY state 1 = READY state
3:2	—	Reserved
1	IDLE_STS	Indicates the device is in the Idle State. This is a low-power state in which the device can be configured for the required operational behavior. 0 = (Default) Not in IDLE state 1 = IDLE state
0	STARTUP_STS	Indicates the device is in the Startup State. This is the initial state following reset, in which the device performs necessary start-up processes. 0 = (Default) Not in STARTUP state 1 = STARTUP state

7.3.6 DEVICE_STATUS_2

BANK2 Address: 0x12

	7	6	5	4	3	2	1	0
RO	VDDA_STS				—			
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7	VDDA_STS	VDD_A status. Indicates whether a valid VDD_A supply is present. 0 = (Default) VDD_A is present 1 = VDD_A is not present.
6:0	—	Reserved

7.4 BANK3—MSM

7.4.1 BANK

BANKn (n = 0–7) Address: 0x00

	7	6	5	4	3	2	1	0
	DESCRIM				—	BANK		
Access	RO				—	RW		
Default	1	1	0	0	0	0	0	0

Bits	Name	Description
7:4	DESCRIM	Read-only device identifier field. Readback value is 0xC.
3	—	Reserved
2:0	BANK	Selects the active bank for SPI access. 000 = (Default) Bank 0 001 = Bank 1 010 = Bank 2 011 = Bank 3 100 = Bank 4 101 = Bank 5 110 = Bank 6 111 = Bank 7

7.4.2 ASYNC0_0

BANKn (n = 0–7) Address: 0x04

	7	6	5	4	3	2	1	0
RO	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	—	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	ACTIVE_ERROR_STS	Path error status. Indicates an error condition in the Active or Ready states. 0 = (Default) Normal 1 = Error

Bits	Name	Description
4	TEMP_ERROR_STS	Temperature error status. Indicates an overtemperature condition has been detected. 0 = (Default) Normal 1 = Error
3	—	Reserved
2	MCLK_ERROR_STS	MCLK error status. Indicates MCLK is invalid or absent in the Idle State. 0 = (Default) Normal 1 = Error
1	STARTUP_ERROR_STS	Start up error status. Indicates an error detected during start-up. 0 = (Default) Normal 1 = Error
0	BOOT_ERROR_STS	Boot error status. Indicates an error detected during boot. 0 = (Default) Normal 1 = Error

7.4.3 ASYNC0_1

BANKn (n = 0–7) Address: 0x05

	7	6	5	4	3	2	1	0
RW	—							OSC_DISABLE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	OSC_DISABLE	Oscillator disable. Setting this bit places the device in a low-power Sleep State. Note that the host must return the device to the Idle State before writing to any other control registers. 0 = (Default) RCO enabled 1 = RCO disabled

7.4.4 SFT_RESET

BANKn (n = 0–7) Address: 0x08

	7	6	5	4	3	2	1	0
WO	SFT_RESET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	SFT_RESET	Software reset. Write 0x5A to execute a software reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved

7.4.5 BANK

BANKn (n = 0–7) Address: 0x00

	7	6	5	4	3	2	1	0
	DESCRIM				—	BANK		
Access	RO				—	RW		
Default	1	1	0	0	0	0	0	0

Bits	Name	Description
7:4	DESCRIM	Read-only device identifier field. Readback value is 0xC.
3	—	Reserved
2:0	BANK	Selects the active bank for SPI access. 000 = (Default) Bank 0 001 = Bank 1 010 = Bank 2 011 = Bank 3 100 = Bank 4 101 = Bank 5 110 = Bank 6 111 = Bank 7

7.4.6 ASYNC0_0

BANKn (n = 0–7) Address: 0x04

	7	6	5	4	3	2	1	0
RO	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	—	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	ACTIVE_ERROR_STS	Path error status. Indicates an error condition in the Active or Ready states. 0 = (Default) Normal 1 = Error
4	TEMP_ERROR_STS	Temperature error status. Indicates an overtemperature condition has been detected. 0 = (Default) Normal 1 = Error
3	—	Reserved
2	MCLK_ERROR_STS	MCLK error status. Indicates MCLK is invalid or absent in the Idle State. 0 = (Default) Normal 1 = Error
1	STARTUP_ERROR_STS	Start up error status. Indicates an error detected during start-up. 0 = (Default) Normal 1 = Error
0	BOOT_ERROR_STS	Boot error status. Indicates an error detected during boot. 0 = (Default) Normal 1 = Error

7.4.7 ASYNC0_1

BANKn (n = 0–7) Address: 0x05

	7	6	5	4	3	2	1	0
RW	—							OSC_DISABLE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	OSC_DISABLE	Oscillator disable. Setting this bit places the device in a low-power Sleep State. Note that the host must return the device to the Idle State before writing to any other control registers. 0 = (Default) RCO enabled 1 = RCO disabled

7.4.8 SFT_RESET

BANKn (n = 0–7) Address: 0x08

	7	6	5	4	3	2	1	0
WO	SFT_RESET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	SFT_RESET	Software reset. Write 0x5A to execute a software reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved

7.4.9 BANK

BANKn (n = 0–7) Address: 0x00

	7	6	5	4	3	2	1	0
	DESCRIM				—	BANK		
Access	RO				—	RW		
Default	1	1	0	0	0	0	0	0

Bits	Name	Description
7:4	DESCRIM	Read-only device identifier field. Readback value is 0xC.

Bits	Name	Description
3	—	Reserved
2:0	BANK	Selects the active bank for SPI access. 000 = (Default) Bank 0 001 = Bank 1 010 = Bank 2 011 = Bank 3 100 = Bank 4 101 = Bank 5 110 = Bank 6 111 = Bank 7

7.4.10 ASYNC0_0

BANKn (n = 0–7) Address: 0x04

RO	7	6	5	4	3	2	1	0
	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	—	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	ACTIVE_ERROR_STS	Path error status. Indicates an error condition in the Active or Ready states. 0 = (Default) Normal 1 = Error
4	TEMP_ERROR_STS	Temperature error status. Indicates an overtemperature condition has been detected. 0 = (Default) Normal 1 = Error
3	—	Reserved
2	MCLK_ERROR_STS	MCLK error status. Indicates MCLK is invalid or absent in the Idle State. 0 = (Default) Normal 1 = Error
1	STARTUP_ERROR_STS	Start up error status. Indicates an error detected during start-up. 0 = (Default) Normal 1 = Error
0	BOOT_ERROR_STS	Boot error status. Indicates an error detected during boot. 0 = (Default) Normal 1 = Error

7.4.11 ASYNC0_1

BANKn (n = 0–7) Address: 0x05

RW	7	6	5	4	3	2	1	0
	—							OSC_DISABLE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	OSC_DISABLE	Oscillator disable. Setting this bit places the device in a low-power Sleep State. Note that the host must return the device to the Idle State before writing to any other control registers. 0 = (Default) RCO enabled 1 = RCO disabled

7.4.12 SFT_RESET

BANKn (n = 0–7) Address: 0x08

WO	7	6	5	4	3	2	1	0
	SFT_RESET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	SFT_RESET	Software reset. Write 0x5A to execute a software reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved

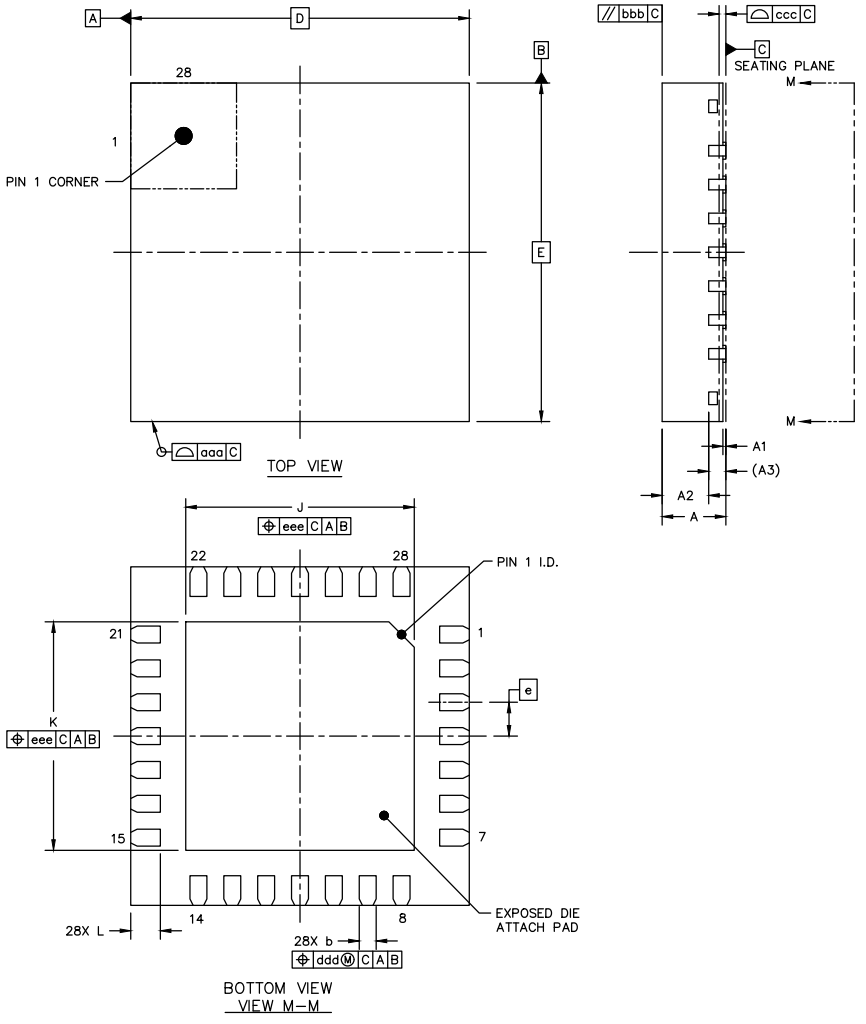
8 Thermal Characteristics

Table 8-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	QFN	Units
Junction-to-ambient thermal resistance	θ_{JA}	37.52	°C/W
Junction-to-board thermal resistance	θ_{JB}	23.05	°C/W
Junction-to-case (top) thermal resistance	θ_{JC}	65.22	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	20.94	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	3.95	°C/W

Notes:
- Natural convection at the maximum recommended operating temperature T_A (see Table 3-1)
- Four-layer, 2s2p PCB as specified by JESD51–9 and JESD51–11; dimensions: 101.5 x 114.5 x 1.6 mm
- Exposed pad is connected to the PCB ground layer through a 3 x 3 thermal via array; vias are 0.3 mm diameter, plated.
- Thermal parameters as defined by JESD51–12

9 Package Dimensions



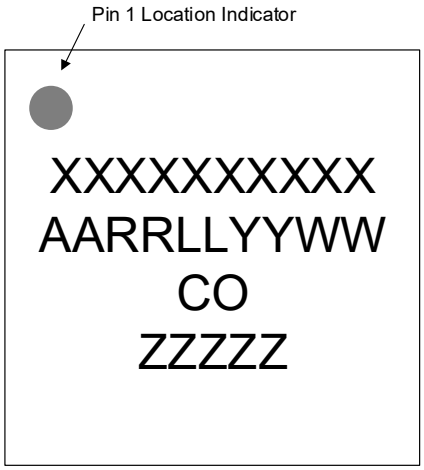
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	2.6	2.7	2.8
	Y	K	2.6	2.7	2.8
LEAD LENGTH		L	0.3	0.35	0.4
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
2.0 TOTAL THICKNESS NOT INCLUDE SAW BURR.

Figure 9-1. QFN 28-pin Package Drawing

10 Package Marking



Top Side Brand
Line 1: Part number
Line 2: Package mark
Line 3: Country of origin (CO)
Line 4: Encoded wafer/device ID

Package Mark Fields
AA = Assembly site code
RR = Device revision code
LL = Lot sequence code
YY = Year of manufacture
WW = Work week of manufacture

Figure 10-1. Package Marking

11 Ordering Information

Table 11-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number
CS82L41	Video AFE with CMOS data output	28-pin QFN	Yes	Commercial	–40 °C to +85 °C	Tape and Reel	CS82L41–DNR
						Tray	CS82L41–DN

12 Revision History

Table 12-1. Revision History

Revision	Changes
F1 APR 2026	• Initial production release

Important: Please check www.cirrus.com or with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.