CS82L46

Six-Channel AFE with Sensor Timing Generation and LVDS/CMOS Data Output

Features

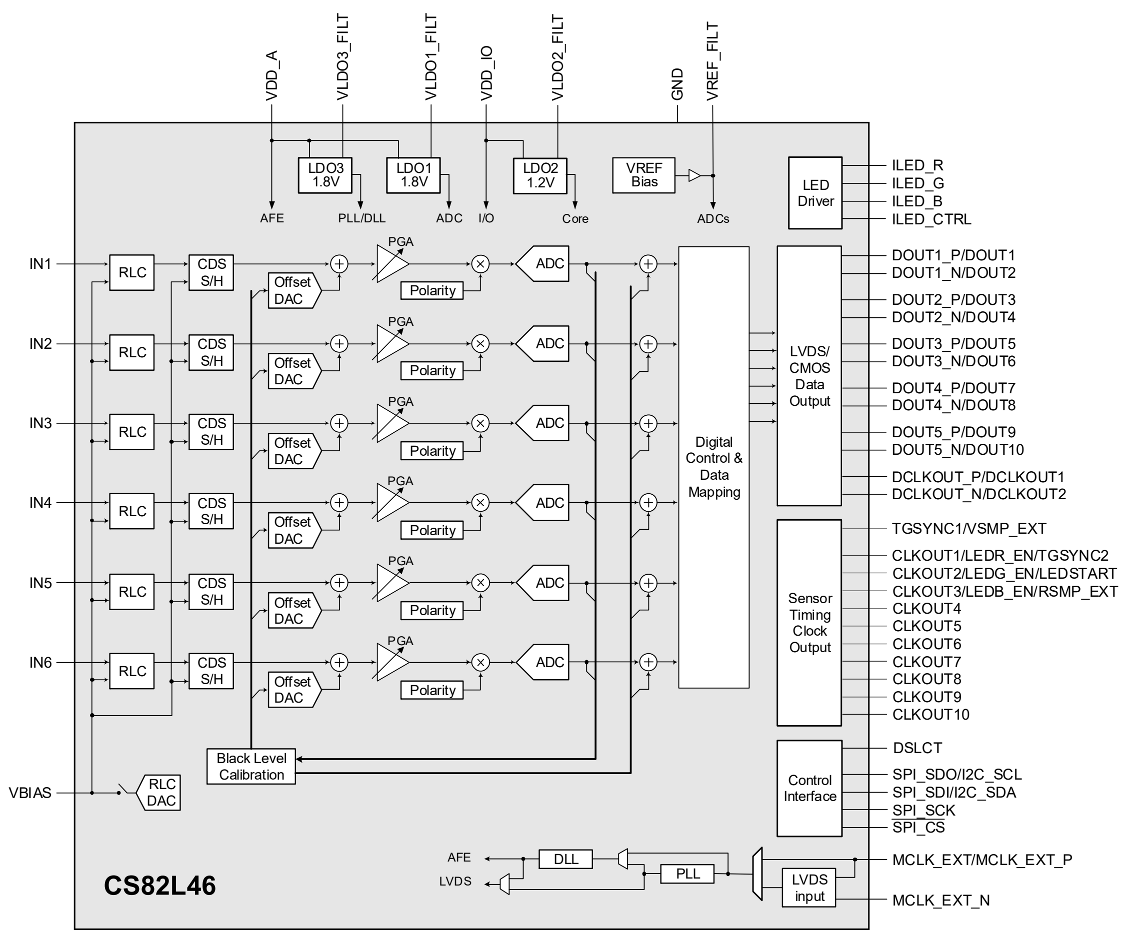
- Six-channel analog front end (AFE)
- Correlated double sampling
- RGB LED current drive and timing control
- Multiplexed data output format
- Internally generated reference voltages
- Timing control for sensor
- Versatile clocking configuration
  - — Tolerant of spread-spectrum clock reference
  - — Programmable DLL and PLL
  - — Spread-spectrum modulation of data output
- SPI or I²C control interface
- 48-pin QFN package

Specifications

- 16-bit data output
- 24 MSPS conversion rate per channel
- 12-bit programmable gain
- 9-bit programmable offset adjust
- 5-bit programmable clamp voltage
- 8-bit LED drive resolution

Applications

- Flatbed and sheet-feed scanners
- USB-compatible scanners
- Multifunction peripherals



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General Description

The CS82L46 is a front-end device for CCD and CIS sensors. The CS82L46 processes and digitizes the analog sensor signals at pixel conversion rates of up to 24 MSPS per channel.

The signal processing for each channel includes reset level clamping (RLC), correlated double sampling (CDS), and programmable polarity, gain and offset adjustment. Voltage references may be generated by an internal DAC or else provided externally.

The output data is available in a variety of digital formats via CMOS or LVDS data interfaces.

The CS82L46 incorporates an RGB LED driver with programmable current sinks and timing control. White LEDs are also supported.

The CS82L46 is available in a commercial-grade 0.4 mm pitch, 48-pin QFN package for operation from –40° to +85°C.

See Section 12 for ordering information.

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1 Pin Assignments and Descriptions

1.1 QFN 48-Pin (Top View, Through-Package)

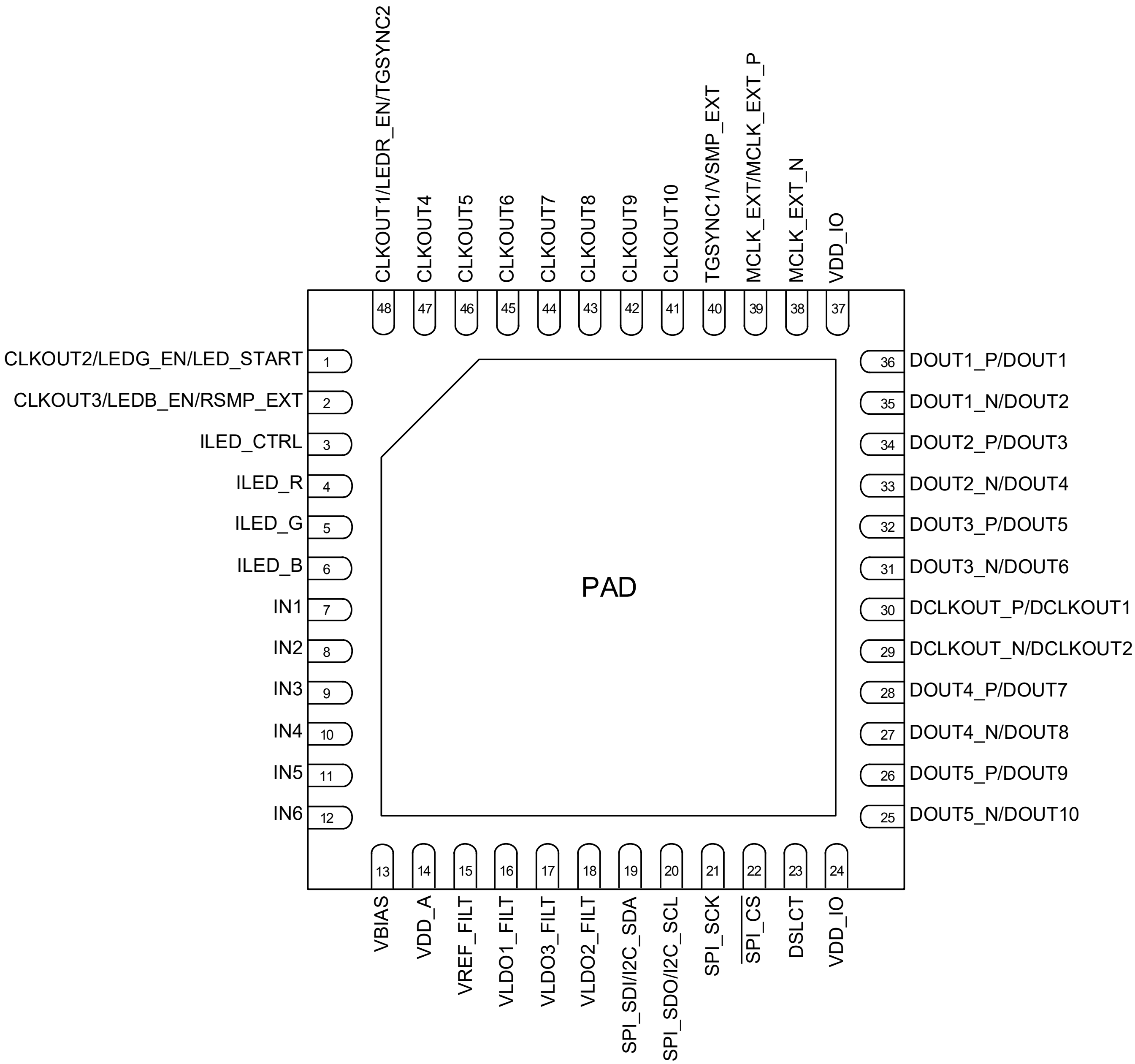


Figure 1-1. QFN 48-pin diagram (Top View, Through Package)

1.2 QFN Pin Descriptions

Table 1-1. QFN Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description	State at Reset
				Digital I/O	
CLKOUT1/LEDR_EN/ TGSYNC2	48	VDD_IO	I/O	Programmable clock output/ Red LED enable/ Timing generator control input/ General-Purpose Input/Output 1	TGSYNC2 input, pull-down
CLKOUT2/LEDG_EN/ LED_START	1	VDD_IO	I/O	Programmable clock output/ Green LED enable/ LED timing control input/ General-Purpose Input/Output 2	LED_START input, pull-down
CLKOUT3/LEDB_EN/ RSMP_EXT	2	VDD_IO	I/O	Programmable clock output/ Blue LED enable/ Reset sample control input/ General-Purpose Input/Output 3/ Clock monitor	RSMP_EXT input, pull-down
CLKOUT4	47	VDD_IO	I/O	Programmable clock output/ General-Purpose Input/Output 4	GPI4 input, pull-down
CLKOUT5	46	VDD_IO	I/O	Programmable clock output/ General-Purpose Input 5	GPI5 input, pull-down
CLKOUT6	45	VDD_IO	I/O	Programmable clock output/ General-Purpose Input 6	GPI6 input, pull-down
CLKOUT7	44	VDD_IO	I/O	Programmable clock output/ General-Purpose Input/Output 7	GPI7 input, pull-down
CLKOUT8	43	VDD_IO	I/O	Programmable clock output/ General-Purpose Input/Output 8	GPI8 input, pull-down
CLKOUT9	42	VDD_IO	I/O	Programmable clock output/ General-Purpose Input/Output 9	GPI9 input, pull-down
CLKOUT10	41	VDD_IO	I/O	Programmable clock output/ General-Purpose Input/Output 10	GPI10 input, pull-down
DCLKOUT_P/DCLKOUT1	30	VDD_IO	O	LVDS +clock output/CMOS clock output 1	Disabled o/p, pull-down
DCLKOUT_N/DCLKOUT2	29	VDD_IO	O	LVDS –clock output/CMOS clock output 2	Disabled o/p, pull-down
DOUT1_P/DOUT1	36	VDD_IO	O	LVDS +data output 1/CMOS data output 1	Disabled o/p, pull-down
DOUT1_N/DOUT2	35	VDD_IO	O	LVDS –data output 1/CMOS data output 2	Disabled o/p, pull-down
DOUT2_P/DOUT3	34	VDD_IO	O	LVDS +data output 2/CMOS data output 3	Disabled o/p, pull-down
DOUT2_N/DOUT4	33	VDD_IO	O	LVDS –data output 2/CMOS data output 4	Disabled o/p, pull-down
DOUT3_P/DOUT5	32	VDD_IO	O	LVDS +data output 3/CMOS data output 5	Disabled o/p, pull-down
DOUT3_N/DOUT6	31	VDD_IO	O	LVDS –data output 3/CMOS data output 6	Disabled o/p, pull-down
DOUT4_P/DOUT7	28	VDD_IO	O	LVDS +data output 4/CMOS data output 7	Disabled o/p, pull-down
DOUT4_N/DOUT8	27	VDD_IO	O	LVDS –data output 4/CMOS data output 8	Disabled o/p, pull-down
DOUT5_P/DOUT9	26	VDD_IO	O	LVDS +data output 5/CMOS data output 9	Disabled o/p, pull-down
DOUT5_N/DOUT10	25	VDD_IO	O	LVDS –data output 5/CMOS data output 10	Disabled o/p, pull-down
MCLK_EXT/MCLK_EXT_P	39	VDD_IO	I	Reference clock input/LVDS +clock input	MCLK_EXT input, pull-down

Table 1-1. QFN Pin Descriptions *(Cont.)*

Pin Name	Pin #	Power Supply	I/O	Description	State at Reset
MCLK_EXT_N	38	VDD_IO	I	LVDS –clock input/General-Purpose Input 12	GPI12 input, pull-down
SPI_SDO/I2C_SCL	20	VDD_IO	I/O	SPI data output/I²C clock input	Input, pull-down
SPI_SDI/I2C_SDA	19	VDD_IO	I/O	SPI data input/I²C data input/output	Input, pull-down
SPI_SCK	21	VDD_IO	I	SPI clock input	Input, pull-down
$\overline{\text{SPI\_CS}}$	22	VDD_IO	I	SPI peripheral select input	Input, pull-down
TGSYNC1/VSMP_EXT	40	VDD_IO	I/O	Timing generator control input-output/ Video sample control input	VSMP_EXT input, pull-down
				Analog I/O	
DSLCT	23	VDD_IO	I	Control interface address select	—
ILED_B	6	—	I	Blue LED current sink	—
ILED_G	5	—	I	Green LED current sink	—
ILED_R	4	—	I	Red LED current sink	—
ILED_CTRL	3	VDD_A	O	External resistor for LED current control	—
IN1	7	VDD_A	I	Analog input for ADC channel 1	—
IN2	8	VDD_A	I	Analog input for ADC channel 2	—
IN3	9	VDD_A	I	Analog input for ADC channel 3	—
IN4	10	VDD_A	I	Analog input for ADC channel 4	—
IN5	11	VDD_A	I	Analog input for ADC channel 5	—
IN6	12	VDD_A	I	Analog input for ADC channel 6	—
VBIAS	13	VDD_A	I/O	Reference voltage for AFE inputs	—
VLDO1_FILT	16	VDD_A	O	LDO1 output	—
VLDO2_FILT	18	VDD_IO	O	LDO2 output	—
VLDO3_FILT	17	VDD_A	O	LDO3 output	—
VREF_FILT	15	VDD_A	O	Voltage reference for internal circuits	—
				Power Supplies	
GND	PAD	—	—	Ground	—
VDD_A	14	—	—	Supply for LDO1, LDO3, and analog circuits	—
VDD_IO	24, 37	—	—	Supply for LDO2 and digital I/O	—

- See Table 3-1 for recommended operating limits for all pins

1.3 Termination of Unused Pins

Table 1-2 shows the required termination for unused pins (i.e., if the functionality of the pin is not being used). Pins not listed must be connected as shown in the typical connection drawings (see Section 2).

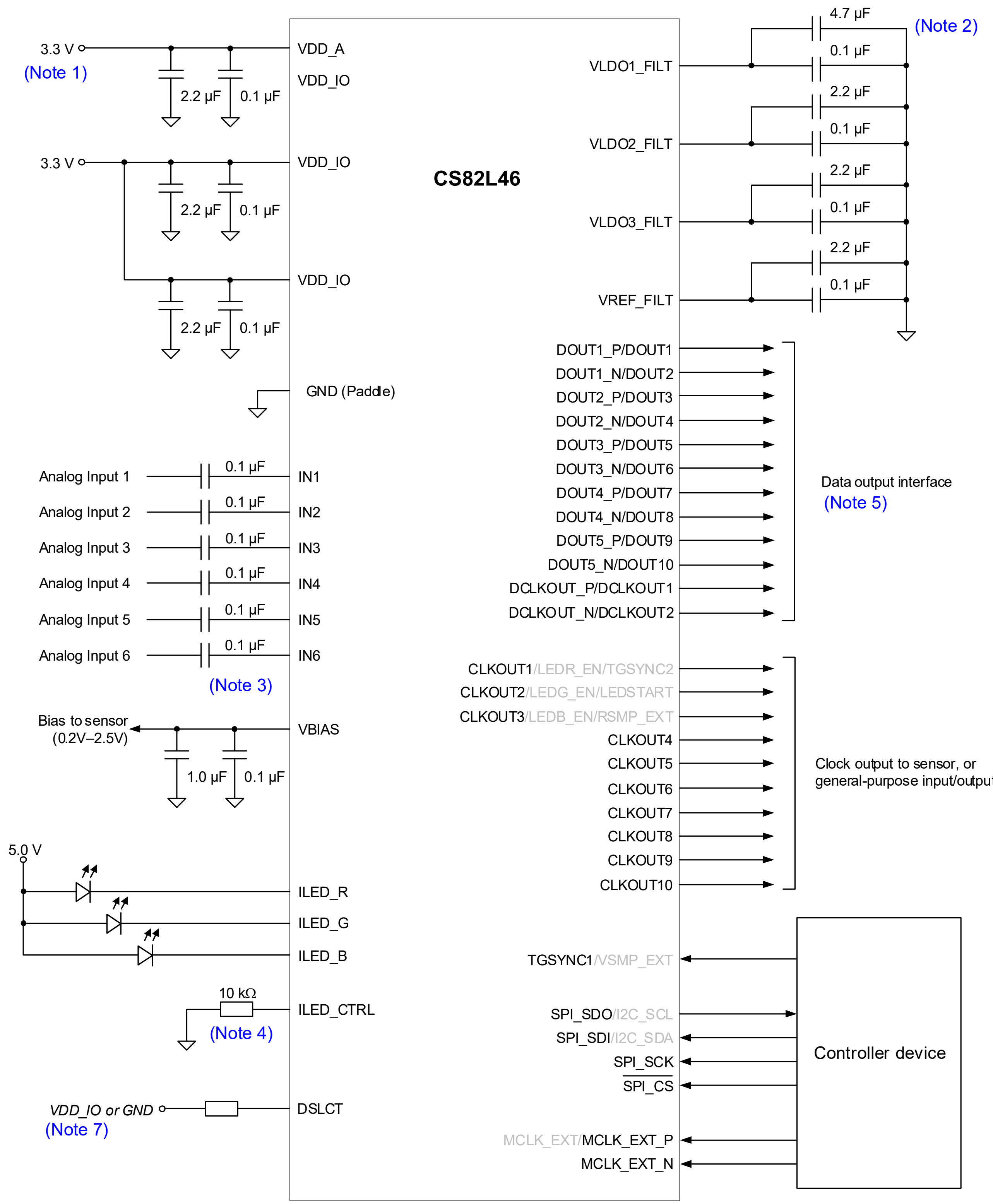
Table 1-2. Termination of Unused Pins

Name	Termination if unused
CLKOUT1/LEDR_EN/TGSYNC2 CLKOUT2/LEDG_EN/LED_START CLKOUT3/LEDB_EN/RSMP_EXT CLKOUT4–CLKOUT10 DCLKOUT_x/DCLKOUTx DOUTx_P/DOUTx DOUTx_N/DOUTx	Float
ILED_x ILED_CTRL INx MCLK_EXT_N SPI_SCK TGSYNC1/VSMP_EXT	Connect to GND
$\overline{\text{SPI\_CS}}$	Connect to VDD_IO

1.4 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS82L46 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD protection standards.

2 Typical Connection Diagram



Note: Unselected signals as part of multifunction pins are shown in gray.

Note - In I2C control mode, a pull-up resistor (to VDD_IO) is required on I2C_SCL and I2C_SDA.

Figure 2-1. Typical Connections—TG Mode

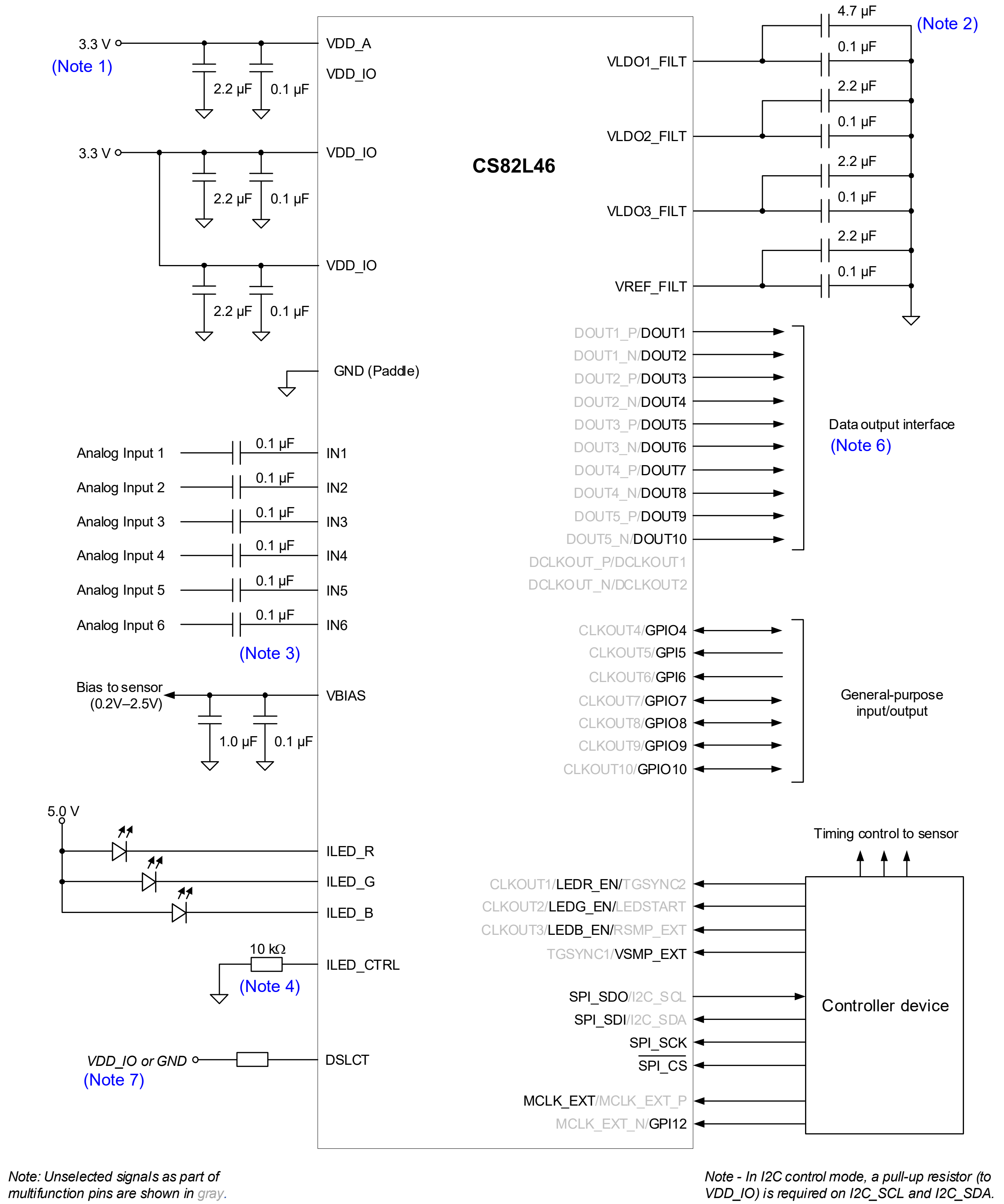


Figure 2-2. Typical Connections—External Mode

Notes referenced in the typical connection diagrams:

1. Power supply decoupling should be placed as close as possible to the CS82L46.
2. All capacitors are X7R, 20% tolerance.
3. Input capacitors are not required for DC-coupled analog input.
4. The LED current-control resistor must be within 1% of the specified value.
5. In TG Mode, data output is supported in LVDS or CMOS (TG) formats.
6. In External Mode, data output is supported in CMOS (External) format only.
7. The control interface is typically configured by connecting DSLCT directly to VDD_IO or GND. If two CS82L46 devices are connected on a shared SPI bus, a pull-up resistor to VDD_IO is used to configure the devices. The capacitive loading on the DSLCT pin must not exceed 100 pF. See Section 4.10 for further details.

3 Characteristics and Specifications

Note: The default register field configurations are used unless specified otherwise in the test conditions.

Table 3-1. Recommended Operating Conditions

Test conditions: Ground = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Typical	Maximum	Unit
DC power supply	Digital input/output supply	VDD_IO	3.04	3.3	3.63	V
	Analog supply[1]	VDD_A	3.04	3.3	3.63	V
Supply ramp up/down (all supplies)		t_{PWR-UD}	0.001	—	0.1	V/µs
LED operating voltage	ILED_R, ILED_G, ILED_B	V_{ILED}	0.25	—	5.5	V
Ambient temperature	Functional Parametric performance	T_A	–40 0	25 25	85 85	ºC ºC

Note: Functionality or parametric performance is not guaranteed or implied outside the limits in this table. Operation outside these limits may adversely affect device reliability.

1. The VDD_A supply is not required in the Idle and Sleep states (see Section 4.2); VDD_A can be disabled in these states to reduce power consumption. Note the sensor must also be powered down if VDD_A is disabled, to ensure the INx analog input voltage does not exceed VDD_A.

Table 3-2. Absolute Maximum Ratings

Test conditions: Ground = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
Analog and digital supplies		VDD_A, VDD_IO	–0.3	4.36	V
External voltage at digital inputs/outputs		V_{INDI}	–0.3	VDD_IO + 0.3	V
External voltage at analog inputs	INn, VBIAS ILED_R, ILED_G, ILED_B	V_{INAI}	–0.3 –0.3	VDD_A + 0.3 6.6	V V
Input current	digital input	I_{in}	—	±10	mA
Ambient operating temperature		T_A	–40	+85	°C
Junction operating temperature		T_J	–40	+125	°C
Storage temperature		T_{STG}	–65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-1 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3-3. Analog Input Path

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

Parameter		Minimum	Typical	Maximum	Unit
ADC sample rate		2	—	24	MHz
Maximum ADC output word length		—	16	—	Bits
Full-scale input voltage	Minimum gain Maximum gain	— —	2.4 0.25	— —	Vpk-pk Vpk-pk
Input capacitance	INx to ground	—	4	8	pF
Full-scale transition error	0 dB gain	—	55	—	mV
Zero-scale transition error	0 dB gain	—	33	—	mV
Differential nonlinearity	10 bit	–0.999	±0.5	+1.5	LSB
Integral nonlinearity	10 bit	—	±1	±4	LSB
Output noise	10 bit, 0 dB gain	—	0.5	1.5	LSB_{RMS}
Crosstalk (channel to channel)	10 bit, 0 dB gain	–0.5	—	0.5	LSB
PGA gain	minimum maximum step size (gain = 1–5 V/V) step size (gain = 5–9.75 V/V)	— — — —	1.0 9.75 0.125 0.25	— — — —	V/V V/V V V
Digital gain	minimum maximum resolution	— — —	0.5 1.99 12	— — —	V/V V/V bits
VBIAS input voltage		0.11	—	2.95	V
VBIAS short-circuit current	short to VDD_A short to GND	— —	42 2	— —	mA mA
VBIAS clamp-on resistance		—	50	—	Ω
VBIAS output resistance	VBIAS_ISEL = 10	—	2	—	Ω
VBIAS leakage current	0 < VBIAS < VDD_A	—	—	1	µA
RLC output voltage	minimum maximum step size	— — —	0.17 2.65 0.08	— — —	V V V
RLC differential nonlinearity		—	±0.5	—	LSB
RLC integral nonlinearity		—	±0.5	—	LSB
Offset voltage	minimum maximum step size	–400 250 —	–343 343 1.34	–250 400 —	mV mV mV
Offset voltage settling time [1]		—	2	—	samples
Offset differential nonlinearity		—	±0.5	±1	LSB
Offset integral nonlinearity		—	±0.5	±1	LSB
Offset temperature drift	T_A = 0°C to 85°C	–2.5	—	2.5	%

1. Measured when changing from the maximum output code to the minimum output code; settling time is defined from the end of the register write to the offset voltage being within 1.3 mV of the final level.

Table 3-4. LED Driver

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; LED control resistor (ILED_CTRL to GND) = 10 kΩ; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

Parameter		Minimum	Typical	Maximum	Unit
Coarse current control [1]	LEDx_COARSE = 00 LEDx_COARSE = 01 LEDx_COARSE = 10 LEDx_COARSE = 11	28 36 44 59	33 41 49 66	38 46 54 73	mA mA mA mA
Fine current control	minimum maximum resolution	— — —	0 Note [2] 8	— — —	mA mA bits
Fine current control DNL		–1	—	1	LSB
Fine current control INL		–1	—	1	LSB
Current control error	LEDx_COARSE = 00, LEDx_FINE > 0x26 LEDx_COARSE = 01, LEDx_FINE > 0x20 LEDx_COARSE = 10, LEDx_FINE > 0x1B LEDx_COARSE = 11, LEDx_FINE > 0x14	— — — —	— — — —	18 15 12 12	% % % %
Maximum LED driver current (sum of all enabled channels)		—	135	—	mA
LED leakage current (LED output disabled)		—	20	—	μA
Maximum LED fault current [3]		—	90	—	mA
Load capacitance		—	—	10	pF

1. Assumes maximum fine-current selection (LEDx_FINE = 0xFF).
2. At the maximum fine-current selection, the LED current is equal to the applicable coarse control setting.
3. Fault conditions include ILED_CTRL resistor short circuit, ILED_CTRL resistor short to GND or supply, and internal driver faults.

Table 3-5. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications; LVDS output load = 100 Ω ±1%.

Parameter			Symbol	Minimum	Typical	Maximum	Unit
CMOS input/output	Input leakage current (per pin)		I_{IN}	—	—	±4	μA
	Input capacitance (per pin)		—	—	—	10	pF
	High-level output	I_{OH} = 1 mA	V_{OH}	0.9×VDD_IO	—	—	V
	Low-level output	I_{OL} = –1 mA	V_{OL}	—	—	0.1×VDD_IO	V
	High-level input		V_{IH}	0.7×VDD_IO	—	—	V
	Low-level input		V_{IL}	—	—	0.3×VDD_IO	V
	Internal weak pull-up/pull-down		—	1.2	1.4	1.6	MΩ
	High-impedance output current	Pin grounded	I_{OZ}	—	—	1	μA
LVDS output	Differential output voltage (steady state)	LVDS_VREF_SEL = 01 LVDS_VREF_SEL = 00	V_{OD}	160 120	200 155	242 187	mV mV
	Change in differential voltage between opposite logic states		ΔV_{OD}	—	—	50	mV
	Common-mode output voltage (steady state)	LVDS_VREF_SEL = 01 LVDS_VREF_SEL = 00	$V_{OC(SS)}$	1.08 0.8	1.2 0.9	1.32 1.0	V V
	Common-mode output voltage (peak-to-peak)		$V_{OC(PP)}$	—	25	50	mV
	Short-circuit current	Short to GND P–N short	—	— –12	— —	24 12	mA mA
LVDS input	Positive-going differential input threshold		—	—	—	100	mV
	Negative-going differential input threshold		—	–100	—	—	mV
	Differential input range		—	100	—	600	mV
	DC common-mode range		—	0.82	—	1.375	V
	Differential input impedance		—	90	100	110	Ω

Table 3-6. DC Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

Parameter			Minimum	Typical	Maximum	Unit
Voltage reference (VREF_FILT)	Output voltage		—	1.2	—	V
Power-on reset	VDD_IO reset threshold	VDD_IO rising VDD_IO falling	1.97 1.80	— —	2.89 2.67	V V
	VDD_A reset threshold	VDD_A rising VDD_A falling	1.92 1.75	— —	2.89 2.67	V V

Table 3-7. System Clocking, Startup and Shutdown

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

Parameter			Minimum	Typical	Maximum	Unit
Reset	Power-on reset to control port active [1,2]		—	—	2	ms
	Software reset to control port active [2]		—	—	2	ms
	Power-on reset to Idle State		—	—	4	ms
	Software reset to Idle State		—	—	4	ms
Ready	Idle to Ready State		—	—	4	ms
Power-down	Ready to Idle State		—	—	10	ms
MCLK input	Input reference frequency (MCLK_EXT)	TG Mode External Mode	2 4	— —	24 60	MHz MHz
	Duty cycle	TG Mode External Mode	40 45	— —	60 55	% %
	Spread-spectrum modulation tolerance	Amplitude [3] Frequency	–3 —	— —	3 60	% kHz
Phase-locked loop (PLL)/Delay-locked loop (DLL)	Input reference frequency		2	—	24	MHz
	PLL lock time	MCLK_EXT = 2 MHz MCLK_EXT = 24 MHz	— —	1 0.5	— —	ms ms
	DLL lock time	MCLK_EXT = 2 MHz MCLK_EXT = 24 MHz	— —	0.6 0.25	— —	ms ms

1. Measured from VDD_IO above its reset threshold.
2. It is recommended to confirm the device has reached the Idle State before configuring the control registers.
3. Note the instantaneous frequency must always be within the specified input range.

Table 3-8. Temperature Monitoring and Protection Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground.

Parameter	Minimum	Typical	Maximum	Unit
Overtemperature warning threshold	—	135	—	°C
Overtemperature error threshold [1]	—	155	—	°C
Overtemperature warning/error threshold deviation [2]	–10	—	10	°C

1. The same internal temperature-measuring circuitry is used to create both the overtemperature warning and error signals, overtemperature warning/error threshold deviation is applied equally to both thresholds, which results in the individual thresholds being inaccurate to the same degree and of the same polarity as all other values.
2. The overtemperature warning/error threshold deviation specifies the accuracy of the temperature-detection circuitry. This specification relates how many degrees above or below the threshold the overtemperature warning/error circuitry may trigger.

Table 3-9. Device Power Consumption

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; input signal (Active State only) = 1.5 V pk-pk, 1 MHz sine wave; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

Use Configuration			Typical	Maximum	Unit
Sleep State (MCLK stopped, oscillator disabled)	VDD_IO current	T_A = +25ºC T_A = 0–85ºC	285 —	600 2500	µA µA
	VDD_A current		—	155	µA
Idle State (MCLK stopped, default register conditions)	VDD_IO current	T_A = +25ºC T_A = 0–85ºC	645 —	1000 3800	µA µA
	VDD_A current		—	155	µA
Active State, External Mode	Total power consumption [1] MCLK = 12 MHz, sample rate = 2 MSPS, output rate = 24 Mbit/s per DOUT, Format ID = 4 (6 channels, 16-bit data, 8 x DOUT), low-power mode		103	—	mW
	Total power consumption [1] MCLK = 60 MHz, sample rate = 10 MSPS, output rate = 120 Mbit/s per DOUT, Format ID = 4 (6 channels, 16-bit data, 8 x DOUT), high-performance mode		241	—	mW
Active State, TG Mode, CMOS input/output	Total power consumption [1] MCLK = 2 MHz, sample rate = 2 MSPS, output rate = 12 Mbit/s per DOUT, Format ID = 75 (6 channels, 10-bit data, 10 x DOUT), low-power mode, PLL1/PLL2 disabled		103	—	mW
	Total power consumption [1] MCLK = 10 MHz, sample rate = 10 MSPS, output rate = 60 Mbit/s per DOUT, Format ID = 75 (6 channels, 10-bit data, 10 x DOUT), high-performance mode, PLL1/PLL2 disabled		240	—	mW
Active State, TG Mode, LVDS input/output	Total power consumption [2] MCLK = 6 MHz, sample rate = 6 MSPS, output rate = 126 Mbit/s per LVDS pair, Format ID = 79 (6 channels, 16-bit data, 5 x LVDS pairs), LVDS clock = 18 MHz low-power mode, PLL1/PLL2 disabled		221	—	mW
	Total power consumption [2] MCLK = 24 MHz, sample rate = 24 MSPS, output rate = 504 Mbit/s per LVDS pair, Format ID = 79 (6 channels, 16-bit data, 5 x LVDS pairs), LVDS clock = 72 MHz, high-performance mode, PLL1/PLL2 disabled		385	—	mW
PLL	Incremental power consumption, PLL1 enabled		6	—	mW
LED Drivers	Incremental power consumption, LED current = 45 mA, fine current = full scale	1 LED enabled 2 LEDs enabled 3 LEDs enabled	1.8 3.2 4.4	— — —	mW mW mW

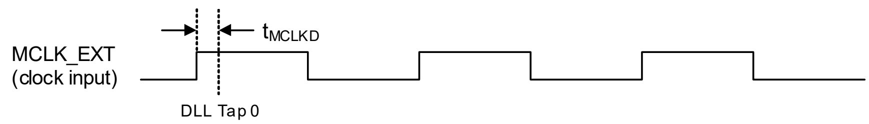
1. Excluding power dissipated by DOUT drivers—assumes no load connected.
2. Includes power dissipated by LVDS drivers—assumes C_{LOAD} = 10 pF.

Table 3-10. Switching Specifications—Video Sample Timing (TG Mode)

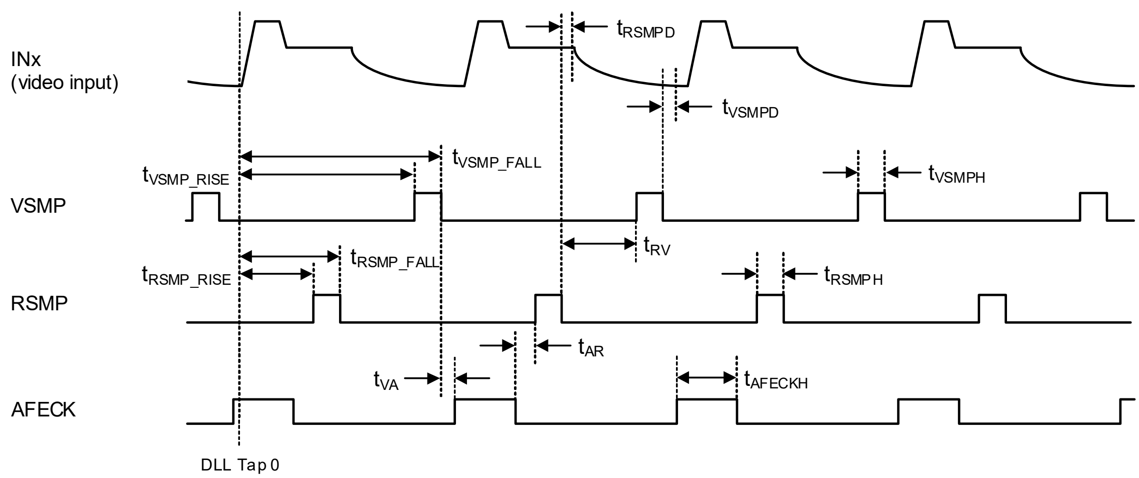
Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

Parameter [1,2,3]		Symbol	Minimum	Typical	Maximum	Unit
MCLK_EXT rising edge to DLL Tap 0, Clocking Mode 0	MCLK_EXT = 2.0 MHz	t_{MCLKD}	—	12	18	ns
	MCLK_EXT = 6.0 MHz		—	8	14	ns
	MCLK_EXT = 9.7 MHz		—	7	12	ns
	MCLK_EXT = 23.0 MHz		—	6.5	11	ns
Aperture delay from RSMP falling edge	CDS mode	t_{RSMPD}	—	3	—	ns
Aperture delay from VSMP falling edge		t_{VSMPD}	—	3	—	ns
RSMP high period	CDS mode	t_{RSMPH}	5	—	—	ns
VSMP high period		t_{VSMPH}	5	—	—	ns
			—	—	28	DLL Taps
AFECK high period		t_{AFECKH}	15	—	—	ns
VSMP falling edge to AFECK rising edge		t_{VA}	—	1	—	DLL Tap
AFECK falling edge to RSMP rising edge	CDS mode	t_{AR}	0	—	—	ns
RSMP falling edge to VSMP rising edge	CDS mode	t_{RV}	0.5	—	—	ns
AFECK falling edge to VSMP rising edge	non-CDS mode	t_{AV}	0	—	—	ns

1. Video input timing—MCLK. If PLL1 is not used (Clocking Mode 0), DLL Tap 0 is derived from the MCLK rising edge.



2. Video input timing—CDS mode. The VSMP and RSMP timing is referenced to DLL Tap 0. See Section 4.6.1 to configure the rise/fall timing.



3. Video input timing—non-CDS mode. The VSMP timing is referenced to DLL Tap 0. See Section 4.6.1 to configure the rise/fall timing.

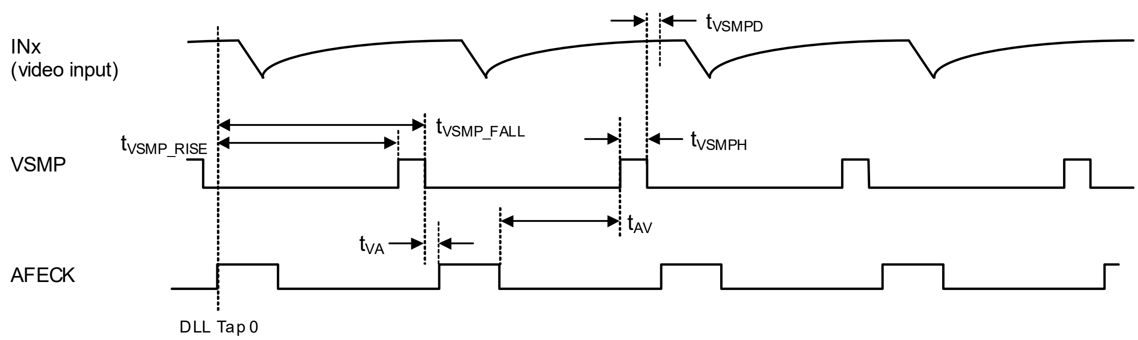
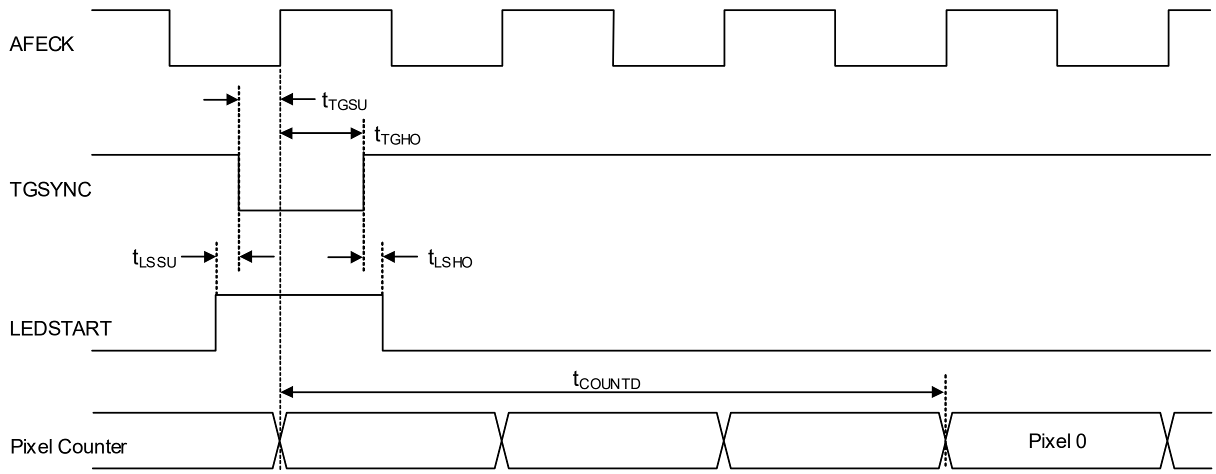


Table 3-11. Switching Specifications—TGSYNC/LEDSTART Timing (TG Slave Mode)

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

Parameter [1,2,3,4]		Symbol	Minimum	Typical	Maximum	Unit
TGSYNC setup time to AFECK rising		t_{TGSU}	4	—	—	ns
TGSYNC hold time from AFECK rising	TGSYNC filter disabled [5]	t_{TGHO}	1	—	—	ns
LEDSTART setup time to TGSYNC active edge		t_{LSSU}	0	—	—	ns
LEDSTART hold time from TGSYNC inactive edge		t_{LSHO}	0	—	—	ns
Delay from TGSYNC pulse to pixel-counter reset [6]		t_{COUNTD}	—	3	—	cycles

1. Assumes Clocking Mode 0; see Section 4.7.3.1 for Clocking Modes 1 and 2.
2. TGSYNC/LEDSTART timing. See Section 4.6.1 for details of AFECK.



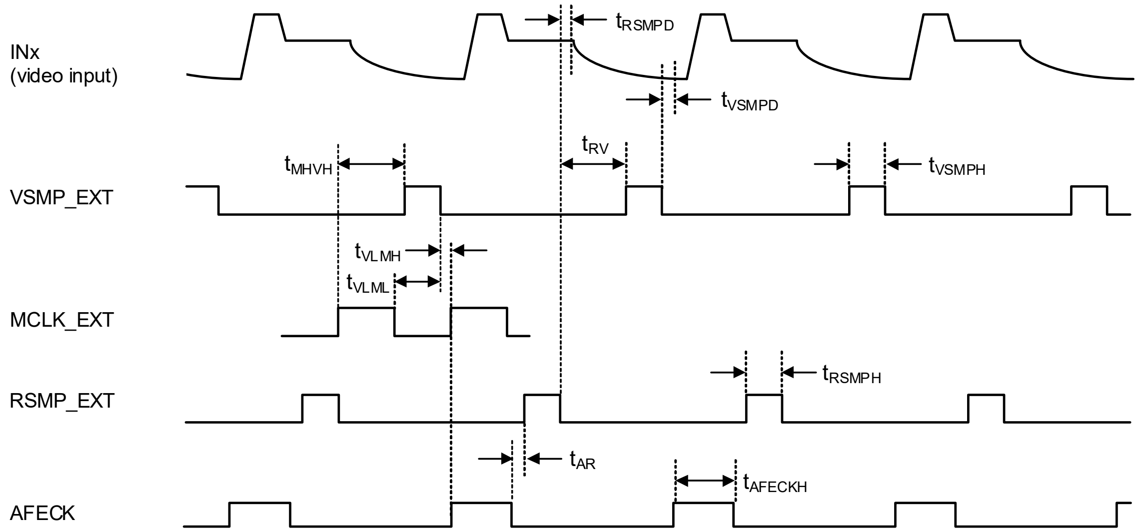
3. TGSYNC input is supported on three different pins—TGSYNC1, TGSYNC2, or LEDSTART.
4. LEDSTART input is only used if LEDSTART_SEQ_INIT is set.
5. See Section 4.7.3.1 for TGSYNC pulse-width requirement if TGSYNC filter is enabled.
6. Assumes TGSYNC_ASYNC = 1 for TG Mode.

Table 3-12. Switching Specifications—Video Sample Timing (External Mode 1)

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

Parameter [1,2]		Symbol	Minimum	Typical	Maximum	Unit
Aperture delay from RSMP falling edge	CDS mode	t_{RSMPD}	—	8	—	ns
Aperture delay from VSMP falling edge		t_{VSMPD}	—	5	—	ns
RSMP high period	CDS mode	t_{RSMPH}	5	—	—	ns
VSMP high period		t_{VSMPH}	5	—	—	ns
AFECK high period		t_{AFECKH}	15	—	—	ns
RSMP falling edge to VSMP rising edge	CDS mode	t_{RV}	0	—	—	ns
AFECK falling edge to RSMP rising edge	CDS mode	t_{AR}	0	—	—	ns
AFECK falling edge to VSMP rising edge	non-CDS mode	t_{AV}	0	—	—	ns
MCLK rising edge to VSMP rising edge		t_{MHVH}	0	—	—	ns
MCLK falling edge to VSMP falling edge		t_{VLML}	0	—	—	ns
VSMP falling edge to MCLK rising edge		t_{VLMH}	2	—	—	ns

1. Video input timing—CDS mode. The VSMP and RSMP timing is controlled by external signals VSMP_EXT and RSMP_EXT.



2. Video input timing—non-CDS mode. The VSMP timing is controlled by external signal VSMP_EXT.

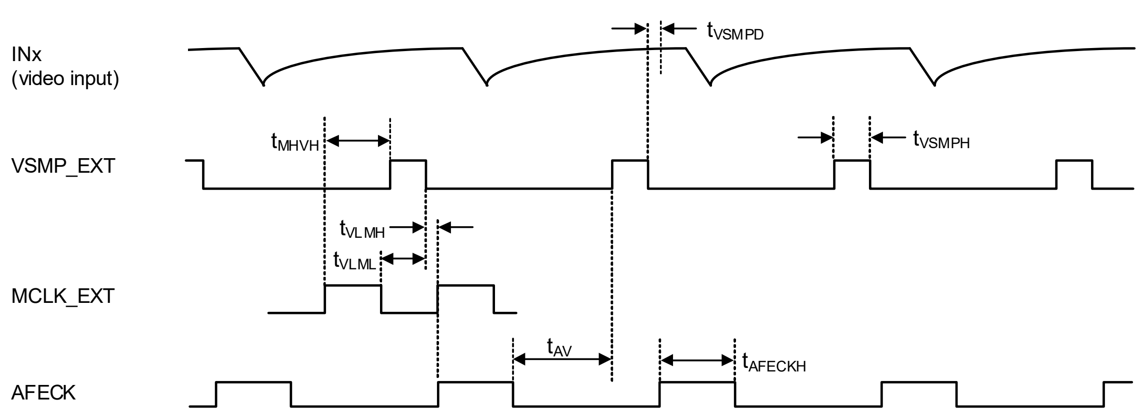
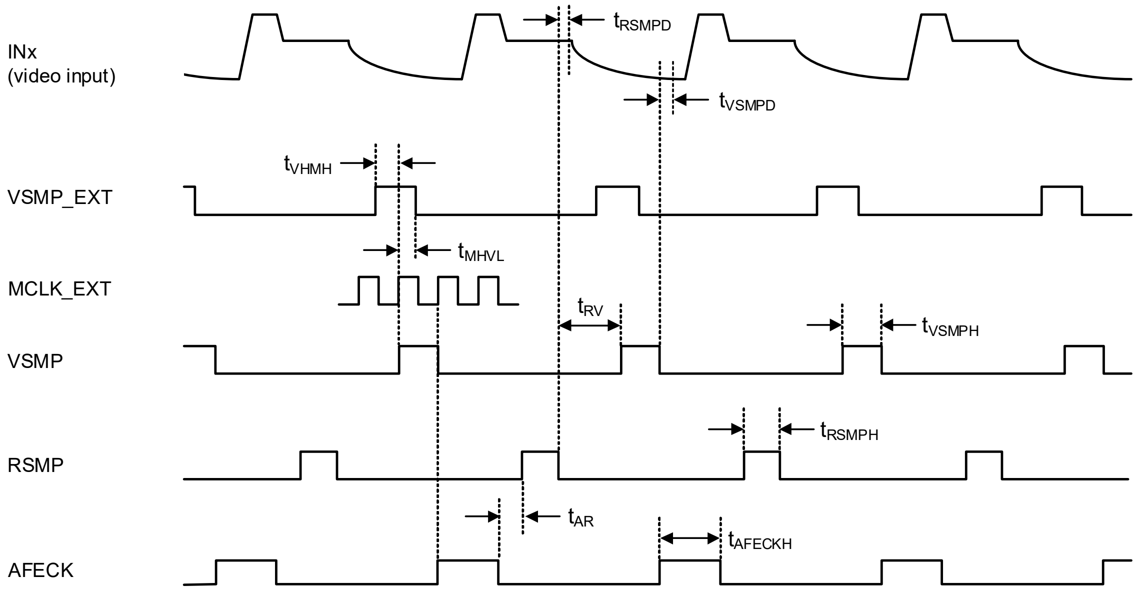


Table 3-13. Switching Specifications—Video Sample Timing (External Mode 2)

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

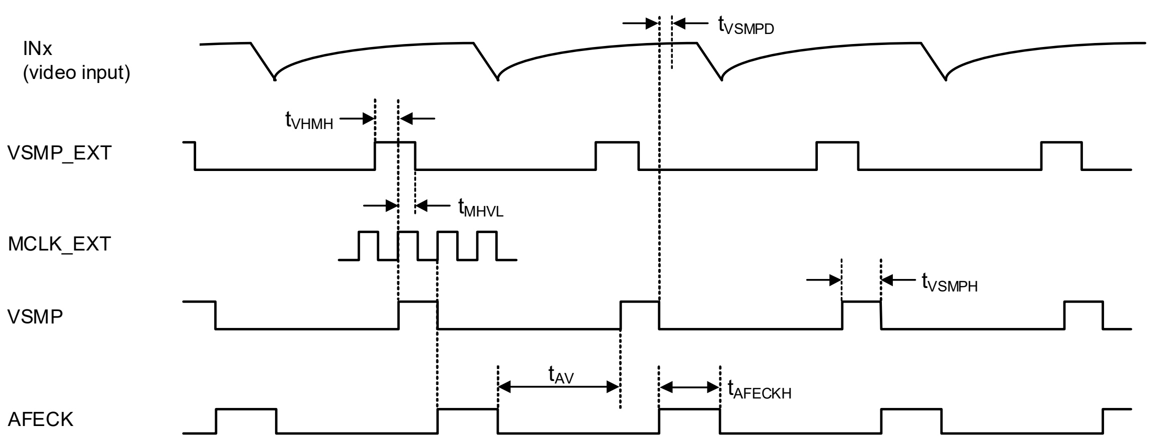
Parameter [1,2]		Symbol	Minimum	Typical	Maximum	Unit
Aperture delay from RSMP falling edge	CDS mode	t_{RSMPD}	—	8	—	ns
Aperture delay from VSMP falling edge		t_{VSMPD}	—	5	—	ns
RSMP high period	CDS mode	t_{RSMPH}	—	1	—	MCLK [3]
VSMP high period		t_{VSMPH}	—	1	—	MCLK [3]
AFECK high period		t_{AFECKH}	15	—	—	ns
RSMP falling edge to VSMP rising edge	CDS mode	t_{RV}	0	—	—	ns
AFECK falling edge to RSMP rising edge	CDS mode	t_{AR}	0.5	—	—	MCLK [3]
AFECK falling edge to VSMP rising edge	non-CDS mode	t_{AV}	0	—	—	ns
VSMP_EXT rising edge to MCLK rising edge		t_{VHMH}	1	—	—	ns
MCLK rising edge to VSMP_EXT falling edge		t_{MHVL}	2.7	—	—	ns

1. Video input timing—CDS mode. The VSMP and RSMP timing is controlled by external signal VSMP_EXT, retimed to MCLK_EXT.



Note: Assumes VSMP_EXT_DLY = 0 (rising edge of VSMP on first MCLK edge)
Assumes VSMP_EXT_POL = 0 (VSMP_EXT rising is the active edge)

2. Video input timing—non-CDS mode. The VSMP timing is controlled by external signal VSMP_EXT, retimed to MCLK_EXT.



Note: Assumes VSMP_EXT_DLY = 0 (rising edge of VSMP on first MCLK edge)
Assumes VSMP_EXT_POL = 0 (VSMP_EXT rising is the active edge)

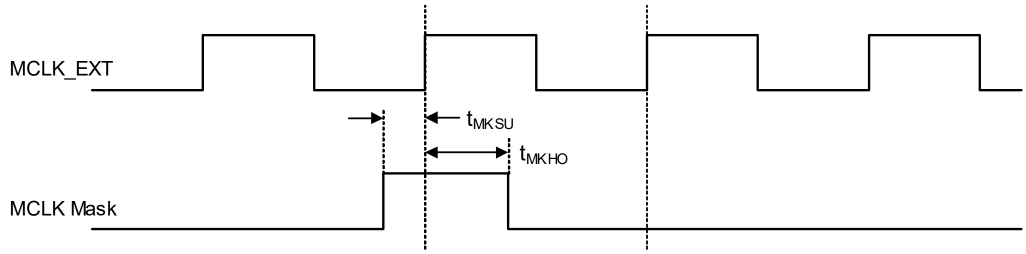
3. The MCLK unit refers to one period of the MCLK_EXT clock.

Table 3-14. Switching Specifications—MCLK Mask Timing (External Mode)

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

Parameter [1,2,3]	Symbol	Minimum	Typical	Maximum	Unit
MCLK Mask input setup time to MCLK rising	t_{MKSU}	5	—	—	ns
MCLK Mask input hold time from MCLK rising	t_{MKHO}	5	—	—	ns

1.Applies to External Mode 1 and External Mode 2.
2.MCLK Mask timing. Assumes mask input polarity is rising-edge triggered.



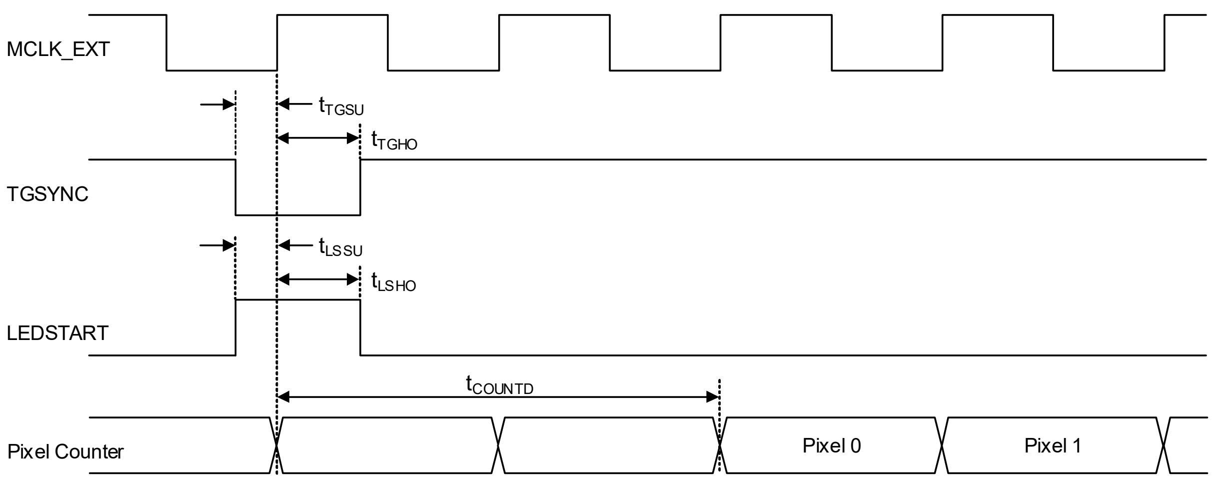
3.MCLK Mask input is supported on seven different pins—LEDR_EN, LEDG_EN, LEDB_EN, TGSYNC1, TGSYNC2, LED_START, or GPIO4.

Table 3-15. Switching Specifications—TGSYNC/LEDSTART Timing (External Mode)

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; T_A = +25ºC for typical specifications, T_A = 0–85ºC for min/max specifications.

Parameter [1,2,3,4]	Symbol	Minimum	Typical	Maximum	Unit
TGSYNC setup time to MCLK rising	t_{TGSU}	2	—	—	ns
TGSYNC hold time from MCLK rising	t_{TGHO}	2.5	—	—	ns
LEDSTART setup time to MCLK rising	t_{LSSU}	1.8	—	—	ns
LEDSTART hold time from MCLK rising [5]	t_{LSHO}	1.7	—	—	ns
Delay from TGSYNC pulse to pixel-counter reset [6]	t_{COUNTD}	—	2	—	cycles

1.Applies to External Mode 1 and External Mode 2. Assumes the TGSYNC filter is disabled; see Section 4.7.3.1 for details of the TGSYNC filter.
2.TGSYNC/LEDSTART timing.



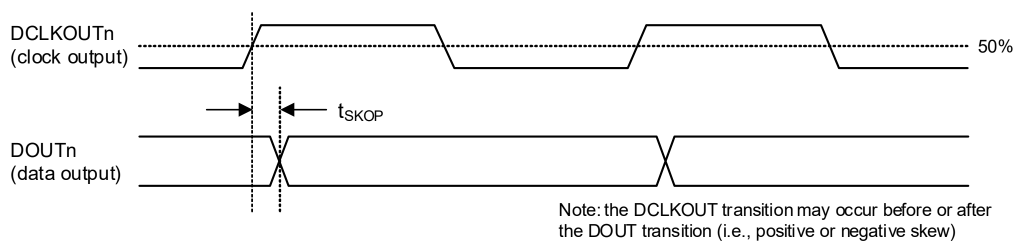
3.TGSYNC input is supported on three different pins—TGSYNC1, TGSYNC2, or LEDSTART.
4.LEDSTART input is only used if LEDSTART_SEQ_INIT is set.
5.LEDSTART hold time is measured from the second MCLK rising edge after the LEDSTART active edge.
6.Assumes TGSYNC_ASYNC = 0 for External Mode.

Table 3-16. Switching Specifications—Data Output

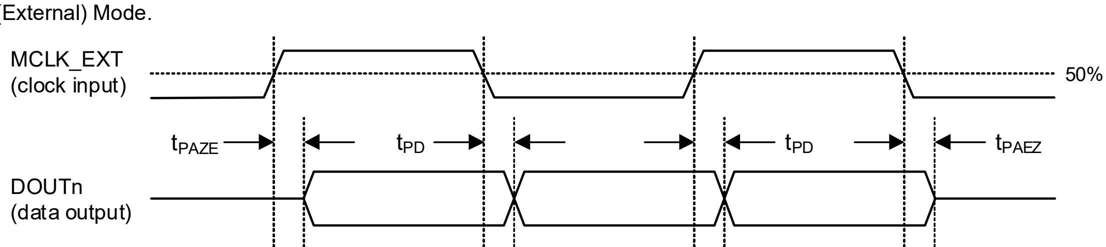
Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; Load capacitance = 10 pF; T_A = 0–85ºC.

Parameter [1,2,3]			Symbol	Minimum	Typical	Maximum	Unit
CMOS (TG) Mode	Clock frequency		—	—	—	60	MHz
	Data output skew		t_{SKOP}	–200	—	900	ps
CMOS (External) Mode	Propagation delay		t_{PD}	6	—	12	ns
	Output enable time	TDM Mode	t_{PAZE}	—	—	12	ns
	Output disable time	TDM Mode	t_{PAEZ}	—	—	12	ns
LVDS output	Clock frequency [4]	DCLKOUT_P/_N output	f_{LVCK}	—	—	72	MHz
	Data rate per output pair		—	—	—	504	Mbit/s
	Data output rise time (20%–80%)	3.6 mA drive strength 1.2 mA drive strength	t_{LVTR}	100 160	— —	250 330	ps ps
	Data output fall time (80%–20%)	3.6 mA drive strength 1.2 mA drive strength	t_{LVTF}	100 160	— —	250 330	ps ps
	Data output transition timing (t_{LVCK} = 1 / f_{LVCK})	Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 Bit 6 Bit 5	t_{LVDn}	–250 $t_{LVCK}/7$ – 250 $2t_{LVCK}/7$ – 250 $3t_{LVCK}/7$ – 250 $4t_{LVCK}/7$ – 250 $5t_{LVCK}/7$ – 250 $6t_{LVCK}/7$ – 250	0 $t_{LVCK}/7$ $2t_{LVCK}/7$ $3t_{LVCK}/7$ $4t_{LVCK}/7$ $5t_{LVCK}/7$ $6t_{LVCK}/7$	250 $t_{LVCK}/7$ + 250 $2t_{LVCK}/7$ + 250 $3t_{LVCK}/7$ + 250 $4t_{LVCK}/7$ + 250 $5t_{LVCK}/7$ + 250 $6t_{LVCK}/7$ + 250	ps ps ps ps ps ps ps

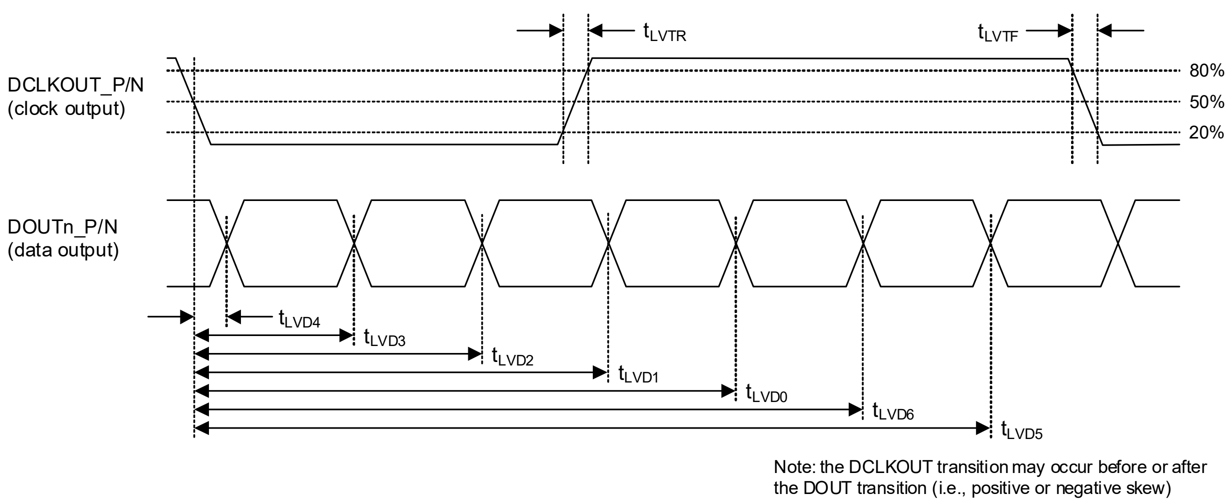
1. Output data timing—CMOS (TG) Mode.



2. Output data timing—CMOS (External) Mode.



3. Output data timing—Low-voltage differential signaling (LVDS).



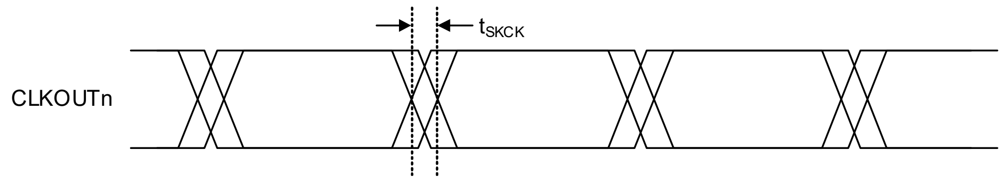
4. Assumes spread-spectrum modulation is disabled. If spread-spectrum modulation is enabled, the maximum instantaneous frequency may be higher.

Table 3-17. Switching Specifications—Clock Output

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; Load capacitance = 20 pF; T_A = 0–85ºC.

Parameter			Symbol	Minimum	Typical	Maximum	Unit
Pulse waveform clocks (P_CK)	Output skew [1,2]	Outputs with same CLKOUTx_POL	t_{SKCK}	0	—	1	ns
		Outputs with different CLKOUTx_POL		0	—	4	ns
	Propagation delay	PCKx_DLY = 0x0	—	—	0	—	ns
		PCKx_DLY = 0x1		—	1.5	—	ns
		PCKx_DLY = 0x2		—	2.0	—	ns
		PCKx_DLY = 0x3		—	3.5	—	ns
High speed clocks (C_CK)	Output skew [1,3]	Outputs with same CLKOUTx_POL	t_{SKCK}	0	—	1	ns
		Outputs with different CLKOUTx_POL		0	—	4	ns

1.Clock output skew. CLKOUT1–6 can be configured for high-speed clock outputs (C_CK) or pulse-waveform clock (P_CK) output.



2.Variation in timing between different P_CK outputs configured to toggle at the same pixel count. Assumes the same PCKx_DLY setting in each case.
3.Variation in timing between different C_CK outputs configured to toggle at the same DLL tap.

Table 3-18. Switching Specifications—Monitor Output

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; Load capacitance = 10 pF; T_A = 0–85ºC.

Parameter [1]		Symbol	Minimum	Typical	Maximum	Unit
Propagation delay	VSMP, RSMP	t_{PD}	—	2.5	—	ns

1.Output data timing.

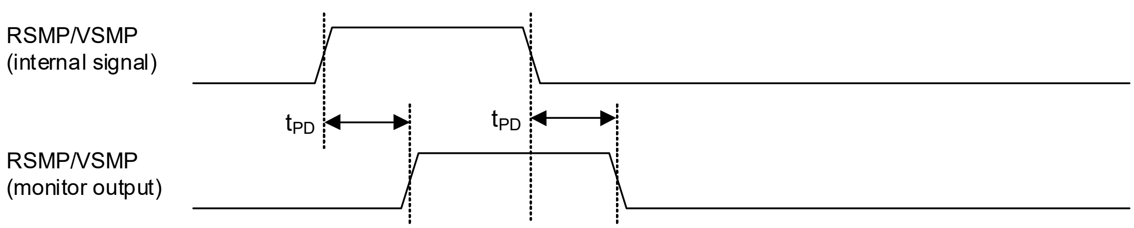
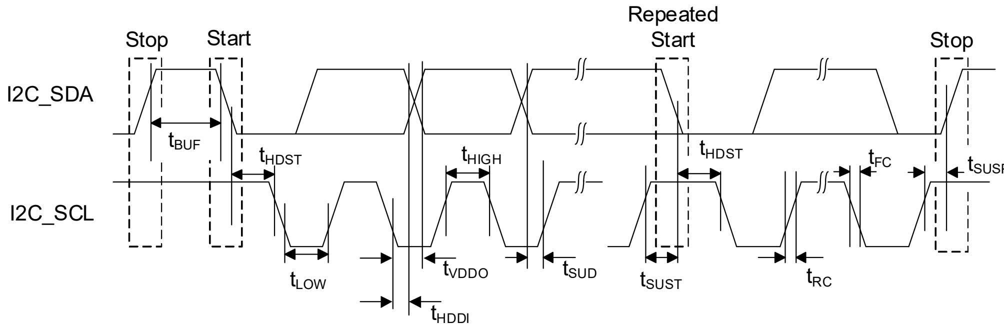


Table 3-19. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for CMOS input/output (as specified in Table 3-5); T_A = 0–85ºC.

Parameter [1]		Symbol	Minimum	Maximum	Unit
SCL clock frequency		f_{SCL}	—	1000	kHz
Clock low time		t_{LOW}	500	—	ns
Clock high time		t_{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)		t_{HDST}	260	—	ns
Setup time for repeated start		t_{SUST}	260	—	ns
Rise time of SCL and SDA	f_{SCL} ≤ 100 kHz 100 kHz < f_{SCL} ≤ 400 kHz 400 kHz < f_{SCL} ≤ 1000 kHz	t_{RC}	600 180 72	1000 300 120	ns ns ns
Fall time of SCL and SDA	f_{SCL} ≤ 100 kHz 100 kHz < f_{SCL} ≤ 400 kHz 400 kHz < f_{SCL} ≤ 1000 kHz	t_{FC}	6.5 6.5 6.5	300 300 120	ns ns ns
Rise time variation between SDA and SCL		—	—	1.67	x
Fall time variation between SDA and SCL	f_{SCL} ≤ 100 kHz 100 kHz < f_{SCL} ≤ 400 kHz 400 kHz < f_{SCL} ≤ 1000 kHz	—	— — —	100 100 75	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
SDA setup time to SCL rising		t_{SUD}	50	—	ns
SDA input hold time from SCL falling [2]		t_{HDDI}	0	—	ns
Output data valid (Data/ACK) [3]	f_{SCL} ≤ 100 kHz 100 kHz < f_{SCL} ≤ 400 kHz 400 kHz < f_{SCL} ≤ 1000 kHz	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
SDA bus capacitance		C_B	—	400	pF
SCL/SDA pull-up resistance		R_P	500	—	Ω
Pulse width of spikes to be suppressed		t_{ps}	0	50	ns

1.I²C control-port timing.



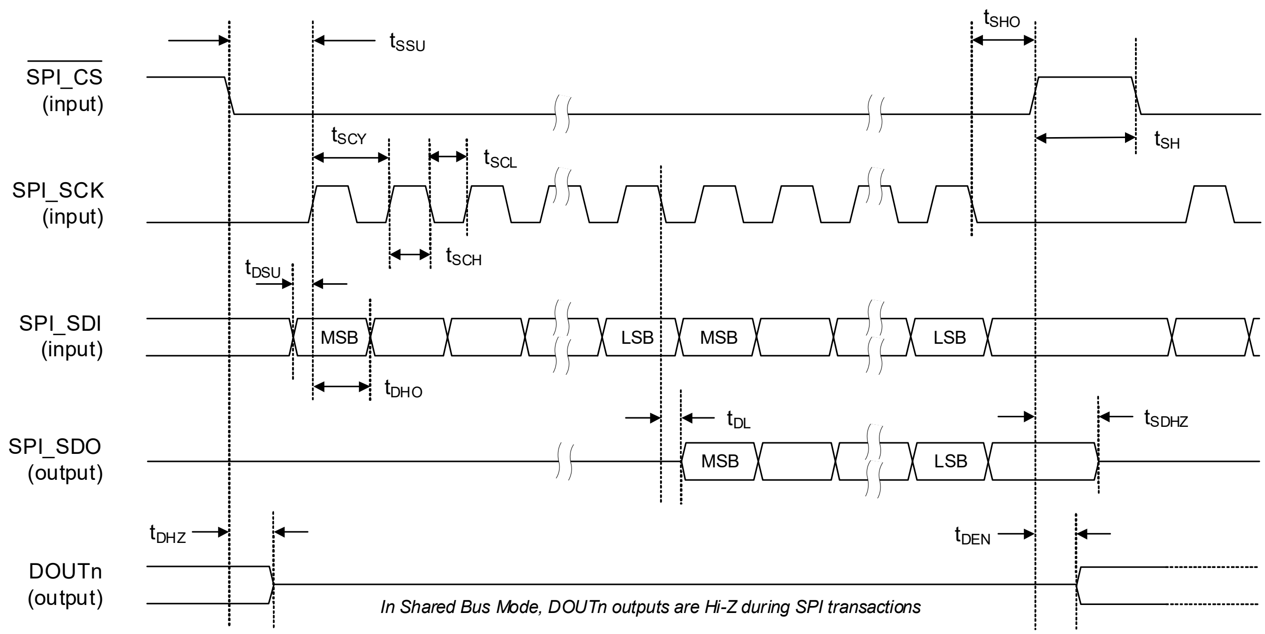
2.Data must be held long enough to bridge the transition time, t_{FC}, of SCL.
3.Time from falling edge of SCL until data output is valid.

Table 3-20. Switching Specifications—SPI Port

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO = 3.3 V; Ground = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for CMOS input/output (as specified in Table 3-5); T_A = 0–85ºC.

Parameter [1]	Symbol	Minimum	Maximum	Unit
SPI_SCK frequency [2,3]	$1/t_{SCY}$	—	12	MHz
SPI_CS falling edge to SPI_SCK rising edge	t_{SSU}	60	—	ns
SPI_SCK falling edge to SPI_CS rising edge	t_{SHO}	20	—	ns
SPI_SCK pulse width low	t_{SCL}	33	—	ns
SPI_SCK pulse width high	t_{SCH}	33	—	ns
SPI_SDI to SPI_SCK setup time	t_{DSU}	20	—	ns
SPI_SDI to SPI_SCK hold time	t_{DHO}	20	—	ns
SPI_SCK falling edge to SPI_SDO transition	t_{DL}	0	33	ns
SPI_CS rising edge to SPI_SDO output high-Z	t_{SDHZ}	0	22	ns
Bus free time between active SPI_CS [3]	t_{SH}	$9/f_{SYSCLK}$	—	ns
DOUT disable time from SPI_CS falling edge [4] Shared Bus Mode	t_{DHZ}	—	8	ns
DOUT enable time from SPI_CS rising edge [4,5] Shared Bus Mode	t_{DEN}	4	—	ns
DOUT disable time from GPI12 falling edge [6] Shared Bus Mode, GPI12_DOUT_CTRL = 1	—	—	10	ns
DOUT enable time from GPI12 rising edge [6] Shared Bus Mode, GPI12_DOUT_CTRL = 1	—	4	—	ns

1. SPI control-port timing.



2. The SPI_SCK frequency must not exceed the system clock frequency (SYSCLK).
3. The system clock frequency (SYSCLK) is a function of the device state (see Section 4.2) and the sample-timing mode (see Section 4.6):
   - In Idle State, SYSCLK = 16 MHz.
   - In Ready/Active states, TG Mode, SYSCLK = pixel sample rate (i.e., PLL1 output, if used; MCLK_EXT input if PLL1 is not used).
   - In Ready/Active states, External Mode, SYSCLK = MCLK_EXT/n, where n is number of channels in the digital output format (see Table 4-5).
4. In Shared Bus Mode, the DOUTn data outputs are disabled (Hi-Z) whenever SPI_CS is asserted (see Section 4.10.2.3).
5. In Shared Bus Mode, some operational constraints must be observed to avoid contention between SPI_SDO and DOUTn (see Section 4.10.2.3).
6. In Shared Bus Mode, if GPI12_DOUT_CTRL = 1, the DOUTn data outputs are disabled (Hi-Z) whenever GPI12 is Logic 0.

4 Functional Description

4.1 Power Supplies and Reset

The CS82L46 is powered using VDD_A and VDD_IO external supplies.

- **VDD_A** is the supply rail for the analog circuits, including internal regulators LDO1 and LDO3.

  The VDD_A supply is not required in the Idle and Sleep states; the VDD_A supply can be disabled in these states to reduce power consumption. Note the sensor must also be powered down if VDD_A is disabled, to ensure the INx analog input voltage does not exceed VDD_A.

  The VDD_A status is indicated using VDDA_STS. A valid VDD_A must be present when transitioning to the Ready or Active states. Sampling and conversion is not supported if VDD_A is not present.
- **VDD_IO** is the supply rail for digital input/output; it also powers other digital circuits via internal regulator LDO2.

There are no power-sequencing requirements—supplies can be enabled in any order.

Note that all digital inputs must be held low until VDD_IO is within the recommended operating limits. Analog video input must not be applied until VDD_A is within recommended operating limits. See Table 3-2 for maximum ratings.

4.1.1 Resets

The CS82L46 is in reset if the VDD_IO or VDD_A supply is below the reset threshold defined in Table 3-6. The POR sequence is scheduled on initial power-up, and following any interruption to VDD_IO or VDD_A that results in a drop below the reset threshold. The POR causes all of the CS82L46 control registers to be reset to their default states.

A software reset is triggered by writing 0x5A to the SFT_RESET field. A software reset causes all of the CS82L46 control registers to be reset to their default states.

On completion of the reset and associated start-up processes, the device transitions to the Idle State (see Section 4.2).

4.2 Operational States

The CS82L46 behavior is defined according to its operational states as follows:

- **Start-Up.** This is the initial state following reset, in which the device performs necessary start-up processes. On successful completion of start-up, the device automatically transitions to the Idle State.
- **Idle.** This is a low-power state in which the device can be configured for the required operational behavior. Register access is supported on the I2C/SPI control interface. After configuring the device, the host can command the device to transition to the Ready State.
- **Ready.** In this state, the analog input path and internal clocking circuits are fully enabled. The data-output clock is enabled, ready to support sample data in the configured format. In this state, the host can select the Active State when required.
- **Active.** This is the fully operational state, supporting active sampling and data output. The external sensor timing signals (CLKOUTn) are enabled, along with the internal pixel counters and associated functions.
- **Error.** This is the error state. See Section 4.2.1 for further details.
- **Sleep.** This is a dormant state with very low power consumption. Note that register access is not possible in this state, other than to wake the device to the Idle State.

The operational state transitions are shown in Fig. 4-1.

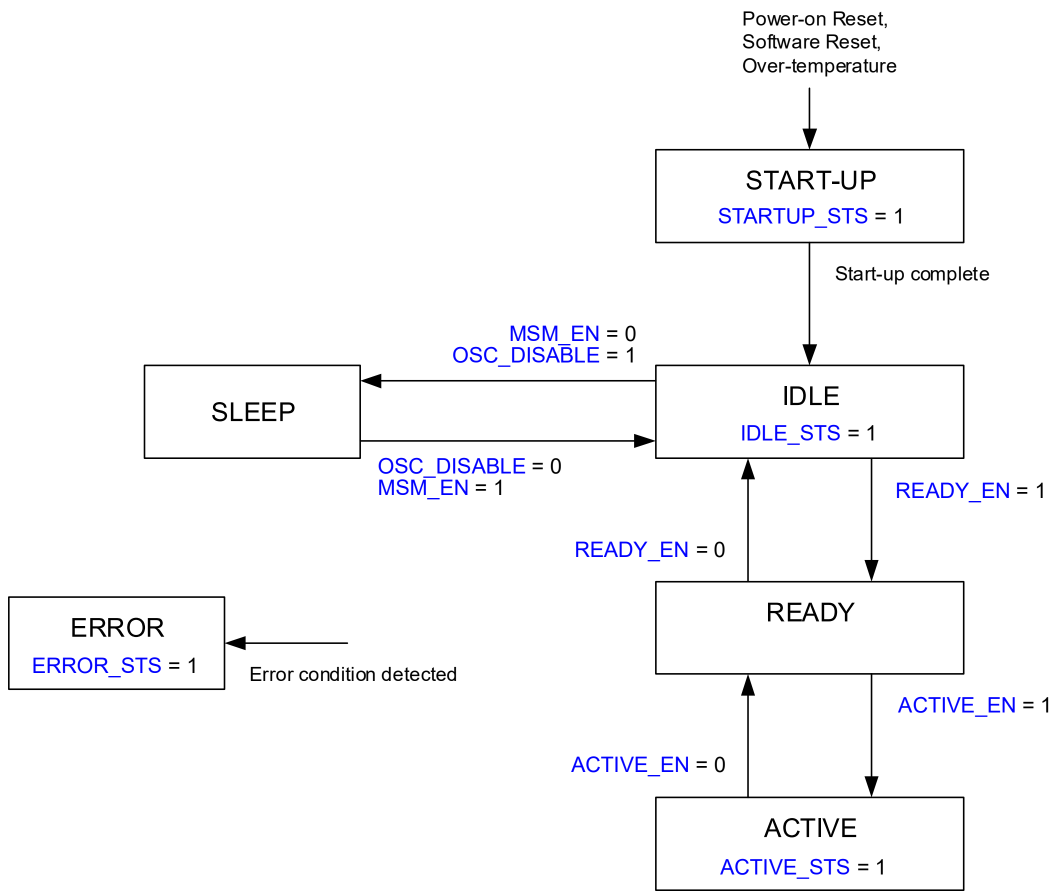


Figure 4-1. Operational States

The Start-Up State is indicated using STARTUP_STS. On successful completion of start-up, the device automatically transitions to the Idle State.

The Idle State is indicated using IDLE_STS. The CS82L46 is configured in the Idle State using the control interface (see Section 4.10). The transition from the Idle State to the Ready State is selected by setting READY_EN.

Notes: By default, the selected data-output format is enabled in the Ready State (the data bits and status flags are held at 0). If DOUT_READY_EN is cleared, the data output is not enabled in the Ready State. In all cases, the selected data-output format is fully enabled in the Active State.

If an invalid data-output format is selected, the transition from Idle to Ready is prevented, and the device remains in the Idle State. See Section 4.5 for further details of the data-output formats.

The Ready State is indicated using READY_STS. The transition from the Ready State to the Active State is selected by setting ACTIVE_EN.

The Active State is indicated using ACTIVE_STS. The transition from the Active State to the Ready State is selected by clearing ACTIVE_EN.

Note: The transition from Active to Ready is configurable using COMPLETE_LINE. If this bit is set, the CS82L46 completes the current scan line before transitioning to the Ready State. The end of line is assumed to correspond to the next sequence-state transition. This feature is supported in TG Master Mode only. See Section 4.7 for further details of the TG Sync and sequence-state options.

In the Ready State, the transition to the Idle State is selected by clearing READY_EN.

The Error State is selected if an error condition is detected; this is indicated using ERROR_STS. See Section 4.2.1 for further details.

The Sleep State is selected by clearing MSM_EN, then setting OSC_DISABLE. To exit the Sleep State, the host must clear OSC_DISABLE, then set MSM_EN. On exiting the Sleep State, the device transitions to the Idle State.

Note: The Sleep State should only be selected from the Idle State.

4.2.1 Error Conditions

If an error condition is detected, the error state is indicated using ERROR_STS. A more specific indication of the error is provided using the following fields.

- TEMP_ERROR_STS—Indicates an overtemperature error. In this event, an automatic reset shuts down all functions. The host must set TEMP_ERROR_CLR to return to the Idle State (provided the error has cleared). After returning to the Idle State, the host should then clear TEMP_ERROR_CLR.

  If TEMP_ERROR_RST_MASK is set, there is no reset following a temperature error; instead, there is a controlled shutdown of the analog path. The host must set TEMP_ERROR_CLR to return to the Idle State (provided the error has cleared). The host must also clear ACTIVE_EN and READY_EN. After returning to the Idle State, the host should then clear TEMP_ERROR_CLR.
- ACTIVE_ERROR_STS—Indicates an error in the Active or Ready state. The errors include clocking, temperature warning, AVDD absent, LDO error, LED driver errors, and data-output FIFO errors. The host must clear ACTIVE_EN and READY_EN to return to the Idle State (provided the error has cleared).
- STARTUP_ERROR_STS—Indicates a start-up error. This error can only be cleared by resetting the device.
- BOOT_ERROR_STS—Indicates a boot error. This error can only be cleared by resetting the device.
- MCLK_ERROR_STS—Indicates an invalid or absent MCLK in the Idle State. No corrective action is required by the host—the Ready State can be selected as usual, provided a valid MCLK has resumed.
- PLL_ERROR_STS—Indicates a PLL1 error condition. The host must clear ACTIVE_EN and READY_EN to return to the Idle State.

4.3 MCLK Input, PLL and DLL

The CS82L46 provides a flexible clocking architecture, supporting different operating configurations. An external clock reference (MCLK_EXT) is used to generate the required clocks and timing signals. The pixel sample rate is derived from the external reference—either directly, or else using a phase-locked loop (PLL) to synthesize a different frequency.

The CS82L46 incorporates PLL and DLL components as follows:

- DLL1 generates pixel-rate clock signals to control the video-input sampling and to generate external clocks
- PLL1 provides clock-frequency synthesis, enabling the pixel sample rate to be configured at a different frequency to the MCLK reference.
- PLL2 is used to control the data-output timing. PLL2 supports spread-spectrum modulation, allowing the data outputs to be modulated without affecting the AFE sample-timing signals.

In TG Mode (see Section 4.6), the clocking architecture is configured in three modes, shown in Fig. 4-2 through Fig. 4-4. In each case, the pixel sample rate is equal to the DLL reference frequency (DLL_REF).

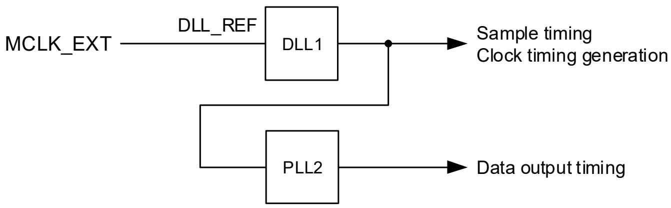


Figure 4-2. Clocking Mode 0

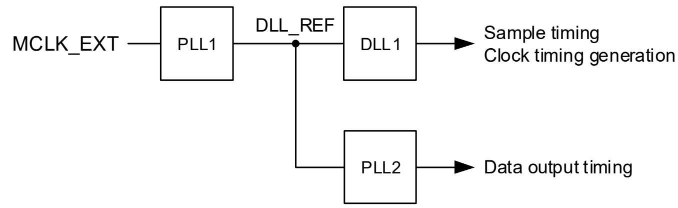


Figure 4-3. Clocking Mode 1

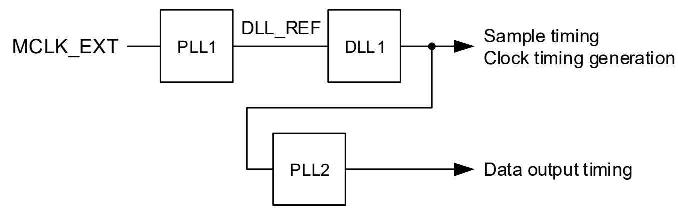


Figure 4-4. Clocking Mode 2

The clocking mode is selected using CLOCK_CFG_MODE. In Clocking Mode 0, the pixel sample rate is equal to the MCLK_EXT frequency. In Clocking Modes 1 and 2, the PLL1 circuit is used to support pixel sample rates that are different to the MCLK_EXT frequency—see Section 4.3.1 to configure PLL1.

The external clock reference (MCLK_EXT) is supported as a single-ended logic level (CMOS) or in differential (LVDS) mode; the applicable configuration is selected using MCLK_EXT_LVDS. In CMOS mode, the clock input is supported on the MCLK_EXT pin. In LVDS mode, the MCLK_EXT_N and MCLK_EXT_P connections are used.

Note: In LVDS mode, the pull resistors on MCLK_EXT_N and MCLK_EXT_P must be disabled using the respective x_PULL fields. See Section 4.11.3 for further details on configuring the digital I/O pins.

The supported frequency range for MCLK_EXT is described in Table 3-7. If spread-spectrum modulation is present on the external clock reference, the MCLK_EXT_SS bit must be set.

The PIXEL_SAMPLE_RATE field must be configured according to the applicable pixel sample rate. The pixel rate is derived from MCLK_EXT—either directly, or else using PLL1 to synthesize a different frequency.

In External Mode (see Section 4.6), the PLL/DLL functions are not supported. The MCLK frequency is a multiple of the pixel-sample rate, where the applicable frequency ratio is dependent on the selected output data format (see Section 4.5). The PIXEL_SAMPLE_RATE field must be configured according to the applicable pixel sample rate.

4.3.1 Phase-Locked Loop (PLL1) Configuration

In Clocking Modes 1 and 2, PLL1 can be used to provide clock-frequency synthesis.

If the pixel sample rate is equal to the MCLK reference frequency, the PLL1 frequency ratios and related parameters are configured automatically by setting PLL1_AUTO. If the required pixel sample rate differs from the MCLK reference frequency, the PLL is configured as described in Section 4.3.1.1.

4.3.1.1 PLL1 Frequency Conversion

PLL1 can be used to synthesize the clocking signals required to support pixel sample rates that are different to the MCLK reference frequency.

A script to calculate the PLL register configuration is provided within the SoundClear^{TM} Studio (SCS) CS82L46 device package. Note that the configuration is dependent on the frequency ratio and on the selected data-output format.

The PLL is configured using the following control fields:

- PLL1_OUTPUT1_DIV—selects the divider ratio for the ADC clock output
- PLL1_VCO_RANGE—configures the VCO frequency range
- PLL1_OUTPUT2_EN—enables the secondary clock output
- PLL1_OUTPUT2_DIV—selects the divider ratio for the data-output clock
- PLL1_REFCLK_DIV_BYPASS—disables the divider on the reference input
- PLL1_REFCLK_DIV_RATIO—selects the divider ratio for the reference input
- PLL1_RATIO—selects the VCO frequency ratio to the reference input
- PLL1_MODE—configures the PLL in fractional or integer mode
- PLL1_PHASE_DET_PAUSE_EN—pauses the phase detection when a phase change occurs in the reference
- PLL1_CP_IBIAS—configures the loop current bias
- PLL1_VCO_GAIN—configures the VCO gain
- PLL1_FILT—configures the PLL filter

4.3.2 Phase-Locked Loop (PLL2) Configuration

PLL2 is used to control the data-output timing in LVDS data-output formats. The spread-spectrum modulation allows the data outputs to be modulated without affecting the AFE sample-timing signals. Note that the spread-spectrum (SS) function is supported for LVDS data-output formats only.

The PLL2 frequency ratios and related parameters are configured automatically by setting PLL2_AUTO. This bit should be set in all use cases.

Spread-spectrum (SS) modulation is enabled on the PLL2 output by setting PLL2_SS_EN.

If SS modulation is enabled, the PLL2_SS_REF_FREQ field must be configured according to the PLL reference (i.e., MCLK) frequency. The automatic option for this field is recommended in all use cases.

The frequency of the SS modulation is configured using PLL2_SS_FREQ. This controls the rate at which the data-output frequency is modulated.

The magnitude of the SS modulation is configured using PLL2_SS_MAG. This controls the maximum deviation from the nominal data-output frequency.

The supported configurations for spread-spectrum modulation are dependent on the selected data-output format and on the pixel sample rate, as shown in Table 4-1. See Section 4.5 for details of the data-output formats.

Table 4-1. Spread Spectrum Configuration

Data Output Format	Pixel Sample Frequency (MHz)	Spread Spectrum Frequency (kHz)	Spread Spectrum Magnitude (max)
Group 1	2–24	12.5–37.5	2.0%
Group 2	2–18	12.5–37.5	2.0%
	18–24	12.5	1.5%
		18.75–37.5	2.0%
Group 3	2–12	12.5–37.5	2.0%
	12–18	12.5	1.5%
		18.75–37.5	2.0%
	18–24	12.5	1.0%
		18.75	1.5%
		25.0–37.5	2.0%
Group 4	2–6	12.5–37.5 kHz	2.0%
	6–12	12.5 kHz	1.5%
		18.75–37.5 kHz	2.0%
	12–18	12.5 kHz	1.0%
		18.75 kHz	1.5%
		25.0–37.5 kHz	2.0%
	18–24	—	—

The data-output formats are categorized in four groups. See Table 4-3 for a definition of the respective Format IDs

- Group 1 = Format ID 29, 76, 80, 84, 87
- Group 2 = Format ID 25, 30, 31, 33, 37, 41, 77, 78, 81, 82, 85, 86, 88, 89, 90, 91
- Group 3 = Format ID 26, 32, 34, 38, 42, 79, 83, 92
- Group 4 = Format ID 35, 27, 39, 43

If SS modulation is enabled, the sample-data FIFO buffer must be regularly flushed and reset to ensure timing differences do not result in underflow/overflow errors.

If FIFO_RESET_CTRL is set, the FIFO is flushed and reset at the start of the initial sequence state (see Section 4.7 for details of the sequence states). The FIFO is flushed by suspending the data written to the FIFO input, while the existing data continues to be read until the FIFO is empty.

The duration of the blank period (when data is not written to the FIFO) is configured using FIFO_BLANK_DUR. The default setting ensures the FIFO is always flushed, but this can be optimized if necessary. After the blank period, new sample data is written to the FIFO; data output restarts when the FIFO is 50% full.

When the FIFO is flushed, new sample data is not available for a period of (9 + n) pixels, where n is the duration configured by FIFO_BLANK_DUR. To avoid data loss, it must be ensured that this period is less than the sensor dummy-pixel period (during which no valid sensor data is available).

The duration of the blank period can be reduced in order to meet the above requirement; the minimum recommended value varies with data-output format as shown in Table 4-2.

Table 4-2. Spread Spectrum Configuration

Data Output Format [1]	Minimum Blank Period (FIFO_BLANK_DUR)
Group 1	0x18 (48 pixels)
Group 2	0x0C (24 pixels)
Group 3	0x08 (16 pixels)
Group 4	0x06 (12 pixels)

1. See Table 4-1 for data-output format groups

If the minimum recommended value is not low enough to avoid data loss, the timing can be reduced further by clearing FIFO_RESET_DLY—if this bit is 0, the flushing of the FIFO results in sample data being unavailable for a period of (2 + n) pixels, where n is the duration configured by FIFO_BLANK_DUR.

4.3.3 MCLK Masking

The CS82L46 provides configurable masking of the MCLK input. This can be used to prevent erroneous behavior in applications where glitches occur on the MCLK signal at certain periods during the scan pattern. The MCLK mask is triggered using an external control signal to indicate times at which the MCLK input may be corrupt.

Note: MCLK masking is valid in External Mode only (see Section 4.6).

The MCLK mask is enabled using MCLK_MASK_EN. The external signal used to trigger the mask is selected using MCLK_MASK_SRC. The active edge of the trigger signal is configured using MCLK_MASK_POL.

The mask trigger can be associated with the LEDR_EN, LEDG_EN, LEDB_EN, TGSYNC1, TGSYNC2, LED_START, or GPIO4 signals. These signals are supported on multifunction pins, which must be configured for the required functions as described in Section 4.11.

Notes: The mask trigger can be configured as the logical AND of the LED-enable signals (LEDx_EN). This option can be selected using MCLK_MASK_SRC.

If GPIO4 is used to trigger the MCLK mask, the pin must be configured for input as described in Section 4.11.3.

The MCLK input is masked if a valid edge is detected on the selected trigger signal. The MCLK_MASK_DLY field selects the time between the trigger condition and the start of the mask period. The duration of the mask period is configured using MCLK_MASK_DUR. A configurable clock period, derived from MCLK, is used to define the mask delay and mask duration; the clock period is configured using MCLK_MASK_CLK_DIV.

Data output is invalid while the MCLK mask is applied. To ensure the data output is correctly reset following the MCLK mask period, the MCLK_MASK_OPF_RST bit must be set.

The MCLK masking is illustrated in Fig. 4-5.

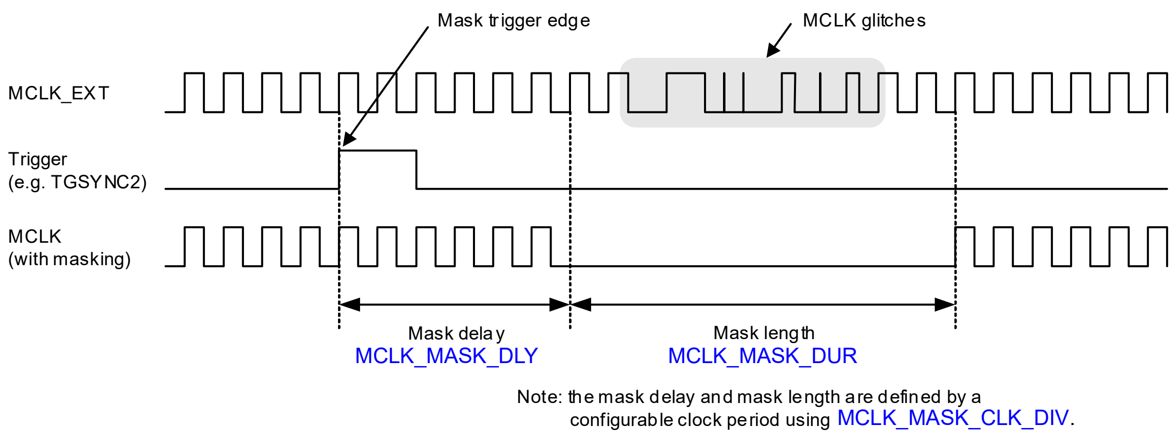


Figure 4-5. MCLK Masking

4.4 Analog Input Path

The analog input path supports video input from an external sensor. The input path can be optimized to support a wide range of CIS and CCD sensors. A voltage reference (VBIAS) for the sensor can be generated internally on the CS82L46, or else can be provided from an external source.

The CS82L46 supports CDS and non-CDS sampling modes. For non-CDS operation, the video signal is sampled once per pixel. For CDS processing, two samples per pixel are used (reset level and video level); the correlated processing of these samples enables common-mode noise to be suppressed.

The clamp circuit allows the device to support video signals that exceed the maximum DC input voltage, and to align the video input to the VBIAS reference. Clamping can be applied during the reset portion of active scan pixels (pixel clamping) or else during black pixels outside the active scan periods (line clamping).

The input path can be optimized for different sensors using configurable offset, gain, and signal inversion. Separate controls are provided for each input channel. Different parameter values can also be set for different sequence states, allowing cyclic configuration for different phases of the scan pattern. Automatic black-level calibration (BLC) is supported.

An integrated test-pattern generator is available to assist with device set-up, with no input signal required.

An overview of the analog input path is shown in Fig. 4-6.

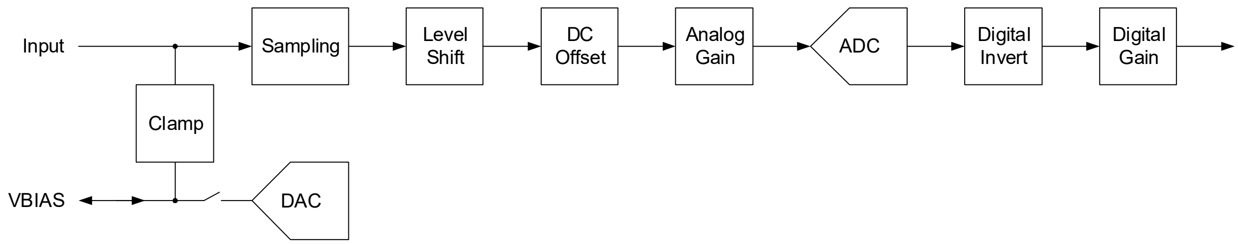


Figure 4-6. Analog Input Path

An example calculation to determine the digital output code for a given analog input voltage is described in Section 5.2.

4.4.1 Input Sampling Mode

The CS82L46 supports a wide range of video input signals. Typical CIS and CCD sensor waveforms are shown in Fig. 4-7.

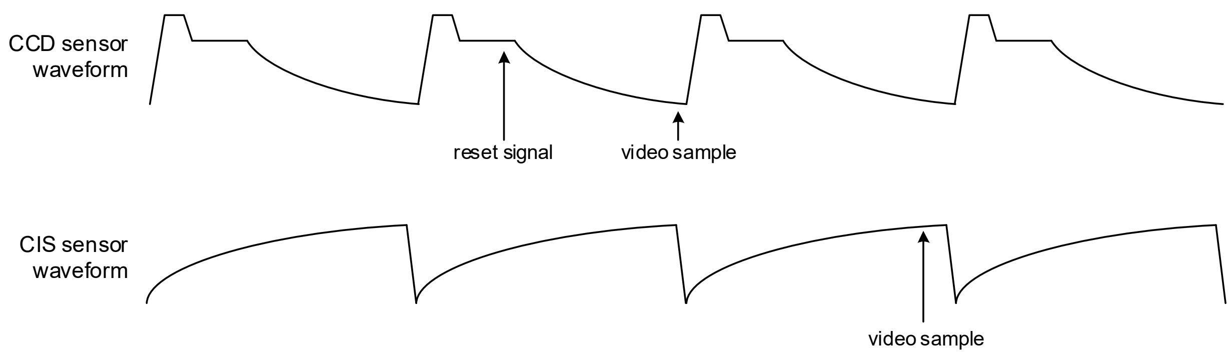


Figure 4-7. Typical CIS/CCD Waveforms

The analog input path can be configured in CDS or non-CDS sampling modes as follows:

- In CDS mode (CDS_EN = 1), the reset level and the video level are sampled for each pixel. This is typically used with CCD sensors, where the video waveform includes a reset level for each pixel. In CDS sampling mode, each video sample is measured relative to the reset level in the same pixel frame.
- In non-CDS mode (CDS_EN = 0), a single video-level sample is used for each pixel. This is typically used with CIS sensors, where the video waveform does not provide a reset level for each pixel. In this case, the video sample is measured relative to the VBIAS reference (see Section 4.4.2).

Note that both sampling modes (CDS or non-CDS) may be used with either type of sensor (CIS or CCD). The suitability of either sampling mode must be determined by the specific waveforms and timing constraints of the target application.

The analog input path can be configured for low-power operation, enabling power savings under suitable operating conditions. The default, high-performance configuration is recommended for pixel sample rates of 10 MHz and above. For slower sample rates, power consumption can be optimized using CHx_AFE_POWER.

4.4.2 Bias Voltage (VBIAS)

The CS82L46 provides a configurable voltage reference on the VBIAS pin; this is used as an input to the external sensor and as a reference for the analog input path. The VBIAS reference is required during active sampling. In non-CDS sampling mode, the bias voltage provides the reference level for the input-signal measurement. When the input clamp is active (see Section 4.4.3), the video input is clamped to the VBIAS reference.

The VBIAS reference is configured using the reset-level clamp (RLC) DAC. The bias is enabled using VBIAS_EN; the output voltage is configured using VBIAS_LVL.

The bias voltage should be configured within the operating conditions of the sensor. If input clamping is enabled, the bias should be set at the desired reset level, ensuring that both the reset level and the full-scale level are within the measurement range of the CS82L46 (see Section 4.4.3 for further details).

The drive strength of the bias is configurable using VBIAS_ISEL and VBIAS_ISEL_BOOST. The internal source for the bias reference is selected using VBIAS_REF; the VREF source is recommended in all cases.

Note: The bias voltage can also be provided externally. The RLC DAC must be disabled if an external reference source is connected to the VBIAS pin.

4.4.3 Clamp Control

The clamp provides a short circuit between the input signal and the VBIAS reference. The clamp is used with AC-coupled inputs to align the video signal within the measurable range of the CS82L46. The clamp enables video signals that exceed the full-scale input level to be accommodated; it can also be used to protect the input circuits from transient voltages that may arise during sensor start-up.

The full-scale input voltage is defined in Table 3-3. If the input signal (at the reset- or video-sample points) exceeds the full-scale level, the clamp must be used to offset the signal level within the permitted limit.

Note: The output from a CCD sensor typically includes transients that do not represent either the reset level or the video sample level; these transients do not need to lie within the measurable range. However, the absolute maximum rating of the input pins (see Table 3-2) must be observed at all times.

If the clamp is used, the inputs must be AC-coupled using a capacitor on the input pins as shown in Section 2. If the clamp is not used, the DC-coupled configuration is recommended (i.e., without a capacitor).

The clamp operation must be timed to coincide with the input reset signal, in order to align the reset (black) level with the VBIAS reference. To ensure correct behavior, the input voltage must be a constant level while the clamp is active.

- In CDS mode, the clamp can be applied during the reset portion of active scan pixels (pixel clamping).
- In non-CDS mode, the clamp is typically used during black pixels outside the active scan periods (line clamping).

The clamp circuit is illustrated in Fig. 4-8. The clamp is used with the VBIAS reference to adjust the video signal level within the operating limits of the CS82L46.

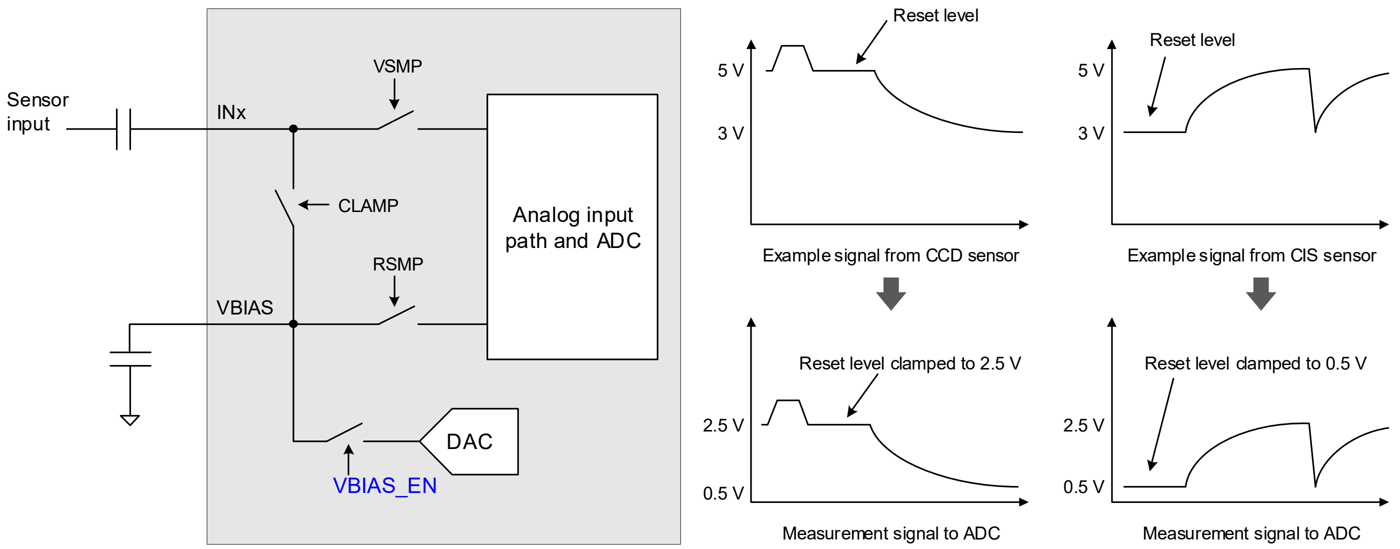


Figure 4-8. Input Clamp

The clamp function is enabled by setting CLAMP_EN. The CLAMP_MODE field is used to select when clamping is applied.

- If CLAMP_MODE = 00, clamping is enabled for all pixels.
- If CLAMP_MODE = 01, clamping is enabled across a defined range of pixel-counter values (valid in TG Mode only).

  In this mode, the pixel range is configured using CLAMP_START and CLAMP_END. The range is referenced to the primary or secondary pixel counter using CLAMP_CNT_SEL.

  If the range is referenced to the secondary pixel counter, the clamp operation can be selectively enabled for individual sequence states using CLAMP_SEQ_SEL. Each bit within these fields enables the clamp in the corresponding state (see Section 4.7.1 for details of the sequence state).
- If CLAMP_MODE = 10, clamping is enabled if RSMP_EXT is asserted (Logic 1). The RSMP_EXT function is supported on a multifunction pin, which must be configured for the required functions as described in Section 4.11.

  Note this option is not valid if CDS sampling is enabled in External Mode 1 (see Section 4.6).

During pixels where clamping is enabled (and the applicable CLAMP_MODE condition is met), the clamp is applied for a portion of the respective pixel frames. In CDS mode, the clamp is applied while RSMP is asserted; in non-CDS mode, the clamp is applied while VSMP is not asserted. See Section 4.6 for further details of the VSMP and RSMP signals.

The clamp timing in CDS mode is illustrated in Fig. 4-9.

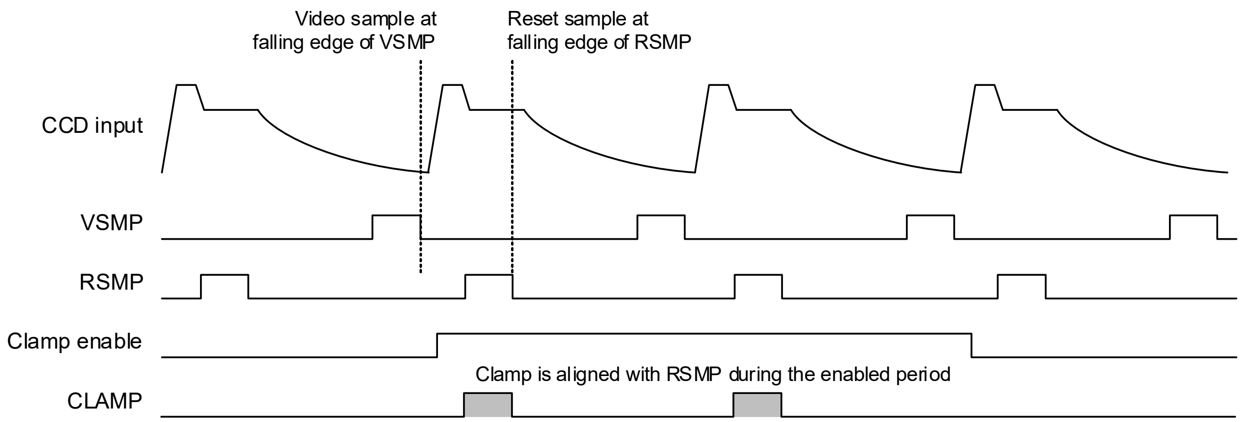


Figure 4-9. Clamp Timing (CDS Mode)

The clamp timing in non-CDS mode is illustrated in Fig. 4-10.

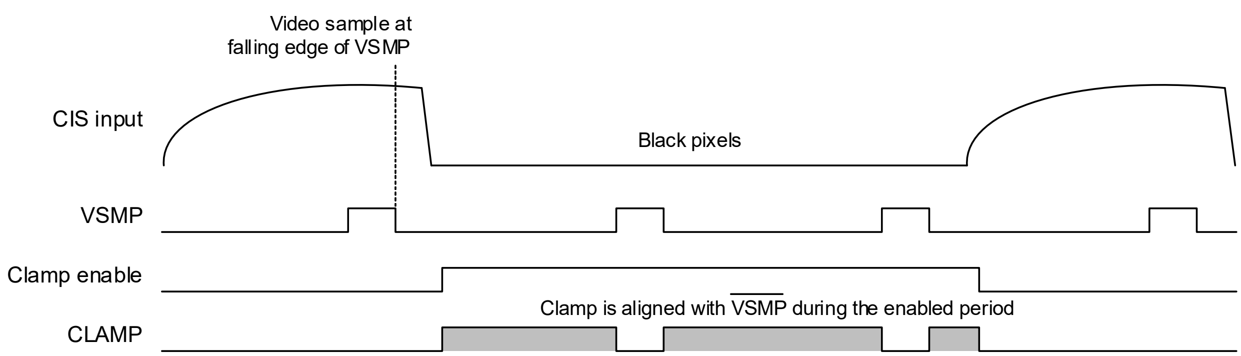


Figure 4-10. Clamp Timing (Non-CDS Mode)

The clamp can also be enabled using CHx_CLAMP_OVRD (where x is 1–6 for the respective input channel). If these bits are set, the respective clamp is enabled continuously until the bit is cleared. This can be used to protect the input circuits from transient voltages that may arise during sensor start-up.

4.4.4 Polarity Select

The analog input path provides selectable polarity control for each input channel; this can be used to accommodate different types of sensor waveform. The polarity of the sensor waveforms are defined as follows:

- For a CCD-type waveform, the reset level is higher than the video sample level; this is inverted polarity.
- For a CIS-type waveform, the reset level is lower than the video sample level; this is non-inverted polarity.

The full-scale signal level for the input path is 2.4 V pk-pk (see Table 3-3). The input signal is measured relative to the VBIAS/reset level, as described in Section 4.4.1.

The analog input path must be configured for the polarity of the input waveform. If inverted polarity is selected, the waveform is level-shifted so the reset-level signal is measured around 2.4 V. If non-inverted polarity is selected, there is no level shift, and the reset-level is measured around 0 V.

Note: The level shift can be combined with additional DC offset as described in Section 4.4.5.

The polarity selection is illustrated in Fig. 4-11 for typical CCD and CIS sensor waveforms. The inverted CCD waveform is level-shifted to the 2.4 V level. The non-inverted CIS waveform is unaffected.

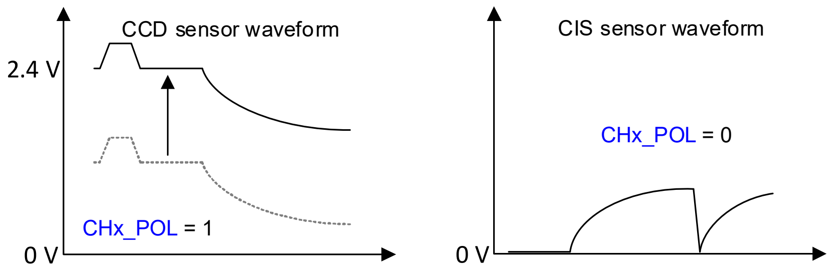


Figure 4-11. Polarity Select

The polarity is configured independently for each input channel using CHx_POL in the respective register block. Note this bit is defined in each of the ADC register blocks 1–6, and must be configured in each block for the respective input channel.

4.4.5 Offset Control

The offset provides DC adjustment to the analog input signal. The offset can be either positive or negative, and can be used to optimize the input path for the video signal.

The offset is illustrated in Fig. 4-12 for typical CCD and CIS sensor waveforms.

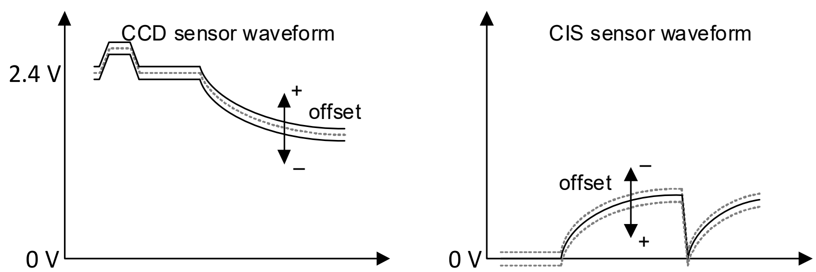


Figure 4-12. Offset Control

The offset can be set in the range –333 mV to +333 mV. The offset is applied differently depending on whether the signal path is inverted (see Section 4.4.4):

- If the signal path is inverted (CHx_POL = 1), the offset is added to signal voltage—a positive offset increases the output voltage, and a negative offset decreases the output voltage.
- If the signal path is not inverted (CHx_POL = 0), the offset is subtracted from the signal voltage—a positive offset decreases the output voltage, and a negative offset increases the output voltage.

The offset can be configured independently for each input channel. The offset is associated with the sequence state, allowing different offsets to be applied automatically according to the current state (see Section 4.7.1 for details of the sequence state).

The offset associated with each sequence state is configured using CHx_SEQn_OFFSET (where *n* is 0–3 for the respective sequence state, and *x* is 1–6 for the respective input channel).

The auto-cycle function is enabled using ACYC_EN. If auto-cycle is enabled, the offset for each channel is determined by the current sequence state. If auto-cycle is disabled, the offset configured State 0 is used.

Note: Auto-cycle is supported in TG Mode only (see Section 4.6). In External Mode, auto-cycle must be disabled.

If auto-cycle is enabled, a different offset is applied for each sequence state. The offset for each sequence state can be applied directly following the respective state transition. Alternatively, the respective offset settings can be controlled by one of the pulse-output sources, PO0–PO10; this can be used to control the timing independently for each sequence state. See Section 4.8.2 for details of the pulse-output sources.

The auto-cycle timing mode is selected using ACYC_MODE. This bit selects one of two behaviors:

- If fixed timing is selected, the offset for each sequence state is applied following a fixed delay after the respective state transition. The delay is configured using ACYC_DELAY.
- If PO timing is selected, the offset for each sequence state is controlled by one of the pulse-waveform sources, PO0–PO10. The applicable pulse source is selected using ACYC_PO_SEL. The active edge is selected using ACYC_PO_POL. The offset associated with the current sequence state is applied on the first active edge of the pulse waveform that occurs during the sequence state.

The black-level calibration (BLC) function can also be used to configure the offset automatically—see Section 4.4.10.

Note: If BLC is enabled, the auto-cycle function must be configured for the minimum timing delay. If BLC is enabled, set ACYC_MODE = 0 and ACYC_DELAY = 0x00.

4.4.6 Analog Gain Control

The analog gain provides control of the input signal amplitude. The analog gain can be used to optimize the input signal to match the measurable range of the ADC.

The analog gain is illustrated in Fig. 4-13 for typical CCD and CIS sensor waveforms.

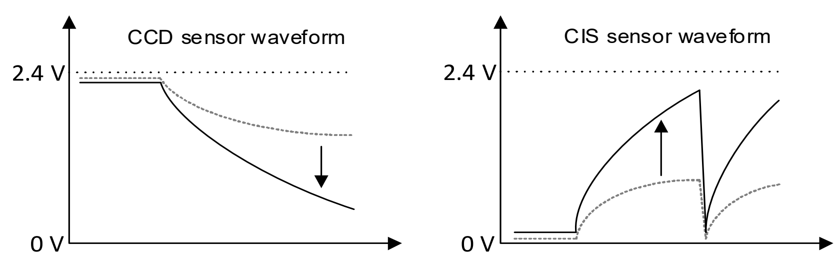


Figure 4-13. Analog Gain

The analog gain can be configured independently for each input channel. The gain is associated with the sequence state, allowing different gain settings to be applied automatically according to the current state.

The analog gain associated with each sequence state is configured using CHx_SEQn_AGAIN (where *n* is 0–3 for the respective sequence state, and *x* is 1–6 for the respective input channel).

The auto-cycle function is enabled using ACYC_EN. If auto-cycle is enabled, the gain for each channel is determined by the current sequence state. If auto-cycle is disabled, the gain configured State 0 is used.

Note: Auto-cycle is supported in TG Mode only (see Section 4.6). In External Mode, auto-cycle must be disabled.

If auto-cycle is enabled, a different gain setting is applied for each sequence state. The gain settings are applied at the same time as the respective offset, as described in Section 4.4.5.

4.4.7 Analog to Digital Converter (ADC)

A high-performance analog-to-digital converter (ADC) is provided for each input channel. The ADC is configured automatically and does not require any user configuration.

4.4.8 Digital Invert

The input path accommodates sensor waveforms of inverted or non-inverted polarity, as described in Section 4.4.4. The digital invert is used to ensure the ADC output is a standardized polarity for all signal types, i.e., the reset (black) signal level is a lower numerical value than the full-scale (white) signal level.

The digital invert is configured automatically to align with the selected polarity of the analog input.

The digital invert is illustrated in Fig. 4-14 for typical CCD and CIS sensor waveforms. The inverted CCD waveform is adjusted so the reset (black) signal level is towards the zero end of the digital range. The non-inverted CIS waveform is unaffected.

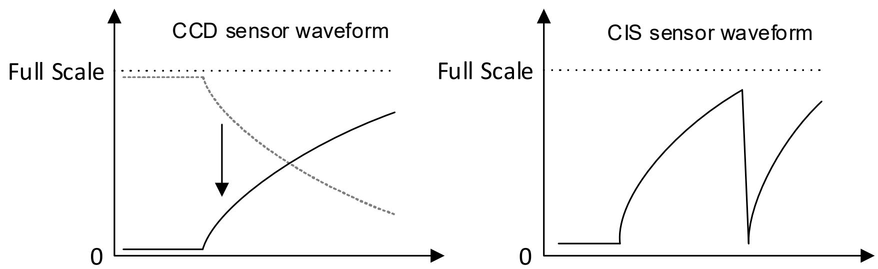


Figure 4-14. Digital Invert

4.4.9 Digital Gain Control

The digital gain provides control of the digital output scaling. In typical applications, the digital gain is configured to set the highest signal level close to the full-scale digital level.

The digital gain is illustrated in Fig. 4-15 for typical CCD and CIS sensor waveforms.

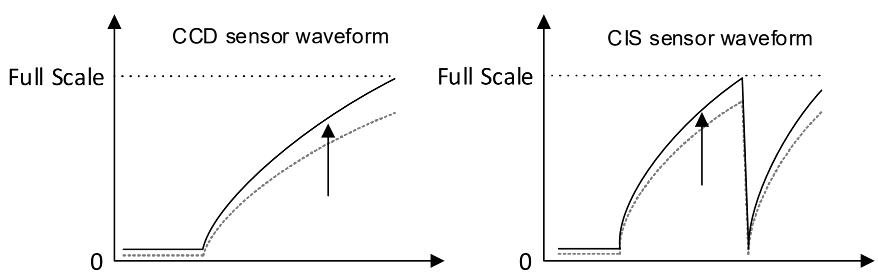


Figure 4-15. Digital Gain

The digital gain can be configured independently for each ADC channel. The gain is associated with the sequence state, allowing different gain settings to be applied automatically according to the current state.

The digital gain associated with each sequence state is configured using CHx_SEQn_DGAIN (where *n* is 0–3 for the respective sequence state, and *x* is 1–6 for the respective ADC channel).

The auto-cycle function is enabled using ACYC_EN. If auto-cycle is enabled, the gain for each channel is determined by the current sequence state. If auto-cycle is disabled, the gain configured for State 0 is used.

Note: Auto-cycle is supported in TG Mode only (see Section 4.6). In External Mode, auto-cycle must be disabled.

If auto-cycle is enabled, a different gain setting is applied for each sequence state. The digital gain settings are applied at the same time as the respective analog gain, as described in Section 4.4.6.

4.4.10 Black-Level Calibration (BLC)

Black-level calibration (BLC) can be used to automatically configure the DC offset in the input signal path. The signal level is monitored at the digital output, and used to adjust the required DC offset. The calibration process uses the black pixels at the start of a scan line to determine the required offset to achieve a specified target level.

Note: BLC is supported in TG Mode only (see Section 4.6). In External Mode, BLC must be disabled.

BLC comprises coarse adjustment and fine adjustment, which can be scheduled in different ways to suit the application. In a typical application, coarse adjustment is performed infrequently (e.g., once per page); fine adjustment can be performed on every line, or else just once per page following the coarse adjustment.

The BLC function is disabled if coarse adjustment is disabled (BLC_COARSE_CYCLES = 0x0) and fine adjustment is disabled (BLC_FINE_EN = 0).

BLC is configured by defining which pixels (at the start of a scan line) are used for calibration. The pixel-count value of the first pixel to be used is configured using BLC_START. The total number of pixels available for calibration is configured using BLC_LENGTH, valid from 18–1023

Note: The scan pattern comprises one or more sequence states (maximum four), as described in Section 4.7. If multiple states are used, the same range of pixels is used for BLC in each state.

The first pixel for BLC is referenced to the primary or secondary pixel counter using BLC_CNT_SEL. If the pixel is referenced to the secondary pixel counter, the BLC function can be selectively enabled for individual sequence states using BLC_SEQ_SEL—each bit within this field enables BLC in the corresponding state. See Section 4.7 for further details of the pixel counters and sequence states.

Coarse adjustment is performed at the start of a frame (e.g., at the start of a page). The controller device signals the start of a frame by setting BLC_FRAME_START. If this bit is set, the start of frame occurs on the next state transition to the initial state (typically State 0). The BLC_FRAME_START bit is cleared automatically after BLC is scheduled.

The number of iterations of coarse adjustment is configured using BLC_COARSE_CYCLES. Each iteration requires a duration of 12 pixels; the total number of pixels used for coarse adjustment must be less than the total number of pixels available for calibration.

Notes: If the desired number of coarse-adjustment iterations is constrained by the total number of pixels available for calibration, the analog gain (see Section 4.4.6) should be reduced to improve the BLC performance.

If BLC is used, the number of coarse-adjustment iterations must be ≥ 1.

Fine adjustment is enabled using BLC_FINE_EN. If enabled, fine adjustment is performed at the start of a frame, immediately following the coarse adjustment. Fine adjustment can be enabled on every scan line using BLC_FINE_EVERYLINE.

If fine adjustment is enabled on every line, the offset calculation can be accumulated from one line to the next, or can be recalculated (from the coarse adjustment result) at the start of each line. The BLC_FINE_ACCUM bit is used to select the accumulating option.

The fine adjustment incorporates a configurable filter to accommodate different input-signal behavior. The filter balances DC-tracking performance against noise suppression. By default, the filter is optimized for noise suppression. If there is significant DC drift during the fine-adjustment process, the filter can be adjusted to improve the DC tracking. The filter is configured using BLC_TRACKING.

The target level for BLC in each sequence state is configured using CHx_SEQn_BLC_TARGET (where *n* is 0–3 for the respective sequence state, and *x* is 1–6 for the respective ADC channel). The selectable range of the BLC target level can be extended using BLC_TARGET_RANGE. If this bit is set, the effective level is multiplied by four.

The target level can be configured within a limited range of the supported digital-output codes, dependent on the output format. If BLC_TARGET_RANGE = 0, the following ranges are supported:

- In 16-bit output format, the target level represents bits [11:4] of the output code. Range 0–4080, step size 16.
- In 12-bit output format, the target level represents bits [7:0] of the output code. Range 0–255, step size 1.
- In 10-bit output format, bits [7:2] of the target level represent bits [5:0] of the output code. Range 0–63, step size 1.

If BLC_TARGET_RANGE = 1, the following ranges are supported:

- In 16-bit output format, the target level represents bits [13:6] of the output code. Range 0–16320, step size 64.
- In 12-bit output format, the target level represents bits [9:2] of the output code. Range 0–1020, step size 4.
- In 10-bit output format, the target level represent bits [7:0] of the output code. Range 0–255, step size 1.

The offset applied by the BLC function is indicated using CHx_BLC_OFFSET for the respective ADC channel.

Examples of the BLC configuration are shown in Fig. 4-16 through Fig. 4-18.

In the example shown in Fig. 4-16, fine adjustment is enabled for every line, with the calibration recalculated for each line. This configuration is suitable if there is large DC drift during a frame.

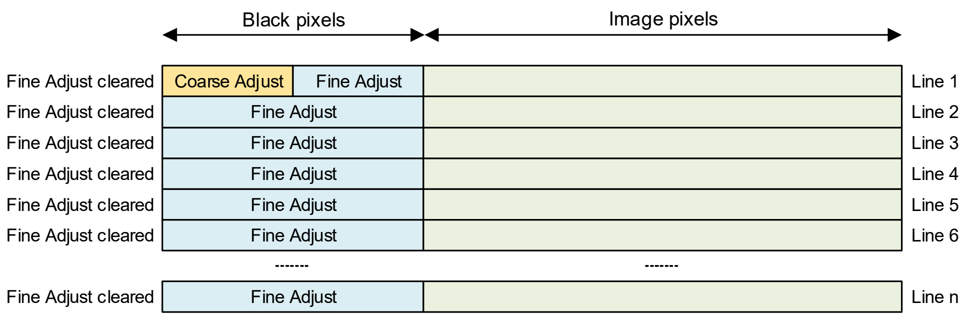


Figure 4-16. Black Level Calibration—Example 1

In the example shown in Fig. 4-17, fine adjustment is enabled for first line only. This configuration is suitable for adjusting DC drift on a frame-by-frame basis.

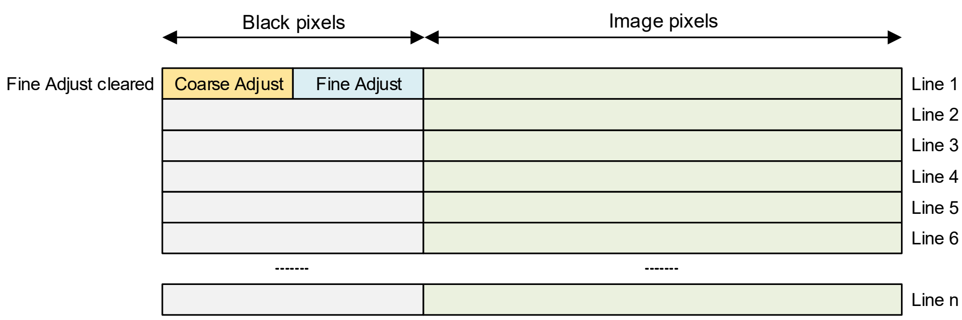


Figure 4-17. Black Level Calibration—Example 2

In the example shown in Fig. 4-18, fine adjustment is enabled for every line, with the calibration accumulated from one line to the next. This configuration minimizes the line-by-line variation, but does not suppress DC drift to the same extent as Example 1.

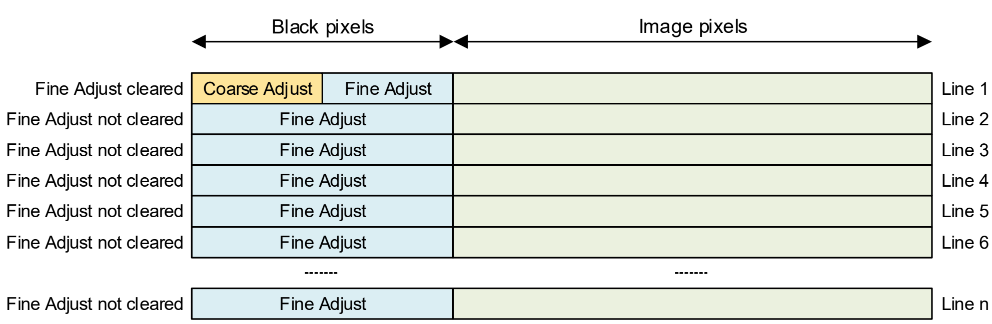


Figure 4-18. Black Level Calibration—Example 3

4.4.11 Pattern Generator

The CS82L46 incorporates a pattern generator, which can be used for set-up and debug purposes. The pattern generator allows the digital output format to be verified without any analog input required. The pattern generator is configurable to support different test patterns on the digital output.

If the pattern generator is enabled, the analog input path is bypassed. Note that other required functions must be configured as for normal operation:

- External clock reference, and PLL1 if required (Section 4.3)
- Digital output in LVDS or CMOS (TG) format (Section 4.5)
- Sample timing control in TG Mode, with valid VSMP, RSMP, AFECK timing (Section 4.6.1)
- TG Sync (master or slave) and pixel counter configuration (Section 4.7)

The latency of the data output is defined in Section 4.6.1. Note that the latency when using the pattern generator differs from the latency in normal operation.

To ensure correct display of the test pattern, the pattern generator must be configured according to how the timing signals are used in the application. See Section 4.7 for details of the sequence states and pixel counters.

- If the scan line corresponds to the primary-counter period (i.e., new line on each cycle of the sequence states), PGEN_CNT_SEL should be cleared.
- If the scan line corresponds to the secondary-counter period (i.e., new line for each sequence-state transition), PGEN_CNT_SEL should be set.

The pattern generator is enabled using PGEN_EN. The pattern should be configured, and PGEN_EN set, while in the Idle State. After transitioning to the Active State, the configured pattern is output following the first TG Sync pulse. To reconfigure the pattern generator, the PGEN_EN bit must be cleared; this can be done while remaining in the Active State.

Note: After clearing PGEN_EN in the Active State, the host system must wait until after the next TG Sync pulse before reconfiguring the pattern.

Four different test patterns can be selected using PGEN_PATT_SEL. If PGEN_MARCH is set, the selection is overridden and the marching pattern is implemented.

The dimensions of the selected pattern are configured using PGEN_WIDTH1 and PGEN_WIDTH2. The intensity of the selected pattern is configured using PGEN_LVL. The pattern intensity can be inverted using PGEN_INV.

Further details of each pattern are provided in Section 4.4.11.1 through Section 4.4.11.5.

4.4.11.1 Constant

If the constant pattern is selected, the intensity is configured using PGEN_LVL. The intensity is the same level for all pixels.

If PGEN_INV is set, the patch intensity is inverted.

4.4.11.2 Vertical Ramp

The vertical ramp pattern comprises a number of horizontal bands; by default, the intensity increases for each band, as illustrated in Fig. 4-19.

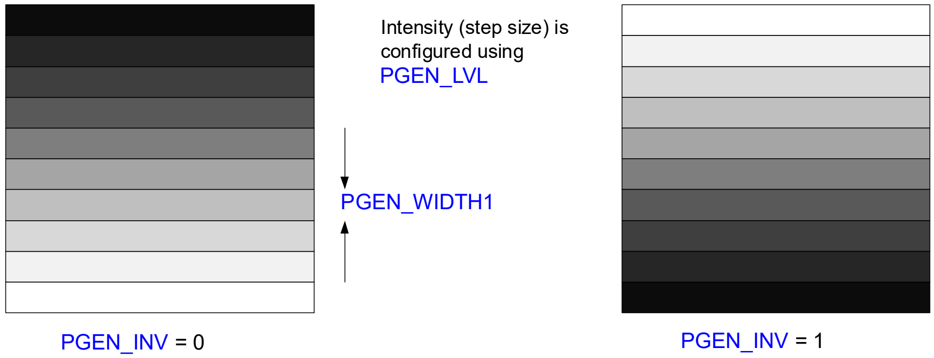


Figure 4-19. Vertical Ramp

The size of the horizontal bands is configured using PGEN_WIDTH1 to select the number of lines in each band (i.e., number of TG Sync pulses).

The intensity of the first band is 0x0000. For each subsequent band, the intensity increases by PGEN_LVL. If the intensity reaches the maximum value (0xFFFF), it returns to 0x0000 and continues to increase from there for each band.

If PGEN_INV is set, the intensity of the first band is 0xFFFF and decreases for each subsequent band, with the step size determined by PGEN_LVL.

4.4.11.3 Horizontal Ramp

The horizontal ramp pattern comprises a number of vertical bands; by default, the intensity increases for each band, as illustrated in Fig. 4-20.

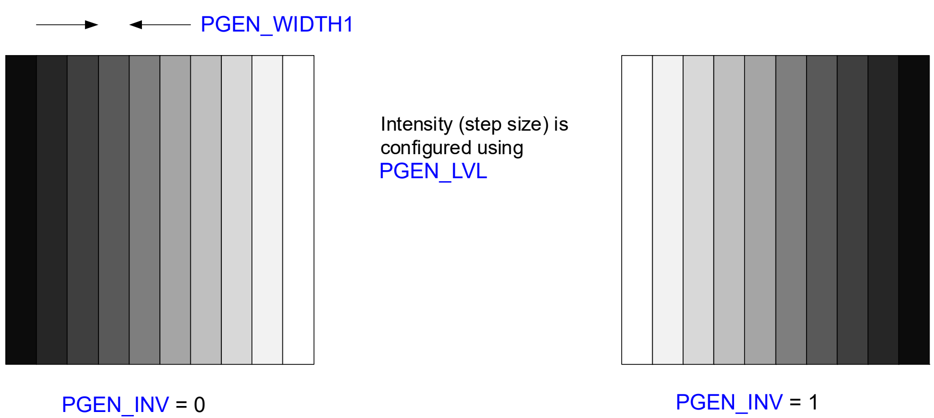


Figure 4-20. Horizontal Ramp

The size of the horizontal bands is configured using PGEN_WIDTH1 to select the number of pixels in each band.

The intensity of the first band is configured using PGEN_LVL. The intensity of each subsequent band increases by the same amount. If the intensity reaches the maximum value (0xFFFF), it returns to 0 and continues to increase from there for each band.

If PGEN_INV is set, the intensity of the first band is 65535 and decreases for each subsequent band, with the step size determined by PGEN_LVL.

4.4.11.4 Patch Pattern

The patch pattern comprises a number of rectangular patches; the intensity is fixed for each patch, as illustrated in Fig. 4-21.

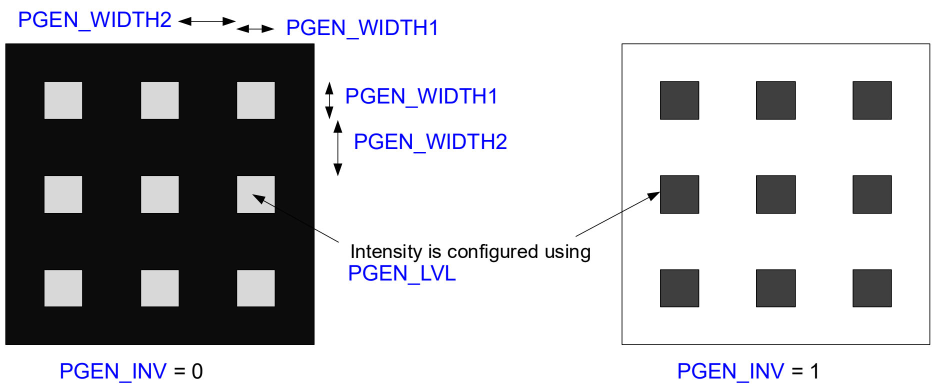


Figure 4-21. Patch Pattern

The size of each patch is configured using PGEN_WIDTH1 to set the width (number of pixels) and the height (number of lines) of the patch.

The spacing of the patches is configured using PGEN_WIDTH2 to set the horizontal separation (number of pixels) and the vertical separation (number of lines) between patches.

The intensity of each patch is configured using PGEN_LVL. The intensity is 0 for all other areas.

If PGEN_INV is set, the patch intensity is inverted; the intensity is 0xFFFF for all other areas.

4.4.11.5 Marching Pattern

The marching pattern comprises horizontal lines; the intensity changes for each line, as illustrated in Fig. 4-22.

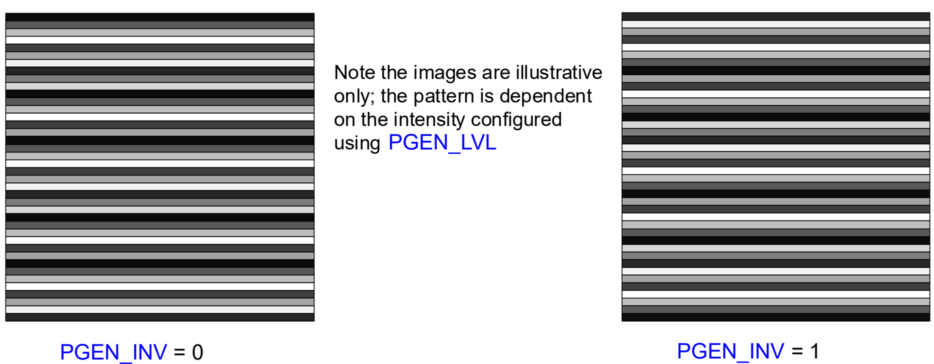


Figure 4-22. Marching Pattern

The intensity of the first line is configured using PGEN_LVL. For each subsequent line, the intensity is determined by a bitwise left rotation of the previous value. The pattern repeats every 16 lines.

4.5 Digital Output Format

The data output from the CS82L46 is supported in different formats to suit a range of applications. The available formats allow users to choose between different electrical standards, number of channels, sample resolution, number of data pins, and the ordering of the data bits.

Data output is supported in the following interface types:

- LVDS—Low-voltage Differential Signaling (LVDS) differential clock/data output (maximum 5 data pairs)
- CMOS (TG)—single ended clock/data output (maximum 10 data lines)
- CMOS (External)—data output synchronized to the MCLK input (maximum 10 data lines)

The valid output formats are dependent on sample-timing mode (see Section 4.6). In TG Mode, the LVDS and CMOS (TG) formats are supported. In External Mode, one of the CMOS (External) formats must be selected.

The output format is selected using FORMAT_SEL. The selected format is applied by setting FORMAT_LOAD.

Note: The FORMAT_LOAD bit is cleared automatically when the selected format is applied; this bit must be set each time a new output format is selected. The host should confirm the CS82L46 is in the Idle State (see Section 4.2) before changing the output format.

4.5.1 Status Flags

The LVDS and CMOS (TG) data formats incorporate configurable status flags, allowing additional information to be provided with the sample data. The status flags can be used to assist with decoding the output data.

LVDS formats support a maximum of five status flags, S0–S4. (Some LVDS formats support fewer than five flags.) CMOS (TG) formats support a single status flag, S0.

The function of each status flag is selected using FLAG_Sx_FN (where *x* is 0–4 for the respective flag). The status flags can be configured to provide the following indications:

- Logic 0, Logic 1—the flag is fixed at the respective logic level.
- Sequence state—two status flags can be used to indicate bits [1:0] of the SEQ_STATE_STS field. See Section 4.7 for further details of the sequence state.
- Flag Pixel 1—the status flag is set if the pixel counter matches one of four configured values. The associated pixel count values are configured using the respective FLAG_PIX1_PIXELx fields. The flag is referenced to the primary or secondary pixel counter using FLAG_PIX1_CNT_SEL. See Section 4.7 for further details of the pixel counters.

  If the flag is referenced to the secondary pixel counter, it can be selectively enabled for individual sequence states using FLAG_PIX1_SEQ_SEL. Each bit within this field enables the flag pixel in the corresponding state.

  The Flag Pixel 1 status is set if the data block contains a sample corresponding to one of the selected pixel-count values.

  In some LVDS output formats, a data block may contain data samples relating to two different pixel numbers. The flag-pixel indicator is set for all data blocks containing samples corresponding to one of the selected pixel-count values; this includes any blocks that also contain data samples for the previous/subsequent pixel.
- Flag Pixel 2—the status flag is set if the pixel counter coincides with a transition/edge of one of the pulse-output sources, PO0–PO10. The applicable pulse source is selected using FLAG_PIX2_PO_SEL. The status flag can be configured to indicate rising edges, falling edges, or all edges of the pulse-output source using FLAG_PIX2_PO_EDGE. See Section 4.8.2 for further details of the pulse-output sources.

  The Flag Pixel 2 status is set if the data block contains a sample corresponding to a toggle point for the selected pulse-output source, POx. Note there is latency associated with the pulse-output sources. If POx is configured to toggle at Pixel *n*, the toggle—and any associated Flag Pixel 2 indication—occurs at the Pixel *n*+1 sample.

  In some LVDS output formats, a data block may contain data samples relating to two different pixel numbers. The flag-pixel indicator is set for all data blocks containing samples corresponding to the applicable pixel-count values; this includes any blocks that also contain data samples for the previous/subsequent pixel.
- Flag DEN 1, Flag DEN 2—the status flag represents one of the pulse-output sources, PO0–PO10. The applicable pulse source is selected using the respective FLAG_DENx_PO_SEL field. See Section 4.8.2 for further details of the pulse-output sources.

- Channel ID—three status flags can be used to indicate bits [2:0] of the channel number (1–6) for the respective data block.

  In LVDS output formats, a data block may contain data samples relating to more than one channel. The first data block indicates Channel 1. The indicated channel for other data blocks is derived from the equivalent bit position in each block as Bit 0 of Channel 1 in the first data block.

4.5.2 LVDS Formats

In LVDS output format, the CS82L46 provides differential clock/data output. The clock is supported on the DCLKOUT_P and DCLKOUT_N pins. The data output is distributed over a maximum of five data pairs, DOUTn_P and DOUTn_N.

Note: If LVDS output format is selected, the pull resistors on DOUTn_P and DOUTn_N must be disabled using the respective x_PULL fields. See Section 4.11.3 for further details on configuring the digital I/O pins.

The LVDS output is defined in blocks, each containing seven data bits per output pair. The sample data for each channel is contained in the assigned bit positions. One or more data blocks are used to convey the data for each pixel. The required number of data blocks per pixel depends on the number of channels and the number of data bits per channel.

A single LVDS block (assuming three data pairs) is illustrated in Fig. 4-23. See Table 3-16 for timing specifications.

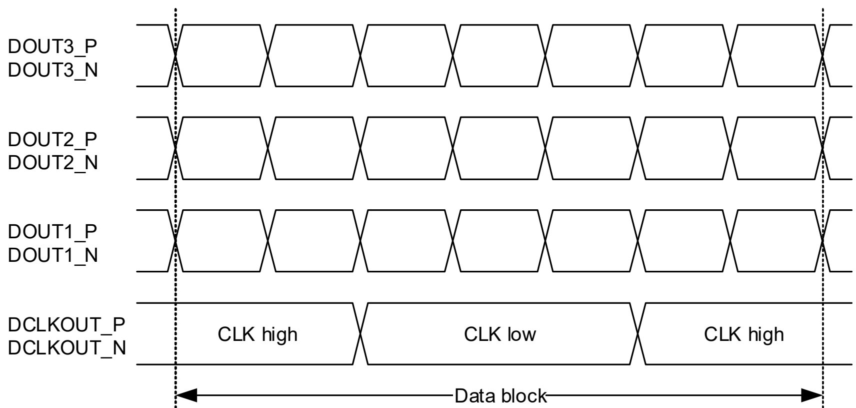


Figure 4-23. LVDS Output Format

The polarity of the differential LVDS output is configurable using LVDS_POL. Under normal conditions, a Logic 1 is represented by a high output on DOUTn_P and a low output on DOUTn_N. If the polarity is inverted (LVDS_POL = 1), a Logic 1 is represented by a low output on DOUTn_P and a high output on DOUTn_N.

The assigned bit positions for the sample data varies between different formats. The bit positions for each format can also be reordered or reversed as follows:

- The LVDS_REVERSE bit, if set, causes each data block to be reversed
- The LVDS_BIT_ORDER bit, if clear, causes the bit order of each sample, and any status flags, to be swapped

An example 16-bit data block is shown in Fig. 4-24. The corresponding reverse format is shown in Fig. 4-25. The swapped bit order is shown in Fig. 4-26. The combination of reverse + swapped bit order is shown in Fig. 4-27.

DOUT3	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DOUT2	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]
DOUT1	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Figure 4-24. LVDS Example

DOUT3	CH1[3]	CH1[2]	CH1[1]	CH1[0]	S2	S1	S0
DOUT2	CH1[10]	CH1[9]	CH1[8]	CH1[7]	CH1[6]	CH1[5]	CH1[4]
DOUT1	S4	S3	CH1[15]	CH1[14]	CH1[13]	CH1[12]	CH1[11]
DCLKOUT	H	H	L	L	L	H	H

Figure 4-25. LVDS Example—Reverse

DOUT3	S4	S3	S2	CH1[15]	CH1[14]	CH1[13]	CH1[12]
DOUT2	CH1[11]	CH1[10]	CH1[9]	CH1[8]	CH1[7]	CH1[6]	CH1[5]
DOUT1	CH1[4]	CH1[3]	CH1[2]	CH1[1]	CH1[0]	S1	S0
DCLKOUT	H	H	L	L	L	H	H

Figure 4-26. LVDS Example—Swapped Bit Order

DOUT3	CH1[12]	CH1[13]	CH1[14]	CH1[15]	S2	S3	S4
DOUT2	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]	CH1[11]
DOUT1	S0	S1	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]
DCLKOUT	H	H	L	L	L	H	H

Figure 4-27. LVDS Example—Reverse + Swapped Bit Order

An example 10-bit data block is shown in Fig. 4-28. The corresponding reverse format is shown in Fig. 4-29. The swapped bit order is shown in Fig. 4-30. The combination of reverse + swapped bit order is shown in Fig. 4-31.

DOUT2	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]
DOUT1	S0	S1	S2	S3	CH2[0]	CH2[1]	CH2[2]
DCLKOUT	H	H	L	L	L	H	H

Figure 4-28. LVDS Example

DOUT2	CH2[9]	CH2[8]	CH2[7]	CH2[6]	CH2[5]	CH2[4]	CH2[3]
DOUT1	CH2[2]	CH2[1]	CH2[0]	S3	S2	S1	S0
DCLKOUT	H	H	L	L	L	H	H

Figure 4-29. LVDS Example—Reverse

DOUT2	CH2[6]	CH2[5]	CH2[4]	CH2[3]	CH2[2]	CH2[1]	CH2[0]
DOUT1	S3	S2	S1	S0	CH2[9]	CH2[8]	CH2[7]
DCLKOUT	H	H	L	L	L	H	H

Figure 4-30. LVDS Example—Swapped Bit Order

DOUT2	CH2[0]	CH2[1]	CH2[2]	CH2[3]	CH2[4]	CH2[5]	CH2[6]
DOUT1	CH2[7]	CH2[8]	CH2[9]	S0	S1	S2	S3
DCLKOUT	H	H	L	L	L	H	H

Figure 4-31. LVDS Example—Reverse + Swapped Bit Order

The CS82L46 supports LVDS output formats as summarized in Table 4-3. Detailed descriptions of each format are provided in Section 5.1.1, and are referenced in the table. Each format is selected by setting the FORMAT_SEL field to the applicable ID value.

The number of clock cycles per pixel indicates the number of DCLKOUT cycles required to transmit one data sample for the applicable number of channels; in some cases, a fractional ratio is specified, indicating the output format spans more than one pixel before repeating (e.g., 1.5 = 3 clock cycles per 2 pixels).

The LVDS output formats are summarized in Table 4-3.

Table 4-3. LVDS Output Formats

Number of Channels	Bits per Channel	Number of Data Pairs	Clock Cycles per Pixel	Number of Status Flags	Format ID	Reference
6	16	5	3	3	79	Fig. 5-1
					83	Fig. 5-27
	12	4	3	4	92	Fig. 5-11
	10	3	3	1	32	Fig. 5-17
		5	2	5	86	Fig. 5-5
					89	Fig. 5-8

Table 4-3. LVDS Output Formats *(Cont.)*

Number of Channels	Bits per Channel	Number of Data Pairs	Clock Cycles per Pixel	Number of Status Flags	Format ID	Reference
4	16	3	4	5	27	Fig. 5-14
					35	Fig. 5-21
					43	Fig. 5-31
		5	2	3	78	Fig. 5-2
					82	Fig. 5-28
	12	4	2	4	91	Fig. 5-12
	10	2	4	4	39	Fig. 5-24
		3	2	1	31	Fig. 5-18
		5	1.33 (4/3)	5	85	Fig. 5-6
					88	Fig. 5-9
3	16	3	3	5	26	Fig. 5-15
					34	Fig. 5-22
					42	Fig. 5-32
		5	1.5 (3/2)	3	77	Fig. 5-3
					81	Fig. 5-29
	12	4	1.5 (3/2)	4	90	Fig. 5-13
	10	2	3	4	38	Fig. 5-25
		3	1.5 (3/2)	1	30	Fig. 5-19
		5	1	5	84	Fig. 5-7
					87	Fig. 5-10
2	16	3	2	5	25	Fig. 5-16
					33	Fig. 5-23
					41	Fig. 5-33
		5	1	3	76	Fig. 5-4
					80	Fig. 5-30
	10	2	2	4	37	Fig. 5-26
		3	1	1	29	Fig. 5-20

4.5.3 CMOS (TG) Formats

In CMOS (TG) output format, the CS82L46 provides single-ended clock/data output. The clock is supported on the DCLKOUT1 pin. A configurable status flag, S0, is supported on the DCLKOUT2 pin. The data output is distributed over a maximum of ten data lines, DOUTn.

The status flag, S0, can be used to indicate the start of the scan image. In typical applications, this is achieved by configuring the status flag as a flag-pixel indication. See Section 4.5.1 to configure the S0 status flag.

The CMOS (TG) format is illustrated in Fig. 4-32. See Table 3-16 for timing specifications.

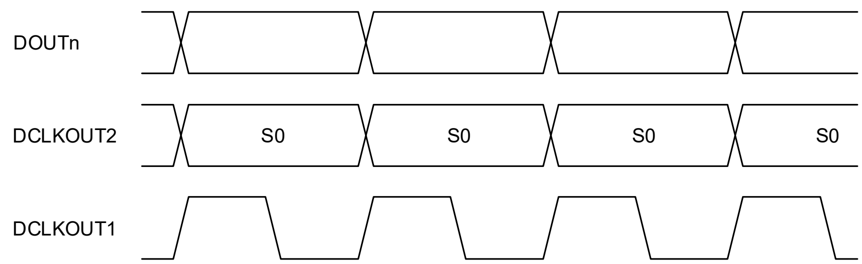


Figure 4-32. CMOS (TG) Output Format

The CS82L46 supports CMOS (TG) output formats as summarized in Table 4-4. Detailed descriptions of each format are provided in Section 5.1.2, and are referenced in the table. Each format is selected by setting the FORMAT_SEL field to the applicable ID value.

The number of clock cycles per pixel indicates the number of DCLKOUT1 cycles required to transmit one data sample for the applicable number of channels. Note that, if this number is greater than six, the CS82L46 must be configured in Clocking Mode 1 or Clocking Mode 2 (see Section 4.3).

The CMOS (TG) output formats are summarized in Table 4-4.

Table 4-4. CMOS (TG) Output Formats

Number of Channels	Bits per Channel	Number of Data Lines	Clock Cycles per Pixel	Format ID	Reference
6	12	6	12 [1]	24	Fig. 5-38
	10	10	6	75	Fig. 5-34
4	12	6	8 [1]	23	Fig. 5-39
	10	10	4	74	Fig. 5-35
3	12	6	6	22	Fig. 5-40
	10	10	3	73	Fig. 5-36
2	12	6	4	21	Fig. 5-41
	10	10	2	72	Fig. 5-37

1.Only supported in Clocking Mode 1 or Clocking Mode 2 (see Section 4.3).

4.5.4 CMOS (External) Formats

In CMOS (External) output format, the CS82L46 provides single-ended data output, distributed over a maximum of ten data lines, DOUTn. Signal timing is referenced to the external clock input (on the MCLK_EXT pin). The data output is supported in single- or double-rate formats:

- In single-data-rate (SDR) formats, the data bit rate is equal to the MCLK rate
- In double-data-rate (DDR) formats, the data bit rate is 2 × MCLK rate

Note that the CMOS (External) output format is supported in External Mode only (see Section 4.6). The MCLK frequency is a multiple of the pixel-sample rate, where the applicable frequency ratio is dependent on the selected output data format.

The latency of the output data from the VSMP_EXT trigger signal is described in Section 4.6.2 and Section 4.6.3.

The CMOS (External) format is illustrated in Fig. 4-33. See Table 3-16 for timing specifications.

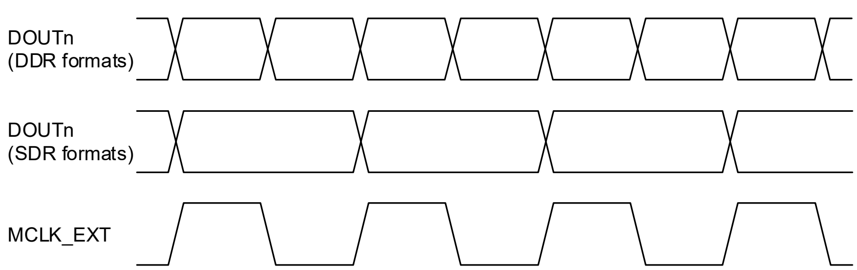


Figure 4-33. CMOS (External) Output Format

The format is configurable using CMOS_EXT_POL, allowing the data output to be referenced to either the rising or falling edge of the MCLK input.

The CS82L46 supports CMOS (External) output formats as summarized in Table 4-5. Detailed descriptions of each format are provided in Section 5.1.3, and are referenced in the table. Each format is selected by setting the FORMAT_SEL field to the applicable ID value.

The number of MCLK cycles per pixel indicates the number of MCLK cycles required to transmit one data sample for the applicable number of channels. The MCLK frequency must be provided at the applicable rate:

$$\text{MCLK frequency} = \text{Pixel rate} \times \text{MCLK cycles per pixel}$$

The CMOS (External) output formats are summarized in Table 4-5.

Table 4-5. CMOS (External) Output Formats

Number of Channels	Bits per Channel	Number of Data Lines	Data Rate	MCLK Cycles per Pixel	Format ID	Reference
6	16	8	DDR	6	4	Fig. 5-42
					20	Fig. 5-49
			SDR	12	12	Fig. 5-58
	10	10	DDR	3	65	Fig. 5-52
			SDR	6	67	Fig. 5-62
					71	Fig. 5-64
	8	8	SDR	6	8	Fig. 5-54
4	16	4	DDR	8	15	Fig. 5-46
		8	DDR	4	3	Fig. 5-43
					19	Fig. 5-50
			SDR	8	11	Fig. 5-59
	10	10	DDR	2	64	Fig. 5-53
			SDR	4	66	Fig. 5-63
					70	Fig. 5-65
	8	8	SDR	4	7	Fig. 5-55
3	16	4	DDR	6	14	Fig. 5-47
		8	DDR	3	2	Fig. 5-44
			SDR	6	10	Fig. 5-60
	10	10	SDR	3	69	Fig. 5-66
	8	8	SDR	3	6	Fig. 5-56
2	16	4	DDR	4	13	Fig. 5-48
		8	DDR	2	1	Fig. 5-45
					17	Fig. 5-51
			SDR	4	9	Fig. 5-61
	10	10	SDR	2	68	Fig. 5-67
	8	8	SDR	2	5	Fig. 5-57

4.5.4.1 TDM Mode

The CS82L46 can be configured in TDM Mode, where the outputs from two devices are multiplexed on a single data bus. This can be used to increase the effective number of channels in the system. Note that TDM is supported in External Mode only (see Section 4.6).

In TDM Mode, the two devices use the same VSMP_EXT and MCLK_EXT timing signals. Both devices must be configured for the same output format. Note that the MCLK frequency must be increased to take account of the data output for both devices.

Typical connections for TDM Mode are shown in Fig. 4-34.

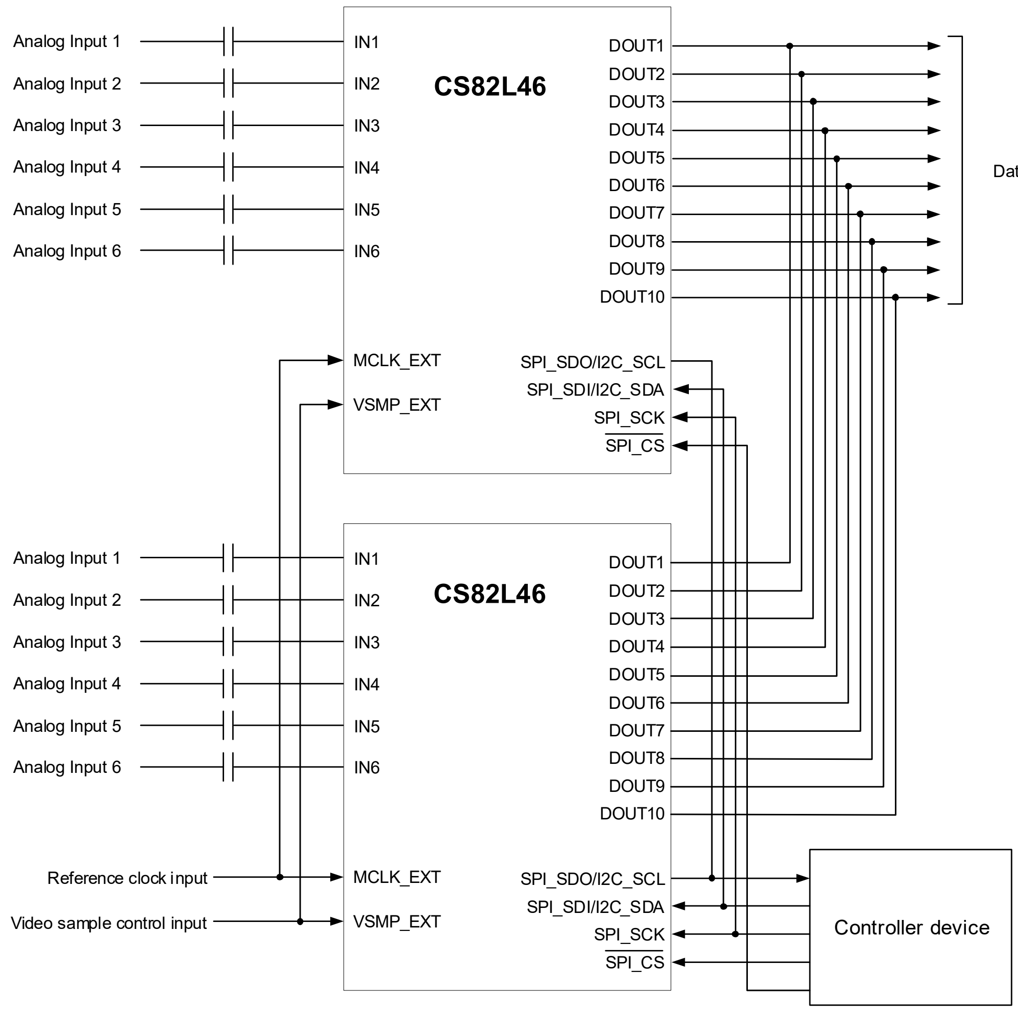


Figure 4-34. TDM Mode

TDM Mode is enabled using TDM_EN. If this bit is set, the output format is configured to allow two devices to transmit data in turn. The DOUTn pins are Hi-Z when not transmitting data, allowing another device to drive the shared output interface.

The timing of the data output is configured using TDM_OFFSET. This field is used to offset the data output of the two devices, ensuring only one device transmits at any time. In typical use cases, the offset between the two devices is set equal to the number of MCLK cycles per pixel in the selected output format (see Table 4-5). For example, one device is configured for the minimum delay (0 MCLK cycles); the other device is configured for the number of MCLK cycles per pixel.

A delay can be configured between one device transmitting and the other; this allows additional time for each device to cease driving the output before the other device starts. There are two options for configuring the delay.

- If TDM_DOUT_DLY_EN is set, a delay is applied each time the output drivers are enabled. The delay is configured using TDM_DOUT_DLY_SEL. This provides fine control of the output timing.
- If TDM_GAP is set, a gap of one MCLK cycle is inserted after each data-output cycle. This bit must be set to the same value on each device. This provides a coarse control of the output timing.

Note: If TDM_GAP is set, the additional latency must also be added to the TDM_OFFSET value (i.e., incremented by 1).

In TDM Mode, the MCLK frequency must be increased to take account of the data output for both devices and the TDM gap, if enabled. The required MCLK frequency can be calculated using the following equation, where *MCLK cycles per pixel* is noted in Table 4-5 for the applicable output format, and *TDM_GAP* is 0 or 1 according to the TDM_GAP bit:

$$\text{MCLK frequency} = 2 \times \text{Pixel rate} \times (\text{MCLK cycles per pixel} + \text{TDM\_GAP})$$

The timing of the output data in TDM Mode is illustrated in Fig. 4-35 and Fig. 4-36. In the examples shown, the data-output format comprises four MCLK cycles for each device.

TDM Mode with TDM_GAP = 0 is shown in Fig. 4-35. The MCLK frequency is 8 × pixel rate.

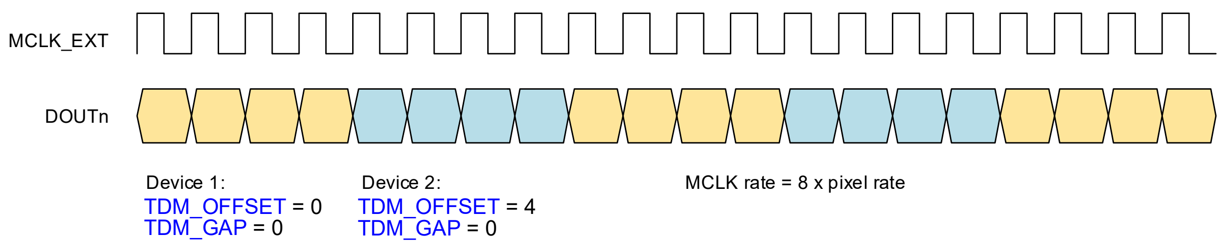


Figure 4-35. TDM Data Timing—Gap Disabled

TDM Mode with TDM_GAP = 1 is shown in Fig. 4-36. The MCLK frequency is 10 × pixel rate.

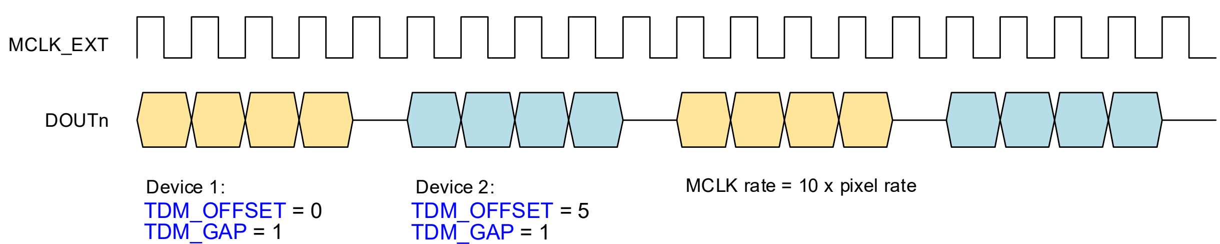


Figure 4-36. TDM Data Timing—Gap Enabled

4.6 Sample Timing Control

The CS82L46 supports CDS and non-CDS sampling modes. CDS refers to correlated double-sampling—in CDS mode, the reset level and the video level are sampled for each pixel; in non-CDS mode, a single video-level sample is used for each pixel. The sampling mode is configured using CDS_EN.

The sample timing is controlled by the internal VSMP and RSMP signals—the video level is sampled on the falling edge of VSMP; the reset level is sampled on the falling edge of RSMP.

Note: The RSMP signal is used in CDS sampling mode only. RSMP is not used in non-CDS sampling mode.

The ADC sample/conversion timing is controlled by the AFECK signal. The rising edge of AFECK occurs after the falling edge of VSMP. The AFECK signal must be optimized according to the application requirements, to ensure correct sequencing of the associated functions.

In typical applications, the VSMP, RSMP, and AFECK timing is generated internally using the DLL. The external MCLK provides the timing reference for the DLL (see Section 4.3 for clocking modes). The 60-tap DLL subdivides the sample period, and is used to define the phase offsets for VSMP, RSMP, and AFECK.

Alternatively, the sample timing can be controlled using external hardware inputs. The external signals can be configured to trigger the internal VSMP and RSMP signals directly, or can be retimed to align with the MCLK reference input. The AFECK timing is configured with reference to the MCLK input.

To assist in debug and timing set-up, the VSMP, RSMP, and AFECK signals can be monitored externally as described in Section 4.12.

The CDS timing for a typical CCD-sensor video signal is shown in Fig. 4-37.

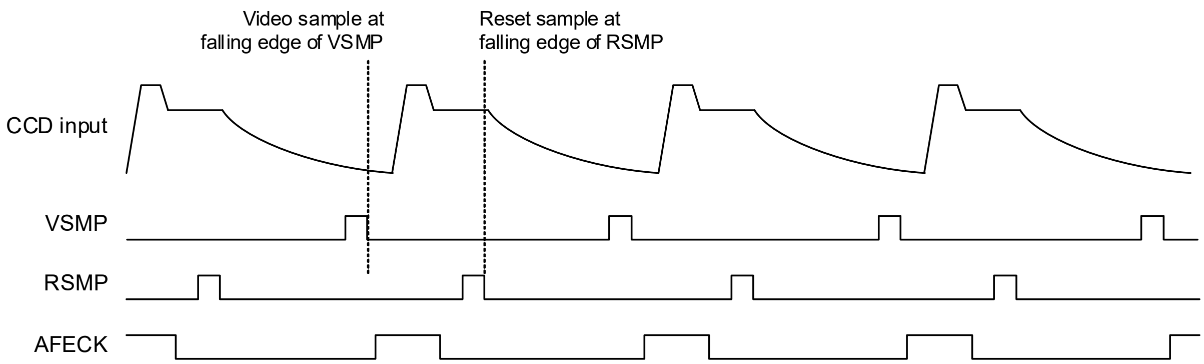


Figure 4-37. Sample Timing Control (CDS Mode)

The non-CDS timing for a typical CIS-sensor video signal is shown in Fig. 4-38.

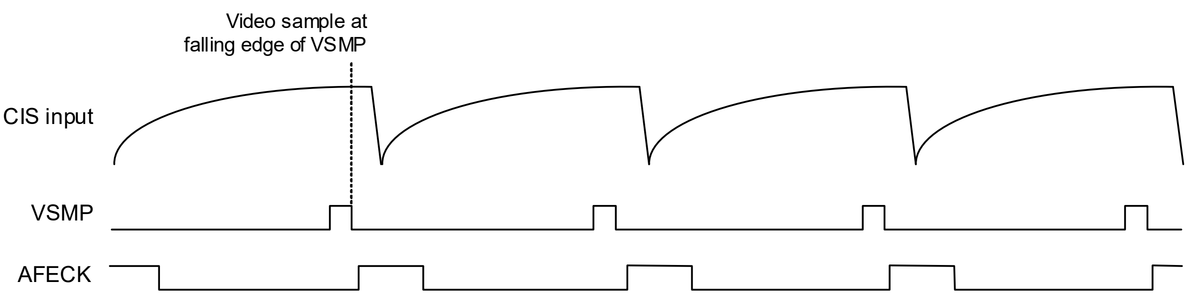


Figure 4-38. Sample Timing Control (non-CDS Mode)

4.6.1 DLL-Controlled Trigger (TG Mode)

In TG Mode, the VSMP, RSMP, and AFECK signals are generated internally using the DLL. The DLL reference (DLL_REF) is derived from the external clock signal (MCLK_EXT)—either directly, or else using PLL1 to synthesize a different sample frequency. TG Mode is selected if EXTERNAL_MODE_EN = 0.

The DLL divides the sample period into 60 stages, enabling the VSMP, RSMP, and AFECK signals to be configured at the required duty cycle and phase offset, referenced to the 1/60 steps of the DLL output.

- The rising and falling edges of VSMP are configured using DLL_VSMP_RISE and DLL_VSMP_FALL to align the respective edge with the applicable DLL Tap (0–59).
- The rising and falling edges of RSMP are configured using DLL_RSMP_RISE and DLL_RSMP_FALL to align the respective edge with the applicable DLL Tap (0–59).
- The rising edge of AFECK occurs 1 Tap after the VSMP falling edge. The falling edge of AFECK is configured using DLL_AFECK_DUR to define the duration of the AFECK pulse.

The timing constraints in Table 3-10 must be observed when configuring the duty cycle and phase offset of VSMP, RSMP, and AFECK. A minimum pulse duration is specified for each signal; it is recommended to configure the shortest possible duration within the defined limits. The VSMP, RSMP, and AFECK pulses must not overlap.

Notes: The VSMP, RSMP, and AFECK pulses can be asserted across the Tap 0 boundary if desired.

The RSMP signal is used in CDS sampling mode only. If CDS_EN = 0, there is no requirement to configure RSMP, and the associated timing constraints do not apply.

The DLL-controlled VSMP, RSMP, and AFECK timing is illustrated in Fig. 4-39.

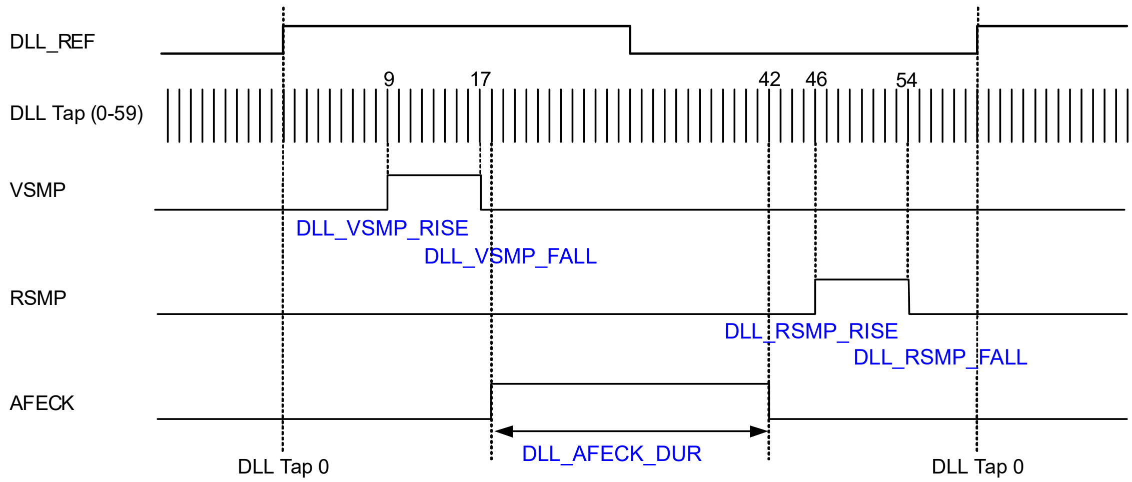


Figure 4-39. DLL Timing Control (TG Mode)

In TG Mode, the data output is supported in LVDS and CMOS (TG) data formats, described in Section 4.5.2 and Section 4.5.3 respectively. The latency of the output is dependent on the selected data format. The latency is defined from the rising edge of AFECK (i.e., the first MCLK rising edge after the VSMP falling edge), as shown in Fig. 4-40.

Note: Latency is defined for Clocking Mode 0 only (see Section 4.3). In this mode, the pixel sample rate is equal to the MCLK frequency. The specified latency has a tolerance of ±1 MCLK cycle.

For LVDS data formats, the latency (measured in MCLK cycles) is defined as follows:

- Output latency = (8 / *Clock cycles per pixel*) + 8
  where *Clock cycles per pixel* is noted in Table 4-3 for the applicable output format
- If using the pattern generator (see Section 4.4.11), the output latency is (8 / *Clock cycles per pixel*) + 4
- The data output latency is illustrated in Fig. 4-40.

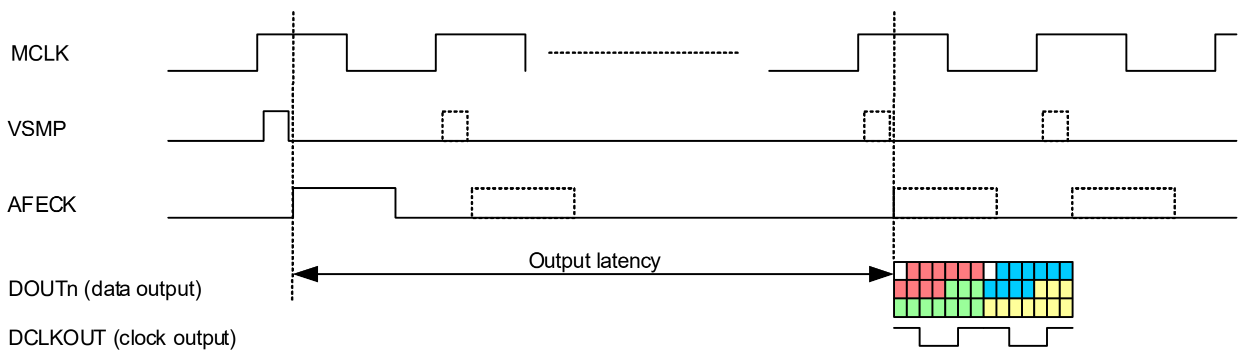


Figure 4-40. Data Output Timing (TG Mode, LVDS Output)

For CMOS (TG) data formats, the latency (measured in MCLK cycles) is defined as follows:

- Output latency = (15 / *Clock cycles per pixel*) + 8
  where *Clock cycles per pixel* is noted in Table 4-4 for the applicable output format
- If using the pattern generator (see Section 4.4.11), the output latency is (15 / *Clock cycles per pixel*) + 4
- The data output latency is illustrated in Fig. 4-41.

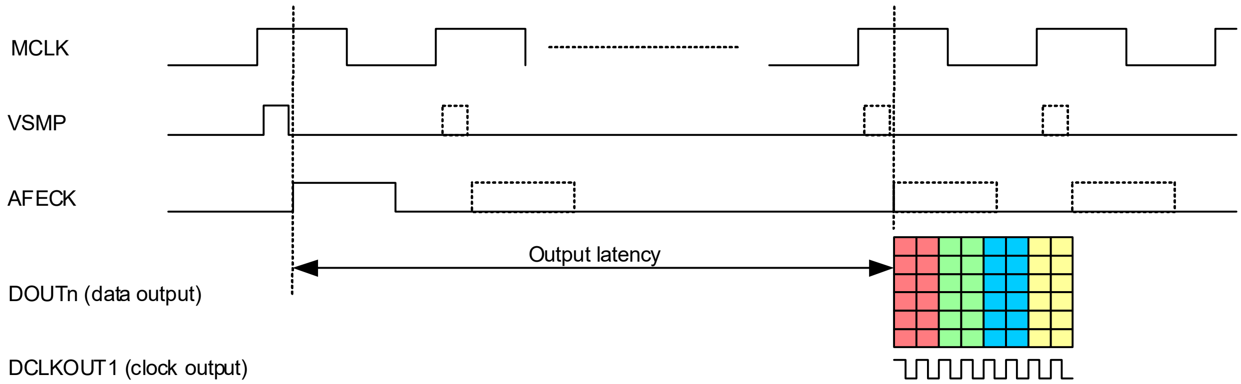


Figure 4-41. Data Output Timing (TG Mode, CMOS Output)

4.6.2 Direct Pin Trigger (External Mode 1)

In External Mode 1, the VSMP and RSMP signals are controlled directly using external hardware inputs. The video sample is triggered on the falling edge of VSMP_EXT; the reset-level sample is triggered on the falling edge of RSMP_EXT.

External Mode 1 is selected if EXTERNAL_MODE_EN = 1 and EXTERNAL_MODE_SEL = 0.

This mode requires that the external MCLK frequency is a multiple of the pixel-sample rate; the applicable frequency ratio is dependent on the selected output data format (see Section 4.5.4).

The rising edge of AFECK occurs on the first MCLK rising edge after the VSMP falling edge. The falling edge of AFECK is configured using EXT_AFECK_DUR to define the duration of the AFECK pulse.

The timing constraints in Table 3-12 must be observed when controlling VSMP and RSMP directly from the external pins. A minimum pulse duration is specified for each signal; it is recommended to configure the shortest possible AFECK pulse within the defined limits. The VSMP, RSMP, and AFECK pulses must not overlap.

Note: Note the RSMP signal is used in CDS sampling mode only. If CDS_EN = 0, the RSMP timing constraints do not apply.

The VSMP_EXT and RSMP_EXT functions are supported on multifunction pins, which must be configured for the required functions as described in Section 4.11.

The direct-pin trigger is illustrated in Fig. 4-42.

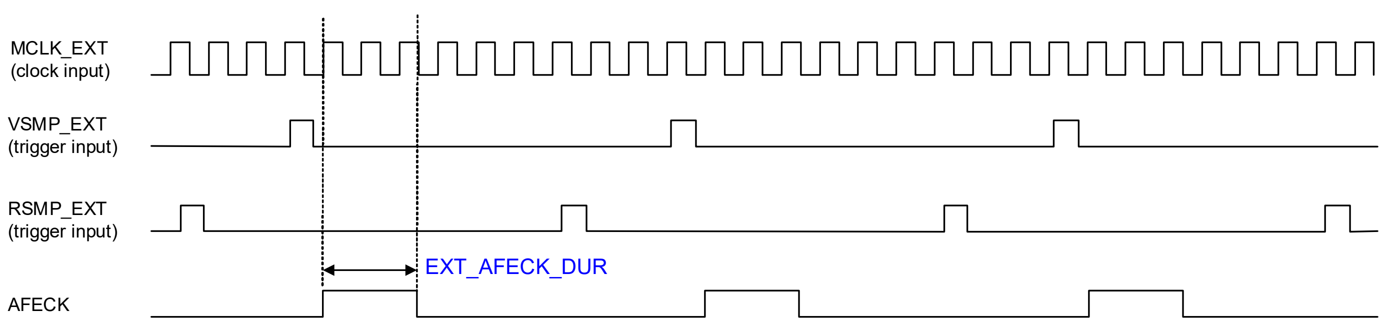


Figure 4-42. Direct-Pin Timing (External Mode 1)

In External Mode 1, the data output is formatted as described in Section 4.5.4. The latency of the output is dependent on the selected data format and the TDM configuration (if applicable). The latency is defined from the rising edge of AFECK (i.e., the first MCLK rising edge after the VSMP falling edge), as shown in Fig. 4-43.

The latency (measured in MCLK cycles) is defined as follows, where *MCLK cycles per pixel* is noted in Table 4-5 for the applicable output format.

- If TDM_EN = 0, output latency = (7 x *MCLK cycles per pixel*) + 15
- If TDM_EN = 1 and TDM_GAP = 0, output latency = (14 x *MCLK cycles per pixel*) + 30
- If TDM_EN = 1 and TDM_GAP = 1, output latency = (14 x (*MCLK cycles per pixel* + 0.5)) + 30
- If CMOS_EXT_POL = 1, the latency is increased by 0.5 MCLK cycle; data output starts on the falling MCLK edge

The data output latency is illustrated in Fig. 4-43.

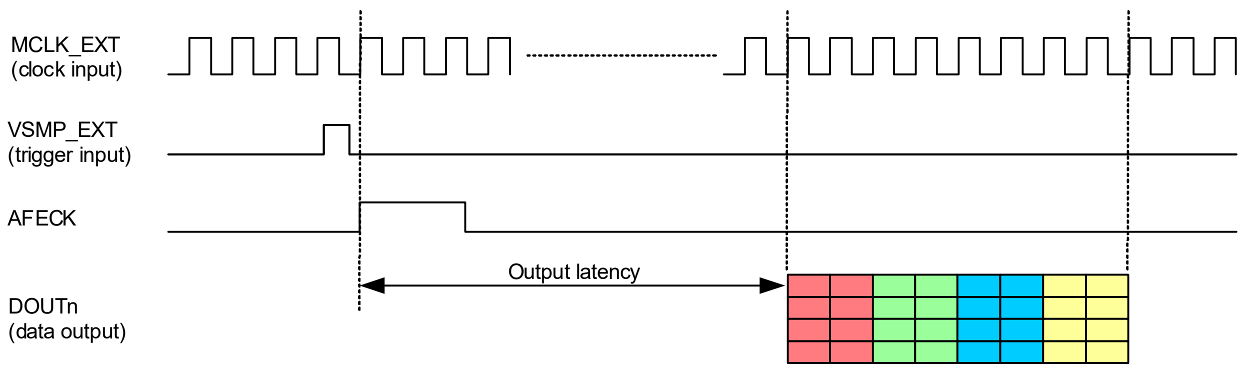


Figure 4-43. Data Output Timing (External Mode 1)

4.6.3 MCLK-Aligned Trigger (External Mode 2)

In External Mode 2, the VSMP, RSMP, and AFECK signals are controlled using the VSMP_EXT pin as the trigger. The active edge of the trigger (rising or falling) is selectable. The internal signals are retimed to align with the MCLK input; this can be used to ensure the internal pulses do not exceed a minimum duration, regardless of the external trigger.

External Mode 2 is selected if EXTERNAL_MODE_EN = 1 and EXTERNAL_MODE_SEL = 1.

This mode requires that the external MCLK frequency is a multiple of the pixel-sample rate; the applicable frequency ratio is dependent on the selected output data format (see Section 4.5.4).

The MCLK-aligned signals are configured as follows:

- The VSMP timing is controlled using VSMP_EXT_DLY to select the number of MCLK cycles between the active VSMP_EXT edge and the rising edge of VSMP. The falling edge of VSMP is one MCLK cycle after the rising edge.
- The RSMP timing is controlled using RSMP_EXT_DLY to select the number of MCLK cycles between rising edge of VSMP and the rising edge of RSMP. The falling edge of RSMP is one MCLK cycle after the rising edge.
- The rising edge of AFECK occurs at the same time as the VSMP falling edge. The falling edge of AFECK is configured using EXT_AFECK_DUR to define the duration of the AFECK pulse.

The rising edge of VSMP is configured as described above. The rising edge is delayed by a number of MCLK cycles—if a delay of n cycles is selected, the rising edge of VSMP occurs on the n-th rising edge of MCLK after the rising edge of the VSMP_EXT signal.

The timing constraints in Table 3-13 must be observed when configuring the phase offset of VSMP, RSMP, and AFECK. It is recommended to configure the shortest possible AFECK pulse within the defined limits. The VSMP, RSMP, and AFECK pulses must not overlap.

Note: The RSMP signal is used in CDS sampling mode only. If CDS_EN = 0, there is no requirement to configure RSMP, and the associated timing constraints do not apply.

The VSMP_EXT function is supported on the TGSYNC1/VSMP_EXT pin, which must be configured for VSMP input as described in Section 4.11. The active trigger edge is selectable using VSMP_EXT_POL.

The MCLK-aligned trigger is illustrated in Fig. 4-44.

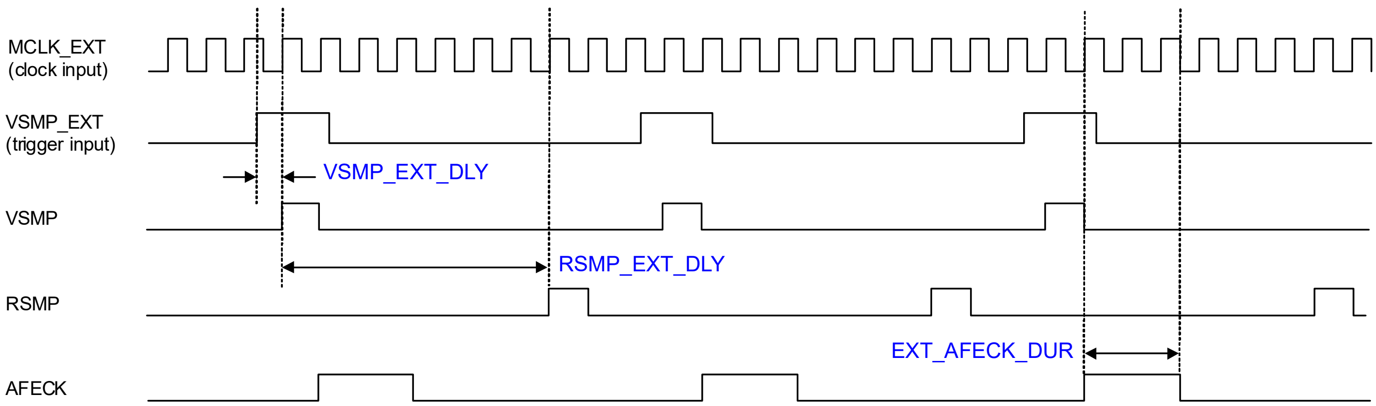


Figure 4-44. MCLK-Aligned Timing Control (External Mode 2)

In External Mode 2, the data output is formatted as described in Section 4.5.4. The latency of the output is dependent on the selected data format and the TDM configuration (if applicable). The latency is defined from the rising edge of AFECK (i.e., the internal VSMP falling edge), as shown in Fig. 4-45.

The latency (measured in MCLK cycles) is defined as follows, where *MCLK cycles per pixel* is noted in Table 4-5 for the applicable output format.

- If TDM_EN = 0, output latency = (7 x *MCLK cycles per pixel*) + 15
- If TDM_EN = 1 and TDM_GAP = 0, output latency = (14 x *MCLK cycles per pixel*) + 30
- If TDM_EN = 1 and TDM_GAP = 1, output latency = (14 x (*MCLK cycles per pixel* + 0.5)) + 30
- If CMOS_EXT_POL = 1, the latency is increased by 0.5 MCLK cycle; data output starts on the falling MCLK edge

Note the latency is defined from the internal VSMP/AFECK signals. The additional latency from the active VSMP_EXT edge to the internal VSMP pulse is configurable using VSMP_EXT_DLY.

The data output latency is illustrated in Fig. 4-45.

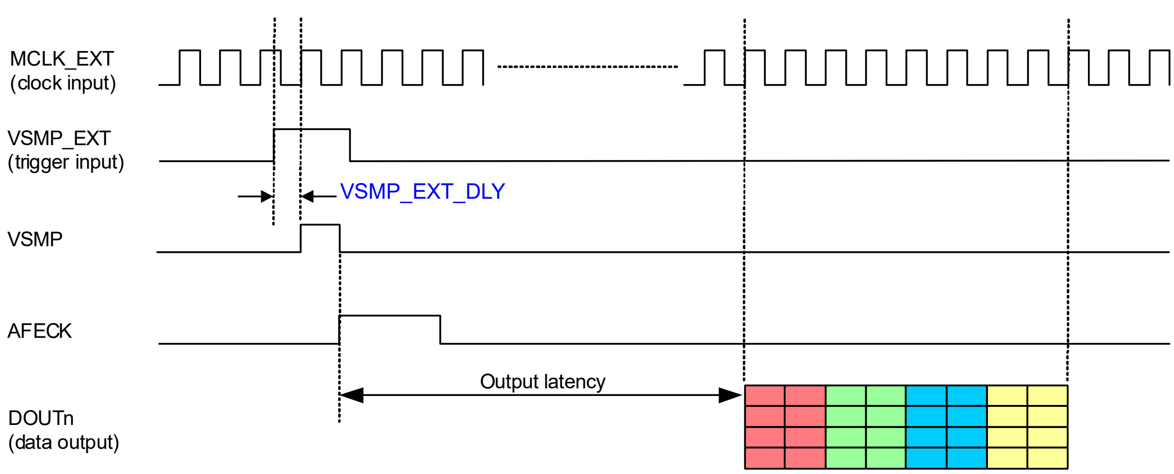


Figure 4-45. Data Output Timing (External Mode 2)

4.7 TG Sync and Pixel Counter Control

The video input signal is sampled on the falling edge of VSMP, as described in Section 4.6. In typical applications, the samples represent pixels within a scan pattern; blocks of samples represent successive lines, or different scan colors, within the scan pattern.

Pixel counters (primary and secondary) are used to monitor the number of samples. The initial sample within the scan pattern is indicated using the TG Sync signal; this can be generated as an output from the CS82L46, or else can be provided as an external input. The sync signal may indicate the start of each scan line, or may signal intermediate stages within a scan line.

The scan pattern can be referenced to a sequence-state parameter, supporting a maximum of four sequential states. Each state represents a different portion of the scan pattern; this can be used to reconfigure the input path for different scan colors, or other functions, for the respective portions of the scan.

In External Mode (see Section 4.6), the pixel counter and related functions are disabled by default. The pixel counter sequence-state configuration can be enabled and used to control the LED output drivers by setting EXTERNAL_MODE_TG_EN. In this configuration, the TG Sync must be an input to the CS82L46 (i.e., TG Slave Mode).

4.7.1 TG Sync Mode and Sequence State

The TG Sync is configured in Master Mode or Slave Mode using TGSYNC_MODE. In Master Mode, TG Sync is an output from the CS82L46. In Slave Mode, TG Sync is an input.

The number of sequence states is configured using NUM_SEQ_STATES. The number of pixels in each state is configured using SEQ_STATEx_LEN (where *x* is 0, 1, 2, or 3 for the respective sequence state).

A maximum of four states is supported. The current sequence state is indicated in SEQ_STATE_STS.

The initial state is State 0 by default; this is configurable using INIT_SEQ_STATEThe sequence state is incremented as described in the following sections; under the applicable conditions, the sequence returns to the initial state.

For example, if the number of sequence states is four, and the initial state is State 1, the resulting sequence is State 1, State 2, State 3, State 0. Under the applicable conditions, the sequence restarts in State 1. Note that the initial state must be configured within the scope of the selected number of states (i.e., INIT_SEQ_STATE ≤ NUM_SEQ_STATES).

4.7.2 TG Master Mode

In Master Mode, TG Sync is an output from the CS82L46. The TG Sync pulse indicates the first pixel in the initial state (typically State 0).

The pixel counters start from zero and increment on each sample, for the configured length of the current sequence state. The sequence state then advances to the next state. The secondary pixel counter is reset on each state transition. At the end of the configured number of sequence states, the sequence state is reset to the initial state, and the TG Sync pulse indicates the start of the next cycle. The primary and secondary pixel counters are reset at the start of the cycle.

The TG Sync signal is supported on the TGSYNC1/VSMP_EXT pin, which must be configured for TGSYNC output as described in Section 4.11. The duration of the TG Sync pulse can be configured using TGSYNC_OUT_DUR.

Master Mode operation with a single sequence state is illustrated in Fig. 4-46. In this configuration, the primary and secondary pixel counters provide the same function. The maximum pixel-counter value is determined by the duration of State 0. The TG Sync pulse is generated each time the pixel counters are reset.

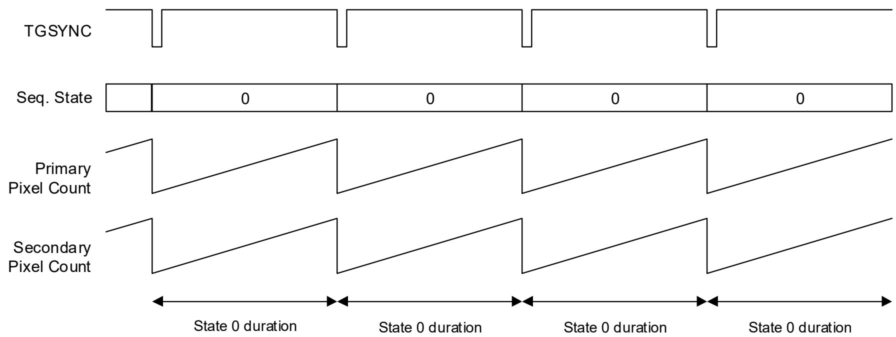


Figure 4-46. TG Master Mode—Single State

Master Mode operation with four sequence states is illustrated in Fig. 4-47. The number of pixels is configured independently for each state. The secondary pixel counter is reset on each state transition. The TG Sync pulse is generated when the primary pixel counter is reset to the initial state.

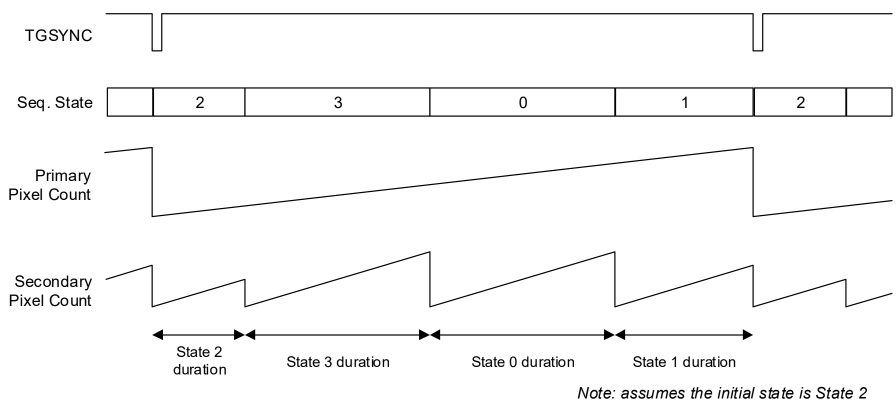


Figure 4-47. TG Master Mode—Multiple States

4.7.3 TG Slave Mode

In Slave Mode, TG Sync is an input to the CS82L46. The TG Sync signal is used to trigger the sequence-state transitions. Optionally, this can be used in conjunction with the LEDSTART signal to provide additional control of the sequence states.

The TGSYNC_SINGLE_SEQ bit selects whether the TG Sync triggers a cycle of multiple state transitions (Multiple Mode) or triggers a single state transition only (Single Mode).

- In Multiple Mode (TGSYNC_SINGLE_SEQ = 0), the TG Sync indicates the first pixel in the initial state. The pixel counters start from zero and increment on each sample, for the configured length of the current sequence state. The sequence state then advances to the next state. The secondary pixel counter is reset on each state transition. At the end of the configured number of sequence states, the pixel counters are frozen until the TG Sync signal indicates the start of the next cycle (typically State 0). The primary and secondary pixel counters are reset at the start of the cycle.
- In Single Mode (TGSYNC_SINGLE_SEQ = 1), the TG Sync indicates the first pixel in each sequence state. The pixel counters start from zero and increment on each sample, for the configured length of the current sequence state. The pixel counters are frozen at the end of each state, until TG Sync triggers the state transition. At the end of the configured number of sequence states, the TG Sync indicates the start of the next cycle (typically State 0). The primary and secondary pixel counters are reset at the start of the cycle.

The LEDSTART_SEQ_INIT bit selects whether the LEDSTART signal is used (in conjunction with TG Sync) to indicate the first pixel in the initial state. If this bit is clear, the sequence-state transitions are controlled using only the TG Sync input. If this bit is set, the LEDSTART and TG Sync signals must both be asserted to restart the sequence.

The TG Sync input is supported on three different pins—TGSYNC1, TGSYNC2, or LEDSTART. The applicable input is selected using TGSYNC_IN_SRC. The polarity of the selected input is configured using TGSYNC_IN_POL.

A filter can be applied to the selected TG Sync input, to avoid erroneous triggers. The filter is enabled using TGSYNC_FILT_EN. The external signal is sampled at the pixel rate, and decimated at a rate selected by TGSYNC_FILT_DECM. The decimated input is tested for a valid transition using the TGSYNC_FILT_STAGE field; for example, if a 6-stage filter is selected, a valid rising edge is detected if a 0–0–0–1–1–1 sequence is detected in the decimated input signal.

If LEDSTART_SEQ_INIT is set, LEDSTART indicates the first pixel in the initial state. In this configuration, the polarity of the LEDSTART input is selected using LEDSTART_POL.

A timing offset can be configured on the TG Sync input using TGSYNC_IN_OFFSET. The offset can be used to compensate for a delayed TG Sync input, enabling the pixel counters on two devices to be synchronized in a Master/Slave configuration. The offset is implemented by adjusting the initial pixel-counter value in each sequence state.

The TG Sync function must be set according to the applicable sample-timing configuration (see Section 4.6). If EXTERNAL_MODE_EN = 0, TGSYNC_ASYNC bit must be set. If EXTERNAL_MODE_EN = 1, TGSYNC_ASYNC bit must be clear.

The TG Sync and LEDSTART functions are supported on multifunction pins, which must be configured for the required functions as described in Section 4.11. See Section 4.7.3.1 for timing information.

Slave Mode operation with a single sequence state is illustrated in Fig. 4-48. In this configuration, the primary and secondary pixel counters provide the same function. The pixel counters are reset on each TG Sync pulse. The maximum pixel-counter value is determined by the duration of State 0; both counters are frozen, if this limit is reached.

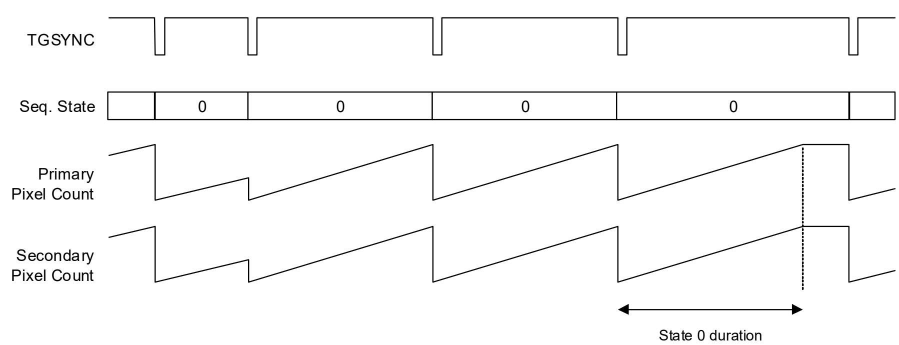


Figure 4-48. TG Slave Mode—Single State

Slave Mode (multiple cycle) operation with four sequence states is illustrated in Fig. 4-49. The maximum number of pixels is configured independently for each state (both counters are frozen, if this limit is reached). The secondary pixel counter is reset on each state transition. The primary pixel counter is reset, and the sequence state is re-initialized, on each TG Sync pulse.

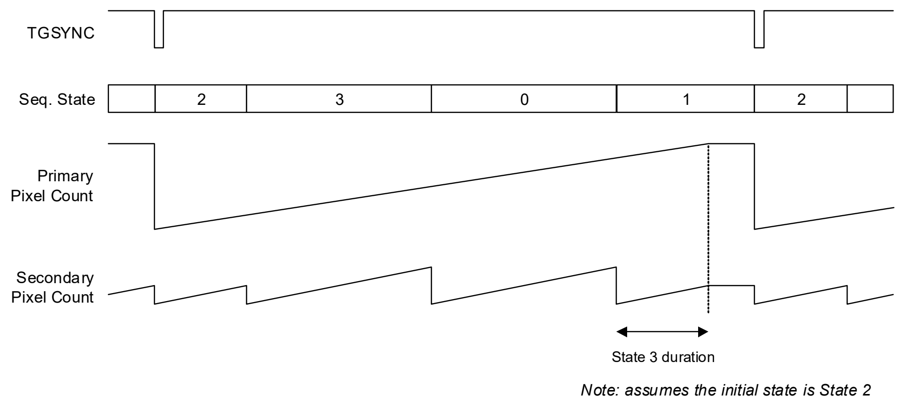


Figure 4-49. TG Slave Mode—Multiple Cycle, TGSYNC Trigger

Slave Mode (single cycle) operation with four sequence states is illustrated in Fig. 4-50. The maximum number of pixels is configured independently for each state (both counters are frozen, if this limit is reached). The secondary pixel counter is reset, and the sequence-state transition is triggered, on each TG Sync pulse. The primary pixel counter is reset when the sequence state returns to the initial state.

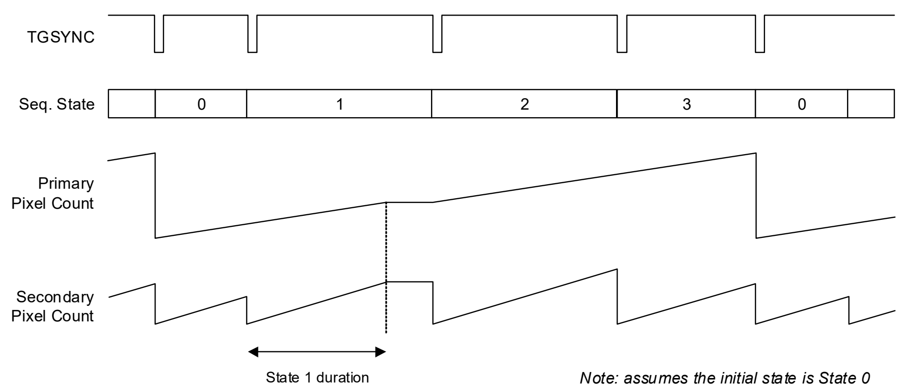


Figure 4-50. TG Slave Mode—Single Cycle, TGSYNC Trigger

Slave Mode (single cycle) operation with four sequence states is illustrated in Fig. 4-51. The maximum number of pixels is configured independently for each state (both counters are frozen, if this limit is reached). The secondary pixel counter is reset, and the sequence-state transition is triggered, on each TG Sync pulse. The primary pixel counter is reset when the sequence state is re-initialized using LEDSTART.

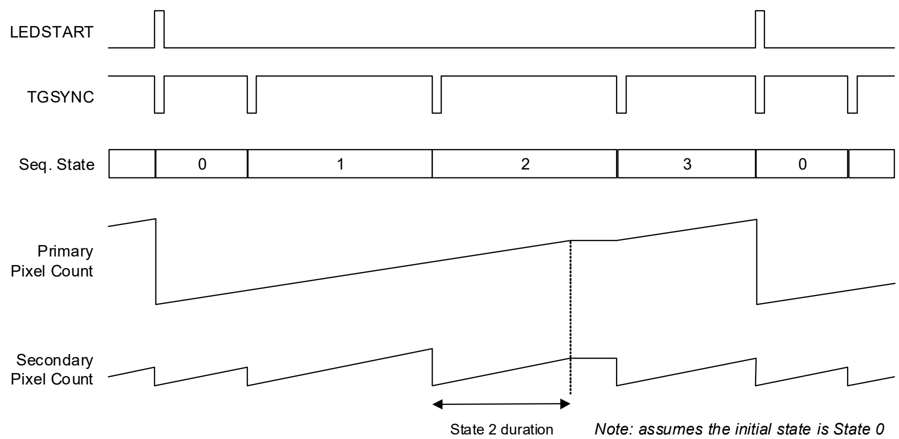


Figure 4-51. TG Slave Mode—Single Cycle, LEDSTART + TGSYNC Trigger

4.7.3.1 TGSYNC and LEDSTART Signal Timing

In TG Slave Mode, the TGSYNC signal is used to trigger the sequence-state transitions. Optionally, LEDSTART can be used to control the transition that re-initializes the sequence. The signals must conform to the applicable timing requirements.

In TG Mode—

- The TGSYNC and LEDSTART timing requirements are defined in Table 3-11, assuming Clocking Mode 0.
- If Clocking Mode 0 is selected and the TGSYNC filter is enabled (TGSYNC_FILT_EN = 1), the minimum TGSYNC pulse width is as follows.

  $$((\textit{Filter Stages} \times \textit{Decimation Ratio} / 2) + 2) \qquad \text{AFECK cycles}$$

  where *Filter Stages* is the number of filter stages selected by TGSYNC_FILT_STAGE and *Decimation Ratio* is the ratio selected by TGSYNC_FILT_DECM. See Section 4.6.1 for details of AFECK.
- If Clocking Mode 1 or 2 is selected and the TGSYNC filter is disabled, the TGSYNC pulse width must be a minimum of 2 AFECK cycles.
- If Clocking Mode 1 or 2 is selected and the TGSYNC filter is enabled, the minimum TGSYNC pulse width is as follows.

  $$((\textit{Filter Stages} \times \textit{Decimation Ratio} / 2) + 2) \qquad \text{AFECK cycles}$$
- If Clocking Mode 1 or 2 is selected, the LEDSTART active edge must occur at least 1 ns before the TGSYNC active edge. The LEDSTART inactive edge must occur at or after the TGSYNC inactive edge.
- The TGSYNC timing applies to whichever pin is selected for TG Sync input (i.e., TGSYNC1, TGSYNC2, or LEDSTART. The LEDSTART timing applies to the LEDSTART function only (LEDSTART_SEQ_INIT = 1).

- If Clocking Mode 1 or 2 is selected, the timing requirements are as illustrated in Fig. 4-52.

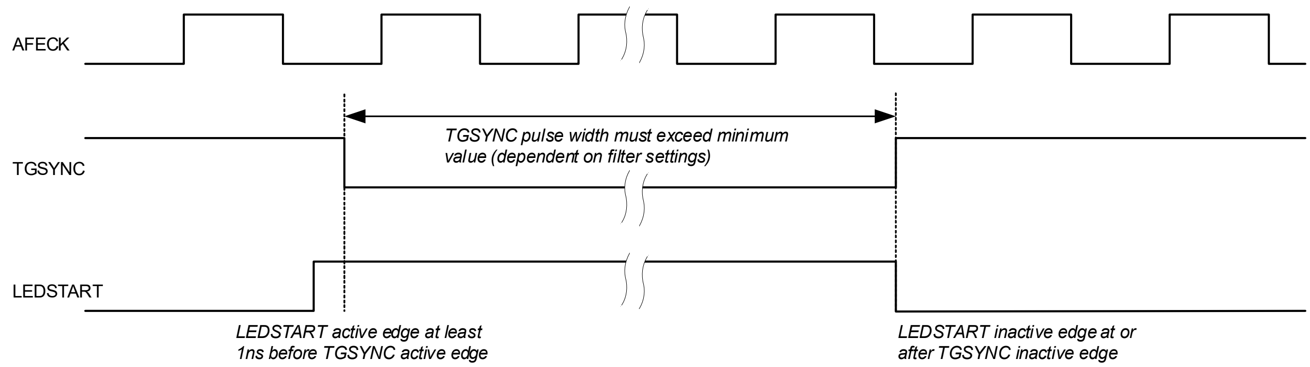


Figure 4-52. TGSYNC/LEDSTART Timing—TG Mode

In External Mode—

- The TGSYNC and LEDSTART timing requirements are defined in Table 3-15, assuming the TGSYNC filter is disabled.
- If the TGSYNC filter is enabled (TGSYNC_FILT_EN = 1), the TGSYNC minimum pulse width is defined by the following equation:

  $$(\textit{Filter Stages} \times \textit{Decimation Ratio} / 2) \quad \text{MCLK cycles}$$

  where *Filter Stages* is the number of filter stages selected by TGSYNC_FILT_STAGE and *Decimation Ratio* is the ratio selected by TGSYNC_FILT_DECM.
- The LEDSTART active edge must occur at least 1 ns before the TGSYNC active edge. The LEDSTART inactive edge must occur at or after the TGSYNC inactive edge.
- The TGSYNC timing applies to whichever pin is selected for TG Sync input (i.e., TGSYNC1, TGSYNC2, or LEDSTART. The LEDSTART timing applies to the LEDSTART function only (LEDSTART_SEQ_INIT = 1).
- If the TGSYNC filter is enabled, the timing requirements are as illustrated in Fig. 4-53.

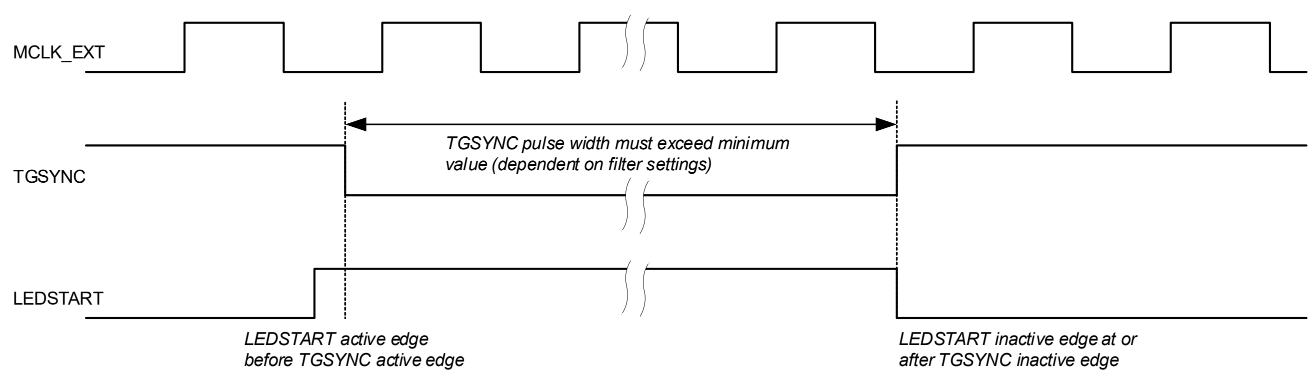


Figure 4-53. TGSYNC/LEDSTART Timing—External Mode

4.8 Clock Timing Generation

The CS82L46 incorporates highly configurable clock-timing functions. The clock signals are used to control various internal functions; they can also be used to provide timing control for external circuits.

The clock signals can be configured with reference to the pixel counters, where the behavior changes at specified pixel-counter values. *Toggle points* can be used to define the respective pixel-counter values. The clocks can also be configured with reference to the sequence state, allowing waveforms to be selectively enabled according to the current state.

The clock-timing signals fall into two types; both types can be provided as external outputs via the CLKOUTn pins.

- High-speed pixel-rate clocks, with configurable phase/duty cycle relative to the DLL reference
- Pulse waveforms that toggle at defined pixel-count boundaries within specified sequence states

The pulse waveforms can be used to control internal functions such as the input-path clamp or the LED output drivers. The same waveform can be selected as the control source to more than one function.

In External Mode (see Section 4.6), the clock-timing functions are disabled by default. The toggle points and pulse-output sources (POn) can be enabled and used to control the LED output drivers by setting EXTERNAL_MODE_TG_EN.

4.8.1 Toggle Points

Toggle points are used to define instants in the scanning sequence where the device behavior should change. A maximum of 32 toggle points can be defined; each toggle point is defined by a pixel-counter value. The output of the clocks or pulse waveforms can be configured to change at specified toggle points.

The toggle points are defined using TP0_PIXEL through TP31_PIXEL. Each toggle point is defined by a pixel-counter value.

The toggle points are referenced to the primary or secondary pixel counter using TP_SEC_OFFSET. Toggle points (TPn) with an index less than the offset value are associated with the primary counter; toggle points with an index greater than or equal to the offset value are associated with the secondary counter.

For example, if TP_SEC_OFFSET = 10, toggle points TP0–TP9 are associated with the primary counter, and TP10–TP31 are associated with the secondary counter.

Note that the toggle points associated with each counter must be configured with incrementing values (TP0_PIXEL < TP1_PIXEL < TP2_PIXEL, etc.). If the pixel counter is reset before it reaches the value configured for a toggle point, that toggle point is ignored.

4.8.2 Pulse Output Sources (POn)

The CS82L46 supports 11 pulse-output sources, PO0–PO10. The pulse-output sources can be configured to rise or fall at specified instants, referenced to the pixel-counter value. The resulting waveforms are used to control various internal functions and can also be used to provide timing control for external circuits.

The POn signals are configured using one of two methods.

- By default, the timing of the POn signals is defined with reference to the 32 toggle points; the toggle points allow efficient device configuration when switching multiple signals at the same pixel-counter values.
- If required, one or more POn signals can be configured using direct control; a limited pulse-output function is supported on the respective POn signals, with dedicated control fields used to define the switching points for each. The direct control allows the POn signals to be configured independently, without reference to the toggle points.

4.8.2.1 Toggle-Point Control

The pulse-output sources (POn) are configured using POx_TP_POL. Each bit within these fields defines whether the pulse source is Logic 0 or Logic 1 at the respective toggle point. See Section 4.8.1 for details of toggle points TP0–TP31.

The POn sources are referenced to the primary or secondary pixel counter using POx_CNT_SEL. The toggle points associated with each counter are configured independently as described in Section 4.8.1.

Note: If the primary pixel counter is selected, the POx_TP_POL bits 0–31 define the logic level at toggle points TO0–TP31 respectively. If the secondary pixel counter is selected, the mapping of the POx_TP_POL bits to the toggle points is offset by a number of bits equal to the TP_SEC_OFFSET value.

For example, if TP_SEC_OFFSET = 10, toggle points TP10–TP31 are associated with the secondary counter. In this case, if the secondary counter is selected, Bit 0 of POx_TP_POL defines the logic level at TP10, Bit 1 of POx_TP_POL defines the logic level at TP11, etc.

The initial logic level (when the selected counter is reset) is configured using POx_INIT_LVL for each pulse-output source. The level can be unchanged from the previous counter cycle, or can be set equal to the logic level of the first toggle point.

If a pulse-output source is referenced to the secondary pixel counter, it can be selectively enabled for individual sequence states using the respective POx_SEQ_SEL field. Each bit within these fields enables the waveform in the corresponding state.

The POn timing is aligned to the rising edge of the AFECK signal. See Section 4.6 to configure the AFECK timing.

Note: There is a latency between the pixel count of the toggle point (TP) and the pixel count of the AFECK pulse at the switching point of the POn signal. If POn is configured to toggle at Pixel *n*, the toggle occurs at the Pixel *n+1* AFECK rising edge.

The POn configuration is illustrated in Fig. 4-54.

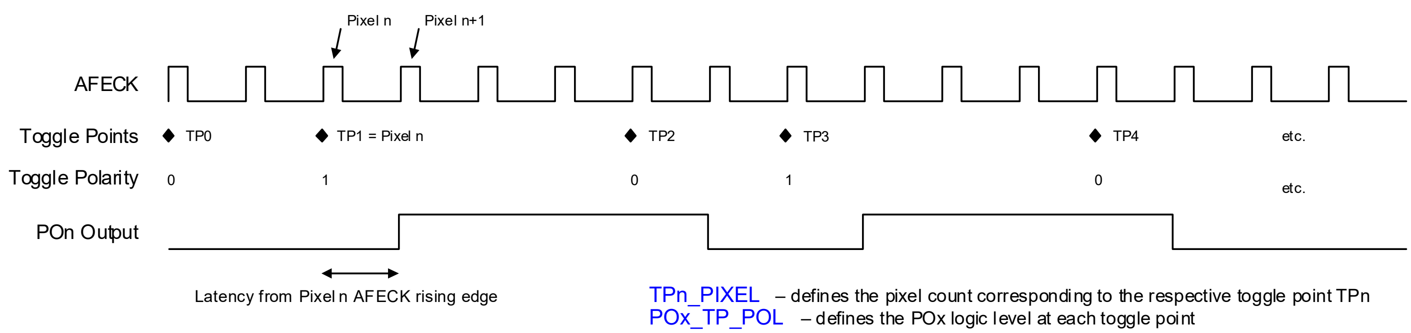


Figure 4-54. Pulse-Output (POn) Configuration—Toggle Point Control

4.8.2.2 Direct Control

One or more of the POn signals can be selected for direct control using NUM_DC_PO. Direct control is supported on pulse outputs PO5–PO10.

If a PO signal is selected for direct control, a single pulse can be configured using the respective POx_TP_POL field to define the pixel-counter value for the rising and falling edges—bits [15:0] configure the rising edge, and bits [31:16] configure the falling edge.

If more than one pulse is required, the DC_PO_2ND_PULSE bit can be used to enable a second pulse. The rising and falling edges of the second pulse are configured using the TPn_PIXEL fields. Depending on the number of POn signals selected for direct control, two or more of the TPn_PIXEL fields are assigned to this purpose, as indicated in Table 4-6.

Notes: The DC_PO_2ND_PULSE bit enables the second pulse for all POn signals selected for direct control. If the second pulse is not required on specific POn signals, it can be disabled by setting the associated TPn_PIXEL fields to the same value, or to a value beyond the active range of the pixel counter (e.g., 0xFFFF).

The available number of toggle points is reduced if the second pulse is enabled for direct-control POn signals.

The control fields used to configure the direct-control POn signals are summarized in Table 4-6.

Table 4-6. Pulse Output (POn) Direct Control

NUM_DC_PO	Direct Control POn Signals	Single Pulse Control [1]	Second Pulse Control (DC_PO_2ND_PULSE = 1) [2]					
			PO5	PO6	PO7	PO8	PO9	PO10
0x0	None	—	—	—	—	—	—	—
0x1	PO10	PO10_TP_POL	—	—	—	—	—	TP30_PIXEL TP31_PIXEL
0x2	PO9–PO10	POx_TP_POL	—	—	—	—	TP28_PIXEL TP29_PIXEL	
0x3	PO8–PO10	POx_TP_POL	—	—	—	TP26_PIXEL TP27_PIXEL		
0x4	PO7–PO10	POx_TP_POL	—	—	TP24_PIXEL TP25_PIXEL			
0x5	PO6–PO10	POx_TP_POL	—	TP22_PIXEL TP23_PIXEL				
0x6	PO5–PO10	POx_TP_POL	TP20_PIXEL TP21_PIXEL					

1. The POx_TP_POL fields define the rise/fall edges for the respective POn signal.
2. If the second pulse is enabled, the TPn_PIXEL fields define the rise/fall edges for the additional pulse.

If the POx_TP_POL or TPn_PIXEL fields associated with a direct-control POn signal are updated, the new values are buffered and do not become effective until the sequence state is re-initialized on the applicable TG Sync pulse.

The POn sources are referenced to the primary or secondary pixel counter using POx_CNT_SEL.

The initial logic level (when the selected counter is reset) is configured using POx_DC_INIT_LVL for each pulse-output source; the level can be either Logic 0 or Logic 1.

Note: If the initial level is Logic 1, it may be desired for the POn falling edge to occur before the rising edge. The CS82L46 allows the rising and falling edges to be configured in any order.

The pulse-output sources can be selectively enabled for individual sequence states using POx_SEQ_SEL. Each bit within these fields enables the waveform in the corresponding state.

The POn timing is aligned to the rising edge of the AFECK signal. See Section 4.6 to configure the AFECK timing.

Note: There is a latency between the pixel count of the POx pulse edges and the pixel count of the AFECK pulse at the switching point of the POx signal. If POx is configured to toggle at Pixel *n*, the toggle occurs at the Pixel *n+1* AFECK rising edge.

The POn configuration is illustrated in Fig. 4-55, using the PO10 signal as an example.

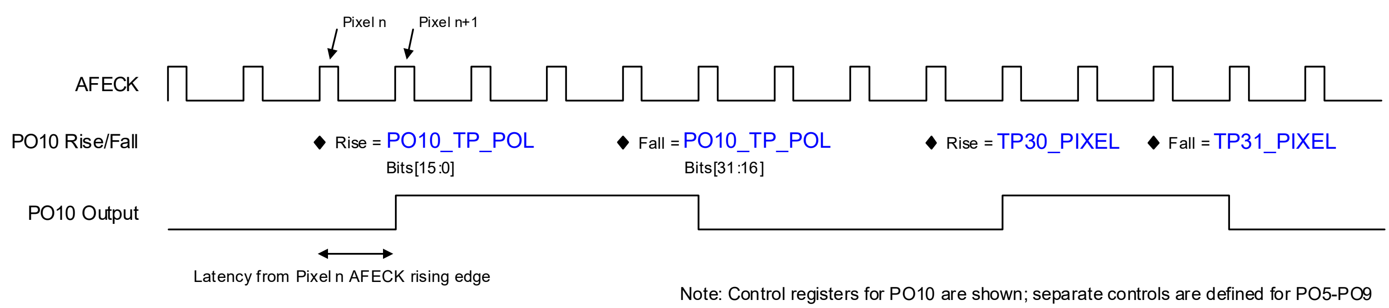


Figure 4-55. Pulse-Output (POn) Configuration—Direct Control

4.8.3 Pulse Waveform Clocks (P_CKn)

The CS82L46 supports ten pulse-waveform clocks, P_CK1–P_CK10. The pulse-waveform clocks can be used to provide timing control signals for external circuits via the respective CLKOUTn pins (see Section 4.8.5).

Each clock (P_CKn) is derived from one of the pulse-output sources, PO0–PO10. The source for each clock is configured using PCKx_PO_SEL. See Section 4.8.2 for details of the pulse-output sources.

The P_CKn timing is aligned to the rising edge of TGCKO. The TGCKO signal is configured using DLL_TGCKO_RISE to align the rising edge with the applicable DLL tap. The timing constraints defined in Section 4.8.6 must be observed when configuring TGCKO.

Note: There is a latency between the switching point of the POn source and the corresponding P_CK output. The P_CK output toggles at the second TGCKO rising edge following a toggle of the source POn signal.

The P_CK timing is illustrated in Fig. 4-56.

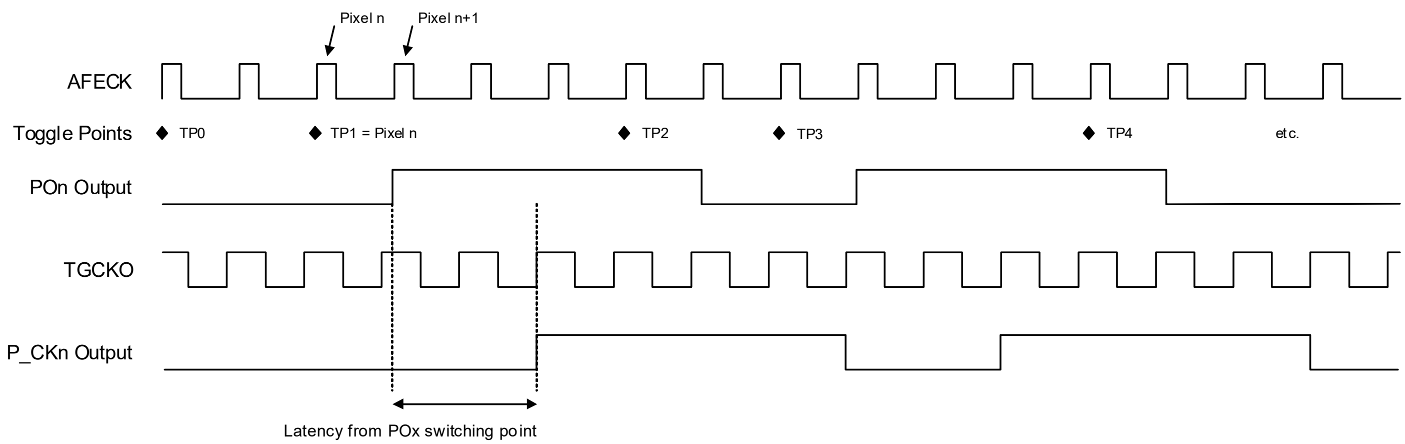


Figure 4-56. Pulse Clock (P_CK) Configuration

The timing of the P_CKn signals is configured with reference to the TGCKO clock. An additional switching delay can be configured for individual clock outputs using PCKx_DLY as shown in Fig. 4-57.

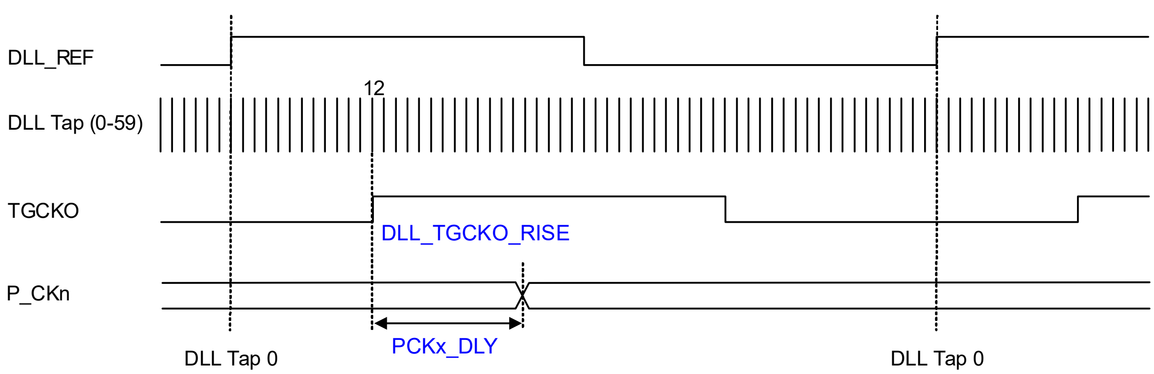


Figure 4-57. Pulse-Clock Switch Timing

4.8.4 High-Speed Clocks (C_CKn)

The CS82L46 supports six high-speed clocks, C_CK1–C_CK6. The high-speed clocks can be used to provide timing control signals for external circuits via the respective CLKOUTn pins (see Section 4.8.5).

The high-speed pixel-rate clocks are derived from the DLL. The rising and falling edges of each clock are configured using DLL_CKx_RISE and DLL_CKx_FALL to align the respective clock edge with the applicable DLL tap.

The high-speed clock configuration is illustrated in Fig. 4-58. Note that the C_CK pulse can be asserted across the Tap 0 boundary if desired.

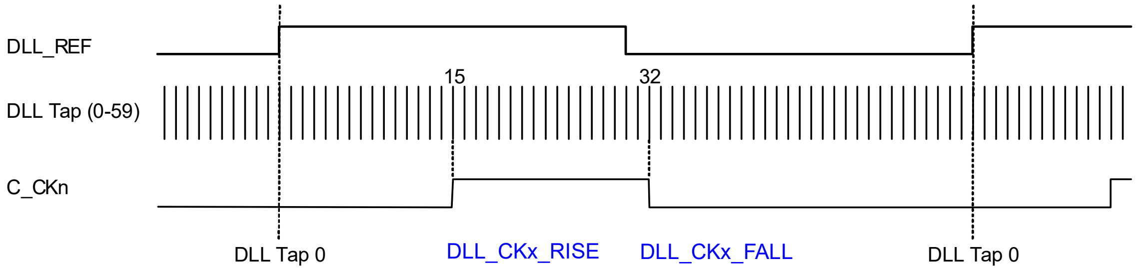


Figure 4-58. High-Speed Clocks (C_CKn)

Configurable masking can be applied to the high-speed clocks—the pixel-rate clock switching is masked through the applicable range of pixel-count values. During the masked periods, the clock signal can be switched to 0 or 1 at any of the defined toggle points TP0–TP31.

- Masking for C_CK1 and C_CK2 is configured using CK_MASK1_START and CK_MASK1_END. Toggle is configured using CK_TOG1_TP_POL.
- Masking for C_CK3 and C_CK4 is configured using CK_MASK2_START and CK_MASK2_END. Toggle is configured using CK_TOG2_TP_POL.
- Masking for C_CK5 and C_CK6 is configured using CK_MASK3_START and CK_MASK3_END. Toggle is configured using CK_TOG3_TP_POL.

The C_CK mask and toggle logic is shown in Fig. 4-59. If the mask is Logic 0, the clock output switches high/low while the toggle control is high; the output is held low while toggle control is low. If the mask is Logic 1, the clock output switches high/low according to the toggle status.

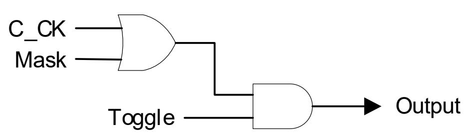


Figure 4-59. C_CK Mask/Toggle Logic

The mask is referenced to the primary or secondary pixel counter using CK_MASKx_CNT_SEL. The toggle is referenced to the primary or secondary pixel counter using CK_TOGx_CNT_SEL. The toggle points (TPn) associated with each counter are configured independently as described in Section 4.8.1.

Note: If the toggle is referenced to the primary pixel counter, the CK_TOGx_TP_POL bits 0–31 define the logic level at toggle points TO0–TP31 respectively. If the toggle is referenced to the secondary pixel counter, the mapping of the CK_TOGx_TP_POL bits to the toggle points is offset by a number of bits equal to the TP_SEC_OFFSET value.

For example, if TP_SEC_OFFSET = 10, toggle points TP10–TP31 are associated with the secondary counter. In this case, if the secondary counter is selected, Bit 0 of CK_TOGx_TP_POL defines the logic level at TP10, Bit 1 of CK_TOGx_TP_POL defines the logic level at TP11, etc.

The initial logic level (when the selected counter is reset) is configured using CK_TOGx_INIT_LVL for each toggle source. The level can be unchanged from the previous counter cycle, or can be set equal to the logic level of the first toggle point.

If a mask/toggle is referenced to the secondary pixel counter, the respective function can be selectively enabled for individual sequence states using CK_MASKx_SEQ_SEL and CK_TOGx_SEQ_SEL. Each bit within these fields enables the mask/toggle function for the corresponding state.

If the mask function is disabled, the clock output switches high/low while the toggle control is high; the output is held low while toggle control is low. If the toggle function is disabled, the output is held low throughout the respective state.

There is a latency between the CK_MASKx_START pixel count and the start of the mask period. Similarly, there is a latency between the CK_MASKx_END pixel count and the end of the mask period. The mask timing has a dependency on the AFECK and TGCKO clocks (see Section 4.6 and Section 4.8.3).

The following definitions assume the C_CK is configured to mask at Pixel *n*:

- If the rising edge of C_CK occurs before the rising edge of TGCKO (each measured from the rising edge of AFECK), the mask begins at the fourth C_CK rising edge following the Pixel *n* AFECK rising edge, as shown in Fig. 4-60.

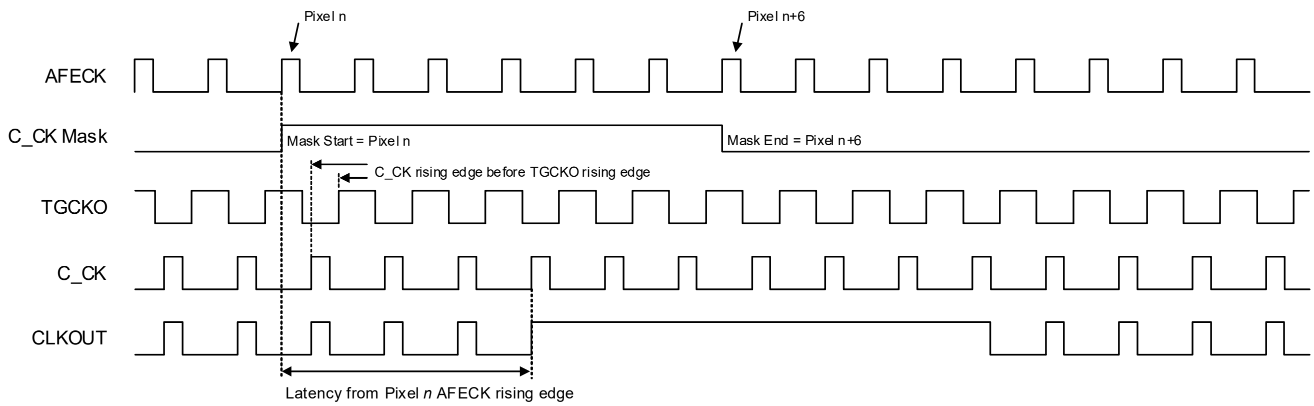


Figure 4-60. Clock Mask Timing—C_CK before TGCKO

- If the rising edge of C_CK occurs after the rising edge of TGCKO (each measured from the rising edge of AFECK), the mask is effective from the third C_CK rising edge following the Pixel *n* AFECK rising edge, as shown in Fig. 4-61.

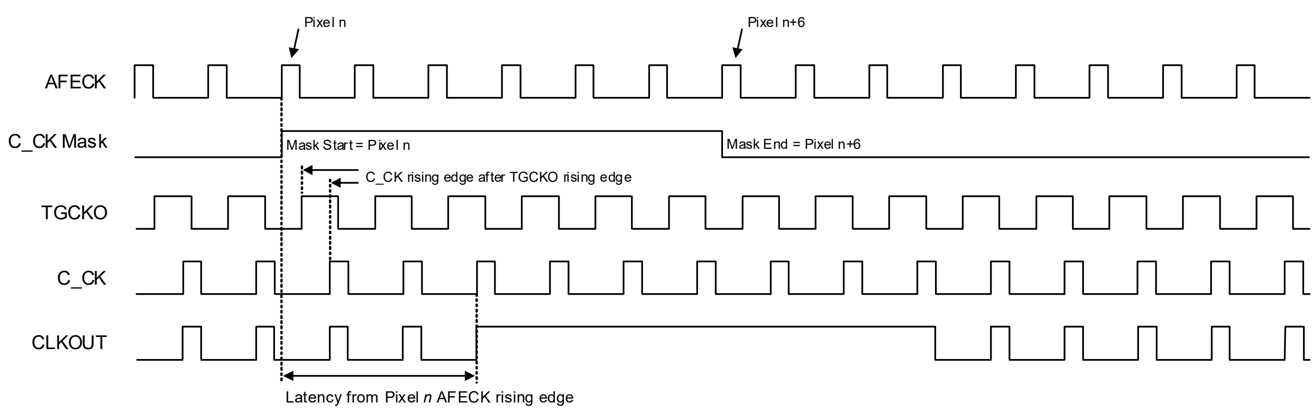


Figure 4-61. Clock Mask Timing—C_CK after TGCKO

If any toggle points (TPn) are defined within the mask period, the C_CK output switches to the logic level defined by the corresponding bit within CK_TOGx_TP_POL. The toggle timing is aligned to the rising edge of the AFECK; the latency is as described in Section 4.8.3 for the P_CKn pulse-output sources.

Note that the toggle configuration (CK_TOGx_TP_POL) must be set to Logic 1 throughout the unmasked pixel ranges. See Section 4.8.1 for details of toggle points TP0–TP31.

4.8.4.1 Clock Divider

A divider can be enabled on the high-speed clocks using DLL_CKx_DIV. If the divider is enabled, the respective C_CK rate is divided by two. The timing of the divided clock is configured using DLL_CKx_RISE to align the clock edges with the applicable DLL tap as illustrated in Fig. 4-62. Note the DLL_CKx_FALL field is not used in this case.

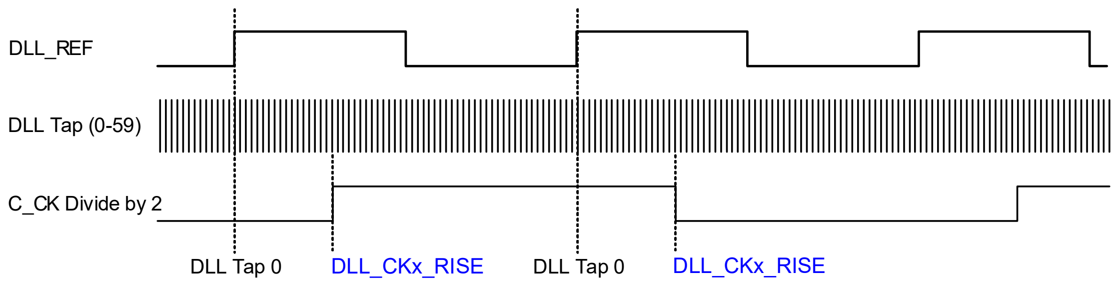


Figure 4-62. Clock Division

The divided clock toggles at half the C_CK rate—one cycle of the divided clock corresponds to two pixel-counter values. The phase relationship of the divided clock to the pixel counter is configured using the P_CK (pulse-waveform) clocks.

If the divider is enabled for C_CKx, the corresponding P_CKx signal provides a reset control for the divided C_CKx. Phase control is achieved by configuring P_CKx to hold the clock low (reset) for one or more pixels, and then enable the divided clock in the required phase.

The P_CKx waveform is derived from a PO (pulse-output) source as described in Section 4.8.3. The PO source is configurable as described in Section 4.8.2.

Phase control of the divided C_CK is illustrated in Fig. 4-63. If P_CK is high, the divided C_CK is held low; if P_CK is low, the divided C_CK is enabled.

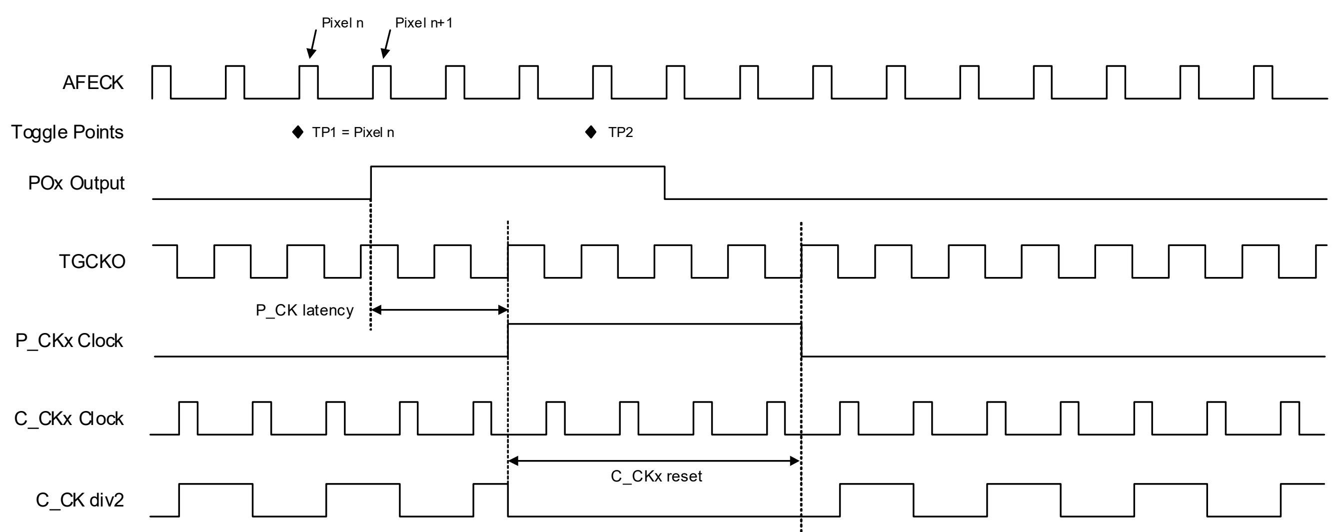
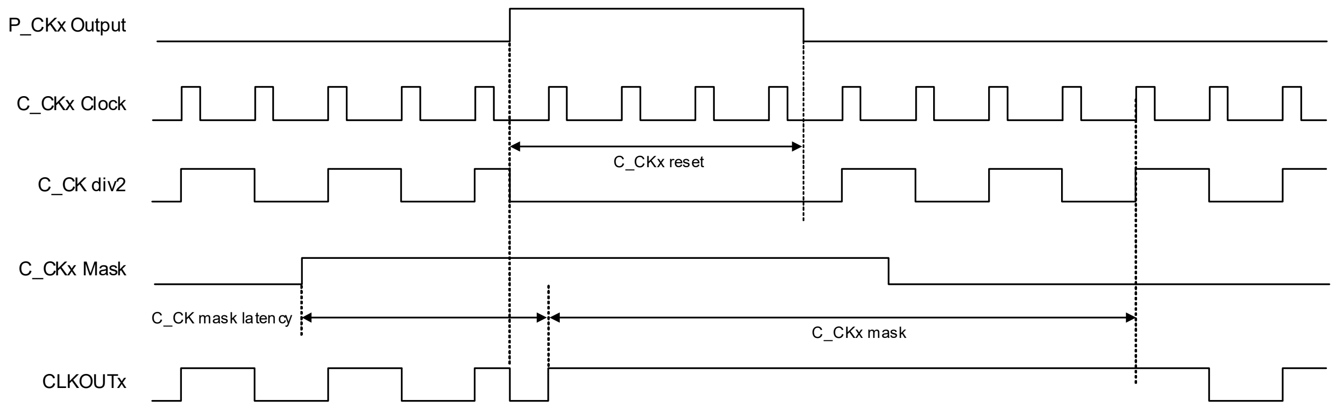


Figure 4-63. Clock Divider Phase Control

Mask and toggle controls are supported on the divided C_CK, as described in Section 4.8.4.

4.8.5 Clock Output Configuration



The CS82L46 supports external clock output on the CLKOUT1–CLKOUT10 pins. These are multifunction pins, which must be configured for the respective CLKOUTn function as described in Section 4.11.

The CLKOUT1–6 pins can be configured to output the respective high-speed clock C_CKn (see Section 4.8.4), or the respective pulse-waveform clock P_CKn (see Section 4.8.3). The applicable source is configured using CLKOUTx_SRC.

The CLKOUT7–10 outputs are each derived from the corresponding P_CKn waveform.

The clock outputs are enabled using CLKOUTx_EN. Signal inversion is available on each output using CLKOUTx_POL.

The clock-output configuration is illustrated in Fig. 4-64.

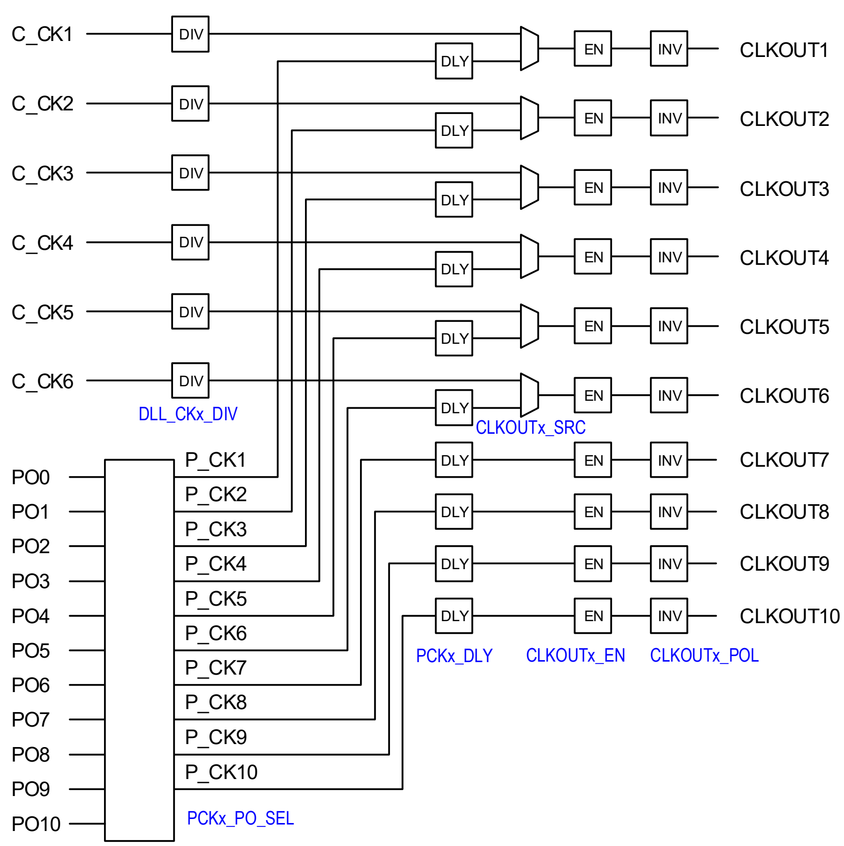


Figure 4-64. Clock Output Configuration

4.8.6 Clocking Configuration Constraints

The configuration of the high-speed clocks (C_CKn), sample-timing signals (VSMP, RSMP, and AFECK), and the TGCKO clock requires careful consideration to ensure the applicable constraints are observed.

The C_CKn clocks are used as control signals for the external sensor; they are configured as described in Section 4.8.4.

The VSMP, RSMP, and AFECK signals are used to control the sample timing and ADC conversion process on the video input signal. These signals are configured as described in Section 4.6.1; timing specifications are noted in Table 3-10. They can also be monitored externally as described in Section 4.12.

The TGCKO clock controls the timing of the pixel-counter increment and the pulse-output waveform functions. The TGCKO clock is configured as described in Section 4.8.3.

The timing constraints are summarized as follows:

- The VSMP, RSMP, and AFECK pulses must not overlap; the minimum duration of each must be observed.
- The TGCKO rising edge must not occur within 0–5 Taps after the AFECK rising edge.
- The TGCKO rising edge must not occur within 0–2 Taps after any C_CKn rising edge.

An example configuration is shown in Fig. 4-65. The constraints governing the TGCKO signal are highlighted.

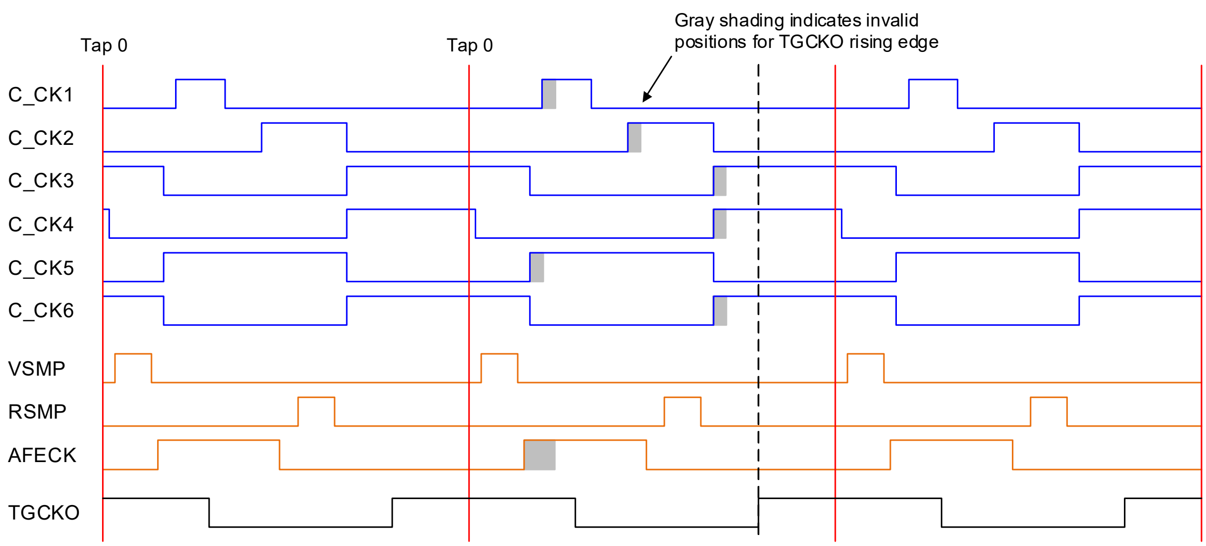


Figure 4-65. Example Clocking Configuration

4.9 LED Driver Control

Three current-sink LED drivers are provided, supporting independently programmable control. The three-channel controller is typically used to drive red, green, and blue LED outputs. White LEDs can also be supported. The LED drivers can be enabled using dedicated hardware pins, or else using pulse waveforms derived from the pixel counter and sequence state.

The LED control functions are enabled using LEDR_EN, LEDG_EN, and LEDB_EN for the red, green, and blue channels respectively.

The control source for the LED drivers is selected using LED_CTRL_SRC. The selection applies to all LED channels.

- If the hardware pin is selected, the LED is enabled if the respective pin is asserted high (Logic 1). The switching edges are synchronized to the pixel-counter clock in order to reduce asynchronous noise in the system.

  The LED control inputs are supported on multifunction pins, which must be configured for the respective function as described in Section 4.11.
- If the pulse waveform is selected, the LED is controlled by one of the pulse output sources, PO0–PO10. The applicable pulse source is selected using LEDx_PO_SEL. The POn signals are programmable waveforms that toggle on/off under configurable pixel-counter and sequence-state conditions. See Section 4.8.2 for details of the pulse-output sources.

The output current of each driver is configured using coarse and fine controls. The maximum available output current is configured using the coarse control, LEDx_COARSE. The output current is selected—from zero to the configured maximum—using the fine control, LEDx_FINE. The fine control provides an 8-bit resolution to set the output current between zero and the configured maximum (coarse) level.

Notes: If the sum of the coarse current selections in the active LED channels exceeds the maximum limit (135 mA in typical combinations), the current levels are automatically restricted to a maximum of 45 mA.

The maximum current limit applies to active channels only, i.e., LED drivers that are enabled using LEDx_EN and by an asserted hardware pin or pulse waveform.

The LED drivers must be disabled before changing the coarse current control. The host should confirm the CS82L46 is in the Idle State (see Section 4.2) before changing the coarse current control.

When an LED driver is enabled/disabled, or the fine current level is changed, the respective current sink ramps up/down to the configured level. The ramp rate is configurable using LED_RAMP_TIME. If the fine current level is changed while a ramp is in progress, the current sink ramps up/down to the new level.

The ramp rate can be modified using LED_RAMP_BOOST, allowing slew rates 2x or 4x faster than the LED_RAMP_TIME rate. Some restrictions are applicable on these faster rates, as noted in the register-field description.

The external connections for the LED drivers are illustrated in Fig. 4-66. An external resistor, connected to ILED_CTRL, is used to calibrate the output current of the LED drivers.

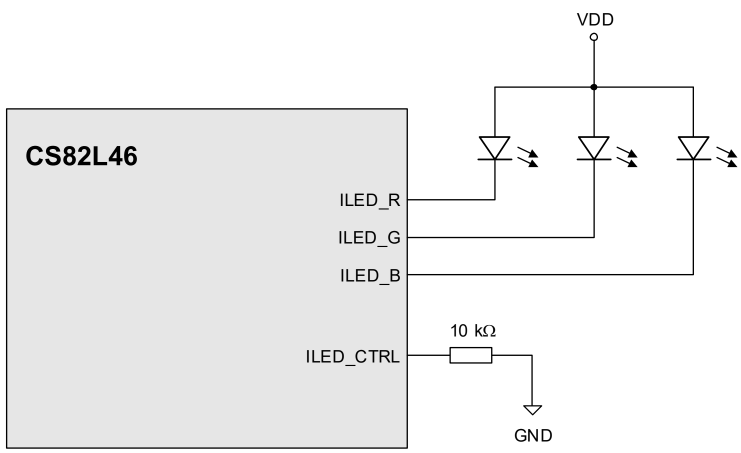


Figure 4-66. LED Output Drivers

The LED drivers are protected in case of fault conditions. Error conditions are indicated using the following control bits:

- LED_MAX_CURRENT_ERR—indicates sum of the coarse current levels (in the enabled channels) exceeds the maximum limit. If this bit is set, the fine current levels are automatically restricted to a maximum of 45 mA.
- LED_CTRL_SHORT_ERR—indicates a short circuit on the external ILED_CTRL resistor.

If a short circuit is detected, the LED drivers are shut down and the CS82L46 enters the Error State. See Section 4.2.1 for further details.

Note there is no specific indication of an open circuit on the external ILED_CTRL resistor, but the LED drivers are protected and disabled in this event.

If an LED output pin is shorted to a supply rail, the driver maintains the selected current through the pin, resulting in increased voltage drop across the internal circuits. The current drawn from the supply is protected, but thermal dissipation in the CS82L46 is increased.

4.10 Control Interface

The CS82L46 incorporates a control port, supporting I2C or SPI modes of operation. The CS82L46 is configured by writing to control registers using the control port.

The control port is automatically configured in I2C mode or SPI mode following the first valid I2C/SPI activity detected after power-on. In SPI mode, the CS82L46 supports a number of different protocols, enabling compatibility with a wide variety of host systems.

4.10.1 I2C Interface

The I2C control port is supported using the I2C_SCL and I2C_SDA pins.

The CS82L46 is a target device on the I2C bus—SCL is a clock input, SDA is a bidirectional data pin. To allow arbitration of multiple targets (and/or multiple controllers) on the same interface, the CS82L46 transmits Logic 1 by tristating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the Logic 1 can be recognized by the controller.

In order to allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit target address (this is not the same as the address of each register in the register map). Note that the LSB of the target address is the read/write bit; this bit is set to Logic 1 for read and Logic 0 for write.

The I2C target address is configured using the DSLCT pin as described in Table 4-7.

Table 4-7. I2C Target Address Selection

DSLCT Pin Connection	I2C Address
Logic 0	0x34 (write), 0x35 (read)
Logic 1	0x36 (write), 0x37 (read)

The host device indicates the start of data transfer with a high-to-low transition on SDA while SCL remains high. This indicates that a device address and subsequent address/data bytes follow. The CS82L46 responds to the start condition and shifts in the next eight bits on SDA (8-bit target address, including read/write bit, MSB first). If the target address received matches the target address of The CS82L46, it responds by pulling SDA low on the next clock pulse (ACK). If the target address is not recognized, the CS82L46 returns to the idle condition and waits for a new start condition.

If the target address matches the target address of the CS82L46, the data transfer continues. The controller indicates the end of data transfer with a low-to-high transition on SDA while SCL remains high. After receiving a complete address and data sequence, the CS82L46 returns to idle and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e., SDA changes while SCL is high), the device returns to the idle condition.

The I2C interface uses a 16-bit register address and 8-bit data words. Note that the full I2C message protocol also includes a target address, a read/ write bit, and other signaling bits (see Fig. 4-67 and Fig. 4-68).

The CS82L46 supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. In these modes, the CS82L46 automatically increments the register address after each data word. Successive data words can be input/output in turn (see Fig. 4-71 and Fig. 4-72).

The I2C protocol for a single, 8-bit register write operation is shown in Fig. 4-67.

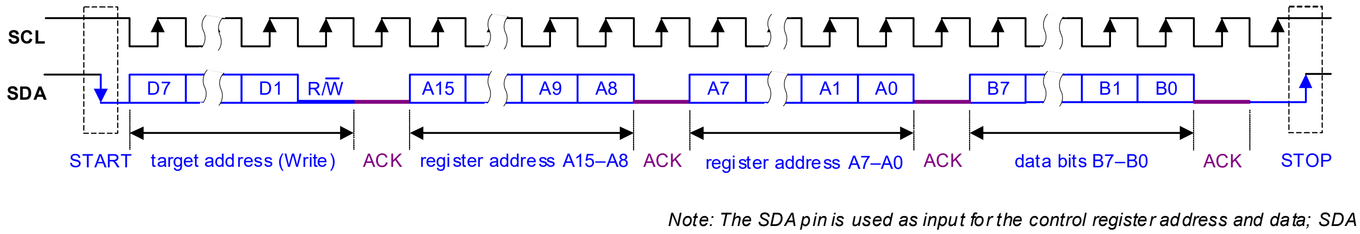


Figure 4-67. Control Interface I2C Register Write

The I2C protocol for a single, 8-bit register read operation is shown in Fig. 4-68.

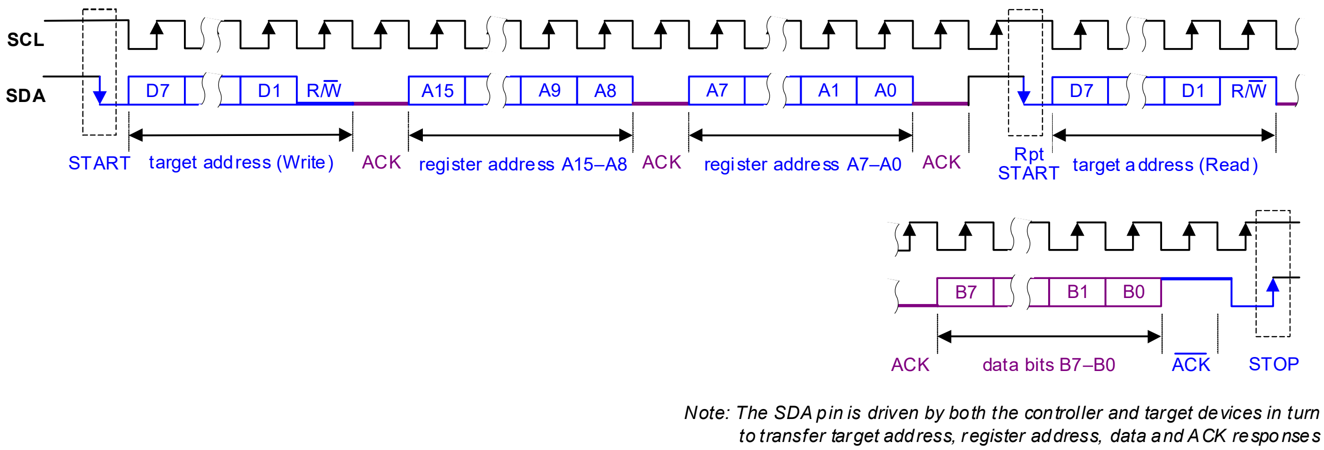


Figure 4-68. Control Interface I2C Register Read

The I2C interface also supports other register operations; the interface protocol for these operations is shown in Fig. 4-69 through Fig. 4-72. The terminology used in the following figures is detailed in Table 4-8.

Table 4-8. Control Interface (I2C) Terminology

Terminology	Description
S	Start condition
Sr	Repeated start
A	Acknowledge (SDA low)
$\overline{A}$	No Acknowledge (SDA high)
P	Stop condition
R/$\overline{W}$	Read/not Write: 0 = Write, 1 = Read
[White field]	Data flow from bus controller to CS82L46
[Gray field]	Data from CS82L46 to bus controller

Fig. 4-69 shows a single register write to a specified address.

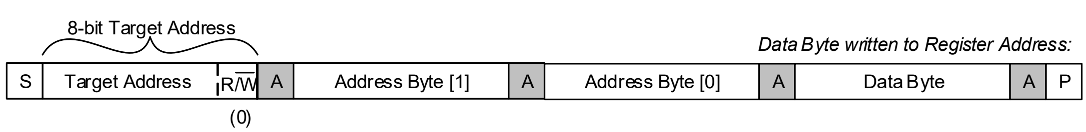


Figure 4-69. Single-Register Write to Specified Address

Fig. 4-70 shows a single register read from a specified address.

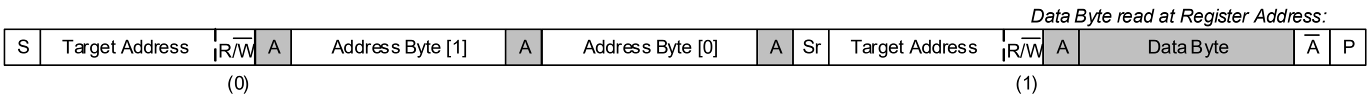


Figure 4-70. Single-Register Read from Specified Address

Fig. 4-71 shows a multiple register write to a specified address.

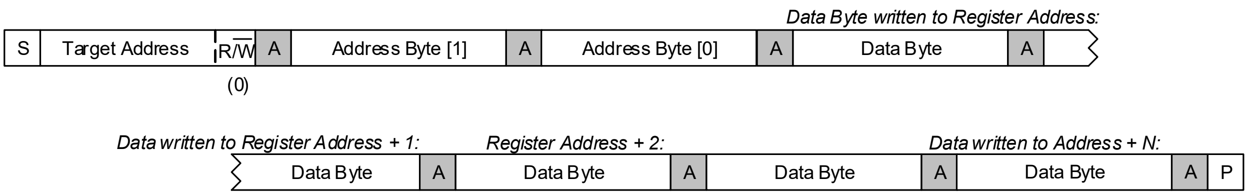


Figure 4-71. Multiple-Register Write to Specified Address

Fig. 4-72 shows a multiple register read from a specified address.

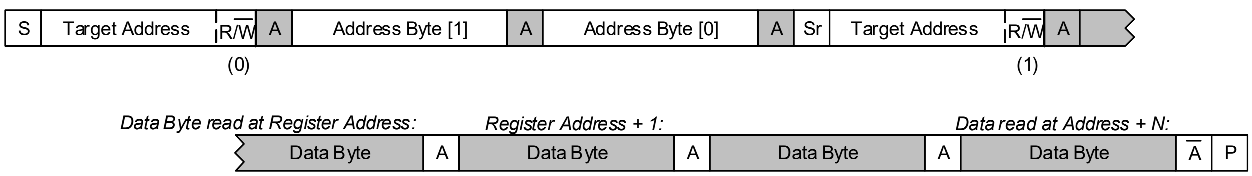


Figure 4-72. Multiple-Register Read from Specified Address

4.10.2 SPI Interface

The SPI interface is supported using the $\overline{\text{SPI\_CS}}$, SPI_SCK, SPI_SDI, and SPI_SDO pins.

The $\overline{\text{SPI\_CS}}$ pin provides the chip-select input (active low). Clocking for the input/output data is supported using SPI_SCK.

The SDI (data-input) pin supports the following behavior:

- In write operations (R/W = 0), the SDI pin input is driven by the controlling device.
- In read operations (R/W = 1), the SDI pin is ignored following receipt of the valid register address.

The SDO (data-output) pin supports the following behavior:

- If $\overline{\text{CS}}$ is asserted (Logic 0), the SDO output is actively driven when outputting data and is high impedance at other times. If $\overline{\text{CS}}$ is not asserted, the SDO output is high impedance.
- The high-impedance state of the SDO output allows the pin to be shared with other peripheral devices.
- The output (SDO) data bit is available to the host device at the rising edge of SCK. See Table 3-20 for timing information.

In SPI Mode, the CS82L46 can be configured for different protocols, enabling compatibility with a wide variety of host systems. The SPI Mode is configured using the DSLCT pin as described in Table 4-9.

Table 4-9. SPI Mode Selection

DSLCT Pin Configuration		SPI Mode	Description
Pull-up to VDD	0 Ω	Flat Mode 0	2-bit chip select, 13-bit register address, 8-bit data. Device responds to read/write access if chip select = 00.
	4.7 kΩ	Flat Mode 1	2-bit chip select, 13-bit register address, 8-bit data. Device responds to read/write access if chip select = 01.
Pull-down to GND	0 Ω	Banked Mode	7-bit register address, 8-bit data. Registers arranged in Bank 0–7; current bank selected using BANK.

Note: The pull-up resistor must be within 1% of the specified value

4.10.2.1 Flat Mode

In Flat Mode, the SPI interface uses a 2-bit chip select, 13-bit register address, and 8-bit data words. A read/write bit is also used to select the transaction type.

The chip-select bits allow the host to control more than one CS82L46 over a shared control interface. The SPI read/write command is valid if the chip-select bits match the configured mode (see Table 4-9).

- In Flat Mode 0, the SPI command is valid if CS[1:0] = 00.
- In Flat Mode 1, the SPI command is valid if CS[1:0] = 01.

Regardless of which mode the device is configured in, a write transaction is also valid if CS[1:0] = 10 or 11. This allows the host to write to more than one device simultaneously. Note that a read transaction is not valid under these conditions, and generates no response.

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS82L46 automatically increments the register address at the end of each data word, for as long as $\overline{CS}$ is held low and SCK is toggled. Successive data words can be input/output every 8 clock cycles.

Fig. 4-73 shows a single register write to a specified address.

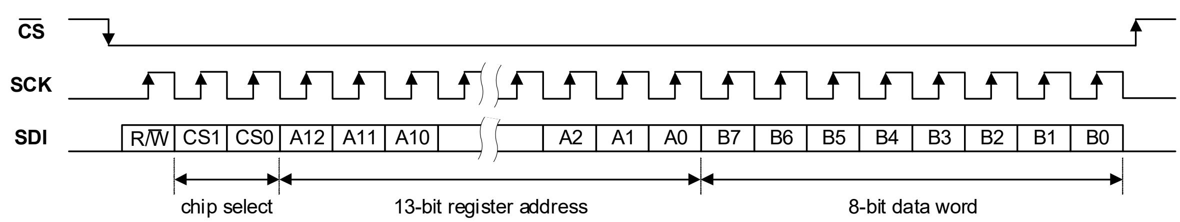


Figure 4-73. Control Interface SPI Register Write—Flat Mode

Fig. 4-74 shows a single register read from a specified address.

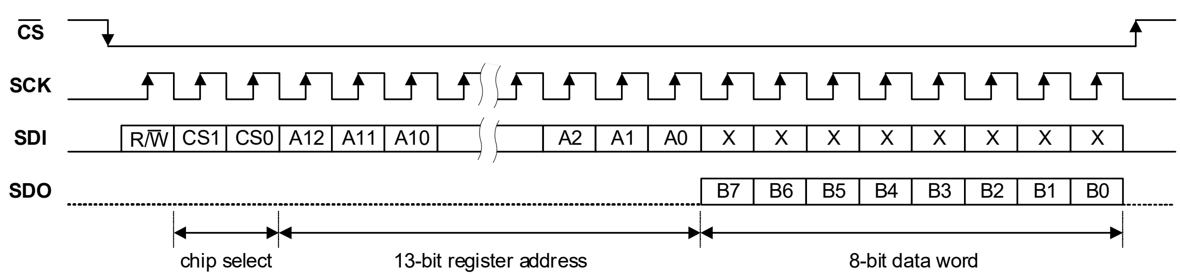


Figure 4-74. Control Interface SPI Register Read—Flat Mode

4.10.2.2 Banked Mode

In Banked Mode, the SPI interface uses a 7-bit register address and 8-bit data words. A read/write bit is also used to select the transaction type.

The register map is arranged in 8 banks, each containing 128 registers. By selecting different banks, all of the CS82L46 control registers can be accessed using the 7-bit register address.

The current bank is configured using BANK. This field is supported at register address 0x00 in all banks, and can therefore be accessed in the same way regardless of which bank is currently selected.

Note: An overview of the register map in Banked Mode is described in Section 6.

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS82L46 automatically increments the register address at the end of each data word, for as long as CS is held low and SCK is toggled. Successive data words can be input/output every 8 clock cycles.

Fig. 4-75 shows a single register write to a specified address.

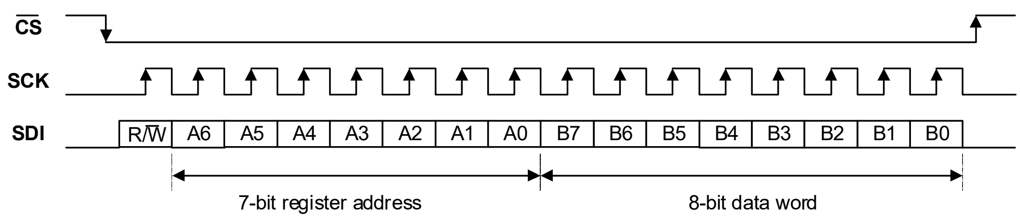


Figure 4-75. Control Interface SPI Register Write—Banked Mode

Fig. 4-76 shows a single register read from a specified address.

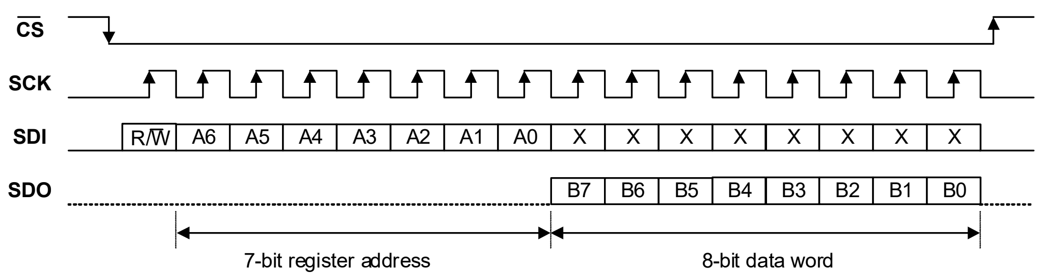


Figure 4-76. Control Interface SPI Register Read—Banked Mode

4.10.2.3 Shared Bus Mode

The CS82L46 can be configured in Shared Bus Mode, where the SPI control interface and the digital data output are supported on shared pins. This can be used to reduce the number of I/O connections to the host interface. Note that Shared Bus Mode is supported for CMOS data-output formats only (see Section 4.5).

In Shared Bus Mode, the DOUTn data outputs are disabled (Hi-Z) whenever SPI_CS is asserted. The SPI_SDO output is disabled (Hi-Z) whenever SPI_CS is not asserted. This allows the two interfaces to be connected together and used in turn.

If required, the GPI12 input can be used to disable the DOUTn data outputs (Hi-Z). This can be used to ensure there is no bus contention, by disabling the data outputs before SPI_CS is asserted and re-enabling them after the SPI transactions are complete.

Typical connections for Shared Bus Mode are shown in Fig. 4-77.

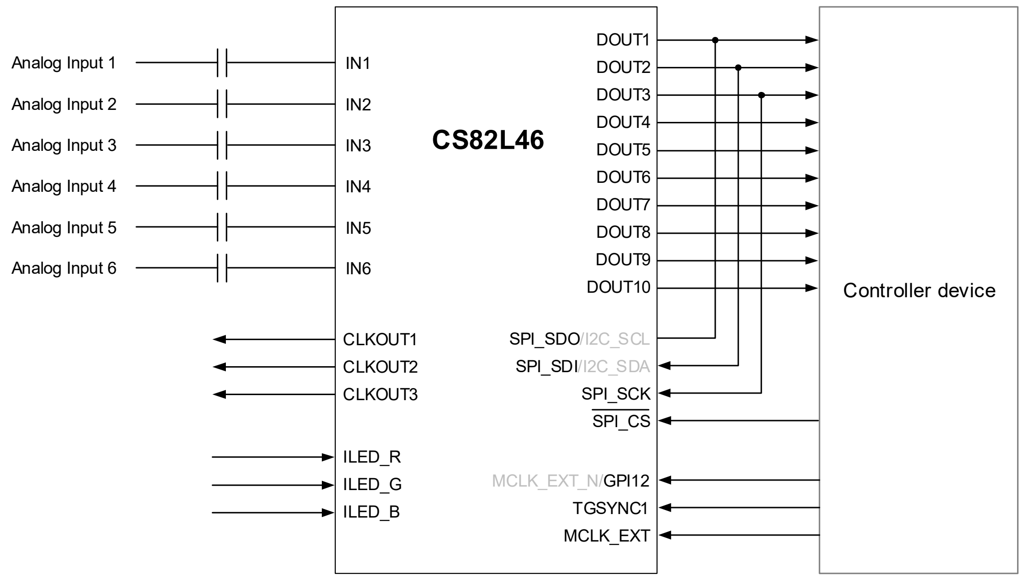


Figure 4-77. Shared Bus Mode

Shared Bus Mode is enabled using SHARED_BUS_MODE. If this bit is set, the DOUTn pins are controlled to allow these pins to be shared with the SPI control interface. The DOUTn pins are Hi-Z when SPI_CS is asserted (Logic 0), allowing the host to access the control registers using the SPI interface.

The GPI12 input can be configured to control the data-output pins by setting GPI12_DOUT_CTRL. If this bit is set, the data-output pins are enabled by applying a Logic 1 to the GPI12 input; the pins are disabled (Hi-Z) by applying a Logic 0. The GPI12 function is supported on the MCLK_EXT_N pin, which must be configured for general-purpose input as described in Section 4.11.

In Shared Bus Mode, the host must ensure the DOUTn pins are Hi-Z before driving the shared signal lines. The host must cease driving the shared signal lines before the DOUTn pins are driven. Timing specifications are shown in Table 3-20.

The following operational constraints must be observed to avoid contention between the SPI_SDO and DOUTn outputs:

- In the Idle State, SPI read and SPI write operations are supported.
- In the Ready State, SPI write operations are supported. SPI read operations are supported if DOUT_READY_EN is cleared (see Section 4.2 for further information).
- In the Active State, SPI write operations are supported. SPI read operations are not supported.

In a typical application, the host configures the device in the Idle State (see Section 4.2). When the host selects the Active State, the data output commences after SPI_CS is deasserted high (and GPI12 is asserted high, if applicable). The data output ceases when SPI_CS is asserted low (or GPI12 is deasserted low, if applicable).

Note: The selected data-output format is enabled by default in the Ready State (the data bits and status flags are held at 0). If the SPI and DOUT pins are connected on the PCB, the Shared Bus Mode must be enabled prior to selecting the Ready State in order to avoid bus contention.

The DOUTn pins can be shared with the SPI_SDI, SPI_SDO, and SPI_SCK pins in any configuration; the connections shown in Fig. 4-77 are an example configuration only.

4.11 Pin Configuration and General-Purpose Input/Output

Many of the digital input/output functions are supported on multifunction pins. These pins are used for sample/frame timing control, clock outputs, and LED control inputs. General-purpose input/output is also supported.

4.11.1 Pin Function Select

The multifunction pins are configured for the required function using the control fields described in Table 4-10.

Table 4-10. Pin Function Select

Pin Name	Control Field	Selection	Reference
TGSYNC1/VSMP_EXT	TGSYNC1_VSMP_FN	00 = VSMP input	Section 4.6.2, Section 4.6.3
		01 = TGSYNC1 input [1]	Section 4.7.3
		10 = Not used (Hi-Z)	—
		11 = TGSYNC output	Section 4.7.2
CLKOUT1/LEDR_EN/ TGSYNC2	CLKOUT1_FN	00 = Red LED control input [1]	Section 4.9
		01 = TGSYNC2 input [1]	Section 4.7.3
		10 = General-purpose input/output 1	Section 4.11.2
		11 = CLKOUT1	Section 4.8.5
CLKOUT2/LEDG_EN/ LEDSTART	CLKOUT2_FN	00 = Green LED control input [1]	Section 4.9
		01 = LEDSTART [1]	Section 4.7.3
		10 = General-purpose input/output 2	Section 4.11.2
		11 = CLKOUT2	Section 4.8.5
CLKOUT3/LEDB_EN/ RSMP_EXT	CLKOUT3_FN	000 = Blue LED control input [1]	Section 4.9
		001 = RSMP input [2]	Section 4.6.2
		010 = General-purpose input/output 3	Section 4.11.2
		011 = CLKOUT3	Section 4.8.5
		100 = Monitor/test output	Section 4.12
		101–111 = Reserved	—
CLKOUT4	CLKOUT4_FN	0 = General-purpose input/output 4 [1]	Section 4.11.2
		1 = CLKOUT4	Section 4.8.5
CLKOUT5	CLKOUT5_FN	0 = General-purpose input 5	Section 4.11.2
		1 = CLKOUT5	Section 4.8.5
CLKOUT6	CLKOUT6_FN	0 = General-purpose input 6	Section 4.11.2
		1 = CLKOUT6	Section 4.8.5
CLKOUT7	CLKOUT7_FN	0 = General-purpose input/output 7	Section 4.11.2
		1 = CLKOUT7	Section 4.8.5
CLKOUT8	CLKOUT8_FN	0 = General-purpose input/output 8	Section 4.11.2
		1 = CLKOUT8	Section 4.8.5
CLKOUT9	CLKOUT9_FN	0 = General-purpose input/output 9	Section 4.11.2
		1 = CLKOUT9	Section 4.8.5
CLKOUT10	CLKOUT10_FN	0 = General-purpose input/output 10	Section 4.11.2
		1 = CLKOUT10	Section 4.8.5
MCLK_EXT_N	MCLK_EXT_LVDS	0 = General-purpose input 12 [3]	Section 4.11.2
		1 = LVDS clock input	Section 4.3

1. The TGSYNC, LED-enable, LEDSTART, and GPIO4 input can also be used to control the MCLK mask, as described in Section 4.3.2.
2. The RSMP input can also be used to control the input clamp, as described in Section 4.4.3.
3. The GPI12 input can also be used to control the DOUT pins, as described in Section 4.10.2.3.

4.11.2 General Purpose Input/Output

The CS82L46 supports general-purpose (GP) input/output on selected digital I/O pins. The input function can be used to allow readback of hardware signals from other devices. The output function can be used to control other devices.

The general-purpose inputs are multiplexed with other pin functions. Each pin is configured for GP input/output using the respective x_FN field as noted in Table 4-10.

The general-purpose I/O functions are configured as input by default. The output function is enabled by setting the respective GPx_DIR bit. Note that GP output is supported on GPIO1–4 and GPIO7–10 only.

- If a pin is configured for GP input, the logic level is indicated using GPx_IN_STS.
- If a pin is configured for GP output, the output level is controlled using GPx_OUT_LVL.

4.11.3 Digital I/O Pin Configuration

The digital I/O pins are configurable to support flexible integration with other devices. Configurable options are provided for all of the digital I/O listed in Table 1-1—this includes MCLK input, data output, clock output, and the multifunction pins listed in Table 4-10.

Integrated pull-up and pull-down resistors are configured and enabled using the respective x_PULL fields. A bus-keeper function can also be enabled using the x_PULL fields; the bus-keeper holds the logic level unchanged whenever the pin is undriven (e.g., if the signal is tristated).

Note: The pull-up and pull-down resistors are valid for CMOS input/output only; if a pin is operating in LVDS mode, the pull resistors must be disabled using the respective x_PULL fields.

The drive strength for CMOS digital output is configured using x_DRV_STR. The drive strength for LVDS output is configured using x_TXDRV.

The input function on each pin is enabled using x_IE. This bit must be set to support input functions on the respective pin.

The pins can be configured in a high-impedance state using x_HIZ_EN. This option is supported for CMOS input/output only; the field has no effect on any pin configured for LVDS data output. Note that, to configure the high-impedance state, the pull-up and pull-down resistors must also be disabled using x_PULL.

The voltage reference for LVDS input/output is selectable using LVDS_VREF_SEL.

An LVDS termination resistor can be enabled on the MCLK input by setting MCLK_LVDS_RT_EN.

4.12 Debug Monitor Output

The MON output allows internal clock signals to be monitored externally for timing set-up and debug purposes. The MON function is supported on a multifunction pin, which must be configured for monitor output as described in Section 4.11.

The MON output is configured using MON_SEL. The following output signals are supported:

- VSMP—video sample control
- RSMP—reset sample control
- AFECK—ADC sample/conversion control
- Data clock—output formatter clock
  In TG Mode, the data clock equates to DCLKOUT; in External Mode, the data clock equates to MCLK.
- PLL1—frequency synthesizer output

If using the monitor output to configure the signal timing for an application, it is recommended to take account of the propagation delay from the internal signal to the monitor output. The propagation delay is defined in Table 3-18.

4.13 Device ID

The device ID, and other associated data, can be read from the control fields listed in Table 4-11.

Table 4-11. Device ID

Label	Description
DEVID	Device ID
AREVID	All-layer device revision
MTLREVID	Metal-layer device revision
RELID	Software device revision
DESCRIM	Device identifier (readback value 0xC)

5 Applications

5.1 Digital Output Definitions

5.1.1 LVDS Output Format

The LVDS output formats are defined in this section. See Section 4.5 for details of the CS82L46 output formats.

LVDS Format 79 is defined in Fig. 5-1.

Format ID: 79
Number of channels: 6
Bits per channel: 16
Clock cycles per pixel: 3
Number of data pairs: 5

DOUT5	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DOUT4	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]
DOUT3	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]	CH2[0]	CH2[1]
DOUT2	CH2[2]	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]
DOUT1	CH2[9]	CH2[10]	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT5	S0	S1	S2	CH3[0]	CH3[1]	CH3[2]	CH3[3]
DOUT4	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH3[10]
DOUT3	CH3[11]	CH3[12]	CH3[13]	CH3[14]	CH3[15]	CH4[0]	CH4[1]
DOUT2	CH4[2]	CH4[3]	CH4[4]	CH4[5]	CH4[6]	CH4[7]	CH4[8]
DOUT1	CH4[9]	CH4[10]	CH4[11]	CH4[12]	CH4[13]	CH4[14]	CH4[15]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT5	S0	S1	S2	CH5[0]	CH5[1]	CH5[2]	CH5[3]
DOUT4	CH5[4]	CH5[5]	CH5[6]	CH5[7]	CH5[8]	CH5[9]	CH5[10]
DOUT3	CH5[11]	CH5[12]	CH5[13]	CH5[14]	CH5[15]	CH6[0]	CH6[1]
DOUT2	CH6[2]	CH6[3]	CH6[4]	CH6[5]	CH6[6]	CH6[7]	CH6[8]
DOUT1	CH6[9]	CH6[10]	CH6[11]	CH6[12]	CH6[13]	CH6[14]	CH6[15]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

Figure 5-1. LVDS Format 79

LVDS Format 78 is defined in Fig. 5-2.

Format ID: 78
Number of channels: 4
Bits per channel: 16
Clock cycles per pixel: 2
Number of data pairs: 5

DOUT5	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DOUT4	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]
DOUT3	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]	CH2[0]	CH2[1]
DOUT2	CH2[2]	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]
DOUT1	CH2[9]	CH2[10]	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT5	S0	S1	S2	CH3[0]	CH3[1]	CH3[2]	CH3[3]
DOUT4	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH3[10]
DOUT3	CH3[11]	CH3[12]	CH3[13]	CH3[14]	CH3[15]	CH4[0]	CH4[1]
DOUT2	CH4[2]	CH4[3]	CH4[4]	CH4[5]	CH4[6]	CH4[7]	CH4[8]
DOUT1	CH4[9]	CH4[10]	CH4[11]	CH4[12]	CH4[13]	CH4[14]	CH4[15]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

Figure 5-2. LVDS Format 78

LVDS Format 77 is defined in Fig. 5-3.

Format ID: 77
Number of channels: 3
Bits per channel: 16
Clock cycles per pixel: 1.5 (3 clock cycles per 2 pixels)
Number of data pairs: 5

DOUT5	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DOUT4	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]
DOUT3	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]	CH2[0]	CH2[1]
DOUT2	CH2[2]	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]
DOUT1	CH2[9]	CH2[10]	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT5	S0	S1	S2	CH3[0]	CH3[1]	CH3[2]	CH3[3]
DOUT4	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH3[10]
DOUT3	CH3[11]	CH3[12]	CH3[13]	CH3[14]	CH3[15]	CH1[0]	CH1[1]
DOUT2	CH1[2]	CH1[3]	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]
DOUT1	CH1[9]	CH1[10]	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT5	S0	S1	S2	CH2[0]	CH2[1]	CH2[2]	CH2[3]
DOUT4	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]	CH2[10]
DOUT3	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]	CH3[0]	CH3[1]
DOUT2	CH3[2]	CH3[3]	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]
DOUT1	CH3[9]	CH3[10]	CH3[11]	CH3[12]	CH3[13]	CH3[14]	CH3[15]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

Figure 5-3. LVDS Format 77

LVDS Format 76 is defined in Fig. 5-4.

Format ID: 76
Number of channels: 2
Bits per channel: 16
Clock cycles per pixel: 1
Number of data pairs: 5

DOUT5	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DOUT4	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]
DOUT3	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]	CH2[0]	CH2[1]
DOUT2	CH2[2]	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]
DOUT1	CH2[9]	CH2[10]	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-4. LVDS Format 76

LVDS Format 86 is defined in Fig. 5-5.

Format ID: 86
Number of channels: 6
Bits per channel: 10
Clock cycles per pixel: 2
Number of data pairs: 5

DOUT5	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DOUT4	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	S3
DOUT3	S4	CH2[0]	CH2[1]	CH2[2]	CH2[3]	CH2[4]	CH2[5]
DOUT2	CH2[6]	CH2[7]	CH2[8]	CH2[9]	CH3[0]	CH3[1]	CH3[2]
DOUT1	CH3[3]	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT5	S0	S1	S2	CH4[0]	CH4[1]	CH4[2]	CH4[3]
DOUT4	CH4[4]	CH4[5]	CH4[6]	CH4[7]	CH4[8]	CH4[9]	S3
DOUT3	S4	CH5[0]	CH5[1]	CH5[2]	CH5[3]	CH5[4]	CH5[5]
DOUT2	CH5[6]	CH5[7]	CH5[8]	CH5[9]	CH6[0]	CH6[1]	CH6[2]
DOUT1	CH6[3]	CH6[4]	CH6[5]	CH6[6]	CH6[7]	CH6[8]	CH6[9]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

Figure 5-5. LVDS Format 86

LVDS Format 85 is defined in Fig. 5-6.

Format ID: 85
Number of channels: 4
Bits per channel: 10
Clock cycles per pixel: 1.33 (4 clock cycles per 3 pixels)
Number of data pairs: 5

DOUT5	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DOUT4	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	S3
DOUT3	S4	CH2[0]	CH2[1]	CH2[2]	CH2[3]	CH2[4]	CH2[5]
DOUT2	CH2[6]	CH2[7]	CH2[8]	CH2[9]	CH3[0]	CH3[1]	CH3[2]
DOUT1	CH3[3]	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT5	S0	S1	S2	CH4[0]	CH4[1]	CH4[2]	CH4[3]
DOUT4	CH4[4]	CH4[5]	CH4[6]	CH4[7]	CH4[8]	CH4[9]	S3
DOUT3	S4	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]	CH1[5]
DOUT2	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH2[0]	CH2[1]	CH2[2]
DOUT1	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT5	S0	S1	S2	CH3[0]	CH3[1]	CH3[2]	CH3[3]
DOUT4	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]	S3
DOUT3	S4	CH4[0]	CH4[1]	CH4[2]	CH4[3]	CH4[4]	CH4[5]
DOUT2	CH4[6]	CH4[7]	CH4[8]	CH4[9]	CH1[0]	CH1[1]	CH1[2]
DOUT1	CH1[3]	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

DOUT5	S0	S1	S2	CH2[0]	CH2[1]	CH2[2]	CH2[3]
DOUT4	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]	S3
DOUT3	S4	CH3[0]	CH3[1]	CH3[2]	CH3[3]	CH3[4]	CH3[5]
DOUT2	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH4[0]	CH4[1]	CH4[2]
DOUT1	CH4[3]	CH4[4]	CH4[5]	CH4[6]	CH4[7]	CH4[8]	CH4[9]
DCLKOUT	H	H	L	L	L	H	H

Data Block 4

Figure 5-6. LVDS Format 85

LVDS Format 84 is defined in Fig. 5-7.

Format ID: 84
Number of channels: 3
Bits per channel: 10
Clock cycles per pixel: 1
Number of data pairs: 5

DOUT5	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DOUT4	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	S3
DOUT3	S4	CH2[0]	CH2[1]	CH2[2]	CH2[3]	CH2[4]	CH2[5]
DOUT2	CH2[6]	CH2[7]	CH2[8]	CH2[9]	CH3[0]	CH3[1]	CH3[2]
DOUT1	CH3[3]	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-7. LVDS Format 84

LVDS Format 89 is defined in Fig. 5-8.

Format ID: 89
Number of channels: 6
Bits per channel: 10
Clock cycles per pixel: 2
Number of data pairs: 5

DOUT5	CH3[0]	CH3[1]	CH3[2]	CH3[3]	CH3[4]	CH3[5]	CH3[6]
DOUT4	CH3[7]	CH3[8]	CH3[9]	CH2[0]	CH2[1]	CH2[2]	CH2[3]
DOUT3	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]	S0
DOUT2	S1	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]	CH1[5]
DOUT1	CH1[6]	CH1[7]	CH1[8]	CH1[9]	S2	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT5	CH6[0]	CH6[1]	CH6[2]	CH6[3]	CH6[4]	CH6[5]	CH6[6]
DOUT4	CH6[7]	CH6[8]	CH6[9]	CH5[0]	CH5[1]	CH5[2]	CH5[3]
DOUT3	CH5[4]	CH5[5]	CH5[6]	CH5[7]	CH5[8]	CH5[9]	S0
DOUT2	S1	CH4[0]	CH4[1]	CH4[2]	CH4[3]	CH4[4]	CH4[5]
DOUT1	CH4[6]	CH4[7]	CH4[8]	CH4[9]	S2	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

Figure 5-8. LVDS Format 89

LVDS Format 88 is defined in Fig. 5-9.

Format ID: 88
Number of channels: 4
Bits per channel: 10
Clock cycles per pixel: 1.33 (4 clock cycles per 3 pixels)
Number of data pairs: 5

DOUT5	CH3[0]	CH3[1]	CH3[2]	CH3[3]	CH3[4]	CH3[5]	CH3[6]
DOUT4	CH3[7]	CH3[8]	CH3[9]	CH2[0]	CH2[1]	CH2[2]	CH2[3]
DOUT3	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]	S0
DOUT2	S1	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]	CH1[5]
DOUT1	CH1[6]	CH1[7]	CH1[8]	CH1[9]	S2	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT5	CH2[0]	CH2[1]	CH2[2]	CH2[3]	CH2[4]	CH2[5]	CH2[6]
DOUT4	CH2[7]	CH2[8]	CH2[9]	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DOUT3	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	S0
DOUT2	S1	CH4[0]	CH4[1]	CH4[2]	CH4[3]	CH4[4]	CH4[5]
DOUT1	CH4[6]	CH4[7]	CH4[8]	CH4[9]	S2	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT5	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]	CH1[5]	CH1[6]
DOUT4	CH1[7]	CH1[8]	CH1[9]	CH4[0]	CH4[1]	CH4[2]	CH4[3]
DOUT3	CH4[4]	CH4[5]	CH4[6]	CH4[7]	CH4[8]	CH4[9]	S0
DOUT2	S1	CH3[0]	CH3[1]	CH3[2]	CH3[3]	CH3[4]	CH3[5]
DOUT1	CH3[6]	CH3[7]	CH3[8]	CH3[9]	S2	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

DOUT5	CH4[0]	CH4[1]	CH4[2]	CH4[3]	CH4[4]	CH4[5]	CH4[6]
DOUT4	CH4[7]	CH4[8]	CH4[9]	CH3[0]	CH3[1]	CH3[2]	CH3[3]
DOUT3	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]	S0
DOUT2	S1	CH2[0]	CH2[1]	CH2[2]	CH2[3]	CH2[4]	CH2[5]
DOUT1	CH2[6]	CH2[7]	CH2[8]	CH2[9]	S2	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Data Block 4

Figure 5-9. LVDS Format 88

LVDS Format 87 is defined in Fig. 5-10.

Format ID: 87
Number of channels: 3
Bits per channel: 10
Clock cycles per pixel: 1
Number of data pairs: 5

DOUT5	CH3[0]	CH3[1]	CH3[2]	CH3[3]	CH3[4]	CH3[5]	CH3[6]
DOUT4	CH3[7]	CH3[8]	CH3[9]	CH2[0]	CH2[1]	CH2[2]	CH2[3]
DOUT3	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]	S0
DOUT2	S1	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]	CH1[5]
DOUT1	CH1[6]	CH1[7]	CH1[8]	CH1[9]	S2	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Figure 5-10. LVDS Format 87

LVDS Format 92 is defined in Fig. 5-11.

Format ID: 92
Number of channels: 6
Bits per channel: 12
Clock cycles per pixel: 3
Number of data pairs: 4

DOUT4	S0	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]	CH1[5]
DOUT3	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]	CH1[11]	S1
DOUT2	S2	S3	CH2[0]	CH2[1]	CH2[2]	CH2[3]	CH2[4]
DOUT1	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]	CH2[10]	CH2[11]
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT4	S0	CH3[0]	CH3[1]	CH3[2]	CH3[3]	CH3[4]	CH3[5]
DOUT3	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH3[10]	CH3[11]	S1
DOUT2	S2	S3	CH4[0]	CH4[1]	CH4[2]	CH4[3]	CH4[4]
DOUT1	CH4[5]	CH4[6]	CH4[7]	CH4[8]	CH4[9]	CH4[10]	CH4[11]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT4	S0	CH5[0]	CH5[1]	CH5[2]	CH5[3]	CH5[4]	CH5[5]
DOUT3	CH5[6]	CH5[7]	CH5[8]	CH5[9]	CH5[10]	CH5[11]	S1
DOUT2	S2	S3	CH6[0]	CH6[1]	CH6[2]	CH6[3]	CH6[4]
DOUT1	CH6[5]	CH6[6]	CH6[7]	CH6[8]	CH6[9]	CH6[10]	CH6[11]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

Figure 5-11. LVDS Format 92

LVDS Format 91 is defined in Fig. 5-12.

Format ID: 91
Number of channels: 4
Bits per channel: 12
Clock cycles per pixel: 2
Number of data pairs: 4

DOUT4	S0	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]	CH1[5]
DOUT3	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]	CH1[11]	S1
DOUT2	S2	S3	CH2[0]	CH2[1]	CH2[2]	CH2[3]	CH2[4]
DOUT1	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]	CH2[10]	CH2[11]
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT4	S0	CH3[0]	CH3[1]	CH3[2]	CH3[3]	CH3[4]	CH3[5]
DOUT3	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH3[10]	CH3[11]	S1
DOUT2	S2	S3	CH4[0]	CH4[1]	CH4[2]	CH4[3]	CH4[4]
DOUT1	CH4[5]	CH4[6]	CH4[7]	CH4[8]	CH4[9]	CH4[10]	CH4[11]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

Figure 5-12. LVDS Format 91

LVDS Format 90 is defined in Fig. 5-13.

Format ID: 90
Number of channels: 3
Bits per channel: 12
Clock cycles per pixel: 1.5 (3 clock cycles per 2 pixels)
Number of data pairs: 4

DOUT4	S0	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]	CH1[5]
DOUT3	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]	CH1[11]	S1
DOUT2	S2	S3	CH2[0]	CH2[1]	CH2[2]	CH2[3]	CH2[4]
DOUT1	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]	CH2[10]	CH2[11]
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT4	S0	CH3[0]	CH3[1]	CH3[2]	CH3[3]	CH3[4]	CH3[5]
DOUT3	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH3[10]	CH3[11]	S1
DOUT2	S2	S3	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]
DOUT1	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]	CH1[11]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT4	S0	CH2[0]	CH2[1]	CH2[2]	CH2[3]	CH2[4]	CH2[5]
DOUT3	CH2[6]	CH2[7]	CH2[8]	CH2[9]	CH2[10]	CH2[11]	S1
DOUT2	S2	S3	CH3[0]	CH3[1]	CH3[2]	CH3[3]	CH3[4]
DOUT1	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH3[10]	CH3[11]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

Figure 5-13. LVDS Format 90

LVDS Format 27 is defined in Fig. 5-14.

Format ID: 27
Number of channels: 4
Bits per channel: 16
Clock cycles per pixel: 4
Number of data pairs: 3

DOUT3	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DOUT2	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]
DOUT1	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT3	S0	S1	S2	CH2[0]	CH2[1]	CH2[2]	CH2[3]
DOUT2	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]	CH2[10]
DOUT1	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT3	S0	S1	S2	CH3[0]	CH3[1]	CH3[2]	CH3[3]
DOUT2	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH3[10]
DOUT1	CH3[11]	CH3[12]	CH3[13]	CH3[14]	CH3[15]	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

DOUT3	S0	S1	S2	CH4[0]	CH4[1]	CH4[2]	CH4[3]
DOUT2	CH4[4]	CH4[5]	CH4[6]	CH4[7]	CH4[8]	CH4[9]	CH4[10]
DOUT1	CH4[11]	CH4[12]	CH4[13]	CH4[14]	CH4[15]	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Data Block 4

Figure 5-14. LVDS Format 27

LVDS Format 26 is defined in Fig. 5-15.

Format ID: 26
Number of channels: 3
Bits per channel: 16
Clock cycles per pixel: 3
Number of data pairs: 3

Data Block 1

DOUT3	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DOUT2	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]
DOUT1	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT3	S0	S1	S2	CH2[0]	CH2[1]	CH2[2]	CH2[3]
DOUT2	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]	CH2[10]
DOUT1	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

DOUT3	S0	S1	S2	CH3[0]	CH3[1]	CH3[2]	CH3[3]
DOUT2	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH3[10]
DOUT1	CH3[11]	CH3[12]	CH3[13]	CH3[14]	CH3[15]	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Figure 5-15. LVDS Format 26

LVDS Format 25 is defined in Fig. 5-16.

Format ID: 25
Number of channels: 2
Bits per channel: 16
Clock cycles per pixel: 2
Number of data pairs: 3

Data Block 1

DOUT3	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DOUT2	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]
DOUT1	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT3	S0	S1	S2	CH2[0]	CH2[1]	CH2[2]	CH2[3]
DOUT2	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]	CH2[10]
DOUT1	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]	S3	S4
DCLKOUT	H	H	L	L	L	H	H

Figure 5-16. LVDS Format 25

LVDS Format 32 is defined in Fig. 5-17.

Format ID: 32
Number of channels: 6
Bits per channel: 10
Clock cycles per pixel: 3
Number of data pairs: 3

Data Block 1

DOUT3	S0	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]	CH1[5]
DOUT2	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH2[0]	CH2[1]	CH2[2]
DOUT1	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT3	S0	CH3[0]	CH3[1]	CH3[2]	CH3[3]	CH3[4]	CH3[5]
DOUT2	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH4[0]	CH4[1]	CH4[2]
DOUT1	CH4[3]	CH4[4]	CH4[5]	CH4[6]	CH4[7]	CH4[8]	CH4[9]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

DOUT3	S0	CH5[0]	CH5[1]	CH5[2]	CH5[3]	CH5[4]	CH5[5]
DOUT2	CH5[6]	CH5[7]	CH5[8]	CH5[9]	CH6[0]	CH6[1]	CH6[2]
DOUT1	CH6[3]	CH6[4]	CH6[5]	CH6[6]	CH6[7]	CH6[8]	CH6[9]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-17. LVDS Format 32

LVDS Format 31 is defined in Fig. 5-18.

Format ID: 31
Number of channels: 4
Bits per channel: 10
Clock cycles per pixel: 2
Number of data pairs: 3

Data Block 1

DOUT3	S0	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]	CH1[5]
DOUT2	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH2[0]	CH2[1]	CH2[2]
DOUT1	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT3	S0	CH3[0]	CH3[1]	CH3[2]	CH3[3]	CH3[4]	CH3[5]
DOUT2	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH4[0]	CH4[1]	CH4[2]
DOUT1	CH4[3]	CH4[4]	CH4[5]	CH4[6]	CH4[7]	CH4[8]	CH4[9]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-18. LVDS Format 31

LVDS Format 30 is defined in Fig. 5-19.

Format ID: 30
Number of channels: 3
Bits per channel: 10
Clock cycles per pixel: 1.5 (3 clock cycles per 2 pixels)
Number of data pairs: 3

DOUT3	S0	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]	CH1[5]
DOUT2	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH2[0]	CH2[1]	CH2[2]
DOUT1	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT3	S0	CH3[0]	CH3[1]	CH3[2]	CH3[3]	CH3[4]	CH3[5]
DOUT2	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH1[0]	CH1[1]	CH1[2]
DOUT1	CH1[3]	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT3	S0	CH2[0]	CH2[1]	CH2[2]	CH2[3]	CH2[4]	CH2[5]
DOUT2	CH2[6]	CH2[7]	CH2[8]	CH2[9]	CH3[0]	CH3[1]	CH3[2]
DOUT1	CH3[3]	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

Figure 5-19. LVDS Format 30

LVDS Format 29 is defined in Fig. 5-20.

Format ID: 29
Number of channels: 2
Bits per channel: 10
Clock cycles per pixel: 1
Number of data pairs: 3

DOUT3	S0	CH1[0]	CH1[1]	CH1[2]	CH1[3]	CH1[4]	CH1[5]
DOUT2	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH2[0]	CH2[1]	CH2[2]
DOUT1	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-20. LVDS Format 29

LVDS Format 35 is defined in Fig. 5-21.

Format ID: 35
Number of channels: 4
Bits per channel: 16
Clock cycles per pixel: 4
Number of data pairs: 3

DOUT3	CH1[9]	CH1[10]	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]
DOUT2	CH1[2]	CH1[3]	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]
DOUT1	S0	S1	S2	S3	S4	CH1[0]	CH1[1]
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT3	CH2[9]	CH2[10]	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]
DOUT2	CH2[2]	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]
DOUT1	S0	S1	S2	S3	S4	CH2[0]	CH2[1]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT3	CH3[9]	CH3[10]	CH3[11]	CH3[12]	CH3[13]	CH3[14]	CH3[15]
DOUT2	CH3[2]	CH3[3]	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]
DOUT1	S0	S1	S2	S3	S4	CH3[0]	CH3[1]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

DOUT3	CH4[9]	CH4[10]	CH4[11]	CH4[12]	CH4[13]	CH4[14]	CH4[15]
DOUT2	CH4[2]	CH4[3]	CH4[4]	CH4[5]	CH4[6]	CH4[7]	CH4[8]
DOUT1	S0	S1	S2	S3	S4	CH4[0]	CH4[1]
DCLKOUT	H	H	L	L	L	H	H

Data Block 4

Figure 5-21. LVDS Format 35

LVDS Format 34 is defined in Fig. 5-22.

Format ID: 34
Number of channels: 3
Bits per channel: 16
Clock cycles per pixel: 3
Number of data pairs: 3

DOUT3	CH1[9]	CH1[10]	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]
DOUT2	CH1[2]	CH1[3]	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]
DOUT1	S0	S1	S2	S3	S4	CH1[0]	CH1[1]
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT3	CH2[9]	CH2[10]	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]
DOUT2	CH2[2]	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]
DOUT1	S0	S1	S2	S3	S4	CH2[0]	CH2[1]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT3	CH3[9]	CH3[10]	CH3[11]	CH3[12]	CH3[13]	CH3[14]	CH3[15]
DOUT2	CH3[2]	CH3[3]	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]
DOUT1	S0	S1	S2	S3	S4	CH3[0]	CH3[1]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

Figure 5-22. LVDS Format 34

LVDS Format 33 is defined in Fig. 5-23.

Format ID: 33
Number of channels: 2
Bits per channel: 16
Clock cycles per pixel: 2
Number of data pairs: 3

Data Block 1

DOUT3	CH1[9]	CH1[10]	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]
DOUT2	CH1[2]	CH1[3]	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]
DOUT1	S0	S1	S2	S3	S4	CH1[0]	CH1[1]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT3	CH2[9]	CH2[10]	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]
DOUT2	CH2[2]	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]
DOUT1	S0	S1	S2	S3	S4	CH2[0]	CH2[1]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-23. LVDS Format 33

LVDS Format 39 is defined in Fig. 5-24.

Format ID: 39
Number of channels: 4
Bits per channel: 10
Clock cycles per pixel: 4
Number of data pairs: 2

Data Block 1

DOUT2	CH1[3]	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]
DOUT1	S0	S1	S2	S3	CH1[0]	CH1[1]	CH1[2]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT2	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]
DOUT1	S0	S1	S2	S3	CH2[0]	CH2[1]	CH2[2]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

DOUT2	CH3[3]	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]
DOUT1	S0	S1	S2	S3	CH3[0]	CH3[1]	CH3[2]
DCLKOUT	H	H	L	L	L	H	H

Data Block 4

DOUT2	CH4[3]	CH4[4]	CH4[5]	CH4[6]	CH4[7]	CH4[8]	CH4[9]
DOUT1	S0	S1	S2	S3	CH4[0]	CH4[1]	CH4[2]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-24. LVDS Format 39

LVDS Format 38 is defined in Fig. 5-25.

Format ID: 38
Number of channels: 3
Bits per channel: 10
Clock cycles per pixel: 3
Number of data pairs: 2

Data Block 1

DOUT2	CH1[3]	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]
DOUT1	S0	S1	S2	S3	CH1[0]	CH1[1]	CH1[2]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT2	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]
DOUT1	S0	S1	S2	S3	CH2[0]	CH2[1]	CH2[2]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

DOUT2	CH3[3]	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]
DOUT1	S0	S1	S2	S3	CH3[0]	CH3[1]	CH3[2]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-25. LVDS Format 38

LVDS Format 37 is defined in Fig. 5-26.

Format ID: 37
Number of channels: 2
Bits per channel: 10
Clock cycles per pixel: 2
Number of data pairs: 2

Data Block 1

DOUT2	CH1[3]	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]
DOUT1	S0	S1	S2	S3	CH1[0]	CH1[1]	CH1[2]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT2	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]
DOUT1	S0	S1	S2	S3	CH2[0]	CH2[1]	CH2[2]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-26. LVDS Format 37

LVDS Format 83 is defined in Fig. 5-27.

Format ID: 83
Number of channels: 6
Bits per channel: 16
Clock cycles per pixel: 3
Number of data pairs: 5

Data Block 1

DOUT5	CH2[9]	CH2[10]	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]
DOUT4	CH2[2]	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]
DOUT3	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]	CH2[0]	CH2[1]
DOUT2	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]
DOUT1	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT5	CH4[9]	CH4[10]	CH4[11]	CH4[12]	CH4[13]	CH4[14]	CH4[15]
DOUT4	CH4[2]	CH4[3]	CH4[4]	CH4[5]	CH4[6]	CH4[7]	CH4[8]
DOUT3	CH3[11]	CH3[12]	CH3[13]	CH3[14]	CH3[15]	CH4[0]	CH4[1]
DOUT2	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH3[10]
DOUT1	S0	S1	S2	CH3[0]	CH3[1]	CH3[2]	CH3[3]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

DOUT5	CH6[9]	CH6[10]	CH6[11]	CH6[12]	CH6[13]	CH6[14]	CH6[15]
DOUT4	CH6[2]	CH6[3]	CH6[4]	CH6[5]	CH6[6]	CH6[7]	CH6[8]
DOUT3	CH5[11]	CH5[12]	CH5[13]	CH5[14]	CH5[15]	CH6[0]	CH6[1]
DOUT2	CH5[4]	CH5[5]	CH5[6]	CH5[7]	CH5[8]	CH5[9]	CH5[10]
DOUT1	S0	S1	S2	CH5[0]	CH5[1]	CH5[2]	CH5[3]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-27. LVDS Format 83

LVDS Format 82 is defined in Fig. 5-28.

Format ID: 82
Number of channels: 4
Bits per channel: 16
Clock cycles per pixel: 2
Number of data pairs: 5

Data Block 1

DOUT5	CH2[9]	CH2[10]	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]
DOUT4	CH2[2]	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]
DOUT3	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]	CH2[0]	CH2[1]
DOUT2	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]
DOUT1	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT5	CH4[9]	CH4[10]	CH4[11]	CH4[12]	CH4[13]	CH4[14]	CH4[15]
DOUT4	CH4[2]	CH4[3]	CH4[4]	CH4[5]	CH4[6]	CH4[7]	CH4[8]
DOUT3	CH3[11]	CH3[12]	CH3[13]	CH3[14]	CH3[15]	CH4[0]	CH4[1]
DOUT2	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH3[10]
DOUT1	S0	S1	S2	CH3[0]	CH3[1]	CH3[2]	CH3[3]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-28. LVDS Format 82

LVDS Format 81 is defined in Fig. 5-29.

Format ID: 81
Number of channels: 3
Bits per channel: 16
Clock cycles per pixel: 1.5 (3 clock cycles per 2 pixels)
Number of data pairs: 5

Data Block 1

DOUT5	CH2[9]	CH2[10]	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]
DOUT4	CH2[2]	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]
DOUT3	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]	CH2[0]	CH2[1]
DOUT2	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]
DOUT1	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT5	CH1[9]	CH1[10]	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]
DOUT4	CH1[2]	CH1[3]	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]
DOUT3	CH3[11]	CH3[12]	CH3[13]	CH3[14]	CH3[15]	CH1[0]	CH1[1]
DOUT2	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]	CH3[9]	CH3[10]
DOUT1	S0	S1	S2	CH3[0]	CH3[1]	CH3[2]	CH3[3]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

DOUT5	CH3[9]	CH3[10]	CH3[11]	CH3[12]	CH3[13]	CH3[14]	CH3[15]
DOUT4	CH3[2]	CH3[3]	CH3[4]	CH3[5]	CH3[6]	CH3[7]	CH3[8]
DOUT3	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]	CH3[0]	CH3[1]
DOUT2	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]	CH2[9]	CH2[10]
DOUT1	S0	S1	S2	CH2[0]	CH2[1]	CH2[2]	CH2[3]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-29. LVDS Format 81

LVDS Format 80 is defined in Fig. 5-30.

Format ID: 80
Number of channels: 2
Bits per channel: 16
Clock cycles per pixel: 1
Number of data pairs: 5

DOUT5	CH2[9]	CH2[10]	CH2[11]	CH2[12]	CH2[13]	CH2[14]	CH2[15]
DOUT4	CH2[2]	CH2[3]	CH2[4]	CH2[5]	CH2[6]	CH2[7]	CH2[8]
DOUT3	CH1[11]	CH1[12]	CH1[13]	CH1[14]	CH1[15]	CH2[0]	CH2[1]
DOUT2	CH1[4]	CH1[5]	CH1[6]	CH1[7]	CH1[8]	CH1[9]	CH1[10]
DOUT1	S0	S1	S2	CH1[0]	CH1[1]	CH1[2]	CH1[3]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-30. LVDS Format 80

LVDS Format 43 is defined in Fig. 5-31.

Format ID: 43
Number of channels: 4
Bits per channel: 16
Clock cycles per pixel: 4
Number of data pairs: 3

Data Block 1

DOUT3	CH1[12]	CH1[11]	CH1[10]	CH1[9]	CH1[8]	CH1[7]	CH1[6]
DOUT2	CH1[3]	CH1[2]	CH1[1]	CH1[0]	CH1[15]	CH1[14]	CH1[13]
DOUT1	S0	S1	S2	S3	S4	CH1[5]	CH1[4]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT3	CH2[12]	CH2[11]	CH2[10]	CH2[9]	CH2[8]	CH2[7]	CH2[6]
DOUT2	CH2[3]	CH2[2]	CH2[1]	CH2[0]	CH2[15]	CH2[14]	CH2[13]
DOUT1	S0	S1	S2	S3	S4	CH2[5]	CH2[4]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

DOUT3	CH3[12]	CH3[11]	CH3[10]	CH3[9]	CH3[8]	CH3[7]	CH3[6]
DOUT2	CH3[3]	CH3[2]	CH3[1]	CH3[0]	CH3[15]	CH3[14]	CH3[13]
DOUT1	S0	S1	S2	S3	S4	CH3[5]	CH3[4]
DCLKOUT	H	H	L	L	L	H	H

Data Block 4

DOUT3	CH4[12]	CH4[11]	CH4[10]	CH4[9]	CH4[8]	CH4[7]	CH4[6]
DOUT2	CH4[3]	CH4[2]	CH4[1]	CH4[0]	CH4[15]	CH4[14]	CH4[13]
DOUT1	S0	S1	S2	S3	S4	CH4[5]	CH4[4]
DCLKOUT	H	H	L	L	L	H	H

Figure 5-31. LVDS Format 43

LVDS Format 42 is defined in Fig. 5-32.

Format ID: 42
Number of channels: 3
Bits per channel: 16
Clock cycles per pixel: 3
Number of data pairs: 3

DOUT3	CH1[12]	CH1[11]	CH1[10]	CH1[9]	CH1[8]	CH1[7]	CH1[6]
DOUT2	CH1[3]	CH1[2]	CH1[1]	CH1[0]	CH1[15]	CH1[14]	CH1[13]
DOUT1	S0	S1	S2	S3	S4	CH1[5]	CH1[4]
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT3	CH2[12]	CH2[11]	CH2[10]	CH2[9]	CH2[8]	CH2[7]	CH2[6]
DOUT2	CH2[3]	CH2[2]	CH2[1]	CH2[0]	CH2[15]	CH2[14]	CH2[13]
DOUT1	S0	S1	S2	S3	S4	CH2[5]	CH2[4]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

DOUT3	CH3[12]	CH3[11]	CH3[10]	CH3[9]	CH3[8]	CH3[7]	CH3[6]
DOUT2	CH3[3]	CH3[2]	CH3[1]	CH3[0]	CH3[15]	CH3[14]	CH3[13]
DOUT1	S0	S1	S2	S3	S4	CH3[5]	CH3[4]
DCLKOUT	H	H	L	L	L	H	H

Data Block 3

Figure 5-32. LVDS Format 42

LVDS Format 41 is defined in Fig. 5-33.

Format ID: 41
Number of channels: 2
Bits per channel: 16
Clock cycles per pixel: 2
Number of data pairs: 3

DOUT3	CH1[12]	CH1[11]	CH1[10]	CH1[9]	CH1[8]	CH1[7]	CH1[6]
DOUT2	CH1[3]	CH1[2]	CH1[1]	CH1[0]	CH1[15]	CH1[14]	CH1[13]
DOUT1	S0	S1	S2	S3	S4	CH1[5]	CH1[4]
DCLKOUT	H	H	L	L	L	H	H

Data Block 1

DOUT3	CH2[12]	CH2[11]	CH2[10]	CH2[9]	CH2[8]	CH2[7]	CH2[6]
DOUT2	CH2[3]	CH2[2]	CH2[1]	CH2[0]	CH2[15]	CH2[14]	CH2[13]
DOUT1	S0	S1	S2	S3	S4	CH2[5]	CH2[4]
DCLKOUT	H	H	L	L	L	H	H

Data Block 2

Figure 5-33. LVDS Format 41

5.1.2 CMOS (TG) Output Format

The CMOS (TG) output formats are defined in this section. See Section 4.5 for details of the CS82L46 output formats.

CMOS (TG) Format 75 is defined in Fig. 5-34.

Format ID: 75
Number of channels: 6
Bits per channel: 10
Clock cycles per pixel: 6
Number of data lines: 10

<table>
<tr><td>DOUT10</td><td colspan="2">CH1[9]</td><td colspan="2">CH2[9]</td><td colspan="2">CH3[9]</td><td colspan="2">CH4[9]</td><td colspan="2">CH5[9]</td><td colspan="2">CH6[9]</td></tr>
<tr><td>DOUT9</td><td colspan="2">CH1[8]</td><td colspan="2">CH2[8]</td><td colspan="2">CH3[8]</td><td colspan="2">CH4[8]</td><td colspan="2">CH5[8]</td><td colspan="2">CH6[8]</td></tr>
<tr><td>DOUT8</td><td colspan="2">CH1[7]</td><td colspan="2">CH2[7]</td><td colspan="2">CH3[7]</td><td colspan="2">CH4[7]</td><td colspan="2">CH5[7]</td><td colspan="2">CH6[7]</td></tr>
<tr><td>DOUT7</td><td colspan="2">CH1[6]</td><td colspan="2">CH2[6]</td><td colspan="2">CH3[6]</td><td colspan="2">CH4[6]</td><td colspan="2">CH5[6]</td><td colspan="2">CH6[6]</td></tr>
<tr><td>DOUT6</td><td colspan="2">CH1[5]</td><td colspan="2">CH2[5]</td><td colspan="2">CH3[5]</td><td colspan="2">CH4[5]</td><td colspan="2">CH5[5]</td><td colspan="2">CH6[5]</td></tr>
<tr><td>DOUT5</td><td colspan="2">CH1[4]</td><td colspan="2">CH2[4]</td><td colspan="2">CH3[4]</td><td colspan="2">CH4[4]</td><td colspan="2">CH5[4]</td><td colspan="2">CH6[4]</td></tr>
<tr><td>DOUT4</td><td colspan="2">CH1[3]</td><td colspan="2">CH2[3]</td><td colspan="2">CH3[3]</td><td colspan="2">CH4[3]</td><td colspan="2">CH5[3]</td><td colspan="2">CH6[3]</td></tr>
<tr><td>DOUT3</td><td colspan="2">CH1[2]</td><td colspan="2">CH2[2]</td><td colspan="2">CH3[2]</td><td colspan="2">CH4[2]</td><td colspan="2">CH5[2]</td><td colspan="2">CH6[2]</td></tr>
<tr><td>DOUT2</td><td colspan="2">CH1[1]</td><td colspan="2">CH2[1]</td><td colspan="2">CH3[1]</td><td colspan="2">CH4[1]</td><td colspan="2">CH5[1]</td><td colspan="2">CH6[1]</td></tr>
<tr><td>DOUT1</td><td colspan="2">CH1[0]</td><td colspan="2">CH2[0]</td><td colspan="2">CH3[0]</td><td colspan="2">CH4[0]</td><td colspan="2">CH5[0]</td><td colspan="2">CH6[0]</td></tr>
<tr><td>DCLKOUT1</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td></tr>
<tr><td>DCLKOUT2</td><td colspan="2">S0</td><td colspan="2">S0</td><td colspan="2">S0</td><td colspan="2">S0</td><td colspan="2">S0</td><td colspan="2">S0</td></tr>
</table>

Figure 5-34. CMOS (TG) Format 75

CMOS (TG) Format 74 is defined in Fig. 5-35.

Format ID: 74
Number of channels: 4
Bits per channel: 10
Clock cycles per pixel: 4
Number of data lines: 10

DOUT10	CH1[9]		CH2[9]		CH3[9]		CH4[9]	
DOUT9	CH1[8]		CH2[8]		CH3[8]		CH4[8]	
DOUT8	CH1[7]		CH2[7]		CH3[7]		CH4[7]	
DOUT7	CH1[6]		CH2[6]		CH3[6]		CH4[6]	
DOUT6	CH1[5]		CH2[5]		CH3[5]		CH4[5]	
DOUT5	CH1[4]		CH2[4]		CH3[4]		CH4[4]	
DOUT4	CH1[3]		CH2[3]		CH3[3]		CH4[3]	
DOUT3	CH1[2]		CH2[2]		CH3[2]		CH4[2]	
DOUT2	CH1[1]		CH2[1]		CH3[1]		CH4[1]	
DOUT1	CH1[0]		CH2[0]		CH3[0]		CH4[0]	
DCLKOUT1	H	L	H	L	H	L	H	L
DCLKOUT2	S0		S0		S0		S0	

Figure 5-35. CMOS (TG) Format 74

CMOS (TG) Format 73 is defined in Fig. 5-36.

Format ID: 73
Number of channels: 3
Bits per channel: 10
Clock cycles per pixel: 3
Number of data lines: 10

DOUT10	CH1[9]		CH2[9]		CH3[9]	
DOUT9	CH1[8]		CH2[8]		CH3[8]	
DOUT8	CH1[7]		CH2[7]		CH3[7]	
DOUT7	CH1[6]		CH2[6]		CH3[6]	
DOUT6	CH1[5]		CH2[5]		CH3[5]	
DOUT5	CH1[4]		CH2[4]		CH3[4]	
DOUT4	CH1[3]		CH2[3]		CH3[3]	
DOUT3	CH1[2]		CH2[2]		CH3[2]	
DOUT2	CH1[1]		CH2[1]		CH3[1]	
DOUT1	CH1[0]		CH2[0]		CH3[0]	
DCLKOUT1	H	L	H	L	H	L
DCLKOUT2	S0		S0		S0	

Figure 5-36. CMOS (TG) Format 73

CMOS (TG) Format 72 is defined in Fig. 5-37.

Format ID: 72
Number of channels: 2
Bits per channel: 10
Clock cycles per pixel: 2
Number of data lines: 10

DOUT10	CH1[9]		CH2[9]	
DOUT9	CH1[8]		CH2[8]	
DOUT8	CH1[7]		CH2[7]	
DOUT7	CH1[6]		CH2[6]	
DOUT6	CH1[5]		CH2[5]	
DOUT5	CH1[4]		CH2[4]	
DOUT4	CH1[3]		CH2[3]	
DOUT3	CH1[2]		CH2[2]	
DOUT2	CH1[1]		CH2[1]	
DOUT1	CH1[0]		CH2[0]	
DCLKOUT1	H	L	H	L
DCLKOUT2	S0		S0	

Figure 5-37. CMOS (TG) Format 72

CMOS (TG) Format 24 is defined in Fig. 5-38.

Format ID: 24
Number of channels: 6
Bits per channel: 12
Clock cycles per pixel: 12
Number of data lines: 6

Note: This format is only supported in Clocking Mode 1 or Clocking Mode 2 (see Section 4.3).

DOUT6	CH1[11]	CH1[5]	CH2[11]	CH2[5]	CH3[11]	CH3[5]	CH4[11]	CH4[5]	CH5[11]	CH5[5]	CH6[11]	CH6[5]
DOUT5	CH1[10]	CH1[4]	CH2[10]	CH2[4]	CH3[10]	CH3[4]	CH4[10]	CH4[4]	CH5[10]	CH5[4]	CH6[10]	CH6[4]
DOUT4	CH1[9]	CH1[3]	CH2[9]	CH2[3]	CH3[9]	CH3[3]	CH4[9]	CH4[3]	CH5[9]	CH5[3]	CH6[9]	CH6[3]
DOUT3	CH1[8]	CH1[2]	CH2[8]	CH2[2]	CH3[8]	CH3[2]	CH4[8]	CH4[2]	CH5[8]	CH5[2]	CH6[8]	CH6[2]
DOUT2	CH1[7]	CH1[1]	CH2[7]	CH2[1]	CH3[7]	CH3[1]	CH4[7]	CH4[1]	CH5[7]	CH5[1]	CH6[7]	CH6[1]
DOUT1	CH1[6]	CH1[0]	CH2[6]	CH2[0]	CH3[6]	CH3[0]	CH4[6]	CH4[0]	CH5[6]	CH5[0]	CH6[6]	CH6[0]
DCLKOUT1	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L
DCLKOUT2	S0	S0	S0	S0	S0	S0	S0	S0	S0	S0	S0	S0

Figure 5-38. CMOS (TG) Format 24

CMOS (TG) Format 23 is defined in Fig. 5-39.

Format ID: 23
Number of channels: 4
Bits per channel: 12
Clock cycles per pixel: 8
Number of data lines: 6

Note: This format is only supported in Clocking Mode 1 or Clocking Mode 2 (see Section 4.3).

DOUT6	CH1[11]	CH1[5]	CH2[11]	CH2[5]	CH3[11]	CH3[5]	CH4[11]	CH4[5]
DOUT5	CH1[10]	CH1[4]	CH2[10]	CH2[4]	CH3[10]	CH3[4]	CH4[10]	CH4[4]
DOUT4	CH1[9]	CH1[3]	CH2[9]	CH2[3]	CH3[9]	CH3[3]	CH4[9]	CH4[3]
DOUT3	CH1[8]	CH1[2]	CH2[8]	CH2[2]	CH3[8]	CH3[2]	CH4[8]	CH4[2]
DOUT2	CH1[7]	CH1[1]	CH2[7]	CH2[1]	CH3[7]	CH3[1]	CH4[7]	CH4[1]
DOUT1	CH1[6]	CH1[0]	CH2[6]	CH2[0]	CH3[6]	CH3[0]	CH4[6]	CH4[0]
DCLKOUT1	H L	H L	H L	H L	H L	H L	H L	H L
DCLKOUT2	S0	S0	S0	S0	S0	S0	S0	S0

Figure 5-39. CMOS (TG) Format 23

CMOS (TG) Format 22 is defined in Fig. 5-40.

Format ID: 22
Number of channels: 3
Bits per channel: 12
Clock cycles per pixel: 6
Number of data lines: 6

DOUT6	CH1[11]	CH1[5]	CH2[11]	CH2[5]	CH3[11]	CH3[5]
DOUT5	CH1[10]	CH1[4]	CH2[10]	CH2[4]	CH3[10]	CH3[4]
DOUT4	CH1[9]	CH1[3]	CH2[9]	CH2[3]	CH3[9]	CH3[3]
DOUT3	CH1[8]	CH1[2]	CH2[8]	CH2[2]	CH3[8]	CH3[2]
DOUT2	CH1[7]	CH1[1]	CH2[7]	CH2[1]	CH3[7]	CH3[1]
DOUT1	CH1[6]	CH1[0]	CH2[6]	CH2[0]	CH3[6]	CH3[0]
DCLKOUT1	H L	H L	H L	H L	H L	H L
DCLKOUT2	S0	S0	S0	S0	S0	S0

Figure 5-40. CMOS (TG) Format 22

CMOS (TG) Format 21 is defined in Fig. 5-41.

Format ID: 21
Number of channels: 2
Bits per channel: 12
Clock cycles per pixel: 4
Number of data lines: 6

DOUT6	CH1[11]	CH1[5]	CH2[11]	CH2[5]
DOUT5	CH1[10]	CH1[4]	CH2[10]	CH2[4]
DOUT4	CH1[9]	CH1[3]	CH2[9]	CH2[3]
DOUT3	CH1[8]	CH1[2]	CH2[8]	CH2[2]
DOUT2	CH1[7]	CH1[1]	CH2[7]	CH2[1]
DOUT1	CH1[6]	CH1[0]	CH2[6]	CH2[0]
DCLKOUT1	H L	H L	H L	H L
DCLKOUT2	S0	S0	S0	S0

Figure 5-41. CMOS (TG) Format 21

5.1.3 CMOS (External) Output Format

The CMOS (External) output formats are defined in this section. See Section 4.5 for details of the CS82L46 output formats.

CMOS (External) Format 4 is defined in Fig. 5-42.

Format ID: 4
Number of channels: 6
Bits per channel: 16
Clock cycles per pixel: 6
Number of data lines: 8

DOUT8	CH1[15]	CH1[7]	CH2[15]	CH2[7]	CH3[15]	CH3[7]	CH4[15]	CH4[7]	CH5[15]	CH5[7]	CH6[15]	CH6[7]
DOUT7	CH1[14]	CH1[6]	CH2[14]	CH2[6]	CH3[14]	CH3[6]	CH4[14]	CH4[6]	CH5[14]	CH5[6]	CH6[14]	CH6[6]
DOUT6	CH1[13]	CH1[5]	CH2[13]	CH2[5]	CH3[13]	CH3[5]	CH4[13]	CH4[5]	CH5[13]	CH5[5]	CH6[13]	CH6[5]
DOUT5	CH1[12]	CH1[4]	CH2[12]	CH2[4]	CH3[12]	CH3[4]	CH4[12]	CH4[4]	CH5[12]	CH5[4]	CH6[12]	CH6[4]
DOUT4	CH1[11]	CH1[3]	CH2[11]	CH2[3]	CH3[11]	CH3[3]	CH4[11]	CH4[3]	CH5[11]	CH5[3]	CH6[11]	CH6[3]
DOUT3	CH1[10]	CH1[2]	CH2[10]	CH2[2]	CH3[10]	CH3[2]	CH4[10]	CH4[2]	CH5[10]	CH5[2]	CH6[10]	CH6[2]
DOUT2	CH1[9]	CH1[1]	CH2[9]	CH2[1]	CH3[9]	CH3[1]	CH4[9]	CH4[1]	CH5[9]	CH5[1]	CH6[9]	CH6[1]
DOUT1	CH1[8]	CH1[0]	CH2[8]	CH2[0]	CH3[8]	CH3[0]	CH4[8]	CH4[0]	CH5[8]	CH5[0]	CH6[8]	CH6[0]
MCLK	H	L	H	L	H	L	H	L	H	L	H	L

Figure 5-42. CMOS (External) Format 4

CMOS (External) Format 3 is defined in Fig. 5-43.

Format ID: 3
Number of channels: 4
Bits per channel: 16
Clock cycles per pixel: 4
Number of data lines: 8

DOUT8	CH1[15]	CH1[7]	CH2[15]	CH2[7]	CH3[15]	CH3[7]	CH4[15]	CH4[7]
DOUT7	CH1[14]	CH1[6]	CH2[14]	CH2[6]	CH3[14]	CH3[6]	CH4[14]	CH4[6]
DOUT6	CH1[13]	CH1[5]	CH2[13]	CH2[5]	CH3[13]	CH3[5]	CH4[13]	CH4[5]
DOUT5	CH1[12]	CH1[4]	CH2[12]	CH2[4]	CH3[12]	CH3[4]	CH4[12]	CH4[4]
DOUT4	CH1[11]	CH1[3]	CH2[11]	CH2[3]	CH3[11]	CH3[3]	CH4[11]	CH4[3]
DOUT3	CH1[10]	CH1[2]	CH2[10]	CH2[2]	CH3[10]	CH3[2]	CH4[10]	CH4[2]
DOUT2	CH1[9]	CH1[1]	CH2[9]	CH2[1]	CH3[9]	CH3[1]	CH4[9]	CH4[1]
DOUT1	CH1[8]	CH1[0]	CH2[8]	CH2[0]	CH3[8]	CH3[0]	CH4[8]	CH4[0]
MCLK	H	L	H	L	H	L	H	L

Figure 5-43. CMOS (External) Format 3

CMOS (External) Format 2 is defined in Fig. 5-44.

Format ID: 2
Number of channels: 3
Bits per channel: 16
Clock cycles per pixel: 3
Number of data lines: 8

DOUT8	CH1[15]	CH1[7]	CH2[15]	CH2[7]	CH3[15]	CH3[7]
DOUT7	CH1[14]	CH1[6]	CH2[14]	CH2[6]	CH3[14]	CH3[6]
DOUT6	CH1[13]	CH1[5]	CH2[13]	CH2[5]	CH3[13]	CH3[5]
DOUT5	CH1[12]	CH1[4]	CH2[12]	CH2[4]	CH3[12]	CH3[4]
DOUT4	CH1[11]	CH1[3]	CH2[11]	CH2[3]	CH3[11]	CH3[3]
DOUT3	CH1[10]	CH1[2]	CH2[10]	CH2[2]	CH3[10]	CH3[2]
DOUT2	CH1[9]	CH1[1]	CH2[9]	CH2[1]	CH3[9]	CH3[1]
DOUT1	CH1[8]	CH1[0]	CH2[8]	CH2[0]	CH3[8]	CH3[0]
MCLK	H	L	H	L	H	L

Figure 5-44. CMOS (External) Format 2

CMOS (External) Format 1 is defined in Fig. 5-45.

Format ID: 1
Number of channels: 2
Bits per channel: 16
Clock cycles per pixel: 2
Number of data lines: 8

DOUT8	CH1[15]	CH1[7]	CH2[15]	CH2[7]
DOUT7	CH1[14]	CH1[6]	CH2[14]	CH2[6]
DOUT6	CH1[13]	CH1[5]	CH2[13]	CH2[5]
DOUT5	CH1[12]	CH1[4]	CH2[12]	CH2[4]
DOUT4	CH1[11]	CH1[3]	CH2[11]	CH2[3]
DOUT3	CH1[10]	CH1[2]	CH2[10]	CH2[2]
DOUT2	CH1[9]	CH1[1]	CH2[9]	CH2[1]
DOUT1	CH1[8]	CH1[0]	CH2[8]	CH2[0]
MCLK	H	L	H	L

Figure 5-45. CMOS (External) Format 1

CMOS (External) Format 15 is defined in Fig. 5-46.

Format ID: 15
Number of channels: 4
Bits per channel: 16
Clock cycles per pixel: 8
Number of data lines: 4

DOUT8	CH1[15]	CH1[11]	CH1[7]	CH1[3]	CH2[15]	CH2[11]	CH2[7]	CH2[3]	CH3[15]	CH3[11]	CH3[7]	CH3[3]	CH4[15]	CH4[11]	CH4[7]	CH4[3]
DOUT7	CH1[14]	CH1[10]	CH1[6]	CH1[2]	CH2[14]	CH2[10]	CH2[6]	CH2[2]	CH3[14]	CH3[10]	CH3[6]	CH3[2]	CH4[14]	CH4[10]	CH4[6]	CH4[2]
DOUT6	CH1[13]	CH1[9]	CH1[5]	CH1[1]	CH2[13]	CH2[9]	CH2[5]	CH2[1]	CH3[13]	CH3[9]	CH3[5]	CH3[1]	CH4[13]	CH4[9]	CH4[5]	CH4[1]
DOUT5	CH1[12]	CH1[8]	CH1[4]	CH1[0]	CH2[12]	CH2[8]	CH2[4]	CH2[0]	CH3[12]	CH3[8]	CH3[4]	CH3[0]	CH4[12]	CH4[8]	CH4[4]	CH4[0]
MCLK	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L

Figure 5-46. CMOS (External) Format 15

CMOS (External) Format 14 is defined in Fig. 5-47.

Format ID: 14
Number of channels: 3
Bits per channel: 16
Clock cycles per pixel: 6
Number of data lines: 4

DOUT8	CH1[15]	CH1[11]	CH1[7]	CH1[3]	CH2[15]	CH2[11]	CH2[7]	CH2[3]	CH3[15]	CH3[11]	CH3[7]	CH3[3]
DOUT7	CH1[14]	CH1[10]	CH1[6]	CH1[2]	CH2[14]	CH2[10]	CH2[6]	CH2[2]	CH3[14]	CH3[10]	CH3[6]	CH3[2]
DOUT6	CH1[13]	CH1[9]	CH1[5]	CH1[1]	CH2[13]	CH2[9]	CH2[5]	CH2[1]	CH3[13]	CH3[9]	CH3[5]	CH3[1]
DOUT5	CH1[12]	CH1[8]	CH1[4]	CH1[0]	CH2[12]	CH2[8]	CH2[4]	CH2[0]	CH3[12]	CH3[8]	CH3[4]	CH3[0]
MCLK	H	L	H	L	H	L	H	L	H	L	H	L

Figure 5-47. CMOS (External) Format 14

CMOS (External) Format 13 is defined in Fig. 5-48.

Format ID: 13
Number of channels: 2
Bits per channel: 16
Clock cycles per pixel: 4
Number of data lines: 4

DOUT8	CH1[15]	CH1[11]	CH1[7]	CH1[3]	CH2[15]	CH2[11]	CH2[7]	CH2[3]
DOUT7	CH1[14]	CH1[10]	CH1[6]	CH1[2]	CH2[14]	CH2[10]	CH2[6]	CH2[2]
DOUT6	CH1[13]	CH1[9]	CH1[5]	CH1[1]	CH2[13]	CH2[9]	CH2[5]	CH2[1]
DOUT5	CH1[12]	CH1[8]	CH1[4]	CH1[0]	CH2[12]	CH2[8]	CH2[4]	CH2[0]
MCLK	H	L	H	L	H	L	H	L

Figure 5-48. CMOS (External) Format 13

CMOS (External) Format 20 is defined in Fig. 5-49.

Format ID: 20
Number of channels: 6
Bits per channel: 16
Clock cycles per pixel: 6
Number of data lines: 8

DOUT8	CH1[15]	CH1[11]	CH1[7]	CH1[3]	CH2[15]	CH2[11]	CH2[7]	CH2[3]	CH3[15]	CH3[11]	CH3[7]	CH3[3]
DOUT7	CH1[14]	CH1[10]	CH1[6]	CH1[2]	CH2[14]	CH2[10]	CH2[6]	CH2[2]	CH3[14]	CH3[10]	CH3[6]	CH3[2]
DOUT6	CH1[13]	CH1[9]	CH1[5]	CH1[1]	CH2[13]	CH2[9]	CH2[5]	CH2[1]	CH3[13]	CH3[9]	CH3[5]	CH3[1]
DOUT5	CH1[12]	CH1[8]	CH1[4]	CH1[0]	CH2[12]	CH2[8]	CH2[4]	CH2[0]	CH3[12]	CH3[8]	CH3[4]	CH3[0]
DOUT4	CH4[15]	CH4[11]	CH4[7]	CH4[3]	CH5[15]	CH5[11]	CH5[7]	CH5[3]	CH6[15]	CH6[11]	CH6[7]	CH6[3]
DOUT3	CH4[14]	CH4[10]	CH4[6]	CH4[2]	CH5[14]	CH5[10]	CH5[6]	CH5[2]	CH6[14]	CH6[10]	CH6[6]	CH6[2]
DOUT2	CH4[13]	CH4[9]	CH4[5]	CH4[1]	CH5[13]	CH5[9]	CH5[5]	CH5[1]	CH6[13]	CH6[9]	CH6[5]	CH6[1]
DOUT1	CH4[12]	CH4[8]	CH4[4]	CH4[0]	CH5[12]	CH5[8]	CH5[4]	CH5[0]	CH6[12]	CH6[8]	CH6[4]	CH6[0]
MCLK	H	L	H	L	H	L	H	L	H	L	H	L

Figure 5-49. CMOS (External) Format 20

CMOS (External) Format 19 is defined in Fig. 5-50.

Format ID: 19
Number of channels: 4
Bits per channel: 16
Clock cycles per pixel: 4
Number of data lines: 8

DOUT8	CH1[15]	CH1[11]	CH1[7]	CH1[3]	CH2[15]	CH2[11]	CH2[7]	CH2[3]
DOUT7	CH1[14]	CH1[10]	CH1[6]	CH1[2]	CH2[14]	CH2[10]	CH2[6]	CH2[2]
DOUT6	CH1[13]	CH1[9]	CH1[5]	CH1[1]	CH2[13]	CH2[9]	CH2[5]	CH2[1]
DOUT5	CH1[12]	CH1[8]	CH1[4]	CH1[0]	CH2[12]	CH2[8]	CH2[4]	CH2[0]
DOUT4	CH3[15]	CH3[11]	CH3[7]	CH3[3]	CH4[15]	CH4[11]	CH4[7]	CH4[3]
DOUT3	CH3[14]	CH3[10]	CH3[6]	CH3[2]	CH4[14]	CH4[10]	CH4[6]	CH4[2]
DOUT2	CH3[13]	CH3[9]	CH3[5]	CH3[1]	CH4[13]	CH4[9]	CH4[5]	CH4[1]
DOUT1	CH3[12]	CH3[8]	CH3[4]	CH3[0]	CH4[12]	CH4[8]	CH4[4]	CH4[0]
MCLK	H	L	H	L	H	L	H	L

Figure 5-50. CMOS (External) Format 19

CMOS (External) Format 17 is defined in Fig. 5-51.

Format ID: 17
Number of channels: 2
Bits per channel: 16
Clock cycles per pixel: 2
Number of data lines: 8

DOUT8	CH1[15]	CH1[11]	CH1[7]	CH1[3]
DOUT7	CH1[14]	CH1[10]	CH1[6]	CH1[2]
DOUT6	CH1[13]	CH1[9]	CH1[5]	CH1[1]
DOUT5	CH1[12]	CH1[8]	CH1[4]	CH1[0]
DOUT4	CH2[15]	CH2[11]	CH2[7]	CH2[3]
DOUT3	CH2[14]	CH2[10]	CH2[6]	CH2[2]
DOUT2	CH2[13]	CH2[9]	CH2[5]	CH2[1]
DOUT1	CH2[12]	CH2[8]	CH2[4]	CH2[0]
MCLK	H	L	H	L

Figure 5-51. CMOS (External) Format 17

CMOS (External) Format 65 is defined in Fig. 5-52.

Format ID: 65
Number of channels: 6
Bits per channel: 10
Clock cycles per pixel: 3
Number of data lines: 10

DOUT10	CH1[9]	CH1[4]	CH2[9]	CH2[4]	CH3[9]	CH3[4]
DOUT9	CH1[8]	CH1[3]	CH2[8]	CH2[3]	CH3[8]	CH3[3]
DOUT8	CH1[7]	CH1[2]	CH2[7]	CH2[2]	CH3[7]	CH3[2]
DOUT7	CH1[6]	CH1[1]	CH2[6]	CH2[1]	CH3[6]	CH3[1]
DOUT6	CH1[5]	CH1[0]	CH2[5]	CH2[0]	CH3[5]	CH3[0]
DOUT5	CH4[9]	CH4[4]	CH5[9]	CH5[4]	CH6[9]	CH6[4]
DOUT4	CH4[8]	CH4[3]	CH5[8]	CH5[3]	CH6[8]	CH6[3]
DOUT3	CH4[7]	CH4[2]	CH5[7]	CH5[2]	CH6[7]	CH6[2]
DOUT2	CH4[6]	CH4[1]	CH5[6]	CH5[1]	CH6[6]	CH6[1]
DOUT1	CH4[5]	CH4[0]	CH5[5]	CH5[0]	CH6[5]	CH6[0]
MCLK	H	L	H	L	H	L

Figure 5-52. CMOS (External) Format 65

CMOS (External) Format 64 is defined in Fig. 5-53.

Format ID: 64
Number of channels: 4
Bits per channel: 10
Clock cycles per pixel: 2
Number of data lines: 10

DOUT10	CH1[9]	CH1[4]	CH2[9]	CH2[4]
DOUT9	CH1[8]	CH1[3]	CH2[8]	CH2[3]
DOUT8	CH1[7]	CH1[2]	CH2[7]	CH2[2]
DOUT7	CH1[6]	CH1[1]	CH2[6]	CH2[1]
DOUT6	CH1[5]	CH1[0]	CH2[5]	CH2[0]
DOUT5	CH3[9]	CH3[4]	CH4[9]	CH4[4]
DOUT4	CH3[8]	CH3[3]	CH4[8]	CH4[3]
DOUT3	CH3[7]	CH3[2]	CH4[7]	CH4[2]
DOUT2	CH3[6]	CH3[1]	CH4[6]	CH4[1]
DOUT1	CH3[5]	CH3[0]	CH4[5]	CH4[0]
MCLK	H	L	H	L

Figure 5-53. CMOS (External) Format 64

CMOS (External) Format 8 is defined in Fig. 5-54.

Format ID: 8
Number of channels: 6
Bits per channel: 8
Clock cycles per pixel: 6
Number of data lines: 8

DOUT8	CH1[7]	CH2[7]	CH3[7]	CH4[7]	CH5[7]	CH6[7]
DOUT7	CH1[6]	CH2[6]	CH3[6]	CH4[6]	CH5[6]	CH6[6]
DOUT6	CH1[5]	CH2[5]	CH3[5]	CH4[5]	CH5[5]	CH6[5]
DOUT5	CH1[4]	CH2[4]	CH3[4]	CH4[4]	CH5[4]	CH6[4]
DOUT4	CH1[3]	CH2[3]	CH3[3]	CH4[3]	CH5[3]	CH6[3]
DOUT3	CH1[2]	CH2[2]	CH3[2]	CH4[2]	CH5[2]	CH6[2]
DOUT2	CH1[1]	CH2[1]	CH3[1]	CH4[1]	CH5[1]	CH6[1]
DOUT1	CH1[0]	CH2[0]	CH3[0]	CH4[0]	CH5[0]	CH6[0]
MCLK	H L	H L	H L	H L	H L	H L

Figure 5-54. CMOS (External) Format 8

CMOS (External) Format 7 is defined in Fig. 5-55.

Format ID: 7
Number of channels: 4
Bits per channel: 8
Clock cycles per pixel: 4
Number of data lines: 8

DOUT8	CH1[7]	CH2[7]	CH3[7]	CH4[7]
DOUT7	CH1[6]	CH2[6]	CH3[6]	CH4[6]
DOUT6	CH1[5]	CH2[5]	CH3[5]	CH4[5]
DOUT5	CH1[4]	CH2[4]	CH3[4]	CH4[4]
DOUT4	CH1[3]	CH2[3]	CH3[3]	CH4[3]
DOUT3	CH1[2]	CH2[2]	CH3[2]	CH4[2]
DOUT2	CH1[1]	CH2[1]	CH3[1]	CH4[1]
DOUT1	CH1[0]	CH2[0]	CH3[0]	CH4[0]
MCLK	H L	H L	H L	H L

Figure 5-55. CMOS (External) Format 7

CMOS (External) Format 6 is defined in Fig. 5-56.

Format ID: 6
Number of channels: 3
Bits per channel: 8
Clock cycles per pixel: 3
Number of data lines: 8

DOUT8	CH1[7]	CH2[7]	CH3[7]
DOUT7	CH1[6]	CH2[6]	CH3[6]
DOUT6	CH1[5]	CH2[5]	CH3[5]
DOUT5	CH1[4]	CH2[4]	CH3[4]
DOUT4	CH1[3]	CH2[3]	CH3[3]
DOUT3	CH1[2]	CH2[2]	CH3[2]
DOUT2	CH1[1]	CH2[1]	CH3[1]
DOUT1	CH1[0]	CH2[0]	CH3[0]
MCLK	H L	H L	H L

Figure 5-56. CMOS (External) Format 6

CMOS (External) Format 5 is defined in Fig. 5-57.

Format ID: 5
Number of channels: 2
Bits per channel: 8
Clock cycles per pixel: 2
Number of data lines: 8

DOUT8	CH1[7]	CH2[7]
DOUT7	CH1[6]	CH2[6]
DOUT6	CH1[5]	CH2[5]
DOUT5	CH1[4]	CH2[4]
DOUT4	CH1[3]	CH2[3]
DOUT3	CH1[2]	CH2[2]
DOUT2	CH1[1]	CH2[1]
DOUT1	CH1[0]	CH2[0]
MCLK	H L	H L

Figure 5-57. CMOS (External) Format 5

CMOS (External) Format 12 is defined in Fig. 5-58.

Format ID: 12
Number of channels: 6
Bits per channel: 16
Clock cycles per pixel: 12
Number of data lines: 8

DOUT8	CH1[15]	CH1[7]	CH2[15]	CH2[7]	CH3[15]	CH3[7]	CH4[15]	CH4[7]	CH5[15]	CH5[7]	CH6[15]	CH6[7]
DOUT7	CH1[14]	CH1[6]	CH2[14]	CH2[6]	CH3[14]	CH3[6]	CH4[14]	CH4[6]	CH5[14]	CH5[6]	CH6[14]	CH6[6]
DOUT6	CH1[13]	CH1[5]	CH2[13]	CH2[5]	CH3[13]	CH3[5]	CH4[13]	CH4[5]	CH5[13]	CH5[5]	CH6[13]	CH6[5]
DOUT5	CH1[12]	CH1[4]	CH2[12]	CH2[4]	CH3[12]	CH3[4]	CH4[12]	CH4[4]	CH5[12]	CH5[4]	CH6[12]	CH6[4]
DOUT4	CH1[11]	CH1[3]	CH2[11]	CH2[3]	CH3[11]	CH3[3]	CH4[11]	CH4[3]	CH5[11]	CH5[3]	CH6[11]	CH6[3]
DOUT3	CH1[10]	CH1[2]	CH2[10]	CH2[2]	CH3[10]	CH3[2]	CH4[10]	CH4[2]	CH5[10]	CH5[2]	CH6[10]	CH6[2]
DOUT2	CH1[9]	CH1[1]	CH2[9]	CH2[1]	CH3[9]	CH3[1]	CH4[9]	CH4[1]	CH5[9]	CH5[1]	CH6[9]	CH6[1]
DOUT1	CH1[8]	CH1[0]	CH2[8]	CH2[0]	CH3[8]	CH3[0]	CH4[8]	CH4[0]	CH5[8]	CH5[0]	CH6[8]	CH6[0]
MCLK	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L

Figure 5-58. CMOS (External) Format 12

CMOS (External) Format 11 is defined in Fig. 5-59.

Format ID: 11
Number of channels: 4
Bits per channel: 16
Clock cycles per pixel: 8
Number of data lines: 8

DOUT8	CH1[15]	CH1[7]	CH2[15]	CH2[7]	CH3[15]	CH3[7]	CH4[15]	CH4[7]
DOUT7	CH1[14]	CH1[6]	CH2[14]	CH2[6]	CH3[14]	CH3[6]	CH4[14]	CH4[6]
DOUT6	CH1[13]	CH1[5]	CH2[13]	CH2[5]	CH3[13]	CH3[5]	CH4[13]	CH4[5]
DOUT5	CH1[12]	CH1[4]	CH2[12]	CH2[4]	CH3[12]	CH3[4]	CH4[12]	CH4[4]
DOUT4	CH1[11]	CH1[3]	CH2[11]	CH2[3]	CH3[11]	CH3[3]	CH4[11]	CH4[3]
DOUT3	CH1[10]	CH1[2]	CH2[10]	CH2[2]	CH3[10]	CH3[2]	CH4[10]	CH4[2]
DOUT2	CH1[9]	CH1[1]	CH2[9]	CH2[1]	CH3[9]	CH3[1]	CH4[9]	CH4[1]
DOUT1	CH1[8]	CH1[0]	CH2[8]	CH2[0]	CH3[8]	CH3[0]	CH4[8]	CH4[0]
MCLK	H L	H L	H L	H L	H L	H L	H L	H L

Figure 5-59. CMOS (External) Format 11

CMOS (External) Format 10 is defined in Fig. 5-60.

Format ID: 10
Number of channels: 3
Bits per channel: 16
Clock cycles per pixel: 6
Number of data lines: 8

DOUT8	CH1[15]	CH1[7]	CH2[15]	CH2[7]	CH3[15]	CH3[7]
DOUT7	CH1[14]	CH1[6]	CH2[14]	CH2[6]	CH3[14]	CH3[6]
DOUT6	CH1[13]	CH1[5]	CH2[13]	CH2[5]	CH3[13]	CH3[5]
DOUT5	CH1[12]	CH1[4]	CH2[12]	CH2[4]	CH3[12]	CH3[4]
DOUT4	CH1[11]	CH1[3]	CH2[11]	CH2[3]	CH3[11]	CH3[3]
DOUT3	CH1[10]	CH1[2]	CH2[10]	CH2[2]	CH3[10]	CH3[2]
DOUT2	CH1[9]	CH1[1]	CH2[9]	CH2[1]	CH3[9]	CH3[1]
DOUT1	CH1[8]	CH1[0]	CH2[8]	CH2[0]	CH3[8]	CH3[0]
MCLK	H L	H L	H L	H L	H L	H L

Figure 5-60. CMOS (External) Format 10

CMOS (External) Format 9 is defined in Fig. 5-61.

Format ID: 9
Number of channels: 2
Bits per channel: 16
Clock cycles per pixel: 4
Number of data lines: 8

DOUT8	CH1[15]	CH1[7]	CH2[15]	CH2[7]
DOUT7	CH1[14]	CH1[6]	CH2[14]	CH2[6]
DOUT6	CH1[13]	CH1[5]	CH2[13]	CH2[5]
DOUT5	CH1[12]	CH1[4]	CH2[12]	CH2[4]
DOUT4	CH1[11]	CH1[3]	CH2[11]	CH2[3]
DOUT3	CH1[10]	CH1[2]	CH2[10]	CH2[2]
DOUT2	CH1[9]	CH1[1]	CH2[9]	CH2[1]
DOUT1	CH1[8]	CH1[0]	CH2[8]	CH2[0]
MCLK	H L	H L	H L	H L

Figure 5-61. CMOS (External) Format 9

CMOS (External) Format 67 is defined in Fig. 5-62.

Format ID: 67
Number of channels: 6
Bits per channel: 10
Clock cycles per pixel: 6
Number of data lines: 10

DOUT10	CH1[9]	CH3[9]	CH5[9]	CH2[9]	CH4[9]	CH6[9]
DOUT9	CH1[8]	CH3[8]	CH5[8]	CH2[8]	CH4[8]	CH6[8]
DOUT8	CH1[7]	CH3[7]	CH5[7]	CH2[7]	CH4[7]	CH6[7]
DOUT7	CH1[6]	CH3[6]	CH5[6]	CH2[6]	CH4[6]	CH6[6]
DOUT6	CH1[5]	CH3[5]	CH5[5]	CH2[5]	CH4[5]	CH6[5]
DOUT5	CH1[4]	CH3[4]	CH5[4]	CH2[4]	CH4[4]	CH6[4]
DOUT4	CH1[3]	CH3[3]	CH5[3]	CH2[3]	CH4[3]	CH6[3]
DOUT3	CH1[2]	CH3[2]	CH5[2]	CH2[2]	CH4[2]	CH6[2]
DOUT2	CH1[1]	CH3[1]	CH5[1]	CH2[1]	CH4[1]	CH6[1]
DOUT1	CH1[0]	CH3[0]	CH5[0]	CH2[0]	CH4[0]	CH6[0]
MCLK	H L	H L	H L	H L	H L	H L

Figure 5-62. CMOS (External) Format 67

CMOS (External) Format 66 is defined in Fig. 5-63.

Format ID: 66
Number of channels: 4
Bits per channel: 10
Clock cycles per pixel: 4
Number of data lines: 10

DOUT10	CH1[9]	CH3[9]	CH2[9]	CH4[9]
DOUT9	CH1[8]	CH3[8]	CH2[8]	CH4[8]
DOUT8	CH1[7]	CH3[7]	CH2[7]	CH4[7]
DOUT7	CH1[6]	CH3[6]	CH2[6]	CH4[6]
DOUT6	CH1[5]	CH3[5]	CH2[5]	CH4[5]
DOUT5	CH1[4]	CH3[4]	CH2[4]	CH4[4]
DOUT4	CH1[3]	CH3[3]	CH2[3]	CH4[3]
DOUT3	CH1[2]	CH3[2]	CH2[2]	CH4[2]
DOUT2	CH1[1]	CH3[1]	CH2[1]	CH4[1]
DOUT1	CH1[0]	CH3[0]	CH2[0]	CH4[0]
MCLK	H L	H L	H L	H L

Figure 5-63. CMOS (External) Format 66

CMOS (External) Format 71 is defined in Fig. 5-64.

Format ID: 71
Number of channels: 6
Bits per channel: 10
Clock cycles per pixel: 6
Number of data lines: 10

DOUT10	CH1[9]	CH2[9]	CH3[9]	CH4[9]	CH5[9]	CH6[9]
DOUT9	CH1[8]	CH2[8]	CH3[8]	CH4[8]	CH5[8]	CH6[8]
DOUT8	CH1[7]	CH2[7]	CH3[7]	CH4[7]	CH5[7]	CH6[7]
DOUT7	CH1[6]	CH2[6]	CH3[6]	CH4[6]	CH5[6]	CH6[6]
DOUT6	CH1[5]	CH2[5]	CH3[5]	CH4[5]	CH5[5]	CH6[5]
DOUT5	CH1[4]	CH2[4]	CH3[4]	CH4[4]	CH5[4]	CH6[4]
DOUT4	CH1[3]	CH2[3]	CH3[3]	CH4[3]	CH5[3]	CH6[3]
DOUT3	CH1[2]	CH2[2]	CH3[2]	CH4[2]	CH5[2]	CH6[2]
DOUT2	CH1[1]	CH2[1]	CH3[1]	CH4[1]	CH5[1]	CH6[1]
DOUT1	CH1[0]	CH2[0]	CH3[0]	CH4[0]	CH5[0]	CH6[0]
MCLK	H L	H L	H L	H L	H L	H L

Figure 5-64. CMOS (External) Format 71

CMOS (External) Format 70 is defined in Fig. 5-65.

Format ID: 70
Number of channels: 4
Bits per channel: 10
Clock cycles per pixel: 4
Number of data lines: 10

DOUT10	CH1[9]	CH2[9]	CH3[9]	CH4[9]
DOUT9	CH1[8]	CH2[8]	CH3[8]	CH4[8]
DOUT8	CH1[7]	CH2[7]	CH3[7]	CH4[7]
DOUT7	CH1[6]	CH2[6]	CH3[6]	CH4[6]
DOUT6	CH1[5]	CH2[5]	CH3[5]	CH4[5]
DOUT5	CH1[4]	CH2[4]	CH3[4]	CH4[4]
DOUT4	CH1[3]	CH2[3]	CH3[3]	CH4[3]
DOUT3	CH1[2]	CH2[2]	CH3[2]	CH4[2]
DOUT2	CH1[1]	CH2[1]	CH3[1]	CH4[1]
DOUT1	CH1[0]	CH2[0]	CH3[0]	CH4[0]
MCLK	H L	H L	H L	H L

Figure 5-65. CMOS (External) Format 70

CMOS (External) Format 69 is defined in Fig. 5-66.

Format ID: 69
Number of channels: 3
Bits per channel: 10
Clock cycles per pixel: 3
Number of data lines: 10

DOUT10	CH1[9]	CH2[9]	CH3[9]
DOUT9	CH1[8]	CH2[8]	CH3[8]
DOUT8	CH1[7]	CH2[7]	CH3[7]
DOUT7	CH1[6]	CH2[6]	CH3[6]
DOUT6	CH1[5]	CH2[5]	CH3[5]
DOUT5	CH1[4]	CH2[4]	CH3[4]
DOUT4	CH1[3]	CH2[3]	CH3[3]
DOUT3	CH1[2]	CH2[2]	CH3[2]
DOUT2	CH1[1]	CH2[1]	CH3[1]
DOUT1	CH1[0]	CH2[0]	CH3[0]
MCLK	H L	H L	H L

Figure 5-66. CMOS (External) Format 69

CMOS (External) Format 68 is defined in Fig. 5-67.

Format ID: 68
Number of channels: 2
Bits per channel: 10
Clock cycles per pixel: 2
Number of data lines: 10

DOUT10	CH1[9]		CH2[9]	
DOUT9	CH1[8]		CH2[8]	
DOUT8	CH1[7]		CH2[7]	
DOUT7	CH1[6]		CH2[6]	
DOUT6	CH1[5]		CH2[5]	
DOUT5	CH1[4]		CH2[4]	
DOUT4	CH1[3]		CH2[3]	
DOUT3	CH1[2]		CH2[2]	
DOUT2	CH1[1]		CH2[1]	
DOUT1	CH1[0]		CH2[0]	
MCLK	H	L	H	L

Figure 5-67. CMOS (External) Format 68

5.2 Output Code Calculation

The digital output code associated with a given analog input voltage is dependent on how the analog input path is configured (see Section 4.4), and on the selected data-output format (see Section 4.5). This section describes a calculation that can be used to predict the digital output code for a given configuration.

The digital output code can be derived as follows:

1. Calculate $V_{OFFSET} = (V_{REF} / 3.6) \times (1 - (2 \times$ CHx_SEQn_OFFSET $/ 511))$
   where V_{REF} = internal reference voltage (1.2 V)
2. Calculate $V_{PGA\_INPUT} = V_{IN} - V_{BIAS}$
   where V_{IN} = analog input voltage, and V_{BIAS} = bias voltage
   if the internal bias is enabled, the bias voltage is configured using VBIAS_LVL
3. Calculate $V_{PGA\_OUTPUT} = (GAIN \times (V_{PGA\_INPUT} + V_{OFFSET})) \times (1 - (2 \times$ CHx_POL$))$
   where GAIN = PGA gain represented by CHx_SEQn_AGAIN
4. Calculate the ADC output code:

$$\text{ADC output code} = \max\left(\min\left(\frac{(V_{PGA\_OUTPUT} - V_{REF}) \times 2^{RES-1}}{V_{REF}} + 2^{RES-1}, 2^{RES} - 1\right), 0\right)$$

   where RES = number of data bits per channel in selected output format

Note: The calculation assumes default digital gain of 1 V/V (CHx_SEQn_DGAIN = 0x800)

5.2.1 Example Calculation

Using example data, the digital output code can be calculated as follows:

- V_{IN} = 2.3 V
- V_{REF} = 1.2 V
- V_{BIAS} = 1.0 V
- Offset code (CHx_SEQn_OFFSET) = 256
- PGA gain (CHx_SEQn_AGAIN) = 1 V/V
- Polarity (CHx_POL) = 0
- Output data resolution = 16 bits

Calculate $V_{OFFSET} = (1.2 / 3.6) \times (1 - (2 \times 256 / 511)) = -0.000652$ V

Calculate $V_{PGA\_INPUT} = 2.3 - 1.0 = 1.3$ V

Calculate V_{PGA_OUTPUT} = (1 × (1.3 – 0.000652)) × (1 – (2 × 0)) = 1.2993348 V

Calculate the ADC output code:

$$\text{ADC output code} = \max\left(\min\left(\frac{(1.2993348 - 1.2) \times 2^{15}}{1.2} + 2^{15}, 2^{16} - 1\right), 0\right) = \max(\min(35481, 65535), 0) = 35481$$

6 Register Quick Reference—Banked Register Mode (SPI)

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

- This register view is for the CS82L46 6-channel imaging AFE/ADC, using the banked host-interface configuration.
- The register field default values are established on power-up and after soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 8 bits wide.
- All visible fields are read/write except where indicated with the following shading:

Read/write access | Read-only access | Write-only access

Table 6-1. Bank Overview Table

Block Name	Register Quick Reference
BANK0—Hardware ID, Clocking, MSM, Timing Gen, Output Format, Pad I/O, DAC, PGA	Section 6.1
BANK1—DAC, PGA, BLC, SARADC	Section 6.2
BANK2—Timing Gen	Section 6.3
BANK3—Timing Gen, Test Pattern Gen	Section 6.4
BANK6—PAD I/O, LED Control, PLL1	Section 6.5
BANK7—Digital Gain	Section 6.6

6.1 BANK0—Hardware ID, Clocking, MSM, Timing Gen, Output Format, Pad I/O, DAC, PGA

Address	Register	7	6	5	4	3	2	1	0
0x00	BANK	DESCRIM				—	BANK		
p. 146		1	1	0	0	0	0	0	0
0x04	ASYNC0_0	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	PLL_ERROR_STS	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
p. 147		0	0	0	0	0	0	0	0
0x05	ASYNC0_1	—							OSC_DISABLE
p. 148		0	0	0	0	0	0	0	0
0x08	SFT_RESET	SFT_RESET							
p. 146		0	0	0	0	0	0	0	0
0x0C	DEVID_0	DEVID_0							
p. 146		0	1	0	0	0	1	0	0
0x0D	DEVID_1	DEVID_1							
p. 147		0	0	1	0	1	0	1	0
0x0E	DEVID_2	DEVID_2							
p. 147		0	0	0	0	1	0	0	0
0x10	REVID	AREVID				MTLREVID			
p. 147		1	0	1	1	0	0	0	0
0x14	RELID	RELID							
p. 147		0	0	0	0	0	0	0	0
0x18	DEVICE_CLK_CFG_0	PIXEL_SAMPLE_RATE							
p. 148		0	1	1	1	1	0	0	0
0x19	DEVICE_CLK_CFG_1	—			EXT_AFECK_DUR			CLOCK_CFG_MODE	
p. 148		0	0	0	0	0	0	0	1
0x1A	DEVICE_CLK_CFG_2	—						PLL2_AUTO	PLL1_AUTO
p. 149		0	0	0	0	0	0	1	1

Address	Register	7	6	5	4	3	2	1	0
0x1B	DEVICE_CLK_CFG_3	PLL2_SS_FREQ			PLL2_SS_MAG				PLL2_SS_EN
p. 149		0	0	0	0	0	0	0	0
0x1E	DEVICE_CLK_CFG2_2	PLL2_SS_REF_FREQ_0							
p. 149		0	0	0	0	0	0	0	0
0x1F	DEVICE_CLK_CFG2_3	DOUT_READY_EN	—		MCLK_EXT_SS	—		PLL2_SS_REF_FREQ_1	
p. 149		1	0	0	0	0	0	0	0
0x20	MCLK_FILT_CFG_0	MCLK_MASK_DLY_0							
p. 150		0	0	0	0	0	0	0	1
0x21	MCLK_FILT_CFG_1	MCLK_MASK_DLY_1							
p. 150		0	0	0	0	0	0	0	0
0x22	MCLK_FILT_CFG_2	MCLK_MASK_POL	MCLK_MASK_EN	MCLK_MASK_DUR					
p. 150		0	0	0	0	0	0	0	1
0x23	MCLK_FILT_CFG_3	MCLK_MASK_CLK_DIV			MCLK_MASK_OPF_RST	—	MCLK_MASK_SRC		
p. 151		0	0	0	0	0	0	0	0
0x28	DEVICE_CTRL_0	—	SHARED_BUS_MODE	GPI12_DOUT_CTRL	—	COMPLETE_LINE	ACTIVE_EN	READY_EN	MSM_EN
p. 151		0	0	0	0	0	0	0	1
0x29	DEVICE_CTRL_1	TEMP_ERROR_RST_MASK	—	TEMP_ERROR_CLR	—				
p. 152		0	0	0	0	0	0	0	0
0x2C	RLCDAC_CTRL_0	—							VBIAS_EN
p. 152		0	0	0	0	0	0	0	0
0x2D	RLCDAC_CTRL_1	—			VBIAS_LVL				
p. 152		0	0	0	0	0	0	0	0
0x2E	RLCDAC_CTRL_2	—				VBIAS_ISEL_BOOST	VBIAS_ISEL		VBIAS_REF
p. 152		0	0	0	0	0	0	0	1
0x34	DEVICE_STATUS_0	ERROR_STS	—	ACTIVE_STS	READY_STS	—		IDLE_STS	STARTUP_STS
p. 153		0	0	0	0	0	0	0	0
0x36	DEVICE_STATUS_2	VDDA_STS	—						
p. 153		0	0	0	0	0	1	0	0
0x48	TG_CONFIG1_0	VSMP_EXT_POL	EXTERNAL_MODE_TG_EN	CDS_EN	CLAMP_EN	CLAMP_MODE		TGSYNC_MODE	EXTERNAL_MODE_EN
p. 153		0	0	0	0	0	0	0	1
0x49	TG_CONFIG1_1	INIT_SEQ_STATE		VSMP_EXT_DLY					EXTERNAL_MODE_SEL
p. 154		0	0	0	0	0	0	0	0
0x4A	TG_CONFIG1_2	—	TGSYNC_SINGLE_SEQ	NUM_SEQ_STATES		RSMP_EXT_DLY			
p. 154		0	0	0	0	0	0	0	1
0x4B	TG_CONFIG1_3	—		CH6_CLAMP_OVRD	CH5_CLAMP_OVRD	CH4_CLAMP_OVRD	CH3_CLAMP_OVRD	CH2_CLAMP_OVRD	CH1_CLAMP_OVRD
p. 155		0	0	0	0	0	0	0	0
0x4C	OP_FORMAT_CFG0_0	FORMAT_LOAD	FORMAT_SEL						
p. 204		0	0	0	0	0	0	0	1
0x4D	OP_FORMAT_CFG0_1	—				LVDS_POL	LVDS_REVERSE	CMOS_EXT_POL	LVDS_BIT_ORDER
p. 204		0	0	0	0	0	0	0	1
0x4E	OP_FORMAT_CFG0_2	—						TDM_GAP	TDM_EN
p. 205		0	0	0	0	0	0	0	0
0x4F	OP_FORMAT_CFG0_3	—			TDM_OFFSET				
p. 205		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x50	OP_FORMAT_CFG1_0	FLAG_S1_FN				FLAG_S0_FN			
p. 205		0	0	0	0	0	0	0	0
0x51	OP_FORMAT_CFG1_1	FLAG_S3_FN				FLAG_S2_FN			
p. 206		0	0	0	0	0	0	0	0
0x52	OP_FORMAT_CFG1_2	—				FLAG_S4_FN			
p. 206		0	0	0	0	0	0	0	0
0x54	CLKOUT_SEL_1_0	CLKOUT4_FN	CLKOUT3_FN			CLKOUT2_FN		CLKOUT1_FN	
p. 206		0	0	0	1	0	1	0	1
0x55	CLKOUT_SEL_1_1	—		CLKOUT10_FN	CLKOUT9_FN	CLKOUT8_FN	CLKOUT7_FN	CLKOUT6_FN	CLKOUT5_FN
p. 207		0	0	0	0	0	0	0	0
0x56	CLKOUT_SEL_1_2	—			MON_SEL			TGSYNC1_VSMP_FN	
p. 207		0	0	0	0	0	0	0	0
0x57	CLKOUT_SEL_1_3	—				TDM_DOUT_DLY_SEL		TDM_DOUT_DLY_EN	MCLK_EXT_LVDS
p. 208		0	0	0	0	0	1	0	0
0x5C	DAC_CTRL_OFS01_CH1_0	CH1_SEQ0_OFFSET_0							
p. 224		0	0	0	0	0	0	0	0
0x5D	DAC_CTRL_OFS01_CH1_1	—							CH1_SEQ0_OFFSET_1
p. 224		0	0	0	0	0	0	0	1
0x5E	DAC_CTRL_OFS01_CH1_2	CH1_SEQ1_OFFSET_0							
p. 225		0	0	0	0	0	0	0	0
0x5F	DAC_CTRL_OFS01_CH1_3	—							CH1_SEQ1_OFFSET_1
p. 225		0	0	0	0	0	0	0	1
0x60	DAC_CTRL_OFS23_CH1_0	CH1_SEQ2_OFFSET_0							
p. 225		0	0	0	0	0	0	0	0
0x61	DAC_CTRL_OFS23_CH1_1	—							CH1_SEQ2_OFFSET_1
p. 225		0	0	0	0	0	0	0	1
0x62	DAC_CTRL_OFS23_CH1_2	CH1_SEQ3_OFFSET_0							
p. 226		0	0	0	0	0	0	0	0
0x63	DAC_CTRL_OFS23_CH1_3	—							CH1_SEQ3_OFFSET_1
p. 226		0	0	0	0	0	0	0	1
0x64	DAC_CTRL_OFS0_CH2_3_0	CH2_SEQ0_OFFSET_0							
p. 226		0	0	0	0	0	0	0	0
0x65	DAC_CTRL_OFS0_CH2_3_1	—							CH2_SEQ0_OFFSET_1
p. 226		0	0	0	0	0	0	0	1
0x66	DAC_CTRL_OFS0_CH2_3_2	CH3_SEQ0_OFFSET_0							
p. 227		0	0	0	0	0	0	0	0
0x67	DAC_CTRL_OFS0_CH2_3_3	—							CH3_SEQ0_OFFSET_1
p. 227		0	0	0	0	0	0	0	1
0x68	DAC_CTRL_OFS0_CH4_5_0	CH4_SEQ0_OFFSET_0							
p. 227		0	0	0	0	0	0	0	0
0x69	DAC_CTRL_OFS0_CH4_5_1	—							CH4_SEQ0_OFFSET_1
p. 227		0	0	0	0	0	0	0	1
0x6A	DAC_CTRL_OFS0_CH4_5_2	CH5_SEQ0_OFFSET_0							
p. 228		0	0	0	0	0	0	0	0
0x6B	DAC_CTRL_OFS0_CH4_5_3	—							CH5_SEQ0_OFFSET_1
p. 228		0	0	0	0	0	0	0	1
0x6C	DAC_CTRL_OFS0_CH6_0	CH6_SEQ0_OFFSET_0							
p. 228		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x6D	DAC_CTRL_OFS0_CH6_1	—							CH6_SEQ0_OFFSET_1
p. 228		0	0	0	0	0	0	0	1
0x74	PGA_CTRL_AGAIN_CH1_0	—		CH1_SEQ0_AGAIN					
p. 236		0	0	0	0	0	0	0	0
0x75	PGA_CTRL_AGAIN_CH1_1	—		CH1_SEQ1_AGAIN					
p. 236		0	0	0	0	0	0	0	0
0x76	PGA_CTRL_AGAIN_CH1_2	—		CH1_SEQ2_AGAIN					
p. 237		0	0	0	0	0	0	0	0
0x77	PGA_CTRL_AGAIN_CH1_3	—		CH1_SEQ3_AGAIN					
p. 237		0	0	0	0	0	0	0	0
0x78	PGA_CTRL_AGAIN_CH2_0	—		CH2_SEQ0_AGAIN					
p. 237		0	0	0	0	0	0	0	0
0x79	PGA_CTRL_AGAIN_CH3_0	—		CH3_SEQ0_AGAIN					
p. 237		0	0	0	0	0	0	0	0
0x7A	PGA_CTRL_AGAIN_CH4_0	—		CH4_SEQ0_AGAIN					
p. 238		0	0	0	0	0	0	0	0
0x7B	PGA_CTRL_AGAIN_CH5_0	—		CH5_SEQ0_AGAIN					
p. 238		0	0	0	0	0	0	0	0
0x7C	PGA_CTRL_AGAIN_CH6_0	—		CH6_SEQ0_AGAIN					
p. 238		0	0	0	0	0	0	0	0

6.2 **BANK1**—DAC, PGA, BLC, SARADC

Address	Register	7	6	5	4	3	2	1	0
0x00	BANK	DESCRIM				—	BANK		
p. 146		1	1	0	0	0	0	0	0
0x04	ASYNC0_0	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	PLL_ERROR_STS	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
p. 147		0	0	0	0	0	0	0	0
0x05	ASYNC0_1	—							OSC_DISABLE
p. 148		0	0	0	0	0	0	0	0
0x08	SFT_RESET	SFT_RESET							
p. 146		0	0	0	0	0	0	0	0
0x0E	DAC_CTRL_OFS1_CH2_2	CH2_SEQ1_OFFSET_0							
p. 229		0	0	0	0	0	0	0	0
0x0F	DAC_CTRL_OFS1_CH2_3	—							CH2_SEQ1_OFFSET_1
p. 229		0	0	0	0	0	0	0	1
0x12	DAC_CTRL_OFS1_CH3_2	CH3_SEQ1_OFFSET_0							
p. 229		0	0	0	0	0	0	0	0
0x13	DAC_CTRL_OFS1_CH3_3	—							CH3_SEQ1_OFFSET_1
p. 229		0	0	0	0	0	0	0	1
0x16	DAC_CTRL_OFS1_CH4_2	CH4_SEQ1_OFFSET_0							
p. 230		0	0	0	0	0	0	0	0
0x17	DAC_CTRL_OFS1_CH4_3	—							CH4_SEQ1_OFFSET_1
p. 230		0	0	0	0	0	0	0	1
0x1A	DAC_CTRL_OFS01_CH5_2	CH5_SEQ1_OFFSET_0							
p. 230		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x1B	DAC_CTRL_OFS01_CH5_3	—							CH5_SEQ1_OFFSET_1
p. 230		0	0	0	0	0	0	0	1
0x1E	DAC_CTRL_OFS1_CH6_2	CH6_SEQ1_OFFSET_0							
p. 231		0	0	0	0	0	0	0	0
0x1F	DAC_CTRL_OFS1_CH6_3	—							CH6_SEQ1_OFFSET_1
p. 231		0	0	0	0	0	0	0	1
0x20	DAC_CTRL_OFS23_CH2_0	CH2_SEQ2_OFFSET_0							
p. 231		0	0	0	0	0	0	0	0
0x21	DAC_CTRL_OFS23_CH2_1	—							CH2_SEQ2_OFFSET_1
p. 231		0	0	0	0	0	0	0	1
0x22	DAC_CTRL_OFS23_CH2_2	CH2_SEQ3_OFFSET_0							
p. 232		0	0	0	0	0	0	0	0
0x23	DAC_CTRL_OFS23_CH2_3	—							CH2_SEQ3_OFFSET_1
p. 232		0	0	0	0	0	0	0	1
0x24	DAC_CTRL_OFS23_CH3_0	CH3_SEQ2_OFFSET_0							
p. 232		0	0	0	0	0	0	0	0
0x25	DAC_CTRL_OFS23_CH3_1	—							CH3_SEQ2_OFFSET_1
p. 232		0	0	0	0	0	0	0	1
0x26	DAC_CTRL_OFS23_CH3_2	CH3_SEQ3_OFFSET_0							
p. 233		0	0	0	0	0	0	0	0
0x27	DAC_CTRL_OFS23_CH3_3	—							CH3_SEQ3_OFFSET_1
p. 233		0	0	0	0	0	0	0	1
0x28	DAC_CTRL_OFS23_CH4_0	CH4_SEQ2_OFFSET_0							
p. 233		0	0	0	0	0	0	0	0
0x29	DAC_CTRL_OFS23_CH4_1	—							CH4_SEQ2_OFFSET_1
p. 233		0	0	0	0	0	0	0	1
0x2A	DAC_CTRL_OFS23_CH4_2	CH4_SEQ3_OFFSET_0							
p. 234		0	0	0	0	0	0	0	0
0x2B	DAC_CTRL_OFS23_CH4_3	—							CH4_SEQ3_OFFSET_1
p. 234		0	0	0	0	0	0	0	1
0x2C	DAC_CTRL_OFS23_CH5_0	CH5_SEQ2_OFFSET_0							
p. 234		0	0	0	0	0	0	0	0
0x2D	DAC_CTRL_OFS23_CH5_1	—							CH5_SEQ2_OFFSET_1
p. 234		0	0	0	0	0	0	0	1
0x2E	DAC_CTRL_OFS23_CH5_2	CH5_SEQ3_OFFSET_0							
p. 235		0	0	0	0	0	0	0	0
0x2F	DAC_CTRL_OFS23_CH5_3	—							CH5_SEQ3_OFFSET_1
p. 235		0	0	0	0	0	0	0	1
0x30	DAC_CTRL_OFS23_CH6_0	CH6_SEQ2_OFFSET_0							
p. 235		0	0	0	0	0	0	0	0
0x31	DAC_CTRL_OFS23_CH6_1	—							CH6_SEQ2_OFFSET_1
p. 235		0	0	0	0	0	0	0	1
0x32	DAC_CTRL_OFS23_CH6_2	CH6_SEQ3_OFFSET_0							
p. 236		0	0	0	0	0	0	0	0
0x33	DAC_CTRL_OFS23_CH6_3	—							CH6_SEQ3_OFFSET_1
p. 236		0	0	0	0	0	0	0	1

Address	Register	7	6	5	4	3	2	1	0
0x35	PGA_CTRL_AGAIN_CH2_1	—		CH2_SEQ1_AGAIN					
p. 238		0	0	0	0	0	0	0	0
0x36	PGA_CTRL_AGAIN_CH2_2	—		CH2_SEQ2_AGAIN					
p. 239		0	0	0	0	0	0	0	0
0x37	PGA_CTRL_AGAIN_CH2_3	—		CH2_SEQ3_AGAIN					
p. 239		0	0	0	0	0	0	0	0
0x39	PGA_CTRL_AGAIN_CH3_1	—		CH3_SEQ1_AGAIN					
p. 239		0	0	0	0	0	0	0	0
0x3A	PGA_CTRL_AGAIN_CH3_2	—		CH3_SEQ2_AGAIN					
p. 239		0	0	0	0	0	0	0	0
0x3B	PGA_CTRL_AGAIN_CH3_3	—		CH3_SEQ3_AGAIN					
p. 240		0	0	0	0	0	0	0	0
0x3D	PGA_CTRL_AGAIN_CH4_1	—		CH4_SEQ1_AGAIN					
p. 240		0	0	0	0	0	0	0	0
0x3E	PGA_CTRL_AGAIN_CH4_2	—		CH4_SEQ2_AGAIN					
p. 240		0	0	0	0	0	0	0	0
0x3F	PGA_CTRL_AGAIN_CH4_3	—		CH4_SEQ3_AGAIN					
p. 240		0	0	0	0	0	0	0	0
0x41	PGA_CTRL_AGAIN_CH5_1	—		CH5_SEQ1_AGAIN					
p. 241		0	0	0	0	0	0	0	0
0x42	PGA_CTRL_AGAIN_CH5_2	—		CH5_SEQ2_AGAIN					
p. 241		0	0	0	0	0	0	0	0
0x43	PGA_CTRL_AGAIN_CH5_3	—		CH5_SEQ3_AGAIN					
p. 241		0	0	0	0	0	0	0	0
0x45	PGA_CTRL_AGAIN_CH6_1	—		CH6_SEQ1_AGAIN					
p. 241		0	0	0	0	0	0	0	0
0x46	PGA_CTRL_AGAIN_CH6_2	—		CH6_SEQ2_AGAIN					
p. 242		0	0	0	0	0	0	0	0
0x47	PGA_CTRL_AGAIN_CH6_3	—		CH6_SEQ3_AGAIN					
p. 242		0	0	0	0	0	0	0	0
0x48	BLC_CTRL1_0	—	BLC_FINE_EVERYLINE	BLC_FINE_ACCUM	BLC_FINE_EN	—	BLC_COARSE_CYCLES		
p. 242		0	0	0	0	0	0	0	0
0x49	BLC_CTRL1_1	BLC_TRACKING				—			BLC_FRAME_START
p. 243		0	0	0	0	0	0	0	0
0x4A	BLC_CTRL1_2	BLC_LENGTH_0							
p. 243		0	0	0	0	0	0	0	0
0x4B	BLC_CTRL1_3	—			BLC_TARGET_RANGE	—		BLC_LENGTH_1	
p. 243		0	0	0	0	0	0	0	0
0x50	BLC_TARGET_CH1_0	CH1_SEQ0_BLC_TARGET							
p. 243		0	0	0	0	0	0	0	0
0x51	BLC_TARGET_CH1_1	CH1_SEQ1_BLC_TARGET							
p. 244		0	0	0	0	0	0	0	0
0x52	BLC_TARGET_CH1_2	CH1_SEQ2_BLC_TARGET							
p. 244		0	0	0	0	0	0	0	0
0x53	BLC_TARGET_CH1_3	CH1_SEQ3_BLC_TARGET							
p. 244		0	0	0	0	0	0	0	0
0x54	BLC_TARGET_CH2_0	CH2_SEQ0_BLC_TARGET							
p. 244		0	0	0	0	0	0	0	0
0x55	BLC_TARGET_CH2_1	CH2_SEQ1_BLC_TARGET							
p. 244		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x56	BLC_TARGET_CH2_2	CH2_SEQ2_BLC_TARGET							
p. 244		0	0	0	0	0	0	0	0
0x57	BLC_TARGET_CH2_3	CH2_SEQ3_BLC_TARGET							
p. 245		0	0	0	0	0	0	0	0
0x58	BLC_TARGET_CH3_0	CH3_SEQ0_BLC_TARGET							
p. 245		0	0	0	0	0	0	0	0
0x59	BLC_TARGET_CH3_1	CH3_SEQ1_BLC_TARGET							
p. 245		0	0	0	0	0	0	0	0
0x5A	BLC_TARGET_CH3_2	CH3_SEQ2_BLC_TARGET							
p. 245		0	0	0	0	0	0	0	0
0x5B	BLC_TARGET_CH3_3	CH3_SEQ3_BLC_TARGET							
p. 245		0	0	0	0	0	0	0	0
0x5C	BLC_TARGET_CH4_0	CH4_SEQ0_BLC_TARGET							
p. 245		0	0	0	0	0	0	0	0
0x5D	BLC_TARGET_CH4_1	CH4_SEQ1_BLC_TARGET							
p. 246		0	0	0	0	0	0	0	0
0x5E	BLC_TARGET_CH4_2	CH4_SEQ2_BLC_TARGET							
p. 246		0	0	0	0	0	0	0	0
0x5F	BLC_TARGET_CH4_3	CH4_SEQ3_BLC_TARGET							
p. 246		0	0	0	0	0	0	0	0
0x60	BLC_TARGET_CH5_0	CH5_SEQ0_BLC_TARGET							
p. 246		0	0	0	0	0	0	0	0
0x61	BLC_TARGET_CH5_1	CH5_SEQ1_BLC_TARGET							
p. 246		0	0	0	0	0	0	0	0
0x62	BLC_TARGET_CH5_2	CH5_SEQ2_BLC_TARGET							
p. 246		0	0	0	0	0	0	0	0
0x63	BLC_TARGET_CH5_3	CH5_SEQ3_BLC_TARGET							
p. 247		0	0	0	0	0	0	0	0
0x64	BLC_TARGET_CH6_0	CH6_SEQ0_BLC_TARGET							
p. 247		0	0	0	0	0	0	0	0
0x65	BLC_TARGET_CH6_1	CH6_SEQ1_BLC_TARGET							
p. 247		0	0	0	0	0	0	0	0
0x66	BLC_TARGET_CH6_2	CH6_SEQ2_BLC_TARGET							
p. 247		0	0	0	0	0	0	0	0
0x67	BLC_TARGET_CH6_3	CH6_SEQ3_BLC_TARGET							
p. 247		0	0	0	0	0	0	0	0
0x69	SAR1_CTRL_1	—					CH1_POL	—	
p. 251		0	0	0	0	0	0	0	0
0x6B	SAR1_CTRL_3	—						CH1_AFE_POWER	
p. 251		0	0	0	0	0	0	1	1
0x6D	SAR2_CTRL_1	—					CH2_POL	—	
p. 251		0	0	0	0	0	0	0	0
0x6F	SAR2_CTRL_3	—						CH2_AFE_POWER	
p. 251		0	0	0	0	0	0	1	1
0x71	SAR3_CTRL_1	—					CH3_POL	—	
p. 252		0	0	0	0	0	0	0	0
0x73	SAR3_CTRL_3	—						CH3_AFE_POWER	
p. 252		0	0	0	0	0	0	1	1
0x75	SAR4_CTRL_1	—					CH4_POL	—	
p. 252		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x77	SAR4_CTRL_3	—						CH4_AFE_POWER	
p. 252		0	0	0	0	0	0	1	1
0x79	SAR5_CTRL_1	—					CH5_POL	—	
p. 253		0	0	0	0	0	0	0	0
0x7B	SAR5_CTRL_3	—						CH5_AFE_POWER	
p. 253		0	0	0	0	0	0	1	1
0x7D	SAR6_CTRL_1	—					CH6_POL	—	
p. 253		0	0	0	0	0	0	0	0
0x7F	SAR6_CTRL_3	—						CH6_AFE_POWER	
p. 253		0	0	0	0	0	0	1	1

6.3 **BANK2**—Timing Gen

Address	Register	7	6	5	4	3	2	1	0
0x00	BANK	DESCRIM				—	BANK		
p. 146		1	1	0	0	0	0	0	0
0x04	ASYNC0_0	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	PLL_ERROR_STS	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
p. 147		0	0	0	0	0	0	0	0
0x05	ASYNC0_1	—							OSC_DISABLE
p. 148		0	0	0	0	0	0	0	0
0x08	SFT_RESET	SFT_RESET							
p. 146		0	0	0	0	0	0	0	0
0x0C	TG_STATUS	—						SEQ_STATE_STS	
p. 155		0	0	0	0	0	0	0	0
0x10	TG_CONFIG2_0	—		LEDSTART_POL	LEDSTART_SEQ_INIT	TGSYNC_ASYNC	TGSYNC_IN_POL	TGSYNC_IN_SRC	
p. 155		0	0	0	0	0	1	0	0
0x11	TG_CONFIG2_1	—	TGSYNC_OUT_DUR			TGSYNC_IN_OFFSET			
p. 156		0	0	1	0	0	0	0	0
0x12	TG_CONFIG2_2	—	TGSYNC_FILT_STAGE			TGSYNC_FILT_DECM			TGSYNC_FILT_EN
p. 156		0	1	0	0	0	1	1	0
0x13	TG_CONFIG2_3	—		TP_SEC_OFFSET					
p. 156		0	0	0	0	0	0	0	0
0x14	TG_CONFIG3_0	LEDG_PO_SEL				LEDR_PO_SEL			
p. 157		0	0	0	1	0	0	0	0
0x15	TG_CONFIG3_1	DC_PO_2ND_PULSE	NUM_DC_PO			LEDB_PO_SEL			
p. 157		0	0	0	0	0	0	1	0
0x16	TG_CONFIG3_2	FLAG_DEN2_PO_SEL				FLAG_DEN1_PO_SEL			
p. 158		1	0	0	1	1	0	0	1
0x17	TG_CONFIG3_3	—		FLAG_PIX2_PO_EDGE		FLAG_PIX2_PO_SEL			
p. 158		0	0	0	0	1	0	1	0
0x18	SEQ_DURATION0_0	SEQ_STATE0_LEN_0							
p. 158		0	0	0	0	0	0	0	0
0x19	SEQ_DURATION0_1	SEQ_STATE0_LEN_1							
p. 158		0	0	0	0	1	0	0	0
0x1A	SEQ_DURATION0_2	SEQ_STATE1_LEN_0							
p. 159		0	0	0	0	0	0	0	0
0x1B	SEQ_DURATION0_3	SEQ_STATE1_LEN_1							
p. 159		0	0	0	0	1	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x1C	SEQ_DURATION1_0	SEQ_STATE2_LEN_0							
p. 159		0	0	0	0	0	0	0	0
0x1D	SEQ_DURATION1_1	SEQ_STATE2_LEN_1							
p. 159		0	0	0	0	1	0	0	0
0x1E	SEQ_DURATION1_2	SEQ_STATE3_LEN_0							
p. 159		0	0	0	0	0	0	0	0
0x1F	SEQ_DURATION1_3	SEQ_STATE3_LEN_1							
p. 159		0	0	0	0	1	0	0	0
0x20	TG_TIMING_CFG0_0	CK_MASK1_START_0							
p. 160		0	0	0	0	0	0	0	0
0x21	TG_TIMING_CFG0_1	CK_MASK1_START_1							
p. 160		0	0	0	0	0	0	0	0
0x22	TG_TIMING_CFG0_2	CK_MASK1_END_0							
p. 160		0	0	0	0	0	0	0	0
0x23	TG_TIMING_CFG0_3	CK_MASK1_END_1							
p. 160		0	0	0	0	0	0	0	0
0x24	TG_TIMING_CFG1_0	CK_MASK2_START_0							
p. 160		0	0	0	0	0	0	0	0
0x25	TG_TIMING_CFG1_1	CK_MASK2_START_1							
p. 161		0	0	0	0	0	0	0	0
0x26	TG_TIMING_CFG1_2	CK_MASK2_END_0							
p. 161		0	0	0	0	0	0	0	0
0x27	TG_TIMING_CFG1_3	CK_MASK2_END_1							
p. 161		0	0	0	0	0	0	0	0
0x28	TG_TIMING_CFG2_0	CK_MASK3_START_0							
p. 161		0	0	0	0	0	0	0	0
0x29	TG_TIMING_CFG2_1	CK_MASK3_START_1							
p. 161		0	0	0	0	0	0	0	0
0x2A	TG_TIMING_CFG2_2	CK_MASK3_END_0							
p. 162		0	0	0	0	0	0	0	0
0x2B	TG_TIMING_CFG2_3	CK_MASK3_END_1							
p. 162		0	0	0	0	0	0	0	0
0x2C	TG_TIMING_CFG3_0	CLAMP_START_0							
p. 162		0	0	0	0	0	0	0	0
0x2D	TG_TIMING_CFG3_1	CLAMP_START_1							
p. 162		0	0	0	0	0	0	0	0
0x2E	TG_TIMING_CFG3_2	CLAMP_END_0							
p. 162		0	0	0	0	0	0	0	0
0x2F	TG_TIMING_CFG3_3	CLAMP_END_1							
p. 163		0	0	0	0	0	0	0	0
0x34	TG_TIMING_CFG5_0	FLAG_PIX1_PIXEL1_0							
p. 163		1	1	1	1	1	1	1	1
0x35	TG_TIMING_CFG5_1	FLAG_PIX1_PIXEL1_1							
p. 163		1	1	1	1	1	1	1	1
0x36	TG_TIMING_CFG5_2	FLAG_PIX1_PIXEL2_0							
p. 163		1	1	1	1	1	1	1	1
0x37	TG_TIMING_CFG5_3	FLAG_PIX1_PIXEL2_1							
p. 163		1	1	1	1	1	1	1	1
0x38	TG_TIMING_CFG6_0	FLAG_PIX1_PIXEL3_0							
p. 164		1	1	1	1	1	1	1	1
0x39	TG_TIMING_CFG6_1	FLAG_PIX1_PIXEL3_1							
p. 164		1	1	1	1	1	1	1	1
0x3A	TG_TIMING_CFG6_2	FLAG_PIX1_PIXEL4_0							
p. 164		1	1	1	1	1	1	1	1

Address	Register	7	6	5	4	3	2	1	0
0x3B	TG_TIMING_CFG6_3	FLAG_PIX1_PIXEL4_1							
p. 164		1	1	1	1	1	1	1	1
0x3C	TG_TIMING_CFG7_0	—	ACYC_PO_POL	ACYC_PO_SEL				ACYC_MODE	ACYC_EN
p. 164		0	0	0	0	0	0	0	0
0x3D	TG_TIMING_CFG7_1	ACYC_DELAY							
p. 165		0	0	0	0	0	0	0	0
0x3E	TG_TIMING_CFG7_2	BLC_START_0							
p. 165		0	0	0	0	0	0	0	0
0x3F	TG_TIMING_CFG7_3	BLC_START_1							
p. 165		0	0	0	0	0	0	0	0
0x40	TG_TIMING_CFG8_0	PO7_INIT_LVL	PO6_INIT_LVL	PO5_INIT_LVL	PO4_INIT_LVL	PO3_INIT_LVL	PO2_INIT_LVL	PO1_INIT_LVL	PO0_INIT_LVL
p. 165		0	0	0	0	0	0	0	0
0x41	TG_TIMING_CFG8_1	—		CK_TOG3_INIT_LVL	CK_TOG2_INIT_LVL	CK_TOG1_INIT_LVL	PO10_INIT_LVL	PO9_INIT_LVL	PO8_INIT_LVL
p. 166		0	0	0	0	0	0	0	0
0x42	TG_TIMING_CFG8_2	FIFO_RESET_DLY	PO10_DC_INIT_LVL	PO9_DC_INIT_LVL	PO8_DC_INIT_LVL	PO7_DC_INIT_LVL	PO6_DC_INIT_LVL	PO5_DC_INIT_LVL	PGEN_CNT_SEL
p. 167		1	0	0	0	0	0	0	1
0x43	TG_TIMING_CFG8_3	FIFO_BLANK_DUR					—		FIFO_RESET_CTRL
p. 167		1	1	0	0	1	0	0	0
0x44	TG_POLARITY_T1_0	CK_TOG1_TP_POL_0							
p. 167		0	0	0	0	0	0	0	0
0x45	TG_POLARITY_T1_1	CK_TOG1_TP_POL_1							
p. 168		0	0	0	0	0	0	0	0
0x46	TG_POLARITY_T1_2	CK_TOG1_TP_POL_2							
p. 168		0	0	0	0	0	0	0	0
0x47	TG_POLARITY_T1_3	CK_TOG1_TP_POL_3							
p. 168		0	0	0	0	0	0	0	0
0x48	TG_POLARITY_T2_0	CK_TOG2_TP_POL_0							
p. 168		0	0	0	0	0	0	0	0
0x49	TG_POLARITY_T2_1	CK_TOG2_TP_POL_1							
p. 168		0	0	0	0	0	0	0	0
0x4A	TG_POLARITY_T2_2	CK_TOG2_TP_POL_2							
p. 168		0	0	0	0	0	0	0	0
0x4B	TG_POLARITY_T2_3	CK_TOG2_TP_POL_3							
p. 169		0	0	0	0	0	0	0	0
0x4C	TG_POLARITY_T3_0	CK_TOG3_TP_POL_0							
p. 169		0	0	0	0	0	0	0	0
0x4D	TG_POLARITY_T3_1	CK_TOG3_TP_POL_1							
p. 169		0	0	0	0	0	0	0	0
0x4E	TG_POLARITY_T3_2	CK_TOG3_TP_POL_2							
p. 169		0	0	0	0	0	0	0	0
0x4F	TG_POLARITY_T3_3	CK_TOG3_TP_POL_3							
p. 169		0	0	0	0	0	0	0	0
0x50	TG_POLARITY_PO0_0	PO0_TP_POL_0							
p. 169		0	0	0	0	0	0	0	0
0x51	TG_POLARITY_PO0_1	PO0_TP_POL_1							
p. 170		0	0	0	0	0	0	0	0
0x52	TG_POLARITY_PO0_2	PO0_TP_POL_2							
p. 170		0	0	0	0	0	0	0	0
0x53	TG_POLARITY_PO0_3	PO0_TP_POL_3							
p. 170		0	0	0	0	0	0	0	0
0x54	TG_POLARITY_PO1_0	PO1_TP_POL_0							
p. 170		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x55 p. 170	TG_POLARITY_PO1_1	PO1_TP_POL_1 0	0	0	0	0	0	0	0
0x56 p. 170	TG_POLARITY_PO1_2	PO1_TP_POL_2 0	0	0	0	0	0	0	0
0x57 p. 171	TG_POLARITY_PO1_3	PO1_TP_POL_3 0	0	0	0	0	0	0	0
0x58 p. 171	TG_POLARITY_PO2_0	PO2_TP_POL_0 0	0	0	0	0	0	0	0
0x59 p. 171	TG_POLARITY_PO2_1	PO2_TP_POL_1 0	0	0	0	0	0	0	0
0x5A p. 171	TG_POLARITY_PO2_2	PO2_TP_POL_2 0	0	0	0	0	0	0	0
0x5B p. 171	TG_POLARITY_PO2_3	PO2_TP_POL_3 0	0	0	0	0	0	0	0
0x5C p. 171	TG_POLARITY_PO3_0	PO3_TP_POL_0 0	0	0	0	0	0	0	0
0x5D p. 172	TG_POLARITY_PO3_1	PO3_TP_POL_1 0	0	0	0	0	0	0	0
0x5E p. 172	TG_POLARITY_PO3_2	PO3_TP_POL_2 0	0	0	0	0	0	0	0
0x5F p. 172	TG_POLARITY_PO3_3	PO3_TP_POL_3 0	0	0	0	0	0	0	0
0x60 p. 172	TG_POLARITY_PO4_0	PO4_TP_POL_0 0	0	0	0	0	0	0	0
0x61 p. 172	TG_POLARITY_PO4_1	PO4_TP_POL_1 0	0	0	0	0	0	0	0
0x62 p. 172	TG_POLARITY_PO4_2	PO4_TP_POL_2 0	0	0	0	0	0	0	0
0x63 p. 173	TG_POLARITY_PO4_3	PO4_TP_POL_3 0	0	0	0	0	0	0	0
0x64 p. 173	TG_POLARITY_PO5_0	PO5_TP_POL_0 0	0	0	0	0	0	0	0
0x65 p. 173	TG_POLARITY_PO5_1	PO5_TP_POL_1 0	0	0	0	0	0	0	0
0x66 p. 173	TG_POLARITY_PO5_2	PO5_TP_POL_2 0	0	0	0	0	0	0	0
0x67 p. 173	TG_POLARITY_PO5_3	PO5_TP_POL_3 0	0	0	0	0	0	0	0
0x68 p. 174	TG_POLARITY_PO6_0	PO6_TP_POL_0 0	0	0	0	0	0	0	0
0x69 p. 174	TG_POLARITY_PO6_1	PO6_TP_POL_1 0	0	0	0	0	0	0	0
0x6A p. 174	TG_POLARITY_PO6_2	PO6_TP_POL_2 0	0	0	0	0	0	0	0
0x6B p. 174	TG_POLARITY_PO6_3	PO6_TP_POL_3 0	0	0	0	0	0	0	0
0x6C p. 174	TG_POLARITY_PO7_0	PO7_TP_POL_0 0	0	0	0	0	0	0	0
0x6D p. 175	TG_POLARITY_PO7_1	PO7_TP_POL_1 0	0	0	0	0	0	0	0
0x6E p. 175	TG_POLARITY_PO7_2	PO7_TP_POL_2 0	0	0	0	0	0	0	0
0x6F p. 175	TG_POLARITY_PO7_3	PO7_TP_POL_3 0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x70	TG_POLARITY_PO8_0	PO8_TP_POL_0							
p. 175		0	0	0	0	0	0	0	0
0x71	TG_POLARITY_PO8_1	PO8_TP_POL_1							
p. 175		0	0	0	0	0	0	0	0
0x72	TG_POLARITY_PO8_2	PO8_TP_POL_2							
p. 176		0	0	0	0	0	0	0	0
0x73	TG_POLARITY_PO8_3	PO8_TP_POL_3							
p. 176		0	0	0	0	0	0	0	0
0x74	TG_POLARITY_PO9_0	PO9_TP_POL_0							
p. 176		0	0	0	0	0	0	0	0
0x75	TG_POLARITY_PO9_1	PO9_TP_POL_1							
p. 176		0	0	0	0	0	0	0	0
0x76	TG_POLARITY_PO9_2	PO9_TP_POL_2							
p. 176		0	0	0	0	0	0	0	0
0x77	TG_POLARITY_PO9_3	PO9_TP_POL_3							
p. 177		0	0	0	0	0	0	0	0
0x78	TG_POLARITY_PO10_0	PO10_TP_POL_0							
p. 177		0	0	0	0	0	0	0	0
0x79	TG_POLARITY_PO10_1	PO10_TP_POL_1							
p. 177		0	0	0	0	0	0	0	0
0x7A	TG_POLARITY_PO10_2	PO10_TP_POL_2							
p. 177		0	0	0	0	0	0	0	0
0x7B	TG_POLARITY_PO10_3	PO10_TP_POL_3							
p. 177		0	0	0	0	0	0	0	0
0x7C	TG_REFCNT_SEL_0	—					CLAMP_CNT_SEL	BLC_CNT_SEL	FLAG_PIX1_CNT_SEL
p. 178		0	0	0	0	0	0	0	0
0x7D	TG_REFCNT_SEL_1	—		CK_TOG3_CNT_SEL	CK_TOG2_CNT_SEL	CK_TOG1_CNT_SEL	CK_MASK3_CNT_SEL	CK_MASK2_CNT_SEL	CK_MASK1_CNT_SEL
p. 178		0	0	0	0	0	0	0	0
0x7E	TG_REFCNT_SEL_2	PO7_CNT_SEL	PO6_CNT_SEL	PO5_CNT_SEL	PO4_CNT_SEL	PO3_CNT_SEL	PO2_CNT_SEL	PO1_CNT_SEL	PO0_CNT_SEL
p. 178		0	0	0	0	0	0	0	0
0x7F	TG_REFCNT_SEL_3	—					PO10_CNT_SEL	PO9_CNT_SEL	PO8_CNT_SEL
p. 179		0	0	0	0	0	0	0	0

6.4 **BANK3**—Timing Gen, Test Pattern Gen

Address	Register	7	6	5	4	3	2	1	0
0x00	BANK	DESCRIM				—	BANK		
p. 146		1	1	0	0	0	0	0	0
0x04	ASYNC0_0	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	PLL_ERROR_STS	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
p. 147		0	0	0	0	0	0	0	0
0x05	ASYNC0_1	—							OSC_DISABLE
p. 148		0	0	0	0	0	0	0	0
0x08	SFT_RESET	SFT_RESET							
p. 146		0	0	0	0	0	0	0	0
0x0C	TG_CYCPAT_CFG0_0	BLC_SEQ_SEL				FLAG_PIX1_SEQ_SEL			
p. 179		0	0	0	0	0	0	0	0
0x0D	TG_CYCPAT_CFG0_1	—				CLAMP_SEQ_SEL			
p. 180		0	0	0	0	0	0	0	0
0x0E	TG_CYCPAT_CFG0_2	CK_MASK2_SEQ_SEL				CK_MASK1_SEQ_SEL			
p. 180		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x0F	TG_CYCPAT_CFG0_3	—				CK_MASK3_SEQ_SEL			
p. 180		0	0	0	0	0	0	0	0
0x10	TG_CYCPAT_CFG1_0	CK_TOG2_SEQ_SEL				CK_TOG1_SEQ_SEL			
p. 181		0	0	0	0	0	0	0	0
0x11	TG_CYCPAT_CFG1_1	PO0_SEQ_SEL				CK_TOG3_SEQ_SEL			
p. 181		0	0	0	0	0	0	0	0
0x12	TG_CYCPAT_CFG1_2	PO2_SEQ_SEL				PO1_SEQ_SEL			
p. 181		0	0	0	0	0	0	0	0
0x13	TG_CYCPAT_CFG1_3	—				PO3_SEQ_SEL			
p. 182		0	0	0	0	0	0	0	0
0x14	TG_CYCPAT_CFG2_0	PO5_SEQ_SEL				PO4_SEQ_SEL			
p. 182		0	0	0	0	0	0	0	0
0x15	TG_CYCPAT_CFG2_1	PO7_SEQ_SEL				PO6_SEQ_SEL			
p. 182		0	0	0	0	0	0	0	0
0x16	TG_CYCPAT_CFG2_2	PO9_SEQ_SEL				PO8_SEQ_SEL			
p. 183		0	0	0	0	0	0	0	0
0x17	TG_CYCPAT_CFG2_3	—				PO10_SEQ_SEL			
p. 183		0	0	0	0	0	0	0	0
0x18	TG_TOGGLE_POINT0_0	TP0_PIXEL_0							
p. 183		0	0	0	0	0	0	0	0
0x19	TG_TOGGLE_POINT0_1	TP0_PIXEL_1							
p. 183		0	0	0	0	0	0	0	0
0x1A	TG_TOGGLE_POINT0_2	TP1_PIXEL_0							
p. 184		0	0	0	0	0	0	0	0
0x1B	TG_TOGGLE_POINT0_3	TP1_PIXEL_1							
p. 184		0	0	0	0	0	0	0	0
0x1C	TG_TOGGLE_POINT1_0	TP2_PIXEL_0							
p. 184		0	0	0	0	0	0	0	0
0x1D	TG_TOGGLE_POINT1_1	TP2_PIXEL_1							
p. 184		0	0	0	0	0	0	0	0
0x1E	TG_TOGGLE_POINT1_2	TP3_PIXEL_0							
p. 184		0	0	0	0	0	0	0	0
0x1F	TG_TOGGLE_POINT1_3	TP3_PIXEL_1							
p. 184		0	0	0	0	0	0	0	0
0x20	TG_TOGGLE_POINT2_0	TP4_PIXEL_0							
p. 185		0	0	0	0	0	0	0	0
0x21	TG_TOGGLE_POINT2_1	TP4_PIXEL_1							
p. 185		0	0	0	0	0	0	0	0
0x22	TG_TOGGLE_POINT2_2	TP5_PIXEL_0							
p. 185		0	0	0	0	0	0	0	0
0x23	TG_TOGGLE_POINT2_3	TP5_PIXEL_1							
p. 185		0	0	0	0	0	0	0	0
0x24	TG_TOGGLE_POINT3_0	TP6_PIXEL_0							
p. 185		0	0	0	0	0	0	0	0
0x25	TG_TOGGLE_POINT3_1	TP6_PIXEL_1							
p. 185		0	0	0	0	0	0	0	0
0x26	TG_TOGGLE_POINT3_2	TP7_PIXEL_0							
p. 186		0	0	0	0	0	0	0	0
0x27	TG_TOGGLE_POINT3_3	TP7_PIXEL_1							
p. 186		0	0	0	0	0	0	0	0
0x28	TG_TOGGLE_POINT4_0	TP8_PIXEL_0							
p. 186		0	0	0	0	0	0	0	0
0x29	TG_TOGGLE_POINT4_1	TP8_PIXEL_1							
p. 186		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x2A p. 186	TG_TOGGLE_POINT4_2	TP9_PIXEL_0							
		0	0	0	0	0	0	0	0
0x2B p. 186	TG_TOGGLE_POINT4_3	TP9_PIXEL_1							
		0	0	0	0	0	0	0	0
0x2C p. 187	TG_TOGGLE_POINT5_0	TP10_PIXEL_0							
		0	0	0	0	0	0	0	0
0x2D p. 187	TG_TOGGLE_POINT5_1	TP10_PIXEL_1							
		0	0	0	0	0	0	0	0
0x2E p. 187	TG_TOGGLE_POINT5_2	TP11_PIXEL_0							
		0	0	0	0	0	0	0	0
0x2F p. 187	TG_TOGGLE_POINT5_3	TP11_PIXEL_1							
		0	0	0	0	0	0	0	0
0x30 p. 187	TG_TOGGLE_POINT6_0	TP12_PIXEL_0							
		0	0	0	0	0	0	0	0
0x31 p. 187	TG_TOGGLE_POINT6_1	TP12_PIXEL_1							
		0	0	0	0	0	0	0	0
0x32 p. 188	TG_TOGGLE_POINT6_2	TP13_PIXEL_0							
		0	0	0	0	0	0	0	0
0x33 p. 188	TG_TOGGLE_POINT6_3	TP13_PIXEL_1							
		0	0	0	0	0	0	0	0
0x34 p. 188	TG_TOGGLE_POINT7_0	TP14_PIXEL_0							
		0	0	0	0	0	0	0	0
0x35 p. 188	TG_TOGGLE_POINT7_1	TP14_PIXEL_1							
		0	0	0	0	0	0	0	0
0x36 p. 188	TG_TOGGLE_POINT7_2	TP15_PIXEL_0							
		0	0	0	0	0	0	0	0
0x37 p. 188	TG_TOGGLE_POINT7_3	TP15_PIXEL_1							
		0	0	0	0	0	0	0	0
0x38 p. 189	TG_TOGGLE_POINT8_0	TP16_PIXEL_0							
		0	0	0	0	0	0	0	0
0x39 p. 189	TG_TOGGLE_POINT8_1	TP16_PIXEL_1							
		0	0	0	0	0	0	0	0
0x3A p. 189	TG_TOGGLE_POINT8_2	TP17_PIXEL_0							
		0	0	0	0	0	0	0	0
0x3B p. 189	TG_TOGGLE_POINT8_3	TP17_PIXEL_1							
		0	0	0	0	0	0	0	0
0x3C p. 189	TG_TOGGLE_POINT9_0	TP18_PIXEL_0							
		0	0	0	0	0	0	0	0
0x3D p. 189	TG_TOGGLE_POINT9_1	TP18_PIXEL_1							
		0	0	0	0	0	0	0	0
0x3E p. 190	TG_TOGGLE_POINT9_2	TP19_PIXEL_0							
		0	0	0	0	0	0	0	0
0x3F p. 190	TG_TOGGLE_POINT9_3	TP19_PIXEL_1							
		0	0	0	0	0	0	0	0
0x40 p. 190	TG_TOGGLE_POINT10_0	TP20_PIXEL_0							
		0	0	0	0	0	0	0	0
0x41 p. 190	TG_TOGGLE_POINT10_1	TP20_PIXEL_1							
		0	0	0	0	0	0	0	0
0x42 p. 190	TG_TOGGLE_POINT10_2	TP21_PIXEL_0							
		0	0	0	0	0	0	0	0
0x43 p. 191	TG_TOGGLE_POINT10_3	TP21_PIXEL_1							
		0	0	0	0	0	0	0	0
0x44 p. 191	TG_TOGGLE_POINT11_0	TP22_PIXEL_0							
		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x45	TG_TOGGLE_POINT11_1	TP22_PIXEL_1							
p. 191		0	0	0	0	0	0	0	0
0x46	TG_TOGGLE_POINT11_2	TP23_PIXEL_0							
p. 191		0	0	0	0	0	0	0	0
0x47	TG_TOGGLE_POINT11_3	TP23_PIXEL_1							
p. 191		0	0	0	0	0	0	0	0
0x48	TG_TOGGLE_POINT12_0	TP24_PIXEL_0							
p. 192		0	0	0	0	0	0	0	0
0x49	TG_TOGGLE_POINT12_1	TP24_PIXEL_1							
p. 192		0	0	0	0	0	0	0	0
0x4A	TG_TOGGLE_POINT12_2	TP25_PIXEL_0							
p. 192		0	0	0	0	0	0	0	0
0x4B	TG_TOGGLE_POINT12_3	TP25_PIXEL_1							
p. 192		0	0	0	0	0	0	0	0
0x4C	TG_TOGGLE_POINT13_0	TP26_PIXEL_0							
p. 192		0	0	0	0	0	0	0	0
0x4D	TG_TOGGLE_POINT13_1	TP26_PIXEL_1							
p. 193		0	0	0	0	0	0	0	0
0x4E	TG_TOGGLE_POINT13_2	TP27_PIXEL_0							
p. 193		0	0	0	0	0	0	0	0
0x4F	TG_TOGGLE_POINT13_3	TP27_PIXEL_1							
p. 193		0	0	0	0	0	0	0	0
0x50	TG_TOGGLE_POINT14_0	TP28_PIXEL_0							
p. 193		0	0	0	0	0	0	0	0
0x51	TG_TOGGLE_POINT14_1	TP28_PIXEL_1							
p. 193		0	0	0	0	0	0	0	0
0x52	TG_TOGGLE_POINT14_2	TP29_PIXEL_0							
p. 194		0	0	0	0	0	0	0	0
0x53	TG_TOGGLE_POINT14_3	TP29_PIXEL_1							
p. 194		0	0	0	0	0	0	0	0
0x54	TG_TOGGLE_POINT15_0	TP30_PIXEL_0							
p. 194		0	0	0	0	0	0	0	0
0x55	TG_TOGGLE_POINT15_1	TP30_PIXEL_1							
p. 194		0	0	0	0	0	0	0	0
0x56	TG_TOGGLE_POINT15_2	TP31_PIXEL_0							
p. 194		0	0	0	0	0	0	0	0
0x57	TG_TOGGLE_POINT15_3	TP31_PIXEL_1							
p. 195		0	0	0	0	0	0	0	0
0x58	TG_OUTMUX_CFG0_0	PCK1_PO_SEL				PCK1_DLY		CLKOUT1_POL	CLKOUT1_EN
p. 195		0	0	0	0	0	0	0	0
0x59	TG_OUTMUX_CFG0_1	PCK2_PO_SEL				PCK2_DLY		CLKOUT2_POL	CLKOUT2_EN
p. 195		0	0	0	0	0	0	0	0
0x5A	TG_OUTMUX_CFG0_2	PCK3_PO_SEL				PCK3_DLY		CLKOUT3_POL	CLKOUT3_EN
p. 196		0	0	0	0	0	0	0	0
0x5B	TG_OUTMUX_CFG0_3	PCK4_PO_SEL				PCK4_DLY		CLKOUT4_POL	CLKOUT4_EN
p. 196		0	0	0	0	0	0	0	0
0x5C	TG_OUTMUX_CFG1_0	PCK5_PO_SEL				PCK5_DLY		CLKOUT5_POL	CLKOUT5_EN
p. 196		0	0	0	0	0	0	0	0
0x5D	TG_OUTMUX_CFG1_1	PCK6_PO_SEL				PCK6_DLY		CLKOUT6_POL	CLKOUT6_EN
p. 197		0	0	0	0	0	0	0	0
0x5E	TG_OUTMUX_CFG1_2	PCK7_PO_SEL				PCK7_DLY		CLKOUT7_POL	CLKOUT7_EN
p. 197		0	0	0	0	0	0	0	0
0x5F	TG_OUTMUX_CFG1_3	PCK8_PO_SEL				PCK8_DLY		CLKOUT8_POL	CLKOUT8_EN
p. 198		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x60	TG_OUTMUX_CFG2_0	PCK9_PO_SEL				PCK9_DLY		CLKOUT9_POL	CLKOUT9_EN
p. 198		0	0	0	0	0	0	0	0
0x61	TG_OUTMUX_CFG2_1	PCK10_PO_SEL				PCK10_DLY		CLKOUT10_POL	CLKOUT10_EN
p. 198		0	0	0	0	0	0	0	0
0x63	TG_OUTMUX_CFG2_3	—		CLKOUT6_SRC	CLKOUT5_SRC	CLKOUT4_SRC	CLKOUT3_SRC	CLKOUT2_SRC	CLKOUT1_SRC
p. 199		0	0	0	0	0	0	0	0
0x64	DLL_CFG1_0	—		DLL_RSMP_RISE					
p. 199		0	0	1	0	0	0	0	0
0x65	DLL_CFG1_1	—		DLL_RSMP_FALL					
p. 200		0	0	1	0	0	1	1	0
0x66	DLL_CFG1_2	—		DLL_VSMP_RISE					
p. 200		0	0	1	0	1	0	0	0
0x67	DLL_CFG1_3	—		DLL_VSMP_FALL					
p. 200		0	0	0	0	1	0	0	0
0x68	DLL_CFG2_0	—		DLL_CK1_RISE					
p. 200		0	0	0	0	1	0	1	0
0x69	DLL_CFG2_1	DLL_CK1_DIV	—	DLL_CK1_FALL					
p. 201		0	0	0	1	1	0	0	1
0x6A	DLL_CFG2_2	—		DLL_CK2_RISE					
p. 201		0	0	0	1	1	0	0	1
0x6B	DLL_CFG2_3	DLL_CK2_DIV	—	DLL_CK2_FALL					
p. 201		0	0	1	0	1	0	0	0
0x6C	DLL_CFG3_0	—		DLL_CK3_RISE					
p. 201		0	0	1	0	1	0	0	0
0x6D	DLL_CFG3_1	DLL_CK3_DIV	—	DLL_CK3_FALL					
p. 202		0	0	0	0	1	0	1	0
0x6E	DLL_CFG3_2	—		DLL_CK4_RISE					
p. 202		0	0	0	0	0	0	0	0
0x6F	DLL_CFG3_3	DLL_CK4_DIV	—	DLL_CK4_FALL					
p. 202		0	0	0	0	0	0	0	0
0x70	DLL_CFG4_0	—		DLL_CK5_RISE					
p. 202		0	0	0	0	1	0	1	0
0x71	DLL_CFG4_1	DLL_CK5_DIV	—	DLL_CK5_FALL					
p. 203		0	0	1	0	1	0	0	0
0x72	DLL_CFG4_2	—		DLL_CK6_RISE					
p. 203		0	0	0	0	1	0	1	0
0x73	DLL_CFG4_3	DLL_CK6_DIV	—	DLL_CK6_FALL					
p. 203		0	0	1	0	1	0	0	0
0x74	DLL_CFG5_0	—		DLL_TGCKO_RISE					
p. 203		0	0	1	1	0	1	1	1
0x75	DLL_CFG5_1	—		DLL_AFECK_DUR					
p. 204		0	0	0	1	0	1	1	0
0x78	PGCONFIG_0	PGEN_MARCH	PGEN_PATT_SEL		PGEN_INV	—			PGEN_EN
p. 266		0	0	0	0	0	0	0	0
0x7A	PGCONFIG_2	PGEN_LVL_0							
p. 266		0	0	0	0	0	0	0	0
0x7B	PGCONFIG_3	PGEN_LVL_1							
p. 266		0	0	0	0	0	0	0	0
0x7C	PGWIDTH_0	PGEN_WIDTH1							
p. 267		0	0	0	0	0	0	0	0
0x7D	PGWIDTH_1	PGEN_WIDTH2							
p. 267		0	0	0	0	0	0	0	0

6.5 BANK6—PAD I/O, LED Control, PLL1

Address	Register	7	6	5	4	3	2	1	0
0x00	BANK	DESCRIM				—	BANK		
p. 146		1	1	0	0	0	0	0	0
0x04	ASYNC0_0	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	PLL_ERROR_STS	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
p. 147		0	0	0	0	0	0	0	0
0x05	ASYNC0_1	—							OSC_DISABLE
p. 148		0	0	0	0	0	0	0	0
0x08	SFT_RESET	SFT_RESET							
p. 146		0	0	0	0	0	0	0	0
0x0C	GPI_VAL_0	GP7_IN_STS	GP6_IN_STS	GP5_IN_STS	GP4_IN_STS	GP3_IN_STS	GP2_IN_STS	GP1_IN_STS	GP12_IN_STS
p. 208		X	X	X	X	X	X	X	X
0x0D	GPI_VAL_1	—					GP10_IN_STS	GP9_IN_STS	GP8_IN_STS
p. 209		0	0	0	0	X	X	X	X
0x0E	GPI_VAL_2	GP10_DIR	GP9_DIR	GP8_DIR	GP7_DIR	GP4_DIR	GP3_DIR	GP2_DIR	GP1_DIR
p. 209		0	0	0	0	0	0	0	0
0x0F	GPI_VAL_3	GP10_OUT_LVL	GP9_OUT_LVL	GP8_OUT_LVL	GP7_OUT_LVL	GP4_OUT_LVL	GP3_OUT_LVL	GP2_OUT_LVL	GP1_OUT_LVL
p. 210		0	0	0	0	0	0	0	0
0x10	LVDS_CFG	—						LVDS_VREF_SEL	
p. 210		0	0	0	0	0	0	0	1
0x18	CMOS_CFG_0	—	SPI_SDO_I2C_SCL_DRV_STR			SPI_SDO_I2C_SCL_PULL		SPI_MISO_I2C_SCL_HIZ_EN	SPI_MISO_I2C_SCL_IE
p. 210		0	0	0	1	1	0	0	1
0x19	CMOS_CFG_1	—	SPI_MOSI_I2C_SDA_DRV_STR			SPI_MOSI_I2C_SDA_PULL		SPI_MOSI_I2C_SDA_HIZ_EN	SPI_MOSI_I2C_SDA_IE
p. 211		0	0	0	1	1	0	0	1
0x1A	CMOS_CFG_2	—				SPI_SCK_PULL		—	SPI_SCK_IE
p. 211		0	0	0	1	1	0	0	1
0x1B	CMOS_CFG_3	—				SPI_CS_PULL		—	SPI_CS_IE
p. 212		0	0	0	1	1	0	0	1
0x1C	MCLK_CFG_0	—	MCLK_LVDS_RT_EN	—					
p. 212		0	0	1	0	0	0	0	0
0x1D	MCLK_CFG_1	—				MCLK_EXT_MCLK_EXT_P_PULL		MCLK_EXT_MCLK_EXT_P_HIZ_EN	MCLK_EXT_MCLK_EXT_P_IE
p. 212		0	0	0	1	1	0	0	1
0x1E	MCLK_CFG_2	—				MCLK_EXT_N_GPI12_PULL		MCLK_EXT_N_GPI12_HIZ_EN	MCLK_EXT_N_GPI12_IE
p. 212		0	0	0	1	1	0	0	1
0x20	CLKOUT1_4_CFG_0	—	CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_DRV_STR			CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_PULL		CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_HIZ_EN	CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_IE
p. 213		0	0	0	1	1	0	0	1
0x21	CLKOUT1_4_CFG_1	—	CLKOUT2_LEDG_EN_LEDSTART_GPIO2_DRV_STR			CLKOUT2_LEDG_EN_LEDSTART_GPIO2_PULL		CLKOUT2_LEDG_EN_LEDSTART_GPIO2_HIZ_EN	CLKOUT2_LEDG_EN_LEDSTART_GPIO2_IE
p. 213		0	0	0	1	1	0	0	1
0x22	CLKOUT1_4_CFG_2	—	CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_DRV_STR			CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_PULL		CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_HIZ_EN	CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_IE
p. 214		0	0	0	1	1	0	0	1
0x23	CLKOUT1_4_CFG_3	—	CLKOUT4_GPIO4_DRV_STR			CLKOUT4_GPIO4_PULL		CLKOUT4_GPIO4_HIZ_EN	CLKOUT4_GPIO4_IE
p. 214		0	0	0	1	1	0	0	1

Address	Register	7	6	5	4	3	2	1	0
0x24	CLKOUT5_GPI5_CFG_0	—	CLKOUT5_GPI5_DRV_STR			CLKOUT5_GPI5_PULL		CLKOUT5_GPI5_HIZ_EN	CLKOUT5_GPI5_IE
p. 214		0	0	0	1	1	0	0	1
0x25	CLKOUT5_GPI5_CFG_1	—	CLKOUT6_GPI6_DRV_STR			CLKOUT6_GPI6_PULL		CLKOUT6_GPI6_HIZ_EN	CLKOUT6_GPI6_IE
p. 215		0	0	0	1	1	0	0	1
0x26	CLKOUT5_GPI5_CFG_2	—	CLKOUT7_GPIO7_DRV_STR			CLKOUT7_GPIO7_PULL		CLKOUT7_GPIO7_HIZ_EN	CLKOUT7_GPIO7_IE
p. 215		0	0	0	1	1	0	0	1
0x27	CLKOUT5_GPI5_CFG_3	—	CLKOUT8_GPIO8_DRV_STR			CLKOUT8_GPIO8_PULL		CLKOUT8_GPIO8_HIZ_EN	CLKOUT8_GPIO8_IE
p. 216		0	0	0	1	1	0	0	1
0x28	CLKOUT9_GPI9_CFG_0	—	CLKOUT9_GPIO9_DRV_STR			CLKOUT9_GPIO9_PULL		CLKOUT9_GPIO9_HIZ_EN	CLKOUT9_GPIO9_IE
p. 216		0	0	0	1	1	0	0	1
0x29	CLKOUT9_GPI9_CFG_1	—	CLKOUT10_GPIO10_DRV_STR			CLKOUT10_GPIO10_PULL		CLKOUT10_GPIO10_HIZ_EN	CLKOUT10_GPIO10_IE
p. 216		0	0	0	1	1	0	0	1
0x2C	TGSYNC1_VSMP_EXT_CFG	—	TGSYNC1_VSMP_EXT_DRV_STR			TGSYNC1_VSMP_EXT_PULL		TGSYNC1_VSMP_EXT_HIZ_EN	TGSYNC1_VSMP_EXT_IE
p. 217		0	0	0	1	1	0	0	1
0x30	DOUT_CH1_CFG_0	—	DOUT1_P_DOUT1_DRV_STR			DOUT1_P_DOUT1_PULL		DOUT1_P_DOUT1_HIZ_EN	DOUT1_P_DOUT1_IE
p. 217		0	0	0	1	1	0	0	0
0x31	DOUT_CH1_CFG_1	—	DOUT1_N_DOUT2_DRV_STR			DOUT1_N_DOUT2_PULL		DOUT1_N_DOUT2_HIZ_EN	DOUT1_N_DOUT2_IE
p. 218		0	0	0	1	1	0	0	0
0x32	DCLKOUT_CFG_2	—				DCLKOUT_LVDS_TXDRV		DCLKOUT_LVDS_TRIM	
p. 218		0	0	0	0	1	0	1	0
0x34	DOUT_CH2_CFG_0	—	DOUT2_P_DOUT3_DRV_STR			DOUT2_P_DOUT3_PULL		DOUT2_P_DOUT3_HIZ_EN	DOUT2_P_DOUT3_IE
p. 218		0	0	0	1	1	0	0	0
0x35	DOUT_CH2_CFG_1	—	DOUT2_N_DOUT4_DRV_STR			DOUT2_N_DOUT4_PULL		DOUT2_N_DOUT4_HIZ_EN	DOUT2_N_DOUT4_IE
p. 219		0	0	0	1	1	0	0	0
0x36	DOUT_CH1_CFG_2	—				DOUT1_LVDS_TXDRV		DOUT1_LVDS_TRIM	
p. 219		0	0	0	0	1	0	1	0
0x38	DOUT_CH3_CFG_0	—	DOUT3_P_DOUT5_DRV_STR			DOUT3_P_DOUT5_PULL		DOUT3_P_DOUT5_HIZ_EN	DOUT3_P_DOUT5_IE
p. 219		0	0	0	1	1	0	0	0
0x39	DOUT_CH3_CFG_1	—	DOUT3_N_DOUT6_DRV_STR			DOUT3_N_DOUT6_PULL		DOUT3_N_DOUT6_HIZ_EN	DOUT3_N_DOUT6_IE
p. 220		0	0	0	1	1	0	0	0
0x3A	DOUT_CH2_CFG_2	—				DOUT2_LVDS_TXDRV		DOUT2_LVDS_TRIM	
p. 220		0	0	0	0	1	0	1	0
0x3C	DOUT_CH4_CFG_0	—	DOUT4_P_DOUT7_DRV_STR			DOUT4_P_DOUT7_PULL		DOUT4_P_DOUT7_HIZ_EN	DOUT4_P_DOUT7_IE
p. 221		0	0	0	1	1	0	0	0
0x3D	DOUT_CH4_CFG_1	—	DOUT4_N_DOUT8_DRV_STR			DOUT4_N_DOUT8_PULL		DOUT4_N_DOUT8_HIZ_EN	DOUT4_N_DOUT8_IE
p. 221		0	0	0	1	1	0	0	0
0x3E	DOUT_CH3_CFG_2	—				DOUT3_LVDS_TXDRV		DOUT3_LVDS_TRIM	
p. 221		0	0	0	0	1	0	1	0
0x40	DOUT_CH5_CFG_0	—	DOUT5_P_DOUT9_DRV_STR			DOUT5_P_DOUT9_PULL		DOUT5_P_DOUT9_HIZ_EN	DOUT5_P_DOUT9_IE
p. 222		0	0	0	1	1	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x41	DOUT_CH5_CFG_1	—	DOUT5_N_DOUT10_DRV_STR			DOUT5_N_DOUT10_PULL		DOUT5_N_DOUT10_HIZ_EN	DOUT5_N_DOUT10_IE
p. 222		0	0	0	1	1	0	0	0
0x42	DOUT_CH4_CFG_2	—				DOUT4_LVDS_TXDRV		DOUT4_LVDS_TRIM	
p. 223		0	0	0	0	1	0	1	0
0x44	DCLKOUT_CFG_0	—	DCLKOUT_P_DCLKOUT1_DOUT7_DRV_STR			DCLKOUT_P_DCLKOUT1_DOUT7_PULL		DCLKOUT_P_DCLKOUT1_DOUT7_HIZ_EN	DCLKOUT_P_DCLKOUT1_DOUT7_IE
p. 223		0	0	0	1	1	0	0	0
0x45	DCLKOUT_CFG_1	—	DCLKOUT_N_DCLKOUT2_DOUT8_DRV_STR			DCLKOUT_N_DCLKOUT2_DOUT8_PULL		DCLKOUT_N_DCLKOUT2_DOUT8_HIZ_EN	DCLKOUT_N_DCLKOUT2_DOUT8_IE
p. 223		0	0	0	1	1	0	0	0
0x46	DOUT_CH5_CFG_2	—				DOUT5_LVDS_TXDRV		DOUT5_LVDS_TRIM	
p. 224		0	0	0	0	1	0	1	0
0x48	LED_CTRL_CONFIG_0	—				LED_CTRL_SRC	LEDB_EN	LEDG_EN	LEDR_EN
p. 267		0	0	0	0	0	0	0	0
0x49	LED_CTRL_CONFIG_1	—				LED_RAMP_TIME			
p. 267		0	0	0	0	0	0	0	0
0x4A	LED_CTRL_CONFIG_2	LED_RAMP_BOOST		LEDB_COARSE		LEDG_COARSE		LEDR_COARSE	
p. 268		0	0	0	0	0	0	0	0
0x4C	LEDX_FINE_0	LEDR_FINE							
p. 268		0	0	0	0	0	0	0	0
0x4D	LEDX_FINE_1	LEDG_FINE							
p. 268		0	0	0	0	0	0	0	0
0x4E	LEDX_FINE_2	LEDB_FINE							
p. 268		0	0	0	0	0	0	0	0
0x50	LED_CTRL_STATUS	—			LED_MAX_CURRENT_ERR	LED_CTRL_SHORT_ERR	—		
p. 269		0	0	0	0	0	0	0	0
0x60	DPLL1_DFLL_DIVIDER_CTRL_0	PLL1_OUTPUT1_DIV_0							—
p. 269		0	0	1	0	0	0	0	0
0x61	DPLL1_DFLL_DIVIDER_CTRL_1	PLL1_VCO_RANGE				—		PLL1_OUTPUT1_DIV_1	
p. 269		0	0	0	0	0	0	0	0
0x62	DPLL1_DFLL_DIVIDER_CTRL_2	PLL1_OUTPUT2_DIV_0							PLL1_OUTPUT2_EN
p. 270		0	0	1	0	0	0	0	0
0x63	DPLL1_DFLL_DIVIDER_CTRL_3	PLL1_REFCLK_DIV_RATIO				PLL1_REFCLK_DIV_BYPASS	—	PLL1_OUTPUT2_DIV_1	
p. 270		0	0	0	0	1	0	0	0
0x64	DPLL1_DFLL_FEEDBACK_RATIO_0	PLL1_RATIO_0							
p. 270		0	0	0	0	0	0	0	0
0x65	DPLL1_DFLL_FEEDBACK_RATIO_1	PLL1_RATIO_1							
p. 270		0	0	0	0	0	0	0	0
0x66	DPLL1_DFLL_FEEDBACK_RATIO_2	PLL1_RATIO_2							
p. 270		0	0	0	1	0	0	0	0
0x67	DPLL1_DFLL_FEEDBACK_RATIO_3	—		PLL1_MODE	PLL1_RATIO_3				
p. 271		0	0	0	0	0	0	0	0
0x68	DPLL1_DFLL_FEATURES_0	PLL1_VCO_GAIN				PLL1_CP_IBIAS			PLL1_PHASE_DET_PAUSE_EN
p. 271		1	0	0	0	0	1	0	0
0x69	DPLL1_DFLL_FEATURES_1	—				PLL1_FILT			
p. 271		0	0	0	0	0	0	0	1

6.6 BANK7—Digital Gain

Address	Register	7	6	5	4	3	2	1	0
0x00	BANK	DESCRIM				—	BANK		
p. 146		1	1	0	0	0	0	0	0
0x04	ASYNC0_0	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	PLL_ERROR_STS	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
p. 147		0	0	0	0	0	0	0	0
0x05	ASYNC0_1	—							OSC_DISABLE
p. 148		0	0	0	0	0	0	0	0
0x08	SFT_RESET	SFT_RESET							
p. 146		0	0	0	0	0	0	0	0
0x0C	DGAIN_SEQ01_CH1_0	CH1_SEQ0_DGAIN_0							
p. 254		0	0	0	0	0	0	0	0
0x0D	DGAIN_SEQ01_CH1_1	—				CH1_SEQ0_DGAIN_1			
p. 254		0	0	0	0	1	0	0	0
0x0E	DGAIN_SEQ01_CH1_2	CH1_SEQ1_DGAIN_0							
p. 254		0	0	0	0	0	0	0	0
0x0F	DGAIN_SEQ01_CH1_3	—				CH1_SEQ1_DGAIN_1			
p. 255		0	0	0	0	1	0	0	0
0x10	DGAIN_SEQ23_CH1_0	CH1_SEQ2_DGAIN_0							
p. 255		0	0	0	0	0	0	0	0
0x11	DGAIN_SEQ23_CH1_1	—				CH1_SEQ2_DGAIN_1			
p. 255		0	0	0	0	1	0	0	0
0x12	DGAIN_SEQ23_CH1_2	CH1_SEQ3_DGAIN_0							
p. 255		0	0	0	0	0	0	0	0
0x13	DGAIN_SEQ23_CH1_3	—				CH1_SEQ3_DGAIN_1			
p. 256		0	0	0	0	1	0	0	0
0x14	DGAIN_SEQ01_CH2_0	CH2_SEQ0_DGAIN_0							
p. 256		0	0	0	0	0	0	0	0
0x15	DGAIN_SEQ01_CH2_1	—				CH2_SEQ0_DGAIN_1			
p. 256		0	0	0	0	1	0	0	0
0x16	DGAIN_SEQ01_CH2_2	CH2_SEQ1_DGAIN_0							
p. 256		0	0	0	0	0	0	0	0
0x17	DGAIN_SEQ01_CH2_3	—				CH2_SEQ1_DGAIN_1			
p. 257		0	0	0	0	1	0	0	0
0x18	DGAIN_SEQ23_CH2_0	CH2_SEQ2_DGAIN_0							
p. 257		0	0	0	0	0	0	0	0
0x19	DGAIN_SEQ23_CH2_1	—				CH2_SEQ2_DGAIN_1			
p. 257		0	0	0	0	1	0	0	0
0x1A	DGAIN_SEQ23_CH2_2	CH2_SEQ3_DGAIN_0							
p. 257		0	0	0	0	0	0	0	0
0x1B	DGAIN_SEQ23_CH2_3	—				CH2_SEQ3_DGAIN_1			
p. 258		0	0	0	0	1	0	0	0
0x1C	DGAIN_SEQ01_CH3_0	CH3_SEQ0_DGAIN_0							
p. 258		0	0	0	0	0	0	0	0
0x1D	DGAIN_SEQ01_CH3_1	—				CH3_SEQ0_DGAIN_1			
p. 258		0	0	0	0	1	0	0	0
0x1E	DGAIN_SEQ01_CH3_2	CH3_SEQ1_DGAIN_0							
p. 258		0	0	0	0	0	0	0	0
0x1F	DGAIN_SEQ01_CH3_3	—				CH3_SEQ1_DGAIN_1			
p. 259		0	0	0	0	1	0	0	0
0x20	DGAIN_SEQ23_CH3_0	CH3_SEQ2_DGAIN_0							
p. 259		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x21	DGAIN_SEQ23_CH3_1	—				CH3_SEQ2_DGAIN_1			
p. 259		0	0	0	0	1	0	0	0
0x22	DGAIN_SEQ23_CH3_2	CH3_SEQ3_DGAIN_0							
p. 259		0	0	0	0	0	0	0	0
0x23	DGAIN_SEQ23_CH3_3	—				CH3_SEQ3_DGAIN_1			
p. 260		0	0	0	0	1	0	0	0
0x24	DGAIN_SEQ01_CH4_0	CH4_SEQ0_DGAIN_0							
p. 260		0	0	0	0	0	0	0	0
0x25	DGAIN_SEQ01_CH4_1	—				CH4_SEQ0_DGAIN_1			
p. 260		0	0	0	0	1	0	0	0
0x26	DGAIN_SEQ01_CH4_2	CH4_SEQ1_DGAIN_0							
p. 260		0	0	0	0	0	0	0	0
0x27	DGAIN_SEQ01_CH4_3	—				CH4_SEQ1_DGAIN_1			
p. 261		0	0	0	0	1	0	0	0
0x28	DGAIN_SEQ23_CH4_0	CH4_SEQ2_DGAIN_0							
p. 261		0	0	0	0	0	0	0	0
0x29	DGAIN_SEQ23_CH4_1	—				CH4_SEQ2_DGAIN_1			
p. 261		0	0	0	0	1	0	0	0
0x2A	DGAIN_SEQ23_CH4_2	CH4_SEQ3_DGAIN_0							
p. 261		0	0	0	0	0	0	0	0
0x2B	DGAIN_SEQ23_CH4_3	—				CH4_SEQ3_DGAIN_1			
p. 262		0	0	0	0	1	0	0	0
0x2C	DGAIN_SEQ01_CH5_0	CH5_SEQ0_DGAIN_0							
p. 262		0	0	0	0	0	0	0	0
0x2D	DGAIN_SEQ01_CH5_1	—				CH5_SEQ0_DGAIN_1			
p. 262		0	0	0	0	1	0	0	0
0x2E	DGAIN_SEQ01_CH5_2	CH5_SEQ1_DGAIN_0							
p. 262		0	0	0	0	0	0	0	0
0x2F	DGAIN_SEQ01_CH5_3	—				CH5_SEQ1_DGAIN_1			
p. 263		0	0	0	0	1	0	0	0
0x30	DGAIN_SEQ23_CH5_0	CH5_SEQ2_DGAIN_0							
p. 263		0	0	0	0	0	0	0	0
0x31	DGAIN_SEQ23_CH5_1	—				CH5_SEQ2_DGAIN_1			
p. 263		0	0	0	0	1	0	0	0
0x32	DGAIN_SEQ23_CH5_2	CH5_SEQ3_DGAIN_0							
p. 263		0	0	0	0	0	0	0	0
0x33	DGAIN_SEQ23_CH5_3	—				CH5_SEQ3_DGAIN_1			
p. 264		0	0	0	0	1	0	0	0
0x34	DGAIN_SEQ01_CH6_0	CH6_SEQ0_DGAIN_0							
p. 264		0	0	0	0	0	0	0	0
0x35	DGAIN_SEQ01_CH6_1	—				CH6_SEQ0_DGAIN_1			
p. 264		0	0	0	0	1	0	0	0
0x36	DGAIN_SEQ01_CH6_2	CH6_SEQ1_DGAIN_0							
p. 264		0	0	0	0	0	0	0	0
0x37	DGAIN_SEQ01_CH6_3	—				CH6_SEQ1_DGAIN_1			
p. 265		0	0	0	0	1	0	0	0
0x38	DGAIN_SEQ23_CH6_0	CH6_SEQ2_DGAIN_0							
p. 265		0	0	0	0	0	0	0	0
0x39	DGAIN_SEQ23_CH6_1	—				CH6_SEQ2_DGAIN_1			
p. 265		0	0	0	0	1	0	0	0
0x3A	DGAIN_SEQ23_CH6_2	CH6_SEQ3_DGAIN_0							
p. 265		0	0	0	0	0	0	0	0
0x3B	DGAIN_SEQ23_CH6_3	—				CH6_SEQ3_DGAIN_1			
p. 266		0	0	0	0	1	0	0	0

7 Register Quick Reference—Flat Register Mode (I2C or SPI)

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

- This register view is for the CS82L46 6-channel imaging AFE/ADC, using the flat host-interface configuration.
- The register field default values are established on power-up and after soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 8 bits wide.
- All visible fields are read/write except where indicated with the following shading:

Read/write access   Read-only access   Write-only access

Table 7-1. Block Base Addresses

Base Address	Block Name	Register Quick Reference	Register Description Reference
0x000 0000	**SW_RESET**—Software Reset and Hardware ID	Section 7.1	Section 8.1
0x000 0100	**CTRL_ASYNC**—Async control	Section 7.2	Section 8.2
0x000 0200	**CCM**—Device Clocking and Sample Rate Control	Section 7.3	Section 8.3
0x000 0300	**MSM**—Power, Global, and Error Control	Section 7.4	Section 8.4
0x000 0400	**TIM_GEN**—Sensor Timing Generator	Section 7.5	Section 8.5
0x000 0500	**OP_FORMAT**—Output Formatter	Section 7.6	Section 8.6
0x000 0600	**PAD_INTF**—Pad Interface I/O Control	Section 7.7	Section 8.7
0x000 0700	**DAC_CTRL**—DAC_CTRL	Section 7.8	Section 8.8
0x000 0800	**PGA_CTRL**—PGA_CTRL	Section 7.9	Section 8.9
0x000 0900	**BLC_CTRL**—BLC_CTRL	Section 7.10	Section 8.10
0x000 0A00	**SARADC_1**—SARADC_1	Section 7.11	Section 8.11
0x000 0B00	**SARADC_2**—SARADC_2	Section 7.12	Section 8.12
0x000 0C00	**SARADC_3**—SARADC_3	Section 7.13	Section 8.13
0x000 0D00	**SARADC_4**—SARADC_4	Section 7.14	Section 8.14
0x000 0E00	**SARADC_5**—SARADC_5	Section 7.15	Section 8.15
0x000 0F00	**SARADC_6**—SARADC_6	Section 7.16	Section 8.16
0x000 1000	**AGC_TOP**—Digital Gain Control	Section 7.17	Section 8.17
0x000 1100	**PAT_GEN**—Test pattern generator	Section 7.18	Section 8.18
0x000 1500	**LED_CTRL**—LED Control	Section 7.19	Section 8.19
0x000 1700	**DPLL1**—DPLL1	Section 7.20	Section 8.20

7.1 SW_RESET—Software Reset and Hardware ID

Address	Register	7	6	5	4	3	2	1	0
0x000 0000	BANK	DESCRIM				—	BANK		
p. 146		1	1	0	0	0	0	0	0
0x000 0008	SFT_RESET	SFT_RESET							
p. 146		0	0	0	0	0	0	0	0
0x000 000C	DEVID_0	DEVID_0							
p. 146		0	1	0	0	0	1	1	0
0x000 000D	DEVID_1	DEVID_1							
p. 147		0	0	1	0	1	0	1	0
0x000 000E	DEVID_2	DEVID_2							
p. 147		0	0	0	0	1	0	0	0
0x000 0010	REVID	AREVID				MTLREVID			
p. 147		1	0	1	1	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 0014	RELID	RELID							
p. 147		0	0	0	0	0	0	0	0

7.2 CTRL_ASYNC—Async control

Address	Register	7	6	5	4	3	2	1	0
0x000 0100	ASYNC0_0	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	PLL_ERROR_STS	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
p. 147		0	0	0	0	0	0	0	0
0x000 0101	ASYNC0_1	—							OSC_DISABLE
p. 148		0	0	0	0	0	0	0	0

7.3 CCM—Device Clocking and Sample Rate Control

Address	Register	7	6	5	4	3	2	1	0
0x000 0200	DEVICE_CLK_CFG_0	PIXEL_SAMPLE_RATE							
p. 148		0	1	1	1	1	0	0	0
0x000 0201	DEVICE_CLK_CFG_1	—			EXT_AFECK_DUR			CLOCK_CFG_MODE	
p. 148		0	0	0	0	0	0	0	1
0x000 0202	DEVICE_CLK_CFG_2	—						PLL2_AUTO	PLL1_AUTO
p. 149		0	0	0	0	0	0	1	1
0x000 0203	DEVICE_CLK_CFG_3	PLL2_SS_FREQ			PLL2_SS_MAG				PLL2_SS_EN
p. 149		0	0	0	0	0	0	0	0
0x000 0206	DEVICE_CLK_CFG2_2	PLL2_SS_REF_FREQ_0							
p. 149		0	0	0	0	0	0	0	0
0x000 0207	DEVICE_CLK_CFG2_3	DOUT_READY_EN	—		MCLK_EXT_SS	—		PLL2_SS_REF_FREQ_1	
p. 149		1	0	0	0	0	0	0	0
0x000 0208	MCLK_FILT_CFG_0	MCLK_MASK_DLY_0							
p. 150		0	0	0	0	0	0	0	1
0x000 0209	MCLK_FILT_CFG_1	MCLK_MASK_DLY_1							
p. 150		0	0	0	0	0	0	0	0
0x000 020A	MCLK_FILT_CFG_2	MCLK_MASK_POL	MCLK_MASK_EN	MCLK_MASK_DUR					
p. 150		0	0	0	0	0	0	0	1
0x000 020B	MCLK_FILT_CFG_3	MCLK_MASK_CLK_DIV			MCLK_MASK_OPF_RST	—	MCLK_MASK_SRC		
p. 151		0	0	0	0	0	0	0	0

7.4 MSM—Power, Global, and Error Control

Address	Register	7	6	5	4	3	2	1	0
0x000 0300	DEVICE_CTRL_0	—	SHARED_BUS_MODE	GPI12_DOUT_CTRL	—	COMPLETE_LINE	ACTIVE_EN	READY_EN	MSM_EN
p. 151		0	0	0	0	0	0	0	1
0x000 0301	DEVICE_CTRL_1	TEMP_ERROR_RST_MASK	—	TEMP_ERROR_CLR	—				
p. 152		0	0	0	0	0	0	0	0
0x000 0304	RLCDAC_CTRL_0	—							VBIAS_EN
p. 152		0	0	0	0	0	0	0	0
0x000 0305	RLCDAC_CTRL_1	—			VBIAS_LVL				
p. 152		0	0	0	0	0	0	0	0
0x000 0306	RLCDAC_CTRL_2	—				VBIAS_ISEL_BOOST	VBIAS_ISEL		VBIAS_REF
p. 152		0	0	0	0	0	0	0	1

Address	Register	7	6	5	4	3	2	1	0
0x000 0310	DEVICE_STATUS_0	ERROR_STS	—	ACTIVE_STS	READY_STS	—		IDLE_STS	STARTUP_STS
p. 153		0	0	0	0	0	0	0	0
0x000 0312	DEVICE_STATUS_2	VDDA_STS	—						
p. 153		0	0	0	0	0	1	0	0

7.5 TIM_GEN—Sensor Timing Generator

Address	Register	7	6	5	4	3	2	1	0
0x000 0400	TG_CONFIG1_0	VSMP_EXT_POL	EXTERNAL_MODE_TG_EN	CDS_EN	CLAMP_EN	CLAMP_MODE		TGSYNC_MODE	EXTERNAL_MODE_EN
p. 153		0	0	0	0	0	0	0	1
0x000 0401	TG_CONFIG1_1	INIT_SEQ_STATE		VSMP_EXT_DLY					EXTERNAL_MODE_SEL
p. 154		0	0	0	0	0	0	0	0
0x000 0402	TG_CONFIG1_2	—	TGSYNC_SINGLE_SEQ	NUM_SEQ_STATES		RSMP_EXT_DLY			
p. 154		0	0	0	0	0	0	0	1
0x000 0403	TG_CONFIG1_3	—		CH6_CLAMP_OVRD	CH5_CLAMP_OVRD	CH4_CLAMP_OVRD	CH3_CLAMP_OVRD	CH2_CLAMP_OVRD	CH1_CLAMP_OVRD
p. 155		0	0	0	0	0	0	0	0
0x000 040C	TG_STATUS	—						SEQ_STATE_STS	
p. 155		0	0	0	0	0	0	0	0
0x000 0410	TG_CONFIG2_0	—		LEDSTART_POL	LEDSTART_SEQ_INIT	TGSYNC_ASYNC	TGSYNC_IN_POL	TGSYNC_IN_SRC	
p. 155		0	0	0	0	0	1	0	0
0x000 0411	TG_CONFIG2_1	—	TGSYNC_OUT_DUR			TGSYNC_IN_OFFSET			
p. 156		0	0	1	0	0	0	0	0
0x000 0412	TG_CONFIG2_2	—	TGSYNC_FILT_STAGE			TGSYNC_FILT_DECM			TGSYNC_FILT_EN
p. 156		0	1	0	0	0	1	1	0
0x000 0413	TG_CONFIG2_3	—		TP_SEC_OFFSET					
p. 156		0	0	0	0	0	0	0	0
0x000 0414	TG_CONFIG3_0	LEDG_PO_SEL				LEDR_PO_SEL			
p. 157		0	0	0	1	0	0	0	0
0x000 0415	TG_CONFIG3_1	DC_PO_2ND_PULSE	NUM_DC_PO			LEDB_PO_SEL			
p. 157		0	0	0	0	0	0	1	0
0x000 0416	TG_CONFIG3_2	FLAG_DEN2_PO_SEL				FLAG_DEN1_PO_SEL			
p. 158		1	0	0	1	1	0	0	1
0x000 0417	TG_CONFIG3_3	—		FLAG_PIX2_PO_EDGE		FLAG_PIX2_PO_SEL			
p. 158		0	0	0	0	1	0	1	0
0x000 0418	SEQ_DURATION0_0	SEQ_STATE0_LEN_0							
p. 158		0	0	0	0	0	0	0	0
0x000 0419	SEQ_DURATION0_1	SEQ_STATE0_LEN_1							
p. 158		0	0	0	0	1	0	0	0
0x000 041A	SEQ_DURATION0_2	SEQ_STATE1_LEN_0							
p. 159		0	0	0	0	0	0	0	0
0x000 041B	SEQ_DURATION0_3	SEQ_STATE1_LEN_1							
p. 159		0	0	0	0	1	0	0	0
0x000 041C	SEQ_DURATION1_0	SEQ_STATE2_LEN_0							
p. 159		0	0	0	0	0	0	0	0
0x000 041D	SEQ_DURATION1_1	SEQ_STATE2_LEN_1							
p. 159		0	0	0	0	1	0	0	0
0x000 041E	SEQ_DURATION1_2	SEQ_STATE3_LEN_0							
p. 159		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 041F	SEQ_DURATION1_3	SEQ_STATE3_LEN_1							
p. 159		0	0	0	0	1	0	0	0
0x000 0420	TG_TIMING_CFG0_0	CK_MASK1_START_0							
p. 160		0	0	0	0	0	0	0	0
0x000 0421	TG_TIMING_CFG0_1	CK_MASK1_START_1							
p. 160		0	0	0	0	0	0	0	0
0x000 0422	TG_TIMING_CFG0_2	CK_MASK1_END_0							
p. 160		0	0	0	0	0	0	0	0
0x000 0423	TG_TIMING_CFG0_3	CK_MASK1_END_1							
p. 160		0	0	0	0	0	0	0	0
0x000 0424	TG_TIMING_CFG1_0	CK_MASK2_START_0							
p. 160		0	0	0	0	0	0	0	0
0x000 0425	TG_TIMING_CFG1_1	CK_MASK2_START_1							
p. 161		0	0	0	0	0	0	0	0
0x000 0426	TG_TIMING_CFG1_2	CK_MASK2_END_0							
p. 161		0	0	0	0	0	0	0	0
0x000 0427	TG_TIMING_CFG1_3	CK_MASK2_END_1							
p. 161		0	0	0	0	0	0	0	0
0x000 0428	TG_TIMING_CFG2_0	CK_MASK3_START_0							
p. 161		0	0	0	0	0	0	0	0
0x000 0429	TG_TIMING_CFG2_1	CK_MASK3_START_1							
p. 161		0	0	0	0	0	0	0	0
0x000 042A	TG_TIMING_CFG2_2	CK_MASK3_END_0							
p. 162		0	0	0	0	0	0	0	0
0x000 042B	TG_TIMING_CFG2_3	CK_MASK3_END_1							
p. 162		0	0	0	0	0	0	0	0
0x000 042C	TG_TIMING_CFG3_0	CLAMP_START_0							
p. 162		0	0	0	0	0	0	0	0
0x000 042D	TG_TIMING_CFG3_1	CLAMP_START_1							
p. 162		0	0	0	0	0	0	0	0
0x000 042E	TG_TIMING_CFG3_2	CLAMP_END_0							
p. 162		0	0	0	0	0	0	0	0
0x000 042F	TG_TIMING_CFG3_3	CLAMP_END_1							
p. 163		0	0	0	0	0	0	0	0
0x000 0434	TG_TIMING_CFG5_0	FLAG_PIX1_PIXEL1_0							
p. 163		1	1	1	1	1	1	1	1
0x000 0435	TG_TIMING_CFG5_1	FLAG_PIX1_PIXEL1_1							
p. 163		1	1	1	1	1	1	1	1
0x000 0436	TG_TIMING_CFG5_2	FLAG_PIX1_PIXEL2_0							
p. 163		1	1	1	1	1	1	1	1
0x000 0437	TG_TIMING_CFG5_3	FLAG_PIX1_PIXEL2_1							
p. 163		1	1	1	1	1	1	1	1
0x000 0438	TG_TIMING_CFG6_0	FLAG_PIX1_PIXEL3_0							
p. 164		1	1	1	1	1	1	1	1
0x000 0439	TG_TIMING_CFG6_1	FLAG_PIX1_PIXEL3_1							
p. 164		1	1	1	1	1	1	1	1
0x000 043A	TG_TIMING_CFG6_2	FLAG_PIX1_PIXEL4_0							
p. 164		1	1	1	1	1	1	1	1
0x000 043B	TG_TIMING_CFG6_3	FLAG_PIX1_PIXEL4_1							
p. 164		1	1	1	1	1	1	1	1
0x000 043C	TG_TIMING_CFG7_0	—	ACYC_PO_POL	ACYC_PO_SEL				ACYC_MODE	ACYC_EN
p. 164		0	0	0	0	0	0	0	0
0x000 043D	TG_TIMING_CFG7_1	ACYC_DELAY							
p. 165		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 043E	TG_TIMING_CFG7_2	BLC_START_0							
p. 165		0	0	0	0	0	0	0	0
0x000 043F	TG_TIMING_CFG7_3	BLC_START_1							
p. 165		0	0	0	0	0	0	0	0
0x000 0440	TG_TIMING_CFG8_0	PO7_INIT_LVL	PO6_INIT_LVL	PO5_INIT_LVL	PO4_INIT_LVL	PO3_INIT_LVL	PO2_INIT_LVL	PO1_INIT_LVL	PO0_INIT_LVL
p. 165		0	0	0	0	0	0	0	0
0x000 0441	TG_TIMING_CFG8_1	—		CK_TOG3_INIT_LVL	CK_TOG2_INIT_LVL	CK_TOG1_INIT_LVL	PO10_INIT_LVL	PO9_INIT_LVL	PO8_INIT_LVL
p. 166		0	0	0	0	0	0	0	0
0x000 0442	TG_TIMING_CFG8_2	FIFO_RESET_DLY	PO10_DC_INIT_LVL	PO9_DC_INIT_LVL	PO8_DC_INIT_LVL	PO7_DC_INIT_LVL	PO6_DC_INIT_LVL	PO5_DC_INIT_LVL	PGEN_CNT_SEL
p. 167		1	0	0	0	0	0	0	1
0x000 0443	TG_TIMING_CFG8_3	FIFO_BLANK_DUR					—		FIFO_RESET_CTRL
p. 167		1	1	0	0	1	0	0	0
0x000 0444	TG_POLARITY_T1_0	CK_TOG1_TP_POL_0							
p. 167		0	0	0	0	0	0	0	0
0x000 0445	TG_POLARITY_T1_1	CK_TOG1_TP_POL_1							
p. 168		0	0	0	0	0	0	0	0
0x000 0446	TG_POLARITY_T1_2	CK_TOG1_TP_POL_2							
p. 168		0	0	0	0	0	0	0	0
0x000 0447	TG_POLARITY_T1_3	CK_TOG1_TP_POL_3							
p. 168		0	0	0	0	0	0	0	0
0x000 0448	TG_POLARITY_T2_0	CK_TOG2_TP_POL_0							
p. 168		0	0	0	0	0	0	0	0
0x000 0449	TG_POLARITY_T2_1	CK_TOG2_TP_POL_1							
p. 168		0	0	0	0	0	0	0	0
0x000 044A	TG_POLARITY_T2_2	CK_TOG2_TP_POL_2							
p. 168		0	0	0	0	0	0	0	0
0x000 044B	TG_POLARITY_T2_3	CK_TOG2_TP_POL_3							
p. 169		0	0	0	0	0	0	0	0
0x000 044C	TG_POLARITY_T3_0	CK_TOG3_TP_POL_0							
p. 169		0	0	0	0	0	0	0	0
0x000 044D	TG_POLARITY_T3_1	CK_TOG3_TP_POL_1							
p. 169		0	0	0	0	0	0	0	0
0x000 044E	TG_POLARITY_T3_2	CK_TOG3_TP_POL_2							
p. 169		0	0	0	0	0	0	0	0
0x000 044F	TG_POLARITY_T3_3	CK_TOG3_TP_POL_3							
p. 169		0	0	0	0	0	0	0	0
0x000 0450	TG_POLARITY_PO0_0	PO0_TP_POL_0							
p. 169		0	0	0	0	0	0	0	0
0x000 0451	TG_POLARITY_PO0_1	PO0_TP_POL_1							
p. 170		0	0	0	0	0	0	0	0
0x000 0452	TG_POLARITY_PO0_2	PO0_TP_POL_2							
p. 170		0	0	0	0	0	0	0	0
0x000 0453	TG_POLARITY_PO0_3	PO0_TP_POL_3							
p. 170		0	0	0	0	0	0	0	0
0x000 0454	TG_POLARITY_PO1_0	PO1_TP_POL_0							
p. 170		0	0	0	0	0	0	0	0
0x000 0455	TG_POLARITY_PO1_1	PO1_TP_POL_1							
p. 170		0	0	0	0	0	0	0	0
0x000 0456	TG_POLARITY_PO1_2	PO1_TP_POL_2							
p. 170		0	0	0	0	0	0	0	0
0x000 0457	TG_POLARITY_PO1_3	PO1_TP_POL_3							
p. 171		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 0458	TG_POLARITY_PO2_0	PO2_TP_POL_0							
p. 171		0	0	0	0	0	0	0	0
0x000 0459	TG_POLARITY_PO2_1	PO2_TP_POL_1							
p. 171		0	0	0	0	0	0	0	0
0x000 045A	TG_POLARITY_PO2_2	PO2_TP_POL_2							
p. 171		0	0	0	0	0	0	0	0
0x000 045B	TG_POLARITY_PO2_3	PO2_TP_POL_3							
p. 171		0	0	0	0	0	0	0	0
0x000 045C	TG_POLARITY_PO3_0	PO3_TP_POL_0							
p. 171		0	0	0	0	0	0	0	0
0x000 045D	TG_POLARITY_PO3_1	PO3_TP_POL_1							
p. 172		0	0	0	0	0	0	0	0
0x000 045E	TG_POLARITY_PO3_2	PO3_TP_POL_2							
p. 172		0	0	0	0	0	0	0	0
0x000 045F	TG_POLARITY_PO3_3	PO3_TP_POL_3							
p. 172		0	0	0	0	0	0	0	0
0x000 0460	TG_POLARITY_PO4_0	PO4_TP_POL_0							
p. 172		0	0	0	0	0	0	0	0
0x000 0461	TG_POLARITY_PO4_1	PO4_TP_POL_1							
p. 172		0	0	0	0	0	0	0	0
0x000 0462	TG_POLARITY_PO4_2	PO4_TP_POL_2							
p. 172		0	0	0	0	0	0	0	0
0x000 0463	TG_POLARITY_PO4_3	PO4_TP_POL_3							
p. 173		0	0	0	0	0	0	0	0
0x000 0464	TG_POLARITY_PO5_0	PO5_TP_POL_0							
p. 173		0	0	0	0	0	0	0	0
0x000 0465	TG_POLARITY_PO5_1	PO5_TP_POL_1							
p. 173		0	0	0	0	0	0	0	0
0x000 0466	TG_POLARITY_PO5_2	PO5_TP_POL_2							
p. 173		0	0	0	0	0	0	0	0
0x000 0467	TG_POLARITY_PO5_3	PO5_TP_POL_3							
p. 173		0	0	0	0	0	0	0	0
0x000 0468	TG_POLARITY_PO6_0	PO6_TP_POL_0							
p. 174		0	0	0	0	0	0	0	0
0x000 0469	TG_POLARITY_PO6_1	PO6_TP_POL_1							
p. 174		0	0	0	0	0	0	0	0
0x000 046A	TG_POLARITY_PO6_2	PO6_TP_POL_2							
p. 174		0	0	0	0	0	0	0	0
0x000 046B	TG_POLARITY_PO6_3	PO6_TP_POL_3							
p. 174		0	0	0	0	0	0	0	0
0x000 046C	TG_POLARITY_PO7_0	PO7_TP_POL_0							
p. 174		0	0	0	0	0	0	0	0
0x000 046D	TG_POLARITY_PO7_1	PO7_TP_POL_1							
p. 175		0	0	0	0	0	0	0	0
0x000 046E	TG_POLARITY_PO7_2	PO7_TP_POL_2							
p. 175		0	0	0	0	0	0	0	0
0x000 046F	TG_POLARITY_PO7_3	PO7_TP_POL_3							
p. 175		0	0	0	0	0	0	0	0
0x000 0470	TG_POLARITY_PO8_0	PO8_TP_POL_0							
p. 175		0	0	0	0	0	0	0	0
0x000 0471	TG_POLARITY_PO8_1	PO8_TP_POL_1							
p. 175		0	0	0	0	0	0	0	0
0x000 0472	TG_POLARITY_PO8_2	PO8_TP_POL_2							
p. 176		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 0473 p. 176	TG_POLARITY_PO8_3	PO8_TP_POL_3 0	0	0	0	0	0	0	0
0x000 0474 p. 176	TG_POLARITY_PO9_0	PO9_TP_POL_0 0	0	0	0	0	0	0	0
0x000 0475 p. 176	TG_POLARITY_PO9_1	PO9_TP_POL_1 0	0	0	0	0	0	0	0
0x000 0476 p. 176	TG_POLARITY_PO9_2	PO9_TP_POL_2 0	0	0	0	0	0	0	0
0x000 0477 p. 177	TG_POLARITY_PO9_3	PO9_TP_POL_3 0	0	0	0	0	0	0	0
0x000 0478 p. 177	TG_POLARITY_PO10_0	PO10_TP_POL_0 0	0	0	0	0	0	0	0
0x000 0479 p. 177	TG_POLARITY_PO10_1	PO10_TP_POL_1 0	0	0	0	0	0	0	0
0x000 047A p. 177	TG_POLARITY_PO10_2	PO10_TP_POL_2 0	0	0	0	0	0	0	0
0x000 047B p. 177	TG_POLARITY_PO10_3	PO10_TP_POL_3 0	0	0	0	0	0	0	0
0x000 047C p. 178	TG_REFCNT_SEL_0	— 0	0	0	0	0	CLAMP_CNT_SEL 0	BLC_CNT_SEL 0	FLAG_PIX1_CNT_SEL 0
0x000 047D p. 178	TG_REFCNT_SEL_1	— 0	0	CK_TOG3_CNT_SEL 0	CK_TOG2_CNT_SEL 0	CK_TOG1_CNT_SEL 0	CK_MASK3_CNT_SEL 0	CK_MASK2_CNT_SEL 0	CK_MASK1_CNT_SEL 0
0x000 047E p. 178	TG_REFCNT_SEL_2	PO7_CNT_SEL 0	PO6_CNT_SEL 0	PO5_CNT_SEL 0	PO4_CNT_SEL 0	PO3_CNT_SEL 0	PO2_CNT_SEL 0	PO1_CNT_SEL 0	PO0_CNT_SEL 0
0x000 047F p. 179	TG_REFCNT_SEL_3	— 0	0	0	0	0	PO10_CNT_SEL 0	PO9_CNT_SEL 0	PO8_CNT_SEL 0
0x000 048C p. 179	TG_CYCPAT_CFG0_0	BLC_SEQ_SEL 0	0	0	0	FLAG_PIX1_SEQ_SEL 0	0	0	0
0x000 048D p. 180	TG_CYCPAT_CFG0_1	— 0	0	0	0	CLAMP_SEQ_SEL 0	0	0	0
0x000 048E p. 180	TG_CYCPAT_CFG0_2	CK_MASK2_SEQ_SEL 0	0	0	0	CK_MASK1_SEQ_SEL 0	0	0	0
0x000 048F p. 180	TG_CYCPAT_CFG0_3	— 0	0	0	0	CK_MASK3_SEQ_SEL 0	0	0	0
0x000 0490 p. 181	TG_CYCPAT_CFG1_0	CK_TOG2_SEQ_SEL 0	0	0	0	CK_TOG1_SEQ_SEL 0	0	0	0
0x000 0491 p. 181	TG_CYCPAT_CFG1_1	PO0_SEQ_SEL 0	0	0	0	CK_TOG3_SEQ_SEL 0	0	0	0
0x000 0492 p. 181	TG_CYCPAT_CFG1_2	PO2_SEQ_SEL 0	0	0	0	PO1_SEQ_SEL 0	0	0	0
0x000 0493 p. 182	TG_CYCPAT_CFG1_3	— 0	0	0	0	PO3_SEQ_SEL 0	0	0	0
0x000 0494 p. 182	TG_CYCPAT_CFG2_0	PO5_SEQ_SEL 0	0	0	0	PO4_SEQ_SEL 0	0	0	0
0x000 0495 p. 182	TG_CYCPAT_CFG2_1	PO7_SEQ_SEL 0	0	0	0	PO6_SEQ_SEL 0	0	0	0
0x000 0496 p. 183	TG_CYCPAT_CFG2_2	PO9_SEQ_SEL 0	0	0	0	PO8_SEQ_SEL 0	0	0	0
0x000 0497 p. 183	TG_CYCPAT_CFG2_3	— 0	0	0	0	PO10_SEQ_SEL 0	0	0	0
0x000 0498 p. 183	TG_TOGGLE_POINT0_0	TP0_PIXEL_0 0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 0499	TG_TOGGLE_POINT0_1	TP0_PIXEL_1							
p. 183		0	0	0	0	0	0	0	0
0x000 049A	TG_TOGGLE_POINT0_2	TP1_PIXEL_0							
p. 184		0	0	0	0	0	0	0	0
0x000 049B	TG_TOGGLE_POINT0_3	TP1_PIXEL_1							
p. 184		0	0	0	0	0	0	0	0
0x000 049C	TG_TOGGLE_POINT1_0	TP2_PIXEL_0							
p. 184		0	0	0	0	0	0	0	0
0x000 049D	TG_TOGGLE_POINT1_1	TP2_PIXEL_1							
p. 184		0	0	0	0	0	0	0	0
0x000 049E	TG_TOGGLE_POINT1_2	TP3_PIXEL_0							
p. 184		0	0	0	0	0	0	0	0
0x000 049F	TG_TOGGLE_POINT1_3	TP3_PIXEL_1							
p. 184		0	0	0	0	0	0	0	0
0x000 04A0	TG_TOGGLE_POINT2_0	TP4_PIXEL_0							
p. 185		0	0	0	0	0	0	0	0
0x000 04A1	TG_TOGGLE_POINT2_1	TP4_PIXEL_1							
p. 185		0	0	0	0	0	0	0	0
0x000 04A2	TG_TOGGLE_POINT2_2	TP5_PIXEL_0							
p. 185		0	0	0	0	0	0	0	0
0x000 04A3	TG_TOGGLE_POINT2_3	TP5_PIXEL_1							
p. 185		0	0	0	0	0	0	0	0
0x000 04A4	TG_TOGGLE_POINT3_0	TP6_PIXEL_0							
p. 185		0	0	0	0	0	0	0	0
0x000 04A5	TG_TOGGLE_POINT3_1	TP6_PIXEL_1							
p. 185		0	0	0	0	0	0	0	0
0x000 04A6	TG_TOGGLE_POINT3_2	TP7_PIXEL_0							
p. 186		0	0	0	0	0	0	0	0
0x000 04A7	TG_TOGGLE_POINT3_3	TP7_PIXEL_1							
p. 186		0	0	0	0	0	0	0	0
0x000 04A8	TG_TOGGLE_POINT4_0	TP8_PIXEL_0							
p. 186		0	0	0	0	0	0	0	0
0x000 04A9	TG_TOGGLE_POINT4_1	TP8_PIXEL_1							
p. 186		0	0	0	0	0	0	0	0
0x000 04AA	TG_TOGGLE_POINT4_2	TP9_PIXEL_0							
p. 186		0	0	0	0	0	0	0	0
0x000 04AB	TG_TOGGLE_POINT4_3	TP9_PIXEL_1							
p. 186		0	0	0	0	0	0	0	0
0x000 04AC	TG_TOGGLE_POINT5_0	TP10_PIXEL_0							
p. 187		0	0	0	0	0	0	0	0
0x000 04AD	TG_TOGGLE_POINT5_1	TP10_PIXEL_1							
p. 187		0	0	0	0	0	0	0	0
0x000 04AE	TG_TOGGLE_POINT5_2	TP11_PIXEL_0							
p. 187		0	0	0	0	0	0	0	0
0x000 04AF	TG_TOGGLE_POINT5_3	TP11_PIXEL_1							
p. 187		0	0	0	0	0	0	0	0
0x000 04B0	TG_TOGGLE_POINT6_0	TP12_PIXEL_0							
p. 187		0	0	0	0	0	0	0	0
0x000 04B1	TG_TOGGLE_POINT6_1	TP12_PIXEL_1							
p. 187		0	0	0	0	0	0	0	0
0x000 04B2	TG_TOGGLE_POINT6_2	TP13_PIXEL_0							
p. 188		0	0	0	0	0	0	0	0
0x000 04B3	TG_TOGGLE_POINT6_3	TP13_PIXEL_1							
p. 188		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 04B4	TG_TOGGLE_POINT7_0	TP14_PIXEL_0							
p. 188		0	0	0	0	0	0	0	0
0x000 04B5	TG_TOGGLE_POINT7_1	TP14_PIXEL_1							
p. 188		0	0	0	0	0	0	0	0
0x000 04B6	TG_TOGGLE_POINT7_2	TP15_PIXEL_0							
p. 188		0	0	0	0	0	0	0	0
0x000 04B7	TG_TOGGLE_POINT7_3	TP15_PIXEL_1							
p. 188		0	0	0	0	0	0	0	0
0x000 04B8	TG_TOGGLE_POINT8_0	TP16_PIXEL_0							
p. 189		0	0	0	0	0	0	0	0
0x000 04B9	TG_TOGGLE_POINT8_1	TP16_PIXEL_1							
p. 189		0	0	0	0	0	0	0	0
0x000 04BA	TG_TOGGLE_POINT8_2	TP17_PIXEL_0							
p. 189		0	0	0	0	0	0	0	0
0x000 04BB	TG_TOGGLE_POINT8_3	TP17_PIXEL_1							
p. 189		0	0	0	0	0	0	0	0
0x000 04BC	TG_TOGGLE_POINT9_0	TP18_PIXEL_0							
p. 189		0	0	0	0	0	0	0	0
0x000 04BD	TG_TOGGLE_POINT9_1	TP18_PIXEL_1							
p. 189		0	0	0	0	0	0	0	0
0x000 04BE	TG_TOGGLE_POINT9_2	TP19_PIXEL_0							
p. 190		0	0	0	0	0	0	0	0
0x000 04BF	TG_TOGGLE_POINT9_3	TP19_PIXEL_1							
p. 190		0	0	0	0	0	0	0	0
0x000 04C0	TG_TOGGLE_POINT10_0	TP20_PIXEL_0							
p. 190		0	0	0	0	0	0	0	0
0x000 04C1	TG_TOGGLE_POINT10_1	TP20_PIXEL_1							
p. 190		0	0	0	0	0	0	0	0
0x000 04C2	TG_TOGGLE_POINT10_2	TP21_PIXEL_0							
p. 190		0	0	0	0	0	0	0	0
0x000 04C3	TG_TOGGLE_POINT10_3	TP21_PIXEL_1							
p. 191		0	0	0	0	0	0	0	0
0x000 04C4	TG_TOGGLE_POINT11_0	TP22_PIXEL_0							
p. 191		0	0	0	0	0	0	0	0
0x000 04C5	TG_TOGGLE_POINT11_1	TP22_PIXEL_1							
p. 191		0	0	0	0	0	0	0	0
0x000 04C6	TG_TOGGLE_POINT11_2	TP23_PIXEL_0							
p. 191		0	0	0	0	0	0	0	0
0x000 04C7	TG_TOGGLE_POINT11_3	TP23_PIXEL_1							
p. 191		0	0	0	0	0	0	0	0
0x000 04C8	TG_TOGGLE_POINT12_0	TP24_PIXEL_0							
p. 192		0	0	0	0	0	0	0	0
0x000 04C9	TG_TOGGLE_POINT12_1	TP24_PIXEL_1							
p. 192		0	0	0	0	0	0	0	0
0x000 04CA	TG_TOGGLE_POINT12_2	TP25_PIXEL_0							
p. 192		0	0	0	0	0	0	0	0
0x000 04CB	TG_TOGGLE_POINT12_3	TP25_PIXEL_1							
p. 192		0	0	0	0	0	0	0	0
0x000 04CC	TG_TOGGLE_POINT13_0	TP26_PIXEL_0							
p. 192		0	0	0	0	0	0	0	0
0x000 04CD	TG_TOGGLE_POINT13_1	TP26_PIXEL_1							
p. 193		0	0	0	0	0	0	0	0
0x000 04CE	TG_TOGGLE_POINT13_2	TP27_PIXEL_0							
p. 193		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 04CF	TG_TOGGLE_POINT13_3	TP27_PIXEL_1							
p. 193		0	0	0	0	0	0	0	0
0x000 04D0	TG_TOGGLE_POINT14_0	TP28_PIXEL_0							
p. 193		0	0	0	0	0	0	0	0
0x000 04D1	TG_TOGGLE_POINT14_1	TP28_PIXEL_1							
p. 193		0	0	0	0	0	0	0	0
0x000 04D2	TG_TOGGLE_POINT14_2	TP29_PIXEL_0							
p. 194		0	0	0	0	0	0	0	0
0x000 04D3	TG_TOGGLE_POINT14_3	TP29_PIXEL_1							
p. 194		0	0	0	0	0	0	0	0
0x000 04D4	TG_TOGGLE_POINT15_0	TP30_PIXEL_0							
p. 194		0	0	0	0	0	0	0	0
0x000 04D5	TG_TOGGLE_POINT15_1	TP30_PIXEL_1							
p. 194		0	0	0	0	0	0	0	0
0x000 04D6	TG_TOGGLE_POINT15_2	TP31_PIXEL_0							
p. 194		0	0	0	0	0	0	0	0
0x000 04D7	TG_TOGGLE_POINT15_3	TP31_PIXEL_1							
p. 195		0	0	0	0	0	0	0	0
0x000 04D8	TG_OUTMUX_CFG0_0	PCK1_PO_SEL				PCK1_DLY		CLKOUT1_POL	CLKOUT1_EN
p. 195		0	0	0	0	0	0	0	0
0x000 04D9	TG_OUTMUX_CFG0_1	PCK2_PO_SEL				PCK2_DLY		CLKOUT2_POL	CLKOUT2_EN
p. 195		0	0	0	0	0	0	0	0
0x000 04DA	TG_OUTMUX_CFG0_2	PCK3_PO_SEL				PCK3_DLY		CLKOUT3_POL	CLKOUT3_EN
p. 196		0	0	0	0	0	0	0	0
0x000 04DB	TG_OUTMUX_CFG0_3	PCK4_PO_SEL				PCK4_DLY		CLKOUT4_POL	CLKOUT4_EN
p. 196		0	0	0	0	0	0	0	0
0x000 04DC	TG_OUTMUX_CFG1_0	PCK5_PO_SEL				PCK5_DLY		CLKOUT5_POL	CLKOUT5_EN
p. 196		0	0	0	0	0	0	0	0
0x000 04DD	TG_OUTMUX_CFG1_1	PCK6_PO_SEL				PCK6_DLY		CLKOUT6_POL	CLKOUT6_EN
p. 197		0	0	0	0	0	0	0	0
0x000 04DE	TG_OUTMUX_CFG1_2	PCK7_PO_SEL				PCK7_DLY		CLKOUT7_POL	CLKOUT7_EN
p. 197		0	0	0	0	0	0	0	0
0x000 04DF	TG_OUTMUX_CFG1_3	PCK8_PO_SEL				PCK8_DLY		CLKOUT8_POL	CLKOUT8_EN
p. 198		0	0	0	0	0	0	0	0
0x000 04E0	TG_OUTMUX_CFG2_0	PCK9_PO_SEL				PCK9_DLY		CLKOUT9_POL	CLKOUT9_EN
p. 198		0	0	0	0	0	0	0	0
0x000 04E1	TG_OUTMUX_CFG2_1	PCK10_PO_SEL				PCK10_DLY		CLKOUT10_POL	CLKOUT10_EN
p. 198		0	0	0	0	0	0	0	0
0x000 04E3	TG_OUTMUX_CFG2_3	—		CLKOUT6_SRC	CLKOUT5_SRC	CLKOUT4_SRC	CLKOUT3_SRC	CLKOUT2_SRC	CLKOUT1_SRC
p. 199		0	0	0	0	0	0	0	0
0x000 04E4	DLL_CFG1_0	—		DLL_RSMP_RISE					
p. 199		0	0	1	0	0	0	0	0
0x000 04E5	DLL_CFG1_1	—		DLL_RSMP_FALL					
p. 200		0	0	1	0	0	1	1	0
0x000 04E6	DLL_CFG1_2	—		DLL_VSMP_RISE					
p. 200		0	0	1	0	1	0	0	0
0x000 04E7	DLL_CFG1_3	—		DLL_VSMP_FALL					
p. 200		0	0	0	0	1	0	0	0
0x000 04E8	DLL_CFG2_0	—		DLL_CK1_RISE					
p. 200		0	0	0	0	1	0	1	0
0x000 04E9	DLL_CFG2_1	DLL_CK1_DIV	—	DLL_CK1_FALL					
p. 201		0	0	0	1	1	0	0	1
0x000 04EA	DLL_CFG2_2	—		DLL_CK2_RISE					
p. 201		0	0	0	1	1	0	0	1

Address	Register	7	6	5	4	3	2	1	0
0x000 04EB	DLL_CFG2_3	DLL_CK2_DIV	—	DLL_CK2_FALL					
p. 201		0	0	1	0	1	0	0	0
0x000 04EC	DLL_CFG3_0	—		DLL_CK3_RISE					
p. 201		0	0	1	0	1	0	0	0
0x000 04ED	DLL_CFG3_1	DLL_CK3_DIV	—	DLL_CK3_FALL					
p. 202		0	0	0	0	1	0	1	0
0x000 04EE	DLL_CFG3_2	—		DLL_CK4_RISE					
p. 202		0	0	0	0	0	0	0	0
0x000 04EF	DLL_CFG3_3	DLL_CK4_DIV	—	DLL_CK4_FALL					
p. 202		0	0	0	0	0	0	0	0
0x000 04F0	DLL_CFG4_0	—		DLL_CK5_RISE					
p. 202		0	0	0	0	1	0	1	0
0x000 04F1	DLL_CFG4_1	DLL_CK5_DIV	—	DLL_CK5_FALL					
p. 203		0	0	1	0	1	0	0	0
0x000 04F2	DLL_CFG4_2	—		DLL_CK6_RISE					
p. 203		0	0	0	0	1	0	1	0
0x000 04F3	DLL_CFG4_3	DLL_CK6_DIV	—	DLL_CK6_FALL					
p. 203		0	0	1	0	1	0	0	0
0x000 04F4	DLL_CFG5_0	—		DLL_TGCKO_RISE					
p. 203		0	0	1	1	0	1	1	1
0x000 04F5	DLL_CFG5_1	—		DLL_AFECK_DUR					
p. 204		0	0	0	1	0	1	1	0

7.6 OP_FORMAT—Output Formatter

Address	Register	7	6	5	4	3	2	1	0
0x000 0500	OP_FORMAT_CFG0_0	FORMAT_LOAD	FORMAT_SEL						
p. 204		0	0	0	0	0	0	0	1
0x000 0501	OP_FORMAT_CFG0_1	—				LVDS_POL	LVDS_REVERSE	CMOS_EXT_POL	LVDS_BIT_ ORDER
p. 204		0	0	0	0	0	0	0	1
0x000 0502	OP_FORMAT_CFG0_2	—						TDM_GAP	TDM_EN
p. 205		0	0	0	0	0	0	0	0
0x000 0503	OP_FORMAT_CFG0_3	—			TDM_OFFSET				
p. 205		0	0	0	0	0	0	0	0
0x000 0504	OP_FORMAT_CFG1_0	FLAG_S1_FN				FLAG_S0_FN			
p. 205		0	0	0	0	0	0	0	0
0x000 0505	OP_FORMAT_CFG1_1	FLAG_S3_FN				FLAG_S2_FN			
p. 206		0	0	0	0	0	0	0	0
0x000 0506	OP_FORMAT_CFG1_2	—				FLAG_S4_FN			
p. 206		0	0	0	0	0	0	0	0

7.7 PAD_INTF—Pad Interface I/O Control

Address	Register	7	6	5	4	3	2	1	0
0x000 0600	CLKOUT_SEL_1_0	CLKOUT4_FN	CLKOUT3_FN			CLKOUT2_FN		CLKOUT1_FN	
p. 206		0	0	0	1	0	1	0	1
0x000 0601	CLKOUT_SEL_1_1	—		CLKOUT10_FN	CLKOUT9_FN	CLKOUT8_FN	CLKOUT7_FN	CLKOUT6_FN	CLKOUT5_FN
p. 207		0	0	0	0	0	0	0	0
0x000 0602	CLKOUT_SEL_1_2	—			MON_SEL			TGSYNC1_VSMP_FN	
p. 207		0	0	0	0	0	0	0	0
0x000 0603	CLKOUT_SEL_1_3	—				TDM_DOUT_DLY_SEL		TDM_DOUT_ DLY_EN	MCLK_EXT_LVDS
p. 208		0	0	0	0	0	1	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 060C	GPI_VAL_0	GP7_IN_STS	GP6_IN_STS	GP5_IN_STS	GP4_IN_STS	GP3_IN_STS	GP2_IN_STS	GP1_IN_STS	GP12_IN_STS
p. 208		X	X	X	X	X	X	X	X
0x000 060D	GPI_VAL_1	—					GP10_IN_STS	GP9_IN_STS	GP8_IN_STS
p. 209		0	0	0	0	X	X	X	X
0x000 060E	GPI_VAL_2	GP10_DIR	GP9_DIR	GP8_DIR	GP7_DIR	GP4_DIR	GP3_DIR	GP2_DIR	GP1_DIR
p. 209		0	0	0	0	0	0	0	0
0x000 060F	GPI_VAL_3	GP10_OUT_LVL	GP9_OUT_LVL	GP8_OUT_LVL	GP7_OUT_LVL	GP4_OUT_LVL	GP3_OUT_LVL	GP2_OUT_LVL	GP1_OUT_LVL
p. 210		0	0	0	0	0	0	0	0
0x000 0610	LVDS_CFG	—						LVDS_VREF_SEL	
p. 210		0	0	0	0	0	0	0	1
0x000 0618	CMOS_CFG_0	—	SPI_SDO_I2C_SCL_DRV_STR			SPI_SDO_I2C_SCL_PULL		SPI_MISO_I2C_SCL_HIZ_EN	SPI_MISO_I2C_SCL_IE
p. 210		0	0	0	1	1	0	0	1
0x000 0619	CMOS_CFG_1	—	SPI_MOSI_I2C_SDA_DRV_STR			SPI_MOSI_I2C_SDA_PULL		SPI_MOSI_I2C_SDA_HIZ_EN	SPI_MOSI_I2C_SDA_IE
p. 211		0	0	0	1	1	0	0	1
0x000 061A	CMOS_CFG_2	—				SPI_SCK_PULL		—	SPI_SCK_IE
p. 211		0	0	0	1	1	0	0	1
0x000 061B	CMOS_CFG_3	—				SPI_CS_PULL		—	SPI_CS_IE
p. 212		0	0	0	1	1	0	0	1
0x000 061C	MCLK_CFG_0	—	MCLK_LVDS_RT_EN	—					
p. 212		0	0	1	0	0	0	0	0
0x000 061D	MCLK_CFG_1	—				MCLK_EXT_MCLK_EXT_P_PULL		MCLK_EXT_MCLK_EXT_P_HIZ_EN	MCLK_EXT_MCLK_EXT_P_IE
p. 212		0	0	0	1	1	0	0	1
0x000 061E	MCLK_CFG_2	—				MCLK_EXT_N_GPI12_PULL		MCLK_EXT_N_GPI12_HIZ_EN	MCLK_EXT_N_GPI12_IE
p. 212		0	0	0	1	1	0	0	1
0x000 0620	CLKOUT1_4_CFG_0	—	CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_DRV_STR			CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_PULL		CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_HIZ_EN	CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_IE
p. 213		0	0	0	1	1	0	0	1
0x000 0621	CLKOUT1_4_CFG_1	—	CLKOUT2_LEDG_EN_LEDSTART_GPIO2_DRV_STR			CLKOUT2_LEDG_EN_LEDSTART_GPIO2_PULL		CLKOUT2_LEDG_EN_LEDSTART_GPIO2_HIZ_EN	CLKOUT2_LEDG_EN_LEDSTART_GPIO2_IE
p. 213		0	0	0	1	1	0	0	1
0x000 0622	CLKOUT1_4_CFG_2	—	CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_DRV_STR			CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_PULL		CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_HIZ_EN	CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_IE
p. 214		0	0	0	1	1	0	0	1
0x000 0623	CLKOUT1_4_CFG_3	—	CLKOUT4_GPIO4_DRV_STR			CLKOUT4_GPIO4_PULL		CLKOUT4_GPIO4_HIZ_EN	CLKOUT4_GPIO4_IE
p. 214		0	0	0	1	1	0	0	1
0x000 0624	CLKOUT5_GPI5_CFG_0	—	CLKOUT5_GPI5_DRV_STR			CLKOUT5_GPI5_PULL		CLKOUT5_GPI5_HIZ_EN	CLKOUT5_GPI5_IE
p. 214		0	0	0	1	1	0	0	1
0x000 0625	CLKOUT5_GPI5_CFG_1	—	CLKOUT6_GPI6_DRV_STR			CLKOUT6_GPI6_PULL		CLKOUT6_GPI6_HIZ_EN	CLKOUT6_GPI6_IE
p. 215		0	0	0	1	1	0	0	1
0x000 0626	CLKOUT5_GPI5_CFG_2	—	CLKOUT7_GPIO7_DRV_STR			CLKOUT7_GPIO7_PULL		CLKOUT7_GPIO7_HIZ_EN	CLKOUT7_GPIO7_IE
p. 215		0	0	0	1	1	0	0	1
0x000 0627	CLKOUT5_GPI5_CFG_3	—	CLKOUT8_GPIO8_DRV_STR			CLKOUT8_GPIO8_PULL		CLKOUT8_GPIO8_HIZ_EN	CLKOUT8_GPIO8_IE
p. 216		0	0	0	1	1	0	0	1
0x000 0628	CLKOUT9_GPI9_CFG_0	—	CLKOUT9_GPIO9_DRV_STR			CLKOUT9_GPIO9_PULL		CLKOUT9_GPIO9_HIZ_EN	CLKOUT9_GPIO9_IE
p. 216		0	0	0	1	1	0	0	1

Address	Register	7	6	5	4	3	2	1	0
0x000 0629	CLKOUT9_GPI9_CFG_1	—	CLKOUT10_GPIO10_DRV_STR			CLKOUT10_GPIO10_PULL		CLKOUT10_GPIO10_HIZ_EN	CLKOUT10_GPIO10_IE
p. 216		0	0	0	1	1	0	0	1
0x000 062C	TGSYNC1_VSMP_EXT_CFG	—	TGSYNC1_VSMP_EXT_DRV_STR			TGSYNC1_VSMP_EXT_PULL		TGSYNC1_VSMP_EXT_HIZ_EN	TGSYNC1_VSMP_EXT_IE
p. 217		0	0	0	1	1	0	0	1
0x000 0630	DOUT_CH1_CFG_0	—	DOUT1_P_DOUT1_DRV_STR			DOUT1_P_DOUT1_PULL		DOUT1_P_DOUT1_HIZ_EN	DOUT1_P_DOUT1_IE
p. 217		0	0	0	1	1	0	0	0
0x000 0631	DOUT_CH1_CFG_1	—	DOUT1_N_DOUT2_DRV_STR			DOUT1_N_DOUT2_PULL		DOUT1_N_DOUT2_HIZ_EN	DOUT1_N_DOUT2_IE
p. 218		0	0	0	1	1	0	0	0
0x000 0632	DCLKOUT_CFG_2	—				DCLKOUT_LVDS_TXDRV		DCLKOUT_LVDS_TRIM	
p. 218		0	0	0	0	1	0	1	0
0x000 0634	DOUT_CH2_CFG_0	—	DOUT2_P_DOUT3_DRV_STR			DOUT2_P_DOUT3_PULL		DOUT2_P_DOUT3_HIZ_EN	DOUT2_P_DOUT3_IE
p. 218		0	0	0	1	1	0	0	0
0x000 0635	DOUT_CH2_CFG_1	—	DOUT2_N_DOUT4_DRV_STR			DOUT2_N_DOUT4_PULL		DOUT2_N_DOUT4_HIZ_EN	DOUT2_N_DOUT4_IE
p. 219		0	0	0	1	1	0	0	0
0x000 0636	DOUT_CH1_CFG_2	—				DOUT1_LVDS_TXDRV		DOUT1_LVDS_TRIM	
p. 219		0	0	0	0	1	0	1	0
0x000 0638	DOUT_CH3_CFG_0	—	DOUT3_P_DOUT5_DRV_STR			DOUT3_P_DOUT5_PULL		DOUT3_P_DOUT5_HIZ_EN	DOUT3_P_DOUT5_IE
p. 219		0	0	0	1	1	0	0	0
0x000 0639	DOUT_CH3_CFG_1	—	DOUT3_N_DOUT6_DRV_STR			DOUT3_N_DOUT6_PULL		DOUT3_N_DOUT6_HIZ_EN	DOUT3_N_DOUT6_IE
p. 220		0	0	0	1	1	0	0	0
0x000 063A	DOUT_CH2_CFG_2	—				DOUT2_LVDS_TXDRV		DOUT2_LVDS_TRIM	
p. 220		0	0	0	0	1	0	1	0
0x000 063C	DOUT_CH4_CFG_0	—	DOUT4_P_DOUT7_DRV_STR			DOUT4_P_DOUT7_PULL		DOUT4_P_DOUT7_HIZ_EN	DOUT4_P_DOUT7_IE
p. 221		0	0	0	1	1	0	0	0
0x000 063D	DOUT_CH4_CFG_1	—	DOUT4_N_DOUT8_DRV_STR			DOUT4_N_DOUT8_PULL		DOUT4_N_DOUT8_HIZ_EN	DOUT4_N_DOUT8_IE
p. 221		0	0	0	1	1	0	0	0
0x000 063E	DOUT_CH3_CFG_2	—				DOUT3_LVDS_TXDRV		DOUT3_LVDS_TRIM	
p. 221		0	0	0	0	1	0	1	0
0x000 0640	DOUT_CH5_CFG_0	—	DOUT5_P_DOUT9_DRV_STR			DOUT5_P_DOUT9_PULL		DOUT5_P_DOUT9_HIZ_EN	DOUT5_P_DOUT9_IE
p. 222		0	0	0	1	1	0	0	0
0x000 0641	DOUT_CH5_CFG_1	—	DOUT5_N_DOUT10_DRV_STR			DOUT5_N_DOUT10_PULL		DOUT5_N_DOUT10_HIZ_EN	DOUT5_N_DOUT10_IE
p. 222		0	0	0	1	1	0	0	0
0x000 0642	DOUT_CH4_CFG_2	—				DOUT4_LVDS_TXDRV		DOUT4_LVDS_TRIM	
p. 223		0	0	0	0	1	0	1	0
0x000 0644	DCLKOUT_CFG_0	—	DCLKOUT_P_DCLKOUT1_DRV_STR			DCLKOUT_P_DCLKOUT1_PULL		DCLKOUT_P_DCLKOUT1_HIZ_EN	DCLKOUT_P_DCLKOUT1_IE
p. 223		0	0	0	1	1	0	0	0
0x000 0645	DCLKOUT_CFG_1	—	DCLKOUT_N_DCLKOUT2_DRV_STR			DCLKOUT_N_DCLKOUT2_PULL		DCLKOUT_N_DCLKOUT2_HIZ_EN	DCLKOUT_N_DCLKOUT2_IE
p. 223		0	0	0	1	1	0	0	0
0x000 0646	DOUT_CH5_CFG_2	—				DOUT5_LVDS_TXDRV		DOUT5_LVDS_TRIM	
p. 224		0	0	0	0	1	0	1	0

7.8 DAC_CTRL—DAC_CTRL

Address	Register	7	6	5	4	3	2	1	0
0x000 0704	DAC_CTRL_OFS01_CH1_0	CH1_SEQ0_OFFSET_0							
p. 224		0	0	0	0	0	0	0	0
0x000 0705	DAC_CTRL_OFS01_CH1_1	—							CH1_SEQ0_OFFSET_1
p. 224		0	0	0	0	0	0	0	1
0x000 0706	DAC_CTRL_OFS01_CH1_2	CH1_SEQ1_OFFSET_0							
p. 225		0	0	0	0	0	0	0	0
0x000 0707	DAC_CTRL_OFS01_CH1_3	—							CH1_SEQ1_OFFSET_1
p. 225		0	0	0	0	0	0	0	1
0x000 0708	DAC_CTRL_OFS23_CH1_0	CH1_SEQ2_OFFSET_0							
p. 225		0	0	0	0	0	0	0	0
0x000 0709	DAC_CTRL_OFS23_CH1_1	—							CH1_SEQ2_OFFSET_1
p. 225		0	0	0	0	0	0	0	1
0x000 070A	DAC_CTRL_OFS23_CH1_2	CH1_SEQ3_OFFSET_0							
p. 226		0	0	0	0	0	0	0	0
0x000 070B	DAC_CTRL_OFS23_CH1_3	—							CH1_SEQ3_OFFSET_1
p. 226		0	0	0	0	0	0	0	1
0x000 070C	DAC_CTRL_OFS0_CH2_3_0	CH2_SEQ0_OFFSET_0							
p. 226		0	0	0	0	0	0	0	0
0x000 070D	DAC_CTRL_OFS0_CH2_3_1	—							CH2_SEQ0_OFFSET_1
p. 226		0	0	0	0	0	0	0	1
0x000 070E	DAC_CTRL_OFS0_CH2_3_2	CH3_SEQ0_OFFSET_0							
p. 227		0	0	0	0	0	0	0	0
0x000 070F	DAC_CTRL_OFS0_CH2_3_3	—							CH3_SEQ0_OFFSET_1
p. 227		0	0	0	0	0	0	0	1
0x000 0710	DAC_CTRL_OFS0_CH4_5_0	CH4_SEQ0_OFFSET_0							
p. 227		0	0	0	0	0	0	0	0
0x000 0711	DAC_CTRL_OFS0_CH4_5_1	—							CH4_SEQ0_OFFSET_1
p. 227		0	0	0	0	0	0	0	1
0x000 0712	DAC_CTRL_OFS0_CH4_5_2	CH5_SEQ0_OFFSET_0							
p. 228		0	0	0	0	0	0	0	0
0x000 0713	DAC_CTRL_OFS0_CH4_5_3	—							CH5_SEQ0_OFFSET_1
p. 228		0	0	0	0	0	0	0	1
0x000 0714	DAC_CTRL_OFS0_CH6_0	CH6_SEQ0_OFFSET_0							
p. 228		0	0	0	0	0	0	0	0
0x000 0715	DAC_CTRL_OFS0_CH6_1	—							CH6_SEQ0_OFFSET_1
p. 228		0	0	0	0	0	0	0	1
0x000 071A	DAC_CTRL_OFS1_CH2_2	CH2_SEQ1_OFFSET_0							
p. 229		0	0	0	0	0	0	0	0
0x000 071B	DAC_CTRL_OFS1_CH2_3	—							CH2_SEQ1_OFFSET_1
p. 229		0	0	0	0	0	0	0	1
0x000 071E	DAC_CTRL_OFS1_CH3_2	CH3_SEQ1_OFFSET_0							
p. 229		0	0	0	0	0	0	0	0
0x000 071F	DAC_CTRL_OFS1_CH3_3	—							CH3_SEQ1_OFFSET_1
p. 229		0	0	0	0	0	0	0	1

Address	Register	7	6	5	4	3	2	1	0
0x000 0722	DAC_CTRL_OFS1_CH4_2	CH4_SEQ1_OFFSET_0							
p. 230		0	0	0	0	0	0	0	0
0x000 0723	DAC_CTRL_OFS1_CH4_3	—							CH4_SEQ1_OFFSET_1
p. 230		0	0	0	0	0	0	0	1
0x000 0726	DAC_CTRL_OFS01_CH5_2	CH5_SEQ1_OFFSET_0							
p. 230		0	0	0	0	0	0	0	0
0x000 0727	DAC_CTRL_OFS01_CH5_3	—							CH5_SEQ1_OFFSET_1
p. 230		0	0	0	0	0	0	0	1
0x000 072A	DAC_CTRL_OFS1_CH6_2	CH6_SEQ1_OFFSET_0							
p. 231		0	0	0	0	0	0	0	0
0x000 072B	DAC_CTRL_OFS1_CH6_3	—							CH6_SEQ1_OFFSET_1
p. 231		0	0	0	0	0	0	0	1
0x000 072C	DAC_CTRL_OFS23_CH2_0	CH2_SEQ2_OFFSET_0							
p. 231		0	0	0	0	0	0	0	0
0x000 072D	DAC_CTRL_OFS23_CH2_1	—							CH2_SEQ2_OFFSET_1
p. 231		0	0	0	0	0	0	0	1
0x000 072E	DAC_CTRL_OFS23_CH2_2	CH2_SEQ3_OFFSET_0							
p. 232		0	0	0	0	0	0	0	0
0x000 072F	DAC_CTRL_OFS23_CH2_3	—							CH2_SEQ3_OFFSET_1
p. 232		0	0	0	0	0	0	0	1
0x000 0730	DAC_CTRL_OFS23_CH3_0	CH3_SEQ2_OFFSET_0							
p. 232		0	0	0	0	0	0	0	0
0x000 0731	DAC_CTRL_OFS23_CH3_1	—							CH3_SEQ2_OFFSET_1
p. 232		0	0	0	0	0	0	0	1
0x000 0732	DAC_CTRL_OFS23_CH3_2	CH3_SEQ3_OFFSET_0							
p. 233		0	0	0	0	0	0	0	0
0x000 0733	DAC_CTRL_OFS23_CH3_3	—							CH3_SEQ3_OFFSET_1
p. 233		0	0	0	0	0	0	0	1
0x000 0734	DAC_CTRL_OFS23_CH4_0	CH4_SEQ2_OFFSET_0							
p. 233		0	0	0	0	0	0	0	0
0x000 0735	DAC_CTRL_OFS23_CH4_1	—							CH4_SEQ2_OFFSET_1
p. 233		0	0	0	0	0	0	0	1
0x000 0736	DAC_CTRL_OFS23_CH4_2	CH4_SEQ3_OFFSET_0							
p. 234		0	0	0	0	0	0	0	0
0x000 0737	DAC_CTRL_OFS23_CH4_3	—							CH4_SEQ3_OFFSET_1
p. 234		0	0	0	0	0	0	0	1
0x000 0738	DAC_CTRL_OFS23_CH5_0	CH5_SEQ2_OFFSET_0							
p. 234		0	0	0	0	0	0	0	0
0x000 0739	DAC_CTRL_OFS23_CH5_1	—							CH5_SEQ2_OFFSET_1
p. 234		0	0	0	0	0	0	0	1
0x000 073A	DAC_CTRL_OFS23_CH5_2	CH5_SEQ3_OFFSET_0							
p. 235		0	0	0	0	0	0	0	0
0x000 073B	DAC_CTRL_OFS23_CH5_3	—							CH5_SEQ3_OFFSET_1
p. 235		0	0	0	0	0	0	0	1
0x000 073C	DAC_CTRL_OFS23_CH6_0	CH6_SEQ2_OFFSET_0							
p. 235		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 073D	DAC_CTRL_OFS23_CH6_1	—							CH6_SEQ2_OFFSET_1
p. 235		0	0	0	0	0	0	0	1
0x000 073E	DAC_CTRL_OFS23_CH6_2	CH6_SEQ3_OFFSET_0							
p. 236		0	0	0	0	0	0	0	0
0x000 073F	DAC_CTRL_OFS23_CH6_3	—							CH6_SEQ3_OFFSET_1
p. 236		0	0	0	0	0	0	0	1

7.9 PGA_CTRL—PGA_CTRL

Address	Register	7	6	5	4	3	2	1	0
0x000 0804	PGA_CTRL_AGAIN_CH1_0	—		CH1_SEQ0_AGAIN					
p. 236		0	0	0	0	0	0	0	0
0x000 0805	PGA_CTRL_AGAIN_CH1_1	—		CH1_SEQ1_AGAIN					
p. 236		0	0	0	0	0	0	0	0
0x000 0806	PGA_CTRL_AGAIN_CH1_2	—		CH1_SEQ2_AGAIN					
p. 237		0	0	0	0	0	0	0	0
0x000 0807	PGA_CTRL_AGAIN_CH1_3	—		CH1_SEQ3_AGAIN					
p. 237		0	0	0	0	0	0	0	0
0x000 0808	PGA_CTRL_AGAIN_CH2_0	—		CH2_SEQ0_AGAIN					
p. 237		0	0	0	0	0	0	0	0
0x000 0809	PGA_CTRL_AGAIN_CH3_0	—		CH3_SEQ0_AGAIN					
p. 237		0	0	0	0	0	0	0	0
0x000 080A	PGA_CTRL_AGAIN_CH4_0	—		CH4_SEQ0_AGAIN					
p. 238		0	0	0	0	0	0	0	0
0x000 080B	PGA_CTRL_AGAIN_CH5_0	—		CH5_SEQ0_AGAIN					
p. 238		0	0	0	0	0	0	0	0
0x000 080C	PGA_CTRL_AGAIN_CH6_0	—		CH6_SEQ0_AGAIN					
p. 238		0	0	0	0	0	0	0	0
0x000 0811	PGA_CTRL_AGAIN_CH2_1	—		CH2_SEQ1_AGAIN					
p. 238		0	0	0	0	0	0	0	0
0x000 0812	PGA_CTRL_AGAIN_CH2_2	—		CH2_SEQ2_AGAIN					
p. 239		0	0	0	0	0	0	0	0
0x000 0813	PGA_CTRL_AGAIN_CH2_3	—		CH2_SEQ3_AGAIN					
p. 239		0	0	0	0	0	0	0	0
0x000 0815	PGA_CTRL_AGAIN_CH3_1	—		CH3_SEQ1_AGAIN					
p. 239		0	0	0	0	0	0	0	0
0x000 0816	PGA_CTRL_AGAIN_CH3_2	—		CH3_SEQ2_AGAIN					
p. 239		0	0	0	0	0	0	0	0
0x000 0817	PGA_CTRL_AGAIN_CH3_3	—		CH3_SEQ3_AGAIN					
p. 240		0	0	0	0	0	0	0	0
0x000 0819	PGA_CTRL_AGAIN_CH4_1	—		CH4_SEQ1_AGAIN					
p. 240		0	0	0	0	0	0	0	0
0x000 081A	PGA_CTRL_AGAIN_CH4_2	—		CH4_SEQ2_AGAIN					
p. 240		0	0	0	0	0	0	0	0
0x000 081B	PGA_CTRL_AGAIN_CH4_3	—		CH4_SEQ3_AGAIN					
p. 240		0	0	0	0	0	0	0	0
0x000 081D	PGA_CTRL_AGAIN_CH5_1	—		CH5_SEQ1_AGAIN					
p. 241		0	0	0	0	0	0	0	0
0x000 081E	PGA_CTRL_AGAIN_CH5_2	—		CH5_SEQ2_AGAIN					
p. 241		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 081F	PGA_CTRL_AGAIN_CH5_3	—		CH5_SEQ3_AGAIN					
p. 241		0	0	0	0	0	0	0	0
0x000 0821	PGA_CTRL_AGAIN_CH6_1	—		CH6_SEQ1_AGAIN					
p. 241		0	0	0	0	0	0	0	0
0x000 0822	PGA_CTRL_AGAIN_CH6_2	—		CH6_SEQ2_AGAIN					
p. 242		0	0	0	0	0	0	0	0
0x000 0823	PGA_CTRL_AGAIN_CH6_3	—		CH6_SEQ3_AGAIN					
p. 242		0	0	0	0	0	0	0	0

7.10 BLC_CTRL—BLC_CTRL

Address	Register	7	6	5	4	3	2	1	0
0x000 0900	BLC_CTRL1_0	—	BLC_FINE_EVERYLINE	BLC_FINE_ACCUM	BLC_FINE_EN	—	BLC_COARSE_CYCLES		
p. 242		0	0	0	0	0	0	0	0
0x000 0901	BLC_CTRL1_1	BLC_TRACKING				—			BLC_FRAME_START
p. 243		0	0	0	0	0	0	0	0
0x000 0902	BLC_CTRL1_2	BLC_LENGTH_0							
p. 243		0	0	0	0	0	0	0	0
0x000 0903	BLC_CTRL1_3	—			BLC_TARGET_RANGE	—		BLC_LENGTH_1	
p. 243		0	0	0	0	0	0	0	0
0x000 0908	BLC_TARGET_CH1_0	CH1_SEQ0_BLC_TARGET							
p. 243		0	0	0	0	0	0	0	0
0x000 0909	BLC_TARGET_CH1_1	CH1_SEQ1_BLC_TARGET							
p. 244		0	0	0	0	0	0	0	0
0x000 090A	BLC_TARGET_CH1_2	CH1_SEQ2_BLC_TARGET							
p. 244		0	0	0	0	0	0	0	0
0x000 090B	BLC_TARGET_CH1_3	CH1_SEQ3_BLC_TARGET							
p. 244		0	0	0	0	0	0	0	0
0x000 090C	BLC_TARGET_CH2_0	CH2_SEQ0_BLC_TARGET							
p. 244		0	0	0	0	0	0	0	0
0x000 090D	BLC_TARGET_CH2_1	CH2_SEQ1_BLC_TARGET							
p. 244		0	0	0	0	0	0	0	0
0x000 090E	BLC_TARGET_CH2_2	CH2_SEQ2_BLC_TARGET							
p. 244		0	0	0	0	0	0	0	0
0x000 090F	BLC_TARGET_CH2_3	CH2_SEQ3_BLC_TARGET							
p. 245		0	0	0	0	0	0	0	0
0x000 0910	BLC_TARGET_CH3_0	CH3_SEQ0_BLC_TARGET							
p. 245		0	0	0	0	0	0	0	0
0x000 0911	BLC_TARGET_CH3_1	CH3_SEQ1_BLC_TARGET							
p. 245		0	0	0	0	0	0	0	0
0x000 0912	BLC_TARGET_CH3_2	CH3_SEQ2_BLC_TARGET							
p. 245		0	0	0	0	0	0	0	0
0x000 0913	BLC_TARGET_CH3_3	CH3_SEQ3_BLC_TARGET							
p. 245		0	0	0	0	0	0	0	0
0x000 0914	BLC_TARGET_CH4_0	CH4_SEQ0_BLC_TARGET							
p. 245		0	0	0	0	0	0	0	0
0x000 0915	BLC_TARGET_CH4_1	CH4_SEQ1_BLC_TARGET							
p. 246		0	0	0	0	0	0	0	0
0x000 0916	BLC_TARGET_CH4_2	CH4_SEQ2_BLC_TARGET							
p. 246		0	0	0	0	0	0	0	0
0x000 0917	BLC_TARGET_CH4_3	CH4_SEQ3_BLC_TARGET							
p. 246		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 0918 p. 246	BLC_TARGET_CH5_0	CH5_SEQ0_BLC_TARGET							
		0	0	0	0	0	0	0	0
0x000 0919 p. 246	BLC_TARGET_CH5_1	CH5_SEQ1_BLC_TARGET							
		0	0	0	0	0	0	0	0
0x000 091A p. 246	BLC_TARGET_CH5_2	CH5_SEQ2_BLC_TARGET							
		0	0	0	0	0	0	0	0
0x000 091B p. 247	BLC_TARGET_CH5_3	CH5_SEQ3_BLC_TARGET							
		0	0	0	0	0	0	0	0
0x000 091C p. 247	BLC_TARGET_CH6_0	CH6_SEQ0_BLC_TARGET							
		0	0	0	0	0	0	0	0
0x000 091D p. 247	BLC_TARGET_CH6_1	CH6_SEQ1_BLC_TARGET							
		0	0	0	0	0	0	0	0
0x000 091E p. 247	BLC_TARGET_CH6_2	CH6_SEQ2_BLC_TARGET							
		0	0	0	0	0	0	0	0
0x000 091F p. 247	BLC_TARGET_CH6_3	CH6_SEQ3_BLC_TARGET							
		0	0	0	0	0	0	0	0
0x000 0928 p. 248	BLC_OFFSET_CH1_0	CH1_BLC_OFFSET_0							
		0	0	0	0	0	0	0	0
0x000 0929 p. 248	BLC_OFFSET_CH1_1	—							CH1_BLC_ OFFSET_1
		0	0	0	0	0	0	0	0
0x000 092C p. 248	BLC_OFFSET_CH2_0	CH2_BLC_OFFSET_0							
		0	0	0	0	0	0	0	0
0x000 092D p. 248	BLC_OFFSET_CH2_1	—							CH2_BLC_ OFFSET_1
		0	0	0	0	0	0	0	0
0x000 0930 p. 249	BLC_OFFSET_CH3_0	CH3_BLC_OFFSET_0							
		0	0	0	0	0	0	0	0
0x000 0931 p. 249	BLC_OFFSET_CH3_1	—							CH3_BLC_ OFFSET_1
		0	0	0	0	0	0	0	0
0x000 0934 p. 249	BLC_OFFSET_CH4_0	CH4_BLC_OFFSET_0							
		0	0	0	0	0	0	0	0
0x000 0935 p. 249	BLC_OFFSET_CH4_1	—							CH4_BLC_ OFFSET_1
		0	0	0	0	0	0	0	0
0x000 0938 p. 250	BLC_OFFSET_CH5_0	CH5_BLC_OFFSET_0							
		0	0	0	0	0	0	0	0
0x000 0939 p. 250	BLC_OFFSET_CH5_1	—							CH5_BLC_ OFFSET_1
		0	0	0	0	0	0	0	0
0x000 093C p. 250	BLC_OFFSET_CH6_0	CH6_BLC_OFFSET_0							
		0	0	0	0	0	0	0	0
0x000 093D p. 250	BLC_OFFSET_CH6_1	—							CH6_BLC_ OFFSET_1
		0	0	0	0	0	0	0	0

7.11 SARADC_1—SARADC_1

Address	Register	7	6	5	4	3	2	1	0
0x000 0A01 p. 251	SAR1_CTRL_1	—					CH1_POL	—	
		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 0A03	SAR1_CTRL_3	—						CH1_AFE_POWER	
p. 251		0	0	0	0	0	0	1	1

7.12 SARADC_2—SARADC_2

Address	Register	7	6	5	4	3	2	1	0
0x000 0B01	SAR2_CTRL_1	—					CH2_POL	—	
p. 251		0	0	0	0	0	0	0	0
0x000 0B03	SAR2_CTRL_3	—						CH2_AFE_POWER	
p. 251		0	0	0	0	0	0	1	1

7.13 SARADC_3—SARADC_3

Address	Register	7	6	5	4	3	2	1	0
0x000 0C01	SAR3_CTRL_1	—					CH3_POL	—	
p. 252		0	0	0	0	0	0	0	0
0x000 0C03	SAR3_CTRL_3	—						CH3_AFE_POWER	
p. 252		0	0	0	0	0	0	1	1

7.14 SARADC_4—SARADC_4

Address	Register	7	6	5	4	3	2	1	0
0x000 0D01	SAR4_CTRL_1	—					CH4_POL	—	
p. 252		0	0	0	0	0	0	0	0
0x000 0D03	SAR4_CTRL_3	—						CH4_AFE_POWER	
p. 252		0	0	0	0	0	0	1	1

7.15 SARADC_5—SARADC_5

Address	Register	7	6	5	4	3	2	1	0
0x000 0E01	SAR5_CTRL_1	—					CH5_POL	—	
p. 253		0	0	0	0	0	0	0	0
0x000 0E03	SAR5_CTRL_3	—						CH5_AFE_POWER	
p. 253		0	0	0	0	0	0	1	1

7.16 SARADC_6—SARADC_6

Address	Register	7	6	5	4	3	2	1	0
0x000 0F01	SAR6_CTRL_1	—					CH6_POL	—	
p. 253		0	0	0	0	0	0	0	0
0x000 0F03	SAR6_CTRL_3	—						CH6_AFE_POWER	
p. 253		0	0	0	0	0	0	1	1

7.17 AGC_TOP—Digital Gain Control

Address	Register	7	6	5	4	3	2	1	0
0x000 108C	DGAIN_SEQ01_CH1_0	CH1_SEQ0_DGAIN_0							
p. 254		0	0	0	0	0	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 108D	DGAIN_SEQ01_CH1_1	—				CH1_SEQ0_DGAIN_1			
p. 254		0	0	0	0	1	0	0	0
0x000 108E	DGAIN_SEQ01_CH1_2	CH1_SEQ1_DGAIN_0							
p. 254		0	0	0	0	0	0	0	0
0x000 108F	DGAIN_SEQ01_CH1_3	—				CH1_SEQ1_DGAIN_1			
p. 255		0	0	0	0	1	0	0	0
0x000 1090	DGAIN_SEQ23_CH1_0	CH1_SEQ2_DGAIN_0							
p. 255		0	0	0	0	0	0	0	0
0x000 1091	DGAIN_SEQ23_CH1_1	—				CH1_SEQ2_DGAIN_1			
p. 255		0	0	0	0	1	0	0	0
0x000 1092	DGAIN_SEQ23_CH1_2	CH1_SEQ3_DGAIN_0							
p. 255		0	0	0	0	0	0	0	0
0x000 1093	DGAIN_SEQ23_CH1_3	—				CH1_SEQ3_DGAIN_1			
p. 256		0	0	0	0	1	0	0	0
0x000 1094	DGAIN_SEQ01_CH2_0	CH2_SEQ0_DGAIN_0							
p. 256		0	0	0	0	0	0	0	0
0x000 1095	DGAIN_SEQ01_CH2_1	—				CH2_SEQ0_DGAIN_1			
p. 256		0	0	0	0	1	0	0	0
0x000 1096	DGAIN_SEQ01_CH2_2	CH2_SEQ1_DGAIN_0							
p. 256		0	0	0	0	0	0	0	0
0x000 1097	DGAIN_SEQ01_CH2_3	—				CH2_SEQ1_DGAIN_1			
p. 257		0	0	0	0	1	0	0	0
0x000 1098	DGAIN_SEQ23_CH2_0	CH2_SEQ2_DGAIN_0							
p. 257		0	0	0	0	0	0	0	0
0x000 1099	DGAIN_SEQ23_CH2_1	—				CH2_SEQ2_DGAIN_1			
p. 257		0	0	0	0	1	0	0	0
0x000 109A	DGAIN_SEQ23_CH2_2	CH2_SEQ3_DGAIN_0							
p. 257		0	0	0	0	0	0	0	0
0x000 109B	DGAIN_SEQ23_CH2_3	—				CH2_SEQ3_DGAIN_1			
p. 258		0	0	0	0	1	0	0	0
0x000 109C	DGAIN_SEQ01_CH3_0	CH3_SEQ0_DGAIN_0							
p. 258		0	0	0	0	0	0	0	0
0x000 109D	DGAIN_SEQ01_CH3_1	—				CH3_SEQ0_DGAIN_1			
p. 258		0	0	0	0	1	0	0	0
0x000 109E	DGAIN_SEQ01_CH3_2	CH3_SEQ1_DGAIN_0							
p. 258		0	0	0	0	0	0	0	0
0x000 109F	DGAIN_SEQ01_CH3_3	—				CH3_SEQ1_DGAIN_1			
p. 259		0	0	0	0	1	0	0	0
0x000 10A0	DGAIN_SEQ23_CH3_0	CH3_SEQ2_DGAIN_0							
p. 259		0	0	0	0	0	0	0	0
0x000 10A1	DGAIN_SEQ23_CH3_1	—				CH3_SEQ2_DGAIN_1			
p. 259		0	0	0	0	1	0	0	0
0x000 10A2	DGAIN_SEQ23_CH3_2	CH3_SEQ3_DGAIN_0							
p. 259		0	0	0	0	0	0	0	0
0x000 10A3	DGAIN_SEQ23_CH3_3	—				CH3_SEQ3_DGAIN_1			
p. 260		0	0	0	0	1	0	0	0
0x000 10A4	DGAIN_SEQ01_CH4_0	CH4_SEQ0_DGAIN_0							
p. 260		0	0	0	0	0	0	0	0
0x000 10A5	DGAIN_SEQ01_CH4_1	—				CH4_SEQ0_DGAIN_1			
p. 260		0	0	0	0	1	0	0	0
0x000 10A6	DGAIN_SEQ01_CH4_2	CH4_SEQ1_DGAIN_0							
p. 260		0	0	0	0	0	0	0	0
0x000 10A7	DGAIN_SEQ01_CH4_3	—				CH4_SEQ1_DGAIN_1			
p. 261		0	0	0	0	1	0	0	0

Address	Register	7	6	5	4	3	2	1	0
0x000 10A8	DGAIN_SEQ23_CH4_0	CH4_SEQ2_DGAIN_0							
p. 261		0	0	0	0	0	0	0	0
0x000 10A9	DGAIN_SEQ23_CH4_1	—				CH4_SEQ2_DGAIN_1			
p. 261		0	0	0	0	1	0	0	0
0x000 10AA	DGAIN_SEQ23_CH4_2	CH4_SEQ3_DGAIN_0							
p. 261		0	0	0	0	0	0	0	0
0x000 10AB	DGAIN_SEQ23_CH4_3	—				CH4_SEQ3_DGAIN_1			
p. 262		0	0	0	0	1	0	0	0
0x000 10AC	DGAIN_SEQ01_CH5_0	CH5_SEQ0_DGAIN_0							
p. 262		0	0	0	0	0	0	0	0
0x000 10AD	DGAIN_SEQ01_CH5_1	—				CH5_SEQ0_DGAIN_1			
p. 262		0	0	0	0	1	0	0	0
0x000 10AE	DGAIN_SEQ01_CH5_2	CH5_SEQ1_DGAIN_0							
p. 262		0	0	0	0	0	0	0	0
0x000 10AF	DGAIN_SEQ01_CH5_3	—				CH5_SEQ1_DGAIN_1			
p. 263		0	0	0	0	1	0	0	0
0x000 10B0	DGAIN_SEQ23_CH5_0	CH5_SEQ2_DGAIN_0							
p. 263		0	0	0	0	0	0	0	0
0x000 10B1	DGAIN_SEQ23_CH5_1	—				CH5_SEQ2_DGAIN_1			
p. 263		0	0	0	0	1	0	0	0
0x000 10B2	DGAIN_SEQ23_CH5_2	CH5_SEQ3_DGAIN_0							
p. 263		0	0	0	0	0	0	0	0
0x000 10B3	DGAIN_SEQ23_CH5_3	—				CH5_SEQ3_DGAIN_1			
p. 264		0	0	0	0	1	0	0	0
0x000 10B4	DGAIN_SEQ01_CH6_0	CH6_SEQ0_DGAIN_0							
p. 264		0	0	0	0	0	0	0	0
0x000 10B5	DGAIN_SEQ01_CH6_1	—				CH6_SEQ0_DGAIN_1			
p. 264		0	0	0	0	1	0	0	0
0x000 10B6	DGAIN_SEQ01_CH6_2	CH6_SEQ1_DGAIN_0							
p. 264		0	0	0	0	0	0	0	0
0x000 10B7	DGAIN_SEQ01_CH6_3	—				CH6_SEQ1_DGAIN_1			
p. 265		0	0	0	0	1	0	0	0
0x000 10B8	DGAIN_SEQ23_CH6_0	CH6_SEQ2_DGAIN_0							
p. 265		0	0	0	0	0	0	0	0
0x000 10B9	DGAIN_SEQ23_CH6_1	—				CH6_SEQ2_DGAIN_1			
p. 265		0	0	0	0	1	0	0	0
0x000 10BA	DGAIN_SEQ23_CH6_2	CH6_SEQ3_DGAIN_0							
p. 265		0	0	0	0	0	0	0	0
0x000 10BB	DGAIN_SEQ23_CH6_3	—				CH6_SEQ3_DGAIN_1			
p. 266		0	0	0	0	1	0	0	0

7.18 PAT_GEN—Test pattern generator

Address	Register	7	6	5	4	3	2	1	0
0x000 1100	PGCONFIG_0	PGEN_MARCH	PGEN_PATT_SEL		PGEN_INV	—			PGEN_EN
p. 266		0	0	0	0	0	0	0	0
0x000 1102	PGCONFIG_2	PGEN_LVL_0							
p. 266		0	0	0	0	0	0	0	0
0x000 1103	PGCONFIG_3	PGEN_LVL_1							
p. 266		0	0	0	0	0	0	0	0
0x000 1104	PGWIDTH_0	PGEN_WIDTH1							
p. 267		0	0	0	0	0	0	0	0
0x000 1105	PGWIDTH_1	PGEN_WIDTH2							
p. 267		0	0	0	0	0	0	0	0

7.19 LED_CTRL—LED Control

Address	Register	7	6	5	4	3	2	1	0
0x000 1500	LED_CTRL_CONFIG_0	—				LED_CTRL_SRC	LEDB_EN	LEDG_EN	LEDR_EN
p. 267		0	0	0	0	0	0	0	0
0x000 1501	LED_CTRL_CONFIG_1	—				LED_RAMP_TIME			
p. 267		0	0	0	0	0	0	0	0
0x000 1502	LED_CTRL_CONFIG_2	LED_RAMP_BOOST		LEDB_COARSE		LEDG_COARSE		LEDR_COARSE	
p. 268		0	0	0	0	0	0	0	0
0x000 1504	LEDX_FINE_0	LEDR_FINE							
p. 268		0	0	0	0	0	0	0	0
0x000 1505	LEDX_FINE_1	LEDG_FINE							
p. 268		0	0	0	0	0	0	0	0
0x000 1506	LEDX_FINE_2	LEDB_FINE							
p. 268		0	0	0	0	0	0	0	0
0x000 1508	LED_CTRL_STATUS	—			LED_MAX_CURRENT_ERR	LED_CTRL_SHORT_ERR	—		
p. 269		0	0	0	0	0	0	0	0

7.20 DPLL1—DPLL1

Address	Register	7	6	5	4	3	2	1	0
0x000 1700	DPLL1_DFLL_DIVIDER_CTRL_0	PLL1_OUTPUT1_DIV_0							—
p. 269		0	0	1	0	0	0	0	0
0x000 1701	DPLL1_DFLL_DIVIDER_CTRL_1	PLL1_VCO_RANGE				—		PLL1_OUTPUT1_DIV_1	
p. 269		0	0	0	0	0	0	0	0
0x000 1702	DPLL1_DFLL_DIVIDER_CTRL_2	PLL1_OUTPUT2_DIV_0							PLL1_OUTPUT2_EN
p. 270		0	0	1	0	0	0	0	0
0x000 1703	DPLL1_DFLL_DIVIDER_CTRL_3	PLL1_REFCLK_DIV_RATIO				PLL1_REFCLK_DIV_BYPASS	—	PLL1_OUTPUT2_DIV_1	
p. 270		0	0	0	0	1	0	0	0
0x000 1704	DPLL1_DFLL_FEEDBACK_RATIO_0	PLL1_RATIO_0							
p. 270		0	0	0	0	0	0	0	0
0x000 1705	DPLL1_DFLL_FEEDBACK_RATIO_1	PLL1_RATIO_1							
p. 270		0	0	0	0	0	0	0	0
0x000 1706	DPLL1_DFLL_FEEDBACK_RATIO_2	PLL1_RATIO_2							
p. 270		0	0	0	1	0	0	0	0
0x000 1707	DPLL1_DFLL_FEEDBACK_RATIO_3	—		PLL1_MODE	PLL1_RATIO_3				
p. 271		0	0	0	0	0	0	0	0
0x000 1708	DPLL1_DFLL_FEATURES_0	PLL1_VCO_GAIN				PLL1_CP_IBIAS			PLL1_PHASE_DET_PAUSE_EN
p. 271		1	0	0	0	0	1	0	0
0x000 1709	DPLL1_DFLL_FEATURES_1	—				PLL1_FILT			
p. 271		0	0	0	0	0	0	0	1

8 Register Descriptions—Flat Register Mode (I2C or SPI)

This section describes each of the control port registers.

- This register view is for the CS82L46 6-channel imaging AFE/ADC, using the flat host-interface configuration.
- The register field default values are established on power-up and after soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 8 bits wide.
- All visible fields are read/write except where indicated with the following shading:

Read/write access | Read-only access | Write-only access

8.1 SW_RESET—Software Reset and Hardware ID

8.1.1 BANK

Address: 0x000 0000
BANKn (n = 0–7) Address: 0x00

	7	6	5	4	3	2	1	0
	DESCRIM				—	BANK		
Access	RO				—	RW		
Default	1	1	0	0	0	0	0	0

Bits	Name	Description
7:4	DESCRIM	Read-only device identifier field. Readback value is 0xC.
3	—	Reserved
2:0	BANK	Bank select. Selects the active bank in Banked SPI Mode. In I2C Mode and SPI Flat Mode, this field should always be set to 0x0. 000 = (Default) Bank 0 001 = Bank 1 010 = Bank 2 011 = Bank 3 100 = Bank 4 101 = Bank 5 110 = Bank 6 111 = Bank 7

8.1.2 SFT_RESET

Address: 0x000 0008
BANKn (n = 0–7) Address: 0x08

WO	7	6	5	4	3	2	1	0
	SFT_RESET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	SFT_RESET	Software reset. Write 0x5A to execute a software reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved

8.1.3 DEVID_0

Address: 0x000 000C
BANK0 Address: 0x0C

RO	7	6	5	4	3	2	1	0
	DEVID_0							
Default	0	1	0	0	0	1	1	0

Bits	Name	Description
7:0	DEVID_0	Device ID (Byte 0)

8.1.4 DEVID_1

Address: 0x000 000D
BANK0 Address: 0x0D

RO	7	6	5	4	3	2	1	0
	DEVID_1							
Default	0	0	1	0	1	0	1	0

Bits	Name	Description
7:0	DEVID_1	Device ID (Byte 1)

8.1.5 DEVID_2

Address: 0x000 000E
BANK0 Address: 0x0E

RO	7	6	5	4	3	2	1	0
	DEVID_2							
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:0	DEVID_2	Device ID (Byte 2)

8.1.6 REVID

Address: 0x000 0010
BANK0 Address: 0x10

RO	7	6	5	4	3	2	1	0
	AREVID				MTLREVID			
Default	1	0	1	1	0	0	0	0

Bits	Name	Description
7:4	AREVID	All-layer device revision. This field is incremented for every all-layer revision of the device.
3:0	MTLREVID	Metal-layer device revision. This field is incremented for every metal-layer revision of the device.

8.1.7 RELID

Address: 0x000 0014
BANK0 Address: 0x14

RO	7	6	5	4	3	2	1	0
	RELID							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	RELID	Software device revision. This field is incremented if software-driver compatibility or software feature support is changed.

8.2 CTRL_ASYNC—Async control

8.2.1 ASYNC0_0

Address: 0x000 0100
BANKn (n = 0–7) Address: 0x04

RO	7	6	5	4	3	2	1	0
	—		ACTIVE_ERROR_STS	TEMP_ERROR_STS	PLL_ERROR_STS	MCLK_ERROR_STS	STARTUP_ERROR_STS	BOOT_ERROR_STS
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	ACTIVE_ERROR_STS	Path error status. Indicates an error condition in the Active or Ready states. 0 = (Default) Normal 1 = Error
4	TEMP_ERROR_STS	Temperature error status. Indicates an overtemperature condition has been detected. 0 = (Default) Normal 1 = Error
3	PLL_ERROR_STS	PLL error status. Indicates a PLL1 error condition. 0 = (Default) Normal 1 = Error

Bits	Name	Description
2	MCLK_ERROR_STS	MCLK error status. Indicates MCLK is invalid or absent in the Idle State. 0 = (Default) Normal 1 = Error
1	STARTUP_ERROR_STS	Start up error status. Indicates an error detected during start-up. 0 = (Default) Normal 1 = Error
0	BOOT_ERROR_STS	Boot error status. Indicates an error detected during boot. 0 = (Default) Normal 1 = Error

8.2.2 ASYNC0_1

Address: 0x000 0101
BANKn (n = 0–7) Address: 0x05

RW	7	6	5	4	3	2	1	0
	—							OSC_DISABLE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	OSC_DISABLE	Oscillator disable. Setting this bit places the device in a low-power Sleep State. Note that the host must return the device to the Idle State before writing to any other control registers. 0 = (Default) RCO enabled 1 = RCO disabled

8.3 CCM—Device Clocking and Sample Rate Control

8.3.1 DEVICE_CLK_CFG_0

Address: 0x000 0200
BANK0 Address: 0x18

RW	7	6	5	4	3	2	1	0
	PIXEL_SAMPLE_RATE							
Default	0	1	1	1	1	0	0	0

Bits	Name	Description
7:0	PIXEL_SAMPLE_RATE	Pixel sample rate (2-24 MHz, in 100 kHz steps) In TG Mode, the pixel rate is derived from MCLK_EXT – either directly, or else using PLL1 to synthesize a different frequency. In External Mode, the pixel rate is a fraction of the MCLK_EXT frequency, depending on the selected output data format. 0x00–0x13 = Reserved 0x14 = 2,000 kHz 0x15 = 2,100 kHz … 0x78 = (Default) 12,000 kHz … 0xF0 = 24,000 kHz 0xF1–0xFF = Reserved

8.3.2 DEVICE_CLK_CFG_1

Address: 0x000 0201
BANK0 Address: 0x19

RW	7	6	5	4	3	2	1	0
	—			EXT_AFECK_DUR			CLOCK_CFG_MODE	
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:5	—	Reserved
4:2	EXT_AFECK_DUR	AFECK pulse duration for External Mode 000 = (Default) 0.5 cycle 001 = 1.0 cycle 010 = 1.5 cycle 011 = 2.0 cycle 100 = 2.5 cycle 101 = 3.0 cycle 110 = 3.5 cycle 111 = 4.0 cycle
1:0	CLOCK_CFG_MODE	Clocking Mode (PLL/DLL connectivity). Valid for TG Mode. 00 = Mode 0 (DLL1 –> PLL2) 01 = (Default) Mode 1 (PLL1 –> (DLL1+PLL2 parallel)) 10 = Mode 2 (PLL1 –> DLL1 –> PLL2) 11 = Reserved

8.3.3 DEVICE_CLK_CFG_2

Address: 0x000 0202
BANK0 Address: 0x1A

RW	7	6	5	4	3	2	1	0
	—						PLL2_AUTO	PLL1_AUTO
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1	PLL2_AUTO	PLL2 division ratio auto-calculation 0 = Disabled 1 = (Default) Enabled
0	PLL1_AUTO	PLL1 division ratio auto-calculation 0 = Disabled 1 = (Default) Enabled

8.3.4 DEVICE_CLK_CFG_3

Address: 0x000 0203
BANK0 Address: 0x1B

RW	7	6	5	4	3	2	1	0
	PLL2_SS_FREQ			PLL2_SS_MAG				PLL2_SS_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	PLL2_SS_FREQ	Set frequency of PLL2 Spread Spectrum 000 = (Default) Reserved 001 = 12.50 kHz 010 = 18.75 kHz 011 = 25.00 kHz 100 = 31.25 kHz 101 = 37.50 kHz 110–111 = Reserved
4:1	PLL2_SS_MAG	Set magnitude of PLL2 Spread Spectrum 0x0 = (Default) '0.125%' 0x1 = '0.25%' 0x2 = '0.5%' 0x3 = '0.75%' 0x4 = '1.0%' 0x5 = '1.25%' 0x6 = '1.5%' 0x7 = '2.0%' 0x8–0xF = Reserved
0	PLL2_SS_EN	Enable Spread Spectrum for PLL2 0 = (Default) Disabled 1 = Enabled

8.3.5 DEVICE_CLK_CFG2_2

Address: 0x000 0206
BANK0 Address: 0x1E

RW	7	6	5	4	3	2	1	0
	PLL2_SS_REF_FREQ_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL2_SS_REF_FREQ_0	Reference frequency for Spread Spectrum modulation. Valid from 2-72 MHz. Bits[7:0] of a 10-bit field 0x00 = (Default) Automatic 0x01–0x13 = Reserved 0x14 = 2,000 kHz 0x15 = 2,100 kHz … 0xFF = 25,500 kHz

8.3.6 DEVICE_CLK_CFG2_3

Address: 0x000 0207
BANK0 Address: 0x1F

RW	7	6	5	4	3	2	1	0
	DOUT_READY_EN	—		MCLK_EXT_SS	—		PLL2_SS_REF_FREQ_1	
Default	1	0	0	0	0	0	0	0

Bits	Name	Description
7	DOUT_READY_EN	Enables data output in the Ready State. (Data output is always enabled in the Active State.) 0 = Data output in Active State only 1 = (Default) Data output in Ready and Active states
6:5	—	Reserved

Bits	Name	Description
4	MCLK_EXT_SS	If spread-spectrum modulation is present on the external MCLK signal, this bit must be set 0 = (Default) Spread-spectrum not present on external MCLK 1 = Spread-spectrum is present on external MCLK
3:2	—	Reserved
1:0	PLL2_SS_REF_FREQ_1	Reference frequency for Spread Spectrum modulation. Valid from 2-72 MHz. Bits[9:8] of a 10-bit field

8.3.7 MCLK_FILT_CFG_0

Address: 0x000 0208
BANK0 Address: 0x20

RW	7	6	5	4	3	2	1	0
	MCLK_MASK_DLY_0							
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:0	MCLK_MASK_DLY_0	MCLK mask delay. Selects the time between the trigger condition asserted and the start of the mask period. The clock period is configured using MCLK_MASK_CLK_DIV. Bits[7:0] of a 16-bit field 0x00 = 8 MCLK + 1 clock period 0x01 = (Default) 8 MCLK + 2 clock periods … 0xFF = 8 MCLK + 256 clock periods

8.3.8 MCLK_FILT_CFG_1

Address: 0x000 0209
BANK0 Address: 0x21

RW	7	6	5	4	3	2	1	0
	MCLK_MASK_DLY_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	MCLK_MASK_DLY_1	MCLK mask delay. Selects the time between the trigger condition asserted and the start of the mask period. The clock period is configured using MCLK_MASK_CLK_DIV. Bits[15:8] of a 16-bit field

8.3.9 MCLK_FILT_CFG_2

Address: 0x000 020A
BANK0 Address: 0x22

RW	7	6	5	4	3	2	1	0
	MCLK_MASK_POL	MCLK_MASK_EN	MCLK_MASK_DUR					
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7	MCLK_MASK_POL	Select trigger polarity for MCLK mask 0 = (Default) Rising edge 1 = Falling edge
6	MCLK_MASK_EN	Enable MCLK mask logic 0 = (Default) Disabled 1 = Enabled
5:0	MCLK_MASK_DUR	MCLK mask duration. The clock period is configured using MCLK_MASK_CLK_DIV. 0x00 = 1 clock periods 0x01 = (Default) 2 clock periods … 0x0F = 16 clock periods 0x10–0x3F = Reserved

8.3.10 MCLK_FILT_CFG_3

Address: 0x000 020B
BANK0 Address: 0x23

RW	7	6	5	4	3	2	1	0
	MCLK_MASK_CLK_DIV			MCLK_MASK_OPF_RST	—	MCLK_MASK_SRC		
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	MCLK_MASK_CLK_DIV	Configures the frequency of clock used for MCLK mask timing 000 = (Default) MCLK/2 001 = MCLK/4 010 = MCLK/6 011 = MCLK/8 100 = MCLK/10 101 = MCLK/12 110 = MCLK/14 111 = MCLK/16
4	MCLK_MASK_OPF_RST	Reset data output after MCLK mask. This bit must be set if MCLK masking is enabled. 0 = (Default) Disabled 1 = Enabled
3	—	Reserved
2:0	MCLK_MASK_SRC	Select control input for MCLK mask 000 = (Default) All HI of LED_R/G/B 001 = LED_R 010 = LED_G 011 = LED_B 100 = tgsync1 101 = tgsync2 110 = led_start 111 = GPI4

8.4 MSM—Power, Global, and Error Control

8.4.1 DEVICE_CTRL_0

Address: 0x000 0300
BANK0 Address: 0x28

RW	7	6	5	4	3	2	1	0
	—	SHARED_BUS_MODE	GPI12_DOUT_CTRL	—	COMPLETE_LINE	ACTIVE_EN	READY_EN	MSM_EN
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7	—	Reserved
6	SHARED_BUS_MODE	Enables SPI control interface to be shared with CMOS data outputs. If this bit is set, the DOUTn pins are configured HiZ during SPI access (while $\overline{\text{SPI\_CS}}$ is low), allowing the DOUTn pins to be shared with the SPI control interface. If SPI and DOUT pins are connected on the PCB, this bit MUST be set before setting READY_EN=1 in order to avoid bus contention. 0 = (Default) Disabled. Bus sharing of the SPI/DOUT pins is not supported. 1 = Enabled. DOUTn are HiZ during SPI access, allowing bus sharing of the SPI/DOUT pins.
5	GPI12_DOUT_CTRL	Configures GPI12 as output enable for the DOUTn pins. 0 = (Default) Disabled. GPI12 has no effect on DOUTn pins 1 = Enabled. GPI12 used to enable DOUTn pins. A Logic 0 input disables DOUTn (HiZ).
4	—	Reserved
3	COMPLETE_LINE	Configures the transition from ACTIVE to READY state. If this bit is set, the device completes the current scan line before transitioning to the READY State. 0 = (Default) Disabled. Sampling stops immediately when ACTIVE_EN=0 1 = Enabled. Sampling stops at the end of line
2	ACTIVE_EN	Selects the ACTIVE state. This bit causes a transition from READY to the ACTIVE state. Note the READY_EN bit must also be set. 0 = (Default) No action 1 = Select ACTIVE state
1	READY_EN	Selects READY state. After the device has been configured, this bit causes a transition from IDLE to the READY state. 0 = (Default) No action 1 = Select READY state
0	MSM_EN	Enables the main state machine (MSM) control. This bit must be set to support any operational control. 0 = Disabled. Operational control not supported. 1 = (Default) Enabled. Operational control is enabled.

8.4.2 DEVICE_CTRL_1

Address: 0x000 0301
BANK0 Address: 0x29

RW	7	6	5	4	3	2	1	0
	TEMP_ERROR_RST_MASK	—	TEMP_ERROR_CLR	—				
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	TEMP_ERROR_RST_MASK	Selects whether an overtemperature error causes a system reset. 0 = (Default) Disabled. Device reset is triggered on overtemperature. 1 = Enabled. Device shuts down on overtemperature, but does not trigger a reset.
6	—	Reserved
5	TEMP_ERROR_CLR	Following an overtemperature error, this bit enables a transition to the IDLE state (provided the error has cleared). This bit should be cleared by the host after the device has entered the IDLE state. 0 = (Default) No action 1 = Clear the overtemperature error and move to IDLE state
4:0	—	Reserved

8.4.3 RLCDAC_CTRL_0

Address: 0x000 0304
BANK0 Address: 0x2C

RW	7	6	5	4	3	2	1	0
	—							VBIAS_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	VBIAS_EN	VBIAS enable 0 = (Default) VBIAS disabled 1 = VBIAS enabled in READY and ACTIVE states

8.4.4 RLCDAC_CTRL_1

Address: 0x000 0305
BANK0 Address: 0x2D

RW	7	6	5	4	3	2	1	0
	—			VBIAS_LVL				
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4:0	VBIAS_LVL	VBIAS output level 0x00 = (Default) 0.17 V 0x01 = 0.25 V … 0x1F = 2.65 V

8.4.5 RLCDAC_CTRL_2

Address: 0x000 0306
BANK0 Address: 0x2E

RW	7	6	5	4	3	2	1	0
	—				VBIAS_ISEL_BOOST	VBIAS_ISEL		VBIAS_REF
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:4	—	Reserved
3	VBIAS_ISEL_BOOST	VBIAS output drive strength doubler 0 = (Default) No doubling of current reference 1 = Double current reference
2:1	VBIAS_ISEL	VBIAS output drive strength. Note the drive strength is doubled if VBIAS_ISEL_BOOST is set. 00 = (Default) 2 mA 01 = 3 mA 10 = 4 mA 11 = Reserved
0	VBIAS_REF	VBIAS reference select 0 = Reference is VDDA 1 = (Default) Reference is VREF

8.4.6 DEVICE_STATUS_0

Address: 0x000 0310
BANK0 Address: 0x34

RO	7	6	5	4	3	2	1	0
	ERROR_STS	—	ACTIVE_STS	READY_STS	—		IDLE_STS	STARTUP_STS
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	ERROR_STS	Indicates the device is in the ERROR state. 0 = (Default) Not in ERROR state 1 = ERROR state
6	—	Reserved
5	ACTIVE_STS	Indicates the device is in the ACTIVE state. This is the fully operational state, supporting active sampling and data output. 0 = (Default) Not in ACTIVE state 1 = ACTIVE state
4	READY_STS	Indicates the device is in the READY state. The analog input path and internal clocking circuits are fully enabled. The data-output interface is enabled (assuming DOUT_READY_EN=1), ready to support sample data in the configured format. 0 = (Default) Not in READY state 1 = READY state
3:2	—	Reserved
1	IDLE_STS	Indicates the device is in the Idle State. This is a low-power state in which the device can be configured for the required operational behavior. 0 = (Default) Not in IDLE state 1 = IDLE state
0	STARTUP_STS	Indicates the device is in the Startup State. This is the initial state following reset, in which the device performs necessary start-up processes. 0 = (Default) Not in STARTUP state 1 = STARTUP state

8.4.7 DEVICE_STATUS_2

Address: 0x000 0312
BANK0 Address: 0x36

RO	7	6	5	4	3	2	1	0
	VDDA_STS	—						
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7	VDDA_STS	VDD_A status. Indicates whether a valid VDD_A supply is present. 0 = (Default) VDD_A is present 1 = VDD_A is not present.
6:0	—	Reserved

8.5 TIM_GEN—Sensor Timing Generator

8.5.1 TG_CONFIG1_0

Address: 0x000 0400
BANK0 Address: 0x48

RW	7	6	5	4	3	2	1	0
	VSMP_EXT_POL	EXTERNAL_MODE_TG_EN	CDS_EN	CLAMP_EN	CLAMP_MODE		TGSYNC_MODE	EXTERNAL_MODE_EN
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7	VSMP_EXT_POL	External Mode 2, VSMP polarity 0 = (Default) VSMP is detected at rising edge of input pad 1 = VSMP is detected at falling edge of input pad
6	EXTERNAL_MODE_TG_EN	Enable TG timer in External Mode 0 = (Default) Disabled 1 = Enabled

Bits	Name	Description
5	CDS_EN	AFE cds mode enable 0 = (Default) non CDS Sampling 1 = CDS Sampling
4	CLAMP_EN	AFE clamp enable 0 = (Default) Disable Clamp 1 = Enable Clamp
3:2	CLAMP_MODE	AFE clamp operation mode select 00 = (Default) Enabled for all pixels 01 = Controlled by clamp start/end 10 = Controlled by external RSMP 11 = Reserved
1	TGSYNC_MODE	Device master/slave selection 0 = (Default) TGSYNC output (master) 1 = TGSYNC input (slave)
0	EXTERNAL_MODE_EN	Device mode selection 0 = TG Mode 1 = (Default) External Mode

8.5.2 TG_CONFIG1_1

Address: 0x000 0401
BANK0 Address: 0x49

RW	7	6	5	4	3	2	1	0
	INIT_SEQ_STATE		VSMP_EXT_DLY					EXTERNAL_MODE_SEL
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	INIT_SEQ_STATE	Selects the initial sequence state 00 = (Default) State 0 01 = State 1 10 = State 2 11 = State 3
5:1	VSMP_EXT_DLY	External Mode 2, internal VSMP latency from VSMP_EXT input 0x00 = (Default) 1 clocks 0x01 = 2 clocks … 0x1F = 32 clocks
0	EXTERNAL_MODE_SEL	External Mode select In External Mode 2, VSMP/RSMP are internally re-generated from VSMP_EXT signal. 0 = (Default) External Mode 1 1 = External Mode 2

8.5.3 TG_CONFIG1_2

Address: 0x000 0402
BANK0 Address: 0x4A

RW	7	6	5	4	3	2	1	0
	—	TGSYNC_SINGLE_SEQ	NUM_SEQ_STATES		RSMP_EXT_DLY			
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7	—	Reserved
6	TGSYNC_SINGLE_SEQ	Cycle mode selection, valid for TG Input Mode only Multi Cycle: one TGSYNC pulse triggers a full cycle of the configured number of states Single Cycle: a TGSYNC pulse is required for each state transition 0 = (Default) Multi Cycle 1 = Single Cycle
5:4	NUM_SEQ_STATES	Number of sequence states 00 = (Default) 1 state 01 = 2 states 10 = 3 states 11 = 4 states
3:0	RSMP_EXT_DLY	External Mode 2, internal RSMP latency from internal VSMP 0x0 = 2 clocks 0x1 = (Default) 3 clocks … 0xF = 17 clocks

8.5.4 TG_CONFIG1_3

Address: 0x000 0403
BANK0 Address: 0x4B

RW	7	6	5	4	3	2	1	0
	—		CH6_CLAMP_OVRD	CH5_CLAMP_OVRD	CH4_CLAMP_OVRD	CH3_CLAMP_OVRD	CH2_CLAMP_OVRD	CH1_CLAMP_OVRD
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	CH6_CLAMP_OVRD	AFE clamp override switch control for CH6 0 = (Default) Disabled 1 = Enabled
4	CH5_CLAMP_OVRD	AFE clamp override switch control for CH5 0 = (Default) Disabled 1 = Enabled
3	CH4_CLAMP_OVRD	AFE clamp override switch control for CH4 0 = (Default) Disabled 1 = Enabled
2	CH3_CLAMP_OVRD	AFE clamp override switch control for CH3 0 = (Default) Disabled 1 = Enabled
1	CH2_CLAMP_OVRD	AFE clamp override switch control for CH2 0 = (Default) Disabled 1 = Enabled
0	CH1_CLAMP_OVRD	AFE clamp override switch control for CH1 0 = (Default) Disabled 1 = Enabled

8.5.5 TG_STATUS

Address: 0x000 040C
BANK2 Address: 0x0C

RO	7	6	5	4	3	2	1	0
	—						SEQ_STATE_STS	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1:0	SEQ_STATE_STS	current sequence state 00 = (Default) State 0 01 = State 1 10 = State 2 11 = State 3

8.5.6 TG_CONFIG2_0

Address: 0x000 0410
BANK2 Address: 0x10

RW	7	6	5	4	3	2	1	0
	—		LEDSTART_POL	LEDSTART_SEQ_INIT	TGSYNC_ASYNC	TGSYNC_IN_POL	TGSYNC_IN_SRC	
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7:6	—	Reserved
5	LEDSTART_POL	LEDSTART input polarity. Selects the active edge of the LEDSTART input. 0 = (Default) Rising 1 = Falling
4	LEDSTART_SEQ_INIT	Sequence start condition selection If this bit is set, the TG sequence can only be initiated using the TGSYNC and LEDSTART signals together. 0 = (Default) TGSYNC 1 = TGSYNC and LEDSTART
3	TGSYNC_ASYNC	TGSYNC Asynchronous Mode (synchroniser enable) This register is ignored if TGSYNC_FILT_EN = 1 0 = (Default) Sync Mode (internal synchroniser disabled) 1 = Async Mode (internal synchroniser enabled)

Bits	Name	Description
2	TGSYNC_IN_POL	TGSYNC input polarity. Selects the active edge of the selected TGSYNC input. 0 = Rising 1 = (Default) Falling
1:0	TGSYNC_IN_SRC	TGSYNC input source selection 00 = (Default) TGSYNC1 01 = TGSYNC2 10 = LEDSTART 11 = Reserved

8.5.7 TG_CONFIG2_1

Address: 0x000 0411
BANK2 Address: 0x11

RW	7	6	5	4	3	2	1	0
	—	TGSYNC_OUT_DUR			TGSYNC_IN_OFFSET			
Default	0	0	1	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	TGSYNC_OUT_DUR	TGSYNC output pulse width in Master Mode 000 = 1 clocks 001 = 2 clocks 010 = (Default) 3 clocks … 111 = 8 clocks
3:0	TGSYNC_IN_OFFSET	TGSYNC input offset delay for Slave Mode (TGSYNC input) 0x0 = (Default) 0 clocks 0x1 = 1 clocks … 0xF = 15 clocks

8.5.8 TG_CONFIG2_2

Address: 0x000 0412
BANK2 Address: 0x12

RW	7	6	5	4	3	2	1	0
	—	TGSYNC_FILT_STAGE			TGSYNC_FILT_DECM			TGSYNC_FILT_EN
Default	0	1	0	0	0	1	1	0

Bits	Name	Description
7	—	Reserved
6:4	TGSYNC_FILT_STAGE	TGSYNC filter stage selection 000 = 2 stage 001 = 4 stage 010 = 6 stage 011 = 8 stage 100 = (Default) 10 stage 101–111 = Reserved
3:1	TGSYNC_FILT_DECM	TGSYNC filter decimation frequency division ratio 000 = 1 divs 001 = 2 divs … 011 = (Default) 4 divs … 111 = 8 divs
0	TGSYNC_FILT_EN	TGSYNC input filter enable 0 = (Default) Disabled 1 = Enabled

8.5.9 TG_CONFIG2_3

Address: 0x000 0413
BANK2 Address: 0x13

RW	7	6	5	4	3	2	1	0
	—		TP_SEC_OFFSET					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	TP_SEC_OFFSET	Toggle point subsequence offset Toggle points (TPn) with an index less than the offset are associated with the primary counter Toggle points with an index greater than or equal to the offset are associated with the secondary counter

8.5.10 TG_CONFIG3_0

Address: 0x000 0414
BANK2 Address: 0x14

RW	7	6	5	4	3	2	1	0
	LEDG_PO_SEL				LEDR_PO_SEL			
Default	0	0	0	1	0	0	0	0

Bits	Name	Description
7:4	LEDG_PO_SEL	LEDG pulse signal selection from PO0 to PO10 0x0 = Pulse Output PO0 0x1 = (Default) Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved
3:0	LEDR_PO_SEL	LEDR pulse signal selection from PO0 to PO10 0x0 = (Default) Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved

8.5.11 TG_CONFIG3_1

Address: 0x000 0415
BANK2 Address: 0x15

RW	7	6	5	4	3	2	1	0
	DC_PO_2ND_PULSE	NUM_DC_PO			LEDB_PO_SEL			
Default	0	0	0	0	0	0	1	0

Bits	Name	Description
7	DC_PO_2ND_PULSE	Enable second rise/fall pulse for direct-controlled PO pulse signals. Second pulse is configured using TP20_PIXEL through TP31_PIXEL. 0 = (Default) Disabled 1 = Enabled
6:4	NUM_DC_PO	Select the number of direct-controlled PO pulse signals. Direct-control PO is configured using POx_TP_POL. 000 = (Default) None 001 = 1 (PO10) 010 = 2 (PO9-PO10) 011 = 3 (PO8-PO10) 100 = 4 (PO7-PO10) 101 = 5 (PO6-PO10) 110 = 6 (PO5-PO10) 111 = Reserved
3:0	LEDB_PO_SEL	LEDB pulse signal selection from PO0 to PO10 0x0 = Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = (Default) Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved

8.5.12 TG_CONFIG3_2

Address: 0x000 0416
BANK2 Address: 0x16

RW	7	6	5	4	3	2	1	0
	FLAG_DEN2_PO_SEL				FLAG_DEN1_PO_SEL			
Default	1	0	0	1	1	0	0	1

Bits	Name	Description
7:4	FLAG_DEN2_PO_SEL	FLAG_DEN2 pulse signal selection from PO0 to PO10 0x0 = Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = (Default) Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved
3:0	FLAG_DEN1_PO_SEL	FLAG_DEN1 pulse signal selection from PO0 to PO10 This is data flag signal for lvds trigger This signal has the same latency as ADC pipeline delay 0x0 = Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = (Default) Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved

8.5.13 TG_CONFIG3_3

Address: 0x000 0417
BANK2 Address: 0x17

RW	7	6	5	4	3	2	1	0
	—		FLAG_PIX2_PO_EDGE		FLAG_PIX2_PO_SEL			
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:6	—	Reserved
5:4	FLAG_PIX2_PO_EDGE	FLAG_PIX2 Pulse Output (PO) edge trigger option 00 = (Default) Disabled 01 = Rising Edge 10 = Falling Edge 11 = Both Edges
3:0	FLAG_PIX2_PO_SEL	FLAG_PIX2 pulse signal selection from PO0 to PO10 0x0 = Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = (Default) Pulse Output PO10 0xB–0xF = Reserved

8.5.14 SEQ_DURATION0_0

Address: 0x000 0418
BANK2 Address: 0x18

RW	7	6	5	4	3	2	1	0
	SEQ_STATE0_LEN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	SEQ_STATE0_LEN_0	Sequence State 0 period (number of pixels in State 0) Bits[7:0] of a 16-bit field.

8.5.15 SEQ_DURATION0_1

Address: 0x000 0419
BANK2 Address: 0x19

RW	7	6	5	4	3	2	1	0
	SEQ_STATE0_LEN_1							
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:0	SEQ_STATE0_LEN_1	Sequence State 0 period (number of pixels in State 0) Bits[15:8] of a 16-bit field.

8.5.16 SEQ_DURATION0_2

Address: 0x000 041A
BANK2 Address: 0x1A

RW	7	6	5	4	3	2	1	0
	SEQ_STATE1_LEN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	SEQ_STATE1_LEN_0	Sequence State 1 period (number of pixels in State 1) Bits[7:0] of a 16-bit field.

8.5.17 SEQ_DURATION0_3

Address: 0x000 041B
BANK2 Address: 0x1B

RW	7	6	5	4	3	2	1	0
	SEQ_STATE1_LEN_1							
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:0	SEQ_STATE1_LEN_1	Sequence State 1 period (number of pixels in State 1) Bits[15:8] of a 16-bit field.

8.5.18 SEQ_DURATION1_0

Address: 0x000 041C
BANK2 Address: 0x1C

RW	7	6	5	4	3	2	1	0
	SEQ_STATE2_LEN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	SEQ_STATE2_LEN_0	Sequence State 2 period (number of pixels in State 2) Bits[7:0] of a 16-bit field.

8.5.19 SEQ_DURATION1_1

Address: 0x000 041D
BANK2 Address: 0x1D

RW	7	6	5	4	3	2	1	0
	SEQ_STATE2_LEN_1							
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:0	SEQ_STATE2_LEN_1	Sequence State 2 period (number of pixels in State 2) Bits[15:8] of a 16-bit field.

8.5.20 SEQ_DURATION1_2

Address: 0x000 041E
BANK2 Address: 0x1E

RW	7	6	5	4	3	2	1	0
	SEQ_STATE3_LEN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	SEQ_STATE3_LEN_0	Sequence State 3 period (number of pixels in State 3) Bits[7:0] of a 16-bit field.

8.5.21 SEQ_DURATION1_3

Address: 0x000 041F
BANK2 Address: 0x1F

RW	7	6	5	4	3	2	1	0
	SEQ_STATE3_LEN_1							
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:0	SEQ_STATE3_LEN_1	Sequence State 3 period (number of pixels in State 3) Bits[15:8] of a 16-bit field.

8.5.22 TG_TIMING_CFG0_0

Address: 0x000 0420
BANK2 Address: 0x20

RW	7	6	5	4	3	2	1	0
	CK_MASK1_START_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_MASK1_START_0	CK_MASK1 start position This should be lower than the sequence-state period Bits[7:0] of a 16-bit field.

8.5.23 TG_TIMING_CFG0_1

Address: 0x000 0421
BANK2 Address: 0x21

RW	7	6	5	4	3	2	1	0
	CK_MASK1_START_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_MASK1_START_1	CK_MASK1 start position This should be lower than the sequence-state period Bits[15:8] of a 16-bit field.

8.5.24 TG_TIMING_CFG0_2

Address: 0x000 0422
BANK2 Address: 0x22

RW	7	6	5	4	3	2	1	0
	CK_MASK1_END_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_MASK1_END_0	CK_MASK1 end position This should be lower than the sequence-state period Bits[7:0] of a 16-bit field.

8.5.25 TG_TIMING_CFG0_3

Address: 0x000 0423
BANK2 Address: 0x23

RW	7	6	5	4	3	2	1	0
	CK_MASK1_END_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_MASK1_END_1	CK_MASK1 end position This should be lower than the sequence-state period Bits[15:8] of a 16-bit field.

8.5.26 TG_TIMING_CFG1_0

Address: 0x000 0424
BANK2 Address: 0x24

RW	7	6	5	4	3	2	1	0
	CK_MASK2_START_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_MASK2_START_0	CK_MASK2 start position This should be lower than the sequence-state period Bits[7:0] of a 16-bit field.

8.5.27 TG_TIMING_CFG1_1

Address: 0x000 0425
BANK2 Address: 0x25

RW	7	6	5	4	3	2	1	0
	CK_MASK2_START_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_MASK2_START_1	CK_MASK2 start position This should be lower than the sequence-state period Bits[15:8] of a 16-bit field.

8.5.28 TG_TIMING_CFG1_2

Address: 0x000 0426
BANK2 Address: 0x26

RW	7	6	5	4	3	2	1	0
	CK_MASK2_END_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_MASK2_END_0	CK_MASK2 end position This should be lower than the sequence-state period Bits[7:0] of a 16-bit field.

8.5.29 TG_TIMING_CFG1_3

Address: 0x000 0427
BANK2 Address: 0x27

RW	7	6	5	4	3	2	1	0
	CK_MASK2_END_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_MASK2_END_1	CK_MASK2 end position This should be lower than the sequence-state period Bits[15:8] of a 16-bit field.

8.5.30 TG_TIMING_CFG2_0

Address: 0x000 0428
BANK2 Address: 0x28

RW	7	6	5	4	3	2	1	0
	CK_MASK3_START_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_MASK3_START_0	CK_MASK3 start position This should be lower than the sequence-state period Bits[7:0] of a 16-bit field.

8.5.31 TG_TIMING_CFG2_1

Address: 0x000 0429
BANK2 Address: 0x29

RW	7	6	5	4	3	2	1	0
	CK_MASK3_START_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_MASK3_START_1	CK_MASK3 start position This should be lower than the sequence-state period Bits[15:8] of a 16-bit field.

8.5.32 TG_TIMING_CFG2_2

Address: 0x000 042A
BANK2 Address: 0x2A

RW	7	6	5	4	3	2	1	0
	CK_MASK3_END_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_MASK3_END_0	CK_MASK3 end position This should be lower than the sequence-state period Bits[7:0] of a 16-bit field.

8.5.33 TG_TIMING_CFG2_3

Address: 0x000 042B
BANK2 Address: 0x2B

RW	7	6	5	4	3	2	1	0
	CK_MASK3_END_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_MASK3_END_1	CK_MASK3 end position This should be lower than the sequence-state period Bits[15:8] of a 16-bit field.

8.5.34 TG_TIMING_CFG3_0

Address: 0x000 042C
BANK2 Address: 0x2C

RW	7	6	5	4	3	2	1	0
	CLAMP_START_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CLAMP_START_0	Clamp start position This should be lower than the sequence-state period Bits[7:0] of a 16-bit field.

8.5.35 TG_TIMING_CFG3_1

Address: 0x000 042D
BANK2 Address: 0x2D

RW	7	6	5	4	3	2	1	0
	CLAMP_START_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CLAMP_START_1	Clamp start position This should be lower than the sequence-state period Bits[15:8] of a 16-bit field.

8.5.36 TG_TIMING_CFG3_2

Address: 0x000 042E
BANK2 Address: 0x2E

RW	7	6	5	4	3	2	1	0
	CLAMP_END_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CLAMP_END_0	Clamp end position This should be lower than the sequence-state period Bits[7:0] of a 16-bit field.

8.5.37 TG_TIMING_CFG3_3

Address: 0x000 042F
BANK2 Address: 0x2F

RW	7	6	5	4	3	2	1	0
	CLAMP_END_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CLAMP_END_1	Clamp end position This should be lower than the sequence-state period Bits[15:8] of a 16-bit field.

8.5.38 TG_TIMING_CFG5_0

Address: 0x000 0434
BANK2 Address: 0x34

RW	7	6	5	4	3	2	1	0
	FLAG_PIX1_PIXEL1_0							
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7:0	FLAG_PIX1_PIXEL1_0	Pixel count for FLAG_PIX1 – 1st flag This should be lower than the sequence-state period Bits[7:0] of a 16-bit field.

8.5.39 TG_TIMING_CFG5_1

Address: 0x000 0435
BANK2 Address: 0x35

RW	7	6	5	4	3	2	1	0
	FLAG_PIX1_PIXEL1_1							
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7:0	FLAG_PIX1_PIXEL1_1	Pixel count for FLAG_PIX1 – 1st flag This should be lower than the sequence-state period Bits[15:8] of a 16-bit field.

8.5.40 TG_TIMING_CFG5_2

Address: 0x000 0436
BANK2 Address: 0x36

RW	7	6	5	4	3	2	1	0
	FLAG_PIX1_PIXEL2_0							
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7:0	FLAG_PIX1_PIXEL2_0	Pixel count for FLAG_PIX1 – 2nd flag This should be lower than the sequence-state period Bits[7:0] of a 16-bit field.

8.5.41 TG_TIMING_CFG5_3

Address: 0x000 0437
BANK2 Address: 0x37

RW	7	6	5	4	3	2	1	0
	FLAG_PIX1_PIXEL2_1							
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7:0	FLAG_PIX1_PIXEL2_1	Pixel count for FLAG_PIX1 – 2nd flag This should be lower than the sequence-state period Bits[15:8] of a 16-bit field.

8.5.42 TG_TIMING_CFG6_0

Address: 0x000 0438
BANK2 Address: 0x38

RW	7	6	5	4	3	2	1	0
	FLAG_PIX1_PIXEL3_0							
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7:0	FLAG_PIX1_ PIXEL3_0	Pixel count for FLAG_PIX1 – 3rd flag This should be lower than the sequence-state period Bits[7:0] of a 16-bit field.

8.5.43 TG_TIMING_CFG6_1

Address: 0x000 0439
BANK2 Address: 0x39

RW	7	6	5	4	3	2	1	0
	FLAG_PIX1_PIXEL3_1							
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7:0	FLAG_PIX1_ PIXEL3_1	Pixel count for FLAG_PIX1 – 3rd flag This should be lower than the sequence-state period Bits[15:8] of a 16-bit field.

8.5.44 TG_TIMING_CFG6_2

Address: 0x000 043A
BANK2 Address: 0x3A

RW	7	6	5	4	3	2	1	0
	FLAG_PIX1_PIXEL4_0							
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7:0	FLAG_PIX1_ PIXEL4_0	Pixel count for FLAG_PIX1 – 4th flag This should be lower than the sequence-state period Bits[7:0] of a 16-bit field.

8.5.45 TG_TIMING_CFG6_3

Address: 0x000 043B
BANK2 Address: 0x3B

RW	7	6	5	4	3	2	1	0
	FLAG_PIX1_PIXEL4_1							
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7:0	FLAG_PIX1_ PIXEL4_1	Pixel count for FLAG_PIX1 – 4th flag This should be lower than the sequence-state period Bits[15:8] of a 16-bit field.

8.5.46 TG_TIMING_CFG7_0

Address: 0x000 043C
BANK2 Address: 0x3C

RW	7	6	5	4	3	2	1	0
	—	ACYC_PO_POL	ACYC_PO_SEL				ACYC_MODE	ACYC_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6	ACYC_PO_POL	Auto-cycle timing reference polarity. Selects which edge of the selected PO source is used to trigger the gain/ offset update. 0 = (Default) Rise 1 = Fall

Bits	Name	Description
5:2	ACYC_PO_SEL	Auto Cycle (ACYC) pulse signal selection from PO0 to PO10 0x0 = (Default) Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved
1	ACYC_MODE	Auto-cycle timing reference selection 0 = (Default) pga_dly 1 = PO signal
0	ACYC_EN	Enables auto-cycle of gain/offset configuration 0 = (Default) Disabled 1 = Enabled

8.5.47 TG_TIMING_CFG7_1

Address: 0x000 043D
BANK2 Address: 0x3D

RW	7	6	5	4	3	2	1	0
	ACYC_DELAY							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ACYC_DELAY	Gain/offset delay from sequence-state transition. Valid in auto-cycle mode (ACYC_EN=1). Note this field should be set to 0x00 if BLC is enabled. 0x00 = (Default) 1 clocks 0x01 = 2 clocks … 0xFF = 256 clocks

8.5.48 TG_TIMING_CFG7_2

Address: 0x000 043E
BANK2 Address: 0x3E

RW	7	6	5	4	3	2	1	0
	BLC_START_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	BLC_START_0	Start pixel for black level calibration (BLC) This should be lower than the sequence-state period Bits[7:0] of a 16-bit field.

8.5.49 TG_TIMING_CFG7_3

Address: 0x000 043F
BANK2 Address: 0x3F

RW	7	6	5	4	3	2	1	0
	BLC_START_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	BLC_START_1	Start pixel for black level calibration (BLC) This should be lower than the sequence-state period Bits[15:8] of a 16-bit field.

8.5.50 TG_TIMING_CFG8_0

Address: 0x000 0440
BANK2 Address: 0x40

RW	7	6	5	4	3	2	1	0
	PO7_INIT_LVL	PO6_INIT_LVL	PO5_INIT_LVL	PO4_INIT_LVL	PO3_INIT_LVL	PO2_INIT_LVL	PO1_INIT_LVL	PO0_INIT_LVL
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	PO7_INIT_LVL	Initial PO7 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of PO7_TP_POL

Bits	Name	Description
6	PO6_INIT_LVL	Initial PO6 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of PO6_TP_POL
5	PO5_INIT_LVL	Initial PO5 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of PO5_TP_POL
4	PO4_INIT_LVL	Initial PO4 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of PO4_TP_POL
3	PO3_INIT_LVL	Initial PO3 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of PO3_TP_POL
2	PO2_INIT_LVL	Initial PO2 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of PO2_TP_POL
1	PO1_INIT_LVL	Initial PO1 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of PO1_TP_POL
0	PO0_INIT_LVL	Initial PO0 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of PO0_TP_POL

8.5.51 TG_TIMING_CFG8_1

Address: 0x000 0441
BANK2 Address: 0x41

RW	7	6	5	4	3	2	1	0
	—		CK_TOG3_INIT_LVL	CK_TOG2_INIT_LVL	CK_TOG1_INIT_LVL	PO10_INIT_LVL	PO9_INIT_LVL	PO8_INIT_LVL
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	CK_TOG3_INIT_LVL	Initial CK_TOG3 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of CK_TOG3_TP_POL
4	CK_TOG2_INIT_LVL	Initial CK_TOG2 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of CK_TOG2_TP_POL
3	CK_TOG1_INIT_LVL	Initial CK_TOG1 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of CK_TOG1_TP_POL
2	PO10_INIT_LVL	Initial PO10 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of PO10_TP_POL
1	PO9_INIT_LVL	Initial PO9 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of PO9_TP_POL
0	PO8_INIT_LVL	Initial PO8 level when the pixel counter is zero 0 = (Default) Initial level is unchanged from previous cycle 1 = Initial level is 1st toggle bit of PO8_TP_POL

8.5.52 TG_TIMING_CFG8_2

Address: 0x000 0442
BANK2 Address: 0x42

RW	7	6	5	4	3	2	1	0
	FIFO_RESET_DLY	PO10_DC_INIT_LVL	PO9_DC_INIT_LVL	PO8_DC_INIT_LVL	PO7_DC_INIT_LVL	PO6_DC_INIT_LVL	PO5_DC_INIT_LVL	PGEN_CNT_SEL
Default	1	0	0	0	0	0	0	1

Bits	Name	Description
7	FIFO_RESET_DLY	Enables a delay between the sequence-state transition and the FIFO reset. Only valid if FIFO_RESET_CTRL=1. 0 = No delay 1 = (Default) Delay 7 pixels
6	PO10_DC_INIT_LVL	Initial PO10 level when the pixel counter is zero. Valid if direct control is selected for PO10. 0 = (Default) 0 1 = 1
5	PO9_DC_INIT_LVL	Initial PO9 level when the pixel counter is zero. Valid if direct control is selected for PO9. 0 = (Default) 0 1 = 1
4	PO8_DC_INIT_LVL	Initial PO8 level when the pixel counter is zero. Valid if direct control is selected for PO8. 0 = (Default) 0 1 = 1
3	PO7_DC_INIT_LVL	Initial PO7 level when the pixel counter is zero. Valid if direct control is selected for PO7. 0 = (Default) 0 1 = 1
2	PO6_DC_INIT_LVL	Initial PO6 level when the pixel counter is zero. Valid if direct control is selected for PO6. 0 = (Default) 0 1 = 1
1	PO5_DC_INIT_LVL	Initial PO5 level when the pixel counter is zero. Valid if direct control is selected for PO5. 0 = (Default) 0 1 = 1
0	PGEN_CNT_SEL	Selects primary or secondary pixel counter to indicate new scan line. 0 = Primary counter (new line at initial sequence state) 1 = (Default) Secondary counter (new line on each sequence state)

8.5.53 TG_TIMING_CFG8_3

Address: 0x000 0443
BANK2 Address: 0x43

RW	7	6	5	4	3	2	1	0
	FIFO_BLANK_DUR					—		FIFO_RESET_CTRL
Default	1	1	0	0	1	0	0	0

Bits	Name	Description
7:3	FIFO_BLANK_DUR	Configures the blanking duration when flushing the FIFO. Only valid if FIFO_RESET_CTRL=1. 0x00 = 0 pixels 0x01 = 2 pixels … 0x19 = (Default) 50 pixels … 0x1F = 62 pixels
2:1	—	Reserved
0	FIFO_RESET_CTRL	Flushes and resets the FIFO at the start of each scan line. This option should be enabled if spread-spectrum modulation is enabled. 0 = (Default) Disabled 1 = Enabled

8.5.54 TG_POLARITY_T1_0

Address: 0x000 0444
BANK2 Address: 0x44

RW	7	6	5	4	3	2	1	0
	CK_TOG1_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_TOG1_TP_POL_0	Toggle Polarity for CK_TOG1; Bits[7:0] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.55 TG_POLARITY_T1_1

Address: 0x000 0445
BANK2 Address: 0x45

RW	7	6	5	4	3	2	1	0
	CK_TOG1_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_TOG1_TP_POL_1	Toggle Polarity for CK_TOG1; Bits[15:8] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.56 TG_POLARITY_T1_2

Address: 0x000 0446
BANK2 Address: 0x46

RW	7	6	5	4	3	2	1	0
	CK_TOG1_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_TOG1_TP_POL_2	Toggle Polarity for CK_TOG1; Bits[23:16] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.57 TG_POLARITY_T1_3

Address: 0x000 0447
BANK2 Address: 0x47

RW	7	6	5	4	3	2	1	0
	CK_TOG1_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_TOG1_TP_POL_3	Toggle Polarity for CK_TOG1; Bits[31:24] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.58 TG_POLARITY_T2_0

Address: 0x000 0448
BANK2 Address: 0x48

RW	7	6	5	4	3	2	1	0
	CK_TOG2_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_TOG2_TP_POL_0	Toggle Polarity for CK_TOG2; Bits[7:0] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.59 TG_POLARITY_T2_1

Address: 0x000 0449
BANK2 Address: 0x49

RW	7	6	5	4	3	2	1	0
	CK_TOG2_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_TOG2_TP_POL_1	Toggle Polarity for CK_TOG2; Bits[15:8] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.60 TG_POLARITY_T2_2

Address: 0x000 044A
BANK2 Address: 0x4A

RW	7	6	5	4	3	2	1	0
	CK_TOG2_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_TOG2_TP_POL_2	Toggle Polarity for CK_TOG2; Bits[23:16] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.61 TG_POLARITY_T2_3

Address: 0x000 044B
BANK2 Address: 0x4B

RW	7	6	5	4	3	2	1	0
	CK_TOG2_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_TOG2_TP_POL_3	Toggle Polarity for CK_TOG2; Bits[31:24] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.62 TG_POLARITY_T3_0

Address: 0x000 044C
BANK2 Address: 0x4C

RW	7	6	5	4	3	2	1	0
	CK_TOG3_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_TOG3_TP_POL_0	Toggle Polarity for CK_TOG3; Bits[7:0] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.63 TG_POLARITY_T3_1

Address: 0x000 044D
BANK2 Address: 0x4D

RW	7	6	5	4	3	2	1	0
	CK_TOG3_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_TOG3_TP_POL_1	Toggle Polarity for CK_TOG3; Bits[15:8] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.64 TG_POLARITY_T3_2

Address: 0x000 044E
BANK2 Address: 0x4E

RW	7	6	5	4	3	2	1	0
	CK_TOG3_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_TOG3_TP_POL_2	Toggle Polarity for CK_TOG3; Bits[23:16] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.65 TG_POLARITY_T3_3

Address: 0x000 044F
BANK2 Address: 0x4F

RW	7	6	5	4	3	2	1	0
	CK_TOG3_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CK_TOG3_TP_POL_3	Toggle Polarity for CK_TOG3; Bits[31:24] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.66 TG_POLARITY_PO0_0

Address: 0x000 0450
BANK2 Address: 0x50

RW	7	6	5	4	3	2	1	0
	PO0_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO0_TP_POL_0	Toggle Polarity for Pulse Out PO0; Bits[7:0] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.67 TG_POLARITY_PO0_1

Address: 0x000 0451
BANK2 Address: 0x51

RW	7	6	5	4	3	2	1	0
	PO0_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO0_TP_POL_1	Toggle Polarity for Pulse Out PO0; Bits[15:8] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.68 TG_POLARITY_PO0_2

Address: 0x000 0452
BANK2 Address: 0x52

RW	7	6	5	4	3	2	1	0
	PO0_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO0_TP_POL_2	Toggle Polarity for Pulse Out PO0; Bits[23:16] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.69 TG_POLARITY_PO0_3

Address: 0x000 0453
BANK2 Address: 0x53

RW	7	6	5	4	3	2	1	0
	PO0_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO0_TP_POL_3	Toggle Polarity for Pulse Out PO0; Bits[31:24] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.70 TG_POLARITY_PO1_0

Address: 0x000 0454
BANK2 Address: 0x54

RW	7	6	5	4	3	2	1	0
	PO1_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO1_TP_POL_0	Toggle Polarity for Pulse Out PO1; Bits[7:0] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.71 TG_POLARITY_PO1_1

Address: 0x000 0455
BANK2 Address: 0x55

RW	7	6	5	4	3	2	1	0
	PO1_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO1_TP_POL_1	Toggle Polarity for Pulse Out PO1; Bits[15:8] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.72 TG_POLARITY_PO1_2

Address: 0x000 0456
BANK2 Address: 0x56

RW	7	6	5	4	3	2	1	0
	PO1_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO1_TP_POL_2	Toggle Polarity for Pulse Out PO1; Bits[23:16] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.73 TG_POLARITY_PO1_3

Address: 0x000 0457
BANK2 Address: 0x57

RW	7	6	5	4	3	2	1	0
	PO1_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO1_TP_POL_3	Toggle Polarity for Pulse Out PO1; Bits[31:24] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.74 TG_POLARITY_PO2_0

Address: 0x000 0458
BANK2 Address: 0x58

RW	7	6	5	4	3	2	1	0
	PO2_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO2_TP_POL_0	Toggle Polarity for Pulse Out PO2; Bits[7:0] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.75 TG_POLARITY_PO2_1

Address: 0x000 0459
BANK2 Address: 0x59

RW	7	6	5	4	3	2	1	0
	PO2_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO2_TP_POL_1	Toggle Polarity for Pulse Out PO2; Bits[15:8] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.76 TG_POLARITY_PO2_2

Address: 0x000 045A
BANK2 Address: 0x5A

RW	7	6	5	4	3	2	1	0
	PO2_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO2_TP_POL_2	Toggle Polarity for Pulse Out PO2; Bits[23:16] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.77 TG_POLARITY_PO2_3

Address: 0x000 045B
BANK2 Address: 0x5B

RW	7	6	5	4	3	2	1	0
	PO2_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO2_TP_POL_3	Toggle Polarity for Pulse Out PO2; Bits[31:24] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.78 TG_POLARITY_PO3_0

Address: 0x000 045C
BANK2 Address: 0x5C

RW	7	6	5	4	3	2	1	0
	PO3_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO3_TP_POL_0	Toggle Polarity for Pulse Out PO3; Bits[7:0] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.79 TG_POLARITY_PO3_1

Address: 0x000 045D
BANK2 Address: 0x5D

RW	7	6	5	4	3	2	1	0
	PO3_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO3_TP_POL_1	Toggle Polarity for Pulse Out PO3; Bits[15:8] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.80 TG_POLARITY_PO3_2

Address: 0x000 045E
BANK2 Address: 0x5E

RW	7	6	5	4	3	2	1	0
	PO3_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO3_TP_POL_2	Toggle Polarity for Pulse Out PO3; Bits[23:16] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.81 TG_POLARITY_PO3_3

Address: 0x000 045F
BANK2 Address: 0x5F

RW	7	6	5	4	3	2	1	0
	PO3_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO3_TP_POL_3	Toggle Polarity for Pulse Out PO3; Bits[31:24] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.82 TG_POLARITY_PO4_0

Address: 0x000 0460
BANK2 Address: 0x60

RW	7	6	5	4	3	2	1	0
	PO4_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO4_TP_POL_0	Toggle Polarity for Pulse Out PO4; Bits[7:0] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.83 TG_POLARITY_PO4_1

Address: 0x000 0461
BANK2 Address: 0x61

RW	7	6	5	4	3	2	1	0
	PO4_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO4_TP_POL_1	Toggle Polarity for Pulse Out PO4; Bits[15:8] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.84 TG_POLARITY_PO4_2

Address: 0x000 0462
BANK2 Address: 0x62

RW	7	6	5	4	3	2	1	0
	PO4_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO4_TP_POL_2	Toggle Polarity for Pulse Out PO4; Bits[23:16] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.85 TG_POLARITY_PO4_3

Address: 0x000 0463
BANK2 Address: 0x63

RW	7	6	5	4	3	2	1	0
	PO4_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO4_TP_POL_3	Toggle Polarity for Pulse Out PO4; Bits[31:24] of a 32-bit field. Each bit represents either 0 or 1 at the corresponding toggle point

8.5.86 TG_POLARITY_PO5_0

Address: 0x000 0464
BANK2 Address: 0x64

RW	7	6	5	4	3	2	1	0
	PO5_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO5_TP_POL_0	Toggle Polarity for Pulse Out PO5; Bits[7:0] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO5 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[7:0] of the rising-edge pixel.

8.5.87 TG_POLARITY_PO5_1

Address: 0x000 0465
BANK2 Address: 0x65

RW	7	6	5	4	3	2	1	0
	PO5_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO5_TP_POL_1	Toggle Polarity for Pulse Out PO5; Bits[15:8] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO5 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[15:8] of the rising-edge pixel.

8.5.88 TG_POLARITY_PO5_2

Address: 0x000 0466
BANK2 Address: 0x66

RW	7	6	5	4	3	2	1	0
	PO5_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO5_TP_POL_2	Toggle Polarity for Pulse Out PO5; Bits[23:16] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO5 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[7:0] of the falling-edge pixel.

8.5.89 TG_POLARITY_PO5_3

Address: 0x000 0467
BANK2 Address: 0x67

RW	7	6	5	4	3	2	1	0
	PO5_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO5_TP_POL_3	Toggle Polarity for Pulse Out PO5; Bits[31:24] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO5 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[15:8] of the falling-edge pixel.

8.5.90 TG_POLARITY_PO6_0

Address: 0x000 0468
BANK2 Address: 0x68

RW	7	6	5	4	3	2	1	0
	PO6_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO6_TP_POL_0	Toggle Polarity for Pulse Out PO6; Bits[7:0] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO6 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[7:0] of the rising-edge pixel.

8.5.91 TG_POLARITY_PO6_1

Address: 0x000 0469
BANK2 Address: 0x69

RW	7	6	5	4	3	2	1	0
	PO6_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO6_TP_POL_1	Toggle Polarity for Pulse Out PO6; Bits[15:8] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO6 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[15:8] of the rising-edge pixel.

8.5.92 TG_POLARITY_PO6_2

Address: 0x000 046A
BANK2 Address: 0x6A

RW	7	6	5	4	3	2	1	0
	PO6_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO6_TP_POL_2	Toggle Polarity for Pulse Out PO6; Bits[23:16] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO6 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[7:0] of the falling-edge pixel.

8.5.93 TG_POLARITY_PO6_3

Address: 0x000 046B
BANK2 Address: 0x6B

RW	7	6	5	4	3	2	1	0
	PO6_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO6_TP_POL_3	Toggle Polarity for Pulse Out PO6; Bits[31:24] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO6 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[15:8] of the falling-edge pixel.

8.5.94 TG_POLARITY_PO7_0

Address: 0x000 046C
BANK2 Address: 0x6C

RW	7	6	5	4	3	2	1	0
	PO7_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO7_TP_POL_0	Toggle Polarity for Pulse Out PO7; Bits[7:0] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO7 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[7:0] of the rising-edge pixel.

8.5.95 TG_POLARITY_PO7_1

Address: 0x000 046D
BANK2 Address: 0x6D

RW	7	6	5	4	3	2	1	0
	PO7_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO7_TP_POL_1	Toggle Polarity for Pulse Out PO7; Bits[15:8] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO7 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[15:8] of the rising-edge pixel.

8.5.96 TG_POLARITY_PO7_2

Address: 0x000 046E
BANK2 Address: 0x6E

RW	7	6	5	4	3	2	1	0
	PO7_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO7_TP_POL_2	Toggle Polarity for Pulse Out PO7; Bits[23:16] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO7 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[7:0] of the falling-edge pixel.

8.5.97 TG_POLARITY_PO7_3

Address: 0x000 046F
BANK2 Address: 0x6F

RW	7	6	5	4	3	2	1	0
	PO7_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO7_TP_POL_3	Toggle Polarity for Pulse Out PO7; Bits[31:24] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO7 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[15:8] of the falling-edge pixel.

8.5.98 TG_POLARITY_PO8_0

Address: 0x000 0470
BANK2 Address: 0x70

RW	7	6	5	4	3	2	1	0
	PO8_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO8_TP_POL_0	Toggle Polarity for Pulse Out PO8; Bits[7:0] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO8 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[7:0] of the rising-edge pixel.

8.5.99 TG_POLARITY_PO8_1

Address: 0x000 0471
BANK2 Address: 0x71

RW	7	6	5	4	3	2	1	0
	PO8_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO8_TP_POL_1	Toggle Polarity for Pulse Out PO8; Bits[15:8] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO8 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[15:8] of the rising-edge pixel.

8.5.100 TG_POLARITY_PO8_2

Address: 0x000 0472
BANK2 Address: 0x72

RW	7	6	5	4	3	2	1	0
	PO8_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO8_TP_POL_2	Toggle Polarity for Pulse Out PO8; Bits[23:16] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO8 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[7:0] of the falling-edge pixel.

8.5.101 TG_POLARITY_PO8_3

Address: 0x000 0473
BANK2 Address: 0x73

RW	7	6	5	4	3	2	1	0
	PO8_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO8_TP_POL_3	Toggle Polarity for Pulse Out PO8; Bits[31:24] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO8 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[15:8] of the falling-edge pixel.

8.5.102 TG_POLARITY_PO9_0

Address: 0x000 0474
BANK2 Address: 0x74

RW	7	6	5	4	3	2	1	0
	PO9_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO9_TP_POL_0	Toggle Polarity for Pulse Out PO9; Bits[7:0] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO9 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[7:0] of the rising-edge pixel.

8.5.103 TG_POLARITY_PO9_1

Address: 0x000 0475
BANK2 Address: 0x75

RW	7	6	5	4	3	2	1	0
	PO9_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO9_TP_POL_1	Toggle Polarity for Pulse Out PO9; Bits[15:8] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO9 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[15:8] of the rising-edge pixel.

8.5.104 TG_POLARITY_PO9_2

Address: 0x000 0476
BANK2 Address: 0x76

RW	7	6	5	4	3	2	1	0
	PO9_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO9_TP_POL_2	Toggle Polarity for Pulse Out PO9; Bits[23:16] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO9 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[7:0] of the falling-edge pixel.

8.5.105 TG_POLARITY_PO9_3

Address: 0x000 0477
BANK2 Address: 0x77

RW	7	6	5	4	3	2	1	0
	PO9_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO9_TP_POL_3	Toggle Polarity for Pulse Out PO9; Bits[31:24] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO9 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[15:8] of the falling-edge pixel.

8.5.106 TG_POLARITY_PO10_0

Address: 0x000 0478
BANK2 Address: 0x78

RW	7	6	5	4	3	2	1	0
	PO10_TP_POL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO10_TP_POL_0	Toggle Polarity for Pulse Out PO10; Bits[7:0] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO10 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[7:0] of the rising-edge pixel.

8.5.107 TG_POLARITY_PO10_1

Address: 0x000 0479
BANK2 Address: 0x79

RW	7	6	5	4	3	2	1	0
	PO10_TP_POL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO10_TP_POL_1	Toggle Polarity for Pulse Out PO10; Bits[15:8] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO10 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[15:8] of the rising-edge pixel.

8.5.108 TG_POLARITY_PO10_2

Address: 0x000 047A
BANK2 Address: 0x7A

RW	7	6	5	4	3	2	1	0
	PO10_TP_POL_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO10_TP_POL_2	Toggle Polarity for Pulse Out PO10; Bits[23:16] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO10 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[7:0] of the falling-edge pixel.

8.5.109 TG_POLARITY_PO10_3

Address: 0x000 047B
BANK2 Address: 0x7B

RW	7	6	5	4	3	2	1	0
	PO10_TP_POL_3							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PO10_TP_POL_3	Toggle Polarity for Pulse Out PO10; Bits[31:24] of a 32-bit field; each bit represents either 0 or 1 at the corresponding toggle point. If PO10 is configured for direct control, this field configures the rising and falling edges of the pulse; this byte is Bits[15:8] of the falling-edge pixel.

8.5.110 TG_REFCNT_SEL_0

Address: 0x000 047C
BANK2 Address: 0x7C

RW	7	6	5	4	3	2	1	0
	—					CLAMP_CNT_SEL	BLC_CNT_SEL	FLAG_PIX1_CNT_SEL
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	CLAMP_CNT_SEL	CLAMP reference counter select 0 = (Default) Primary 1 = Secondary
1	BLC_CNT_SEL	BLC reference counter select 0 = (Default) Primary 1 = Secondary
0	FLAG_PIX1_CNT_SEL	FLAG_PIX1 reference counter select 0 = (Default) Primary 1 = Secondary

8.5.111 TG_REFCNT_SEL_1

Address: 0x000 047D
BANK2 Address: 0x7D

RW	7	6	5	4	3	2	1	0
	—		CK_TOG3_CNT_SEL	CK_TOG2_CNT_SEL	CK_TOG1_CNT_SEL	CK_MASK3_CNT_SEL	CK_MASK2_CNT_SEL	CK_MASK1_CNT_SEL
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	CK_TOG3_CNT_SEL	CK_TOG3 reference counter select 0 = (Default) Primary 1 = Secondary
4	CK_TOG2_CNT_SEL	CK_TOG2 reference counter select 0 = (Default) Primary 1 = Secondary
3	CK_TOG1_CNT_SEL	CK_TOG1 reference counter select 0 = (Default) Primary 1 = Secondary
2	CK_MASK3_CNT_SEL	CK_MASK3 reference counter select 0 = (Default) Primary 1 = Secondary
1	CK_MASK2_CNT_SEL	CK_MASK2 reference counter select 0 = (Default) Primary 1 = Secondary
0	CK_MASK1_CNT_SEL	CK_MASK1 reference counter select 0 = (Default) Primary 1 = Secondary

8.5.112 TG_REFCNT_SEL_2

Address: 0x000 047E
BANK2 Address: 0x7E

RW	7	6	5	4	3	2	1	0
	PO7_CNT_SEL	PO6_CNT_SEL	PO5_CNT_SEL	PO4_CNT_SEL	PO3_CNT_SEL	PO2_CNT_SEL	PO1_CNT_SEL	PO0_CNT_SEL
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	PO7_CNT_SEL	Pulse Output PO7 reference counter select 0 = (Default) Primary 1 = Secondary
6	PO6_CNT_SEL	Pulse Output PO6 reference counter select 0 = (Default) Primary 1 = Secondary

Bits	Name	Description
5	PO5_CNT_SEL	Pulse Output PO5 reference counter select 0 = (Default) Primary 1 = Secondary
4	PO4_CNT_SEL	Pulse Output PO4 reference counter select 0 = (Default) Primary 1 = Secondary
3	PO3_CNT_SEL	Pulse Output PO3 reference counter select 0 = (Default) Primary 1 = Secondary
2	PO2_CNT_SEL	Pulse Output PO2 reference counter select 0 = (Default) Primary 1 = Secondary
1	PO1_CNT_SEL	Pulse Output PO1 reference counter select 0 = (Default) Primary 1 = Secondary
0	PO0_CNT_SEL	Pulse Output PO0 reference counter select 0 = (Default) Primary 1 = Secondary

8.5.113 TG_REFCNT_SEL_3

Address: 0x000 047F
BANK2 Address: 0x7F

RW	7	6	5	4	3	2	1	0
	—					PO10_CNT_SEL	PO9_CNT_SEL	PO8_CNT_SEL
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	PO10_CNT_SEL	Pulse Output PO10 reference counter select 0 = (Default) Primary 1 = Secondary
1	PO9_CNT_SEL	Pulse Output PO9 reference counter select 0 = (Default) Primary 1 = Secondary
0	PO8_CNT_SEL	Pulse Output PO8 reference counter select 0 = (Default) Primary 1 = Secondary

8.5.114 TG_CYCPAT_CFG0_0

Address: 0x000 048C
BANK3 Address: 0x0C

RW	7	6	5	4	3	2	1	0
	BLC_SEQ_SEL				FLAG_PIX1_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	BLC_SEQ_SEL	BLC sequence state select. Valid if BLC first pixel is referenced to the secondary pixel counter (BLC_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3
3:0	FLAG_PIX1_SEQ_SEL	FLAG_PIX1 sequence state select. Valid if flag pixel is referenced to the secondary pixel counter (FLAG_PIX1_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

8.5.115 TG_CYCPAT_CFG0_1

Address: 0x000 048D
BANK3 Address: 0x0D

RW	7	6	5	4	3	2	1	0
	—				CLAMP_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CLAMP_SEQ_SEL	CLAMP sequence state select. Valid if clamp range is referenced to the secondary pixel counter (CLAMP_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

8.5.116 TG_CYCPAT_CFG0_2

Address: 0x000 048E
BANK3 Address: 0x0E

RW	7	6	5	4	3	2	1	0
	CK_MASK2_SEQ_SEL				CK_MASK1_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	CK_MASK2_SEQ_SEL	CK_MASK2 sequence state select. Valid if CK_MASK2 is referenced to the secondary pixel counter (CK_MASK2_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3
3:0	CK_MASK1_SEQ_SEL	CK_MASK1 sequence state select. Valid if CK_MASK1 is referenced to the secondary pixel counter (CK_MASK1_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

8.5.117 TG_CYCPAT_CFG0_3

Address: 0x000 048F
BANK3 Address: 0x0F

RW	7	6	5	4	3	2	1	0
	—				CK_MASK3_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CK_MASK3_SEQ_SEL	CK_MASK3 sequence state select. Valid if CK_MASK3 is referenced to the secondary pixel counter (CK_MASK3_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

8.5.118 TG_CYCPAT_CFG1_0

Address: 0x000 0490
BANK3 Address: 0x10

RW	7	6	5	4	3	2	1	0
	CK_TOG2_SEQ_SEL				CK_TOG1_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	CK_TOG2_SEQ_SEL	CK_TOG2 sequence state select. Valid if CK_TOG2 is referenced to the secondary pixel counter (CK_TOG2_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3
3:0	CK_TOG1_SEQ_SEL	CK_TOG1 sequence state select. Valid if CK_TOG1 is referenced to the secondary pixel counter (CK_TOG1_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

8.5.119 TG_CYCPAT_CFG1_1

Address: 0x000 0491
BANK3 Address: 0x11

RW	7	6	5	4	3	2	1	0
	PO0_SEQ_SEL				CK_TOG3_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PO0_SEQ_SEL	Pulse Output PO0 sequence state select. Valid if PO0 is referenced to the secondary pixel counter (PO0_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3
3:0	CK_TOG3_SEQ_SEL	CK_TOG3 sequence state select. Valid if CK_TOG3 is referenced to the secondary pixel counter (CK_TOG3_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

8.5.120 TG_CYCPAT_CFG1_2

Address: 0x000 0492
BANK3 Address: 0x12

RW	7	6	5	4	3	2	1	0
	PO2_SEQ_SEL				PO1_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PO2_SEQ_SEL	Pulse Output PO2 sequence state select. Valid if PO2 is referenced to the secondary pixel counter (PO2_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3
3:0	PO1_SEQ_SEL	Pulse Output PO1 sequence state select. Valid if PO1 is referenced to the secondary pixel counter (PO1_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

8.5.121 TG_CYCPAT_CFG1_3

Address: 0x000 0493
BANK3 Address: 0x13

RW	7	6	5	4	3	2	1	0
	—				PO3_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	PO3_SEQ_SEL	Pulse Output PO3 sequence state select. Valid if PO3 is referenced to the secondary pixel counter (PO3_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

8.5.122 TG_CYCPAT_CFG2_0

Address: 0x000 0494
BANK3 Address: 0x14

RW	7	6	5	4	3	2	1	0
	PO5_SEQ_SEL				PO4_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PO5_SEQ_SEL	Pulse Output PO5 sequence state select. Valid if PO5 is referenced to the secondary pixel counter (PO5_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3
3:0	PO4_SEQ_SEL	Pulse Output PO4 sequence state select. Valid if PO4 is referenced to the secondary pixel counter (PO4_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

8.5.123 TG_CYCPAT_CFG2_1

Address: 0x000 0495
BANK3 Address: 0x15

RW	7	6	5	4	3	2	1	0
	PO7_SEQ_SEL				PO6_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PO7_SEQ_SEL	Pulse Output PO7 sequence state select. Valid if PO7 is referenced to the secondary pixel counter (PO7_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3
3:0	PO6_SEQ_SEL	Pulse Output PO6 sequence state select. Valid if PO6 is referenced to the secondary pixel counter (PO6_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

8.5.124 TG_CYCPAT_CFG2_2

Address: 0x000 0496
BANK3 Address: 0x16

RW	7	6	5	4	3	2	1	0
	PO9_SEQ_SEL				PO8_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PO9_SEQ_SEL	Pulse Output PO9 sequence state select. Valid if PO9 is referenced to the secondary pixel counter (PO9_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3
3:0	PO8_SEQ_SEL	Pulse Output PO8 sequence state select. Valid if PO8 is referenced to the secondary pixel counter (PO8_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

8.5.125 TG_CYCPAT_CFG2_3

Address: 0x000 0497
BANK3 Address: 0x17

RW	7	6	5	4	3	2	1	0
	—				PO10_SEQ_SEL			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	PO10_SEQ_SEL	Pulse Output PO10 sequence state select. Valid if PO10 is referenced to the secondary pixel counter (PO10_CNT_SEL=1). Bit [0] – enable in State 0 Bit [1] – enable in State 1 Bit [2] – enable in State 2 Bit [3] – enable in State 3

8.5.126 TG_TOGGLE_POINT0_0

Address: 0x000 0498
BANK3 Address: 0x18

RW	7	6	5	4	3	2	1	0
	TP0_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP0_PIXEL_0	TP0 toggle point. Defines the pixel-counter value for TP0. Bits[7:0] of a 16-bit field.

8.5.127 TG_TOGGLE_POINT0_1

Address: 0x000 0499
BANK3 Address: 0x19

RW	7	6	5	4	3	2	1	0
	TP0_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP0_PIXEL_1	TP0 toggle point. Defines the pixel-counter value for TP0. Bits[15:8] of a 16-bit field.

8.5.128 TG_TOGGLE_POINT0_2

Address: 0x000 049A
BANK3 Address: 0x1A

RW	7	6	5	4	3	2	1	0
	TP1_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP1_PIXEL_0	TP1 toggle point. Defines the pixel-counter value for TP1. Bits[7:0] of a 16-bit field.

8.5.129 TG_TOGGLE_POINT0_3

Address: 0x000 049B
BANK3 Address: 0x1B

RW	7	6	5	4	3	2	1	0
	TP1_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP1_PIXEL_1	TP1 toggle point. Defines the pixel-counter value for TP1. Bits[15:8] of a 16-bit field.

8.5.130 TG_TOGGLE_POINT1_0

Address: 0x000 049C
BANK3 Address: 0x1C

RW	7	6	5	4	3	2	1	0
	TP2_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP2_PIXEL_0	TP2 toggle point. Defines the pixel-counter value for TP2. Bits[7:0] of a 16-bit field.

8.5.131 TG_TOGGLE_POINT1_1

Address: 0x000 049D
BANK3 Address: 0x1D

RW	7	6	5	4	3	2	1	0
	TP2_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP2_PIXEL_1	TP2 toggle point. Defines the pixel-counter value for TP2. Bits[15:8] of a 16-bit field.

8.5.132 TG_TOGGLE_POINT1_2

Address: 0x000 049E
BANK3 Address: 0x1E

RW	7	6	5	4	3	2	1	0
	TP3_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP3_PIXEL_0	TP3 toggle point. Defines the pixel-counter value for TP3. Bits[7:0] of a 16-bit field.

8.5.133 TG_TOGGLE_POINT1_3

Address: 0x000 049F
BANK3 Address: 0x1F

RW	7	6	5	4	3	2	1	0
	TP3_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP3_PIXEL_1	TP3 toggle point. Defines the pixel-counter value for TP3. Bits[15:8] of a 16-bit field.

8.5.134 TG_TOGGLE_POINT2_0

Address: 0x000 04A0
BANK3 Address: 0x20

RW	7	6	5	4	3	2	1	0
	TP4_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP4_PIXEL_0	TP4 toggle point. Defines the pixel-counter value for TP4. Bits[7:0] of a 16-bit field.

8.5.135 TG_TOGGLE_POINT2_1

Address: 0x000 04A1
BANK3 Address: 0x21

RW	7	6	5	4	3	2	1	0
	TP4_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP4_PIXEL_1	TP4 toggle point. Defines the pixel-counter value for TP4. Bits[15:8] of a 16-bit field.

8.5.136 TG_TOGGLE_POINT2_2

Address: 0x000 04A2
BANK3 Address: 0x22

RW	7	6	5	4	3	2	1	0
	TP5_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP5_PIXEL_0	TP5 toggle point. Defines the pixel-counter value for TP5. Bits[7:0] of a 16-bit field.

8.5.137 TG_TOGGLE_POINT2_3

Address: 0x000 04A3
BANK3 Address: 0x23

RW	7	6	5	4	3	2	1	0
	TP5_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP5_PIXEL_1	TP5 toggle point. Defines the pixel-counter value for TP5. Bits[15:8] of a 16-bit field.

8.5.138 TG_TOGGLE_POINT3_0

Address: 0x000 04A4
BANK3 Address: 0x24

RW	7	6	5	4	3	2	1	0
	TP6_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP6_PIXEL_0	TP6 toggle point. Defines the pixel-counter value for TP6. Bits[7:0] of a 16-bit field.

8.5.139 TG_TOGGLE_POINT3_1

Address: 0x000 04A5
BANK3 Address: 0x25

RW	7	6	5	4	3	2	1	0
	TP6_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP6_PIXEL_1	TP6 toggle point. Defines the pixel-counter value for TP6. Bits[15:8] of a 16-bit field.

8.5.140 TG_TOGGLE_POINT3_2

Address: 0x000 04A6
BANK3 Address: 0x26

RW	7	6	5	4	3	2	1	0
	TP7_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP7_PIXEL_0	TP7 toggle point. Defines the pixel-counter value for TP7. Bits[7:0] of a 16-bit field.

8.5.141 TG_TOGGLE_POINT3_3

Address: 0x000 04A7
BANK3 Address: 0x27

RW	7	6	5	4	3	2	1	0
	TP7_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP7_PIXEL_1	TP7 toggle point. Defines the pixel-counter value for TP7. Bits[15:8] of a 16-bit field.

8.5.142 TG_TOGGLE_POINT4_0

Address: 0x000 04A8
BANK3 Address: 0x28

RW	7	6	5	4	3	2	1	0
	TP8_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP8_PIXEL_0	TP8 toggle point. Defines the pixel-counter value for TP8. Bits[7:0] of a 16-bit field.

8.5.143 TG_TOGGLE_POINT4_1

Address: 0x000 04A9
BANK3 Address: 0x29

RW	7	6	5	4	3	2	1	0
	TP8_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP8_PIXEL_1	TP8 toggle point. Defines the pixel-counter value for TP8. Bits[15:8] of a 16-bit field.

8.5.144 TG_TOGGLE_POINT4_2

Address: 0x000 04AA
BANK3 Address: 0x2A

RW	7	6	5	4	3	2	1	0
	TP9_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP9_PIXEL_0	TP9 toggle point. Defines the pixel-counter value for TP9. Bits[7:0] of a 16-bit field.

8.5.145 TG_TOGGLE_POINT4_3

Address: 0x000 04AB
BANK3 Address: 0x2B

RW	7	6	5	4	3	2	1	0
	TP9_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP9_PIXEL_1	TP9 toggle point. Defines the pixel-counter value for TP9. Bits[15:8] of a 16-bit field.

8.5.146 TG_TOGGLE_POINT5_0

Address: 0x000 04AC
BANK3 Address: 0x2C

RW	7	6	5	4	3	2	1	0
	TP10_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP10_PIXEL_0	TP10 toggle point. Defines the pixel-counter value for TP10. Bits[7:0] of a 16-bit field.

8.5.147 TG_TOGGLE_POINT5_1

Address: 0x000 04AD
BANK3 Address: 0x2D

RW	7	6	5	4	3	2	1	0
	TP10_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP10_PIXEL_1	TP10 toggle point. Defines the pixel-counter value for TP10. Bits[15:8] of a 16-bit field.

8.5.148 TG_TOGGLE_POINT5_2

Address: 0x000 04AE
BANK3 Address: 0x2E

RW	7	6	5	4	3	2	1	0
	TP11_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP11_PIXEL_0	TP11 toggle point. Defines the pixel-counter value for TP11. Bits[7:0] of a 16-bit field.

8.5.149 TG_TOGGLE_POINT5_3

Address: 0x000 04AF
BANK3 Address: 0x2F

RW	7	6	5	4	3	2	1	0
	TP11_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP11_PIXEL_1	TP11 toggle point. Defines the pixel-counter value for TP11. Bits[15:8] of a 16-bit field.

8.5.150 TG_TOGGLE_POINT6_0

Address: 0x000 04B0
BANK3 Address: 0x30

RW	7	6	5	4	3	2	1	0
	TP12_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP12_PIXEL_0	TP12 toggle point. Defines the pixel-counter value for TP12. Bits[7:0] of a 16-bit field.

8.5.151 TG_TOGGLE_POINT6_1

Address: 0x000 04B1
BANK3 Address: 0x31

RW	7	6	5	4	3	2	1	0
	TP12_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP12_PIXEL_1	TP12 toggle point. Defines the pixel-counter value for TP12. Bits[15:8] of a 16-bit field.

8.5.152 TG_TOGGLE_POINT6_2

Address: 0x000 04B2
BANK3 Address: 0x32

RW	7	6	5	4	3	2	1	0
	TP13_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP13_PIXEL_0	TP13 toggle point. Defines the pixel-counter value for TP13. Bits[7:0] of a 16-bit field.

8.5.153 TG_TOGGLE_POINT6_3

Address: 0x000 04B3
BANK3 Address: 0x33

RW	7	6	5	4	3	2	1	0
	TP13_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP13_PIXEL_1	TP13 toggle point. Defines the pixel-counter value for TP13. Bits[15:8] of a 16-bit field.

8.5.154 TG_TOGGLE_POINT7_0

Address: 0x000 04B4
BANK3 Address: 0x34

RW	7	6	5	4	3	2	1	0
	TP14_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP14_PIXEL_0	TP14 toggle point. Defines the pixel-counter value for TP14. Bits[7:0] of a 16-bit field.

8.5.155 TG_TOGGLE_POINT7_1

Address: 0x000 04B5
BANK3 Address: 0x35

RW	7	6	5	4	3	2	1	0
	TP14_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP14_PIXEL_1	TP14 toggle point. Defines the pixel-counter value for TP14. Bits[15:8] of a 16-bit field.

8.5.156 TG_TOGGLE_POINT7_2

Address: 0x000 04B6
BANK3 Address: 0x36

RW	7	6	5	4	3	2	1	0
	TP15_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP15_PIXEL_0	TP15 toggle point. Defines the pixel-counter value for TP15. Bits[7:0] of a 16-bit field.

8.5.157 TG_TOGGLE_POINT7_3

Address: 0x000 04B7
BANK3 Address: 0x37

RW	7	6	5	4	3	2	1	0
	TP15_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP15_PIXEL_1	TP15 toggle point. Defines the pixel-counter value for TP15. Bits[15:8] of a 16-bit field.

8.5.158 TG_TOGGLE_POINT8_0

Address: 0x000 04B8
BANK3 Address: 0x38

RW	7	6	5	4	3	2	1	0
	TP16_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP16_PIXEL_0	TP16 toggle point. Defines the pixel-counter value for TP16. Bits[7:0] of a 16-bit field.

8.5.159 TG_TOGGLE_POINT8_1

Address: 0x000 04B9
BANK3 Address: 0x39

RW	7	6	5	4	3	2	1	0
	TP16_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP16_PIXEL_1	TP16 toggle point. Defines the pixel-counter value for TP16. Bits[15:8] of a 16-bit field.

8.5.160 TG_TOGGLE_POINT8_2

Address: 0x000 04BA
BANK3 Address: 0x3A

RW	7	6	5	4	3	2	1	0
	TP17_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP17_PIXEL_0	TP17 toggle point. Defines the pixel-counter value for TP17. Bits[7:0] of a 16-bit field.

8.5.161 TG_TOGGLE_POINT8_3

Address: 0x000 04BB
BANK3 Address: 0x3B

RW	7	6	5	4	3	2	1	0
	TP17_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP17_PIXEL_1	TP17 toggle point. Defines the pixel-counter value for TP17. Bits[15:8] of a 16-bit field.

8.5.162 TG_TOGGLE_POINT9_0

Address: 0x000 04BC
BANK3 Address: 0x3C

RW	7	6	5	4	3	2	1	0
	TP18_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP18_PIXEL_0	TP18 toggle point. Defines the pixel-counter value for TP18. Bits[7:0] of a 16-bit field.

8.5.163 TG_TOGGLE_POINT9_1

Address: 0x000 04BD
BANK3 Address: 0x3D

RW	7	6	5	4	3	2	1	0
	TP18_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP18_PIXEL_1	TP18 toggle point. Defines the pixel-counter value for TP18. Bits[15:8] of a 16-bit field.

8.5.164 TG_TOGGLE_POINT9_2

Address: 0x000 04BE
BANK3 Address: 0x3E

RW	7	6	5	4	3	2	1	0
	TP19_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP19_PIXEL_0	TP19 toggle point. Defines the pixel-counter value for TP19. Bits[7:0] of a 16-bit field.

8.5.165 TG_TOGGLE_POINT9_3

Address: 0x000 04BF
BANK3 Address: 0x3F

RW	7	6	5	4	3	2	1	0
	TP19_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP19_PIXEL_1	TP19 toggle point. Defines the pixel-counter value for TP19. Bits[15:8] of a 16-bit field.

8.5.166 TG_TOGGLE_POINT10_0

Address: 0x000 04C0
BANK3 Address: 0x40

RW	7	6	5	4	3	2	1	0
	TP20_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP20_PIXEL_0	TP20 toggle point. Defines the pixel-counter value for TP20. If PO5 is configured for direct control and second pulse is enabled, this field configures the rising edge of the second pulse; TP20 is not supported in this case. Bits[7:0] of a 16-bit field.

8.5.167 TG_TOGGLE_POINT10_1

Address: 0x000 04C1
BANK3 Address: 0x41

RW	7	6	5	4	3	2	1	0
	TP20_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP20_PIXEL_1	TP20 toggle point. Defines the pixel-counter value for TP20. If PO5 is configured for direct control and second pulse is enabled, this field configures the rising edge of the second pulse; TP20 is not supported in this case. Bits[15:8] of a 16-bit field.

8.5.168 TG_TOGGLE_POINT10_2

Address: 0x000 04C2
BANK3 Address: 0x42

RW	7	6	5	4	3	2	1	0
	TP21_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP21_PIXEL_0	TP21 toggle point. Defines the pixel-counter value for TP21. If PO5 is configured for direct control and second pulse is enabled, this field configures the falling edge of the second pulse; TP21 is not supported in this case. Bits[7:0] of a 16-bit field.

8.5.169 TG_TOGGLE_POINT10_3

Address: 0x000 04C3
BANK3 Address: 0x43

RW	7	6	5	4	3	2	1	0
	TP21_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP21_PIXEL_1	TP21 toggle point. Defines the pixel-counter value for TP21. If PO5 is configured for direct control and second pulse is enabled, this field configures the falling edge of the second pulse; TP21 is not supported in this case. Bits[15:8] of a 16-bit field.

8.5.170 TG_TOGGLE_POINT11_0

Address: 0x000 04C4
BANK3 Address: 0x44

RW	7	6	5	4	3	2	1	0
	TP22_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP22_PIXEL_0	TP22 toggle point. Defines the pixel-counter value for TP22. If PO6 is configured for direct control and second pulse is enabled, this field configures the rising edge of the second pulse; TP22 is not supported in this case. Bits[7:0] of a 16-bit field.

8.5.171 TG_TOGGLE_POINT11_1

Address: 0x000 04C5
BANK3 Address: 0x45

RW	7	6	5	4	3	2	1	0
	TP22_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP22_PIXEL_1	TP22 toggle point. Defines the pixel-counter value for TP22. If PO6 is configured for direct control and second pulse is enabled, this field configures the rising edge of the second pulse; TP22 is not supported in this case. Bits[15:8] of a 16-bit field.

8.5.172 TG_TOGGLE_POINT11_2

Address: 0x000 04C6
BANK3 Address: 0x46

RW	7	6	5	4	3	2	1	0
	TP23_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP23_PIXEL_0	TP23 toggle point. Defines the pixel-counter value for TP23. If PO6 is configured for direct control and second pulse is enabled, this field configures the falling edge of the second pulse; TP23 is not supported in this case. Bits[7:0] of a 16-bit field.

8.5.173 TG_TOGGLE_POINT11_3

Address: 0x000 04C7
BANK3 Address: 0x47

RW	7	6	5	4	3	2	1	0
	TP23_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP23_PIXEL_1	TP23 toggle point. Defines the pixel-counter value for TP23. If PO6 is configured for direct control and second pulse is enabled, this field configures the falling edge of the second pulse; TP23 is not supported in this case. Bits[15:8] of a 16-bit field.

8.5.174 TG_TOGGLE_POINT12_0

Address: 0x000 04C8
BANK3 Address: 0x48

RW	7	6	5	4	3	2	1	0
	TP24_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP24_PIXEL_0	TP24 toggle point. Defines the pixel-counter value for TP24. If PO7 is configured for direct control and second pulse is enabled, this field configures the rising edge of the second pulse; TP24 is not supported in this case. Bits[7:0] of a 16-bit field.

8.5.175 TG_TOGGLE_POINT12_1

Address: 0x000 04C9
BANK3 Address: 0x49

RW	7	6	5	4	3	2	1	0
	TP24_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP24_PIXEL_1	TP24 toggle point. Defines the pixel-counter value for TP24. If PO7 is configured for direct control and second pulse is enabled, this field configures the rising edge of the second pulse; TP24 is not supported in this case. Bits[15:8] of a 16-bit field.

8.5.176 TG_TOGGLE_POINT12_2

Address: 0x000 04CA
BANK3 Address: 0x4A

RW	7	6	5	4	3	2	1	0
	TP25_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP25_PIXEL_0	TP25 toggle point. Defines the pixel-counter value for TP25. If PO7 is configured for direct control and second pulse is enabled, this field configures the falling edge of the second pulse; TP25 is not supported in this case. Bits[7:0] of a 16-bit field.

8.5.177 TG_TOGGLE_POINT12_3

Address: 0x000 04CB
BANK3 Address: 0x4B

RW	7	6	5	4	3	2	1	0
	TP25_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP25_PIXEL_1	TP25 toggle point. Defines the pixel-counter value for TP25. If PO7 is configured for direct control and second pulse is enabled, this field configures the falling edge of the second pulse; TP25 is not supported in this case. Bits[15:8] of a 16-bit field.

8.5.178 TG_TOGGLE_POINT13_0

Address: 0x000 04CC
BANK3 Address: 0x4C

RW	7	6	5	4	3	2	1	0
	TP26_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP26_PIXEL_0	TP26 toggle point. Defines the pixel-counter value for TP26. If PO8 is configured for direct control and second pulse is enabled, this field configures the rising edge of the second pulse; TP26 is not supported in this case. Bits[7:0] of a 16-bit field.

8.5.179 TG_TOGGLE_POINT13_1

Address: 0x000 04CD
BANK3 Address: 0x4D

RW	7	6	5	4	3	2	1	0
	TP26_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP26_PIXEL_1	TP26 toggle point. Defines the pixel-counter value for TP26. If PO8 is configured for direct control and second pulse is enabled, this field configures the rising edge of the second pulse; TP26 is not supported in this case. Bits[15:8] of a 16-bit field.

8.5.180 TG_TOGGLE_POINT13_2

Address: 0x000 04CE
BANK3 Address: 0x4E

RW	7	6	5	4	3	2	1	0
	TP27_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP27_PIXEL_0	TP27 toggle point. Defines the pixel-counter value for TP27. If PO8 is configured for direct control and second pulse is enabled, this field configures the falling edge of the second pulse; TP27 is not supported in this case. Bits[7:0] of a 16-bit field.

8.5.181 TG_TOGGLE_POINT13_3

Address: 0x000 04CF
BANK3 Address: 0x4F

RW	7	6	5	4	3	2	1	0
	TP27_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP27_PIXEL_1	TP27 toggle point. Defines the pixel-counter value for TP27. If PO8 is configured for direct control and second pulse is enabled, this field configures the falling edge of the second pulse; TP27 is not supported in this case. Bits[15:8] of a 16-bit field.

8.5.182 TG_TOGGLE_POINT14_0

Address: 0x000 04D0
BANK3 Address: 0x50

RW	7	6	5	4	3	2	1	0
	TP28_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP28_PIXEL_0	TP28 toggle point. Defines the pixel-counter value for TP28. If PO9 is configured for direct control and second pulse is enabled, this field configures the rising edge of the second pulse; TP28 is not supported in this case. Bits[7:0] of a 16-bit field.

8.5.183 TG_TOGGLE_POINT14_1

Address: 0x000 04D1
BANK3 Address: 0x51

RW	7	6	5	4	3	2	1	0
	TP28_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP28_PIXEL_1	TP28 toggle point. Defines the pixel-counter value for TP28. If PO9 is configured for direct control and second pulse is enabled, this field configures the rising edge of the second pulse; TP28 is not supported in this case. Bits[15:8] of a 16-bit field.

8.5.184 TG_TOGGLE_POINT14_2

Address: 0x000 04D2
BANK3 Address: 0x52

RW	7	6	5	4	3	2	1	0
	TP29_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP29_PIXEL_0	TP29 toggle point. Defines the pixel-counter value for TP29. If PO9 is configured for direct control and second pulse is enabled, this field configures the falling edge of the second pulse; TP29 is not supported in this case. Bits[7:0] of a 16-bit field.

8.5.185 TG_TOGGLE_POINT14_3

Address: 0x000 04D3
BANK3 Address: 0x53

RW	7	6	5	4	3	2	1	0
	TP29_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP29_PIXEL_1	TP29 toggle point. Defines the pixel-counter value for TP29. If PO9 is configured for direct control and second pulse is enabled, this field configures the falling edge of the second pulse; TP29 is not supported in this case. Bits[15:8] of a 16-bit field.

8.5.186 TG_TOGGLE_POINT15_0

Address: 0x000 04D4
BANK3 Address: 0x54

RW	7	6	5	4	3	2	1	0
	TP30_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP30_PIXEL_0	TP30 toggle point. Defines the pixel-counter value for TP30. If PO10 is configured for direct control and second pulse is enabled, this field configures the rising edge of the second pulse; TP30 is not supported in this case. Bits[7:0] of a 16-bit field.

8.5.187 TG_TOGGLE_POINT15_1

Address: 0x000 04D5
BANK3 Address: 0x55

RW	7	6	5	4	3	2	1	0
	TP30_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP30_PIXEL_1	TP30 toggle point. Defines the pixel-counter value for TP30. If PO10 is configured for direct control and second pulse is enabled, this field configures the rising edge of the second pulse; TP30 is not supported in this case. Bits[15:8] of a 16-bit field.

8.5.188 TG_TOGGLE_POINT15_2

Address: 0x000 04D6
BANK3 Address: 0x56

RW	7	6	5	4	3	2	1	0
	TP31_PIXEL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP31_PIXEL_0	TP31 toggle point. Defines the pixel-counter value for TP31. If PO10 is configured for direct control and second pulse is enabled, this field configures the falling edge of the second pulse; TP31 is not supported in this case. Bits[7:0] of a 16-bit field.

8.5.189 TG_TOGGLE_POINT15_3

Address: 0x000 04D7
BANK3 Address: 0x57

RW	7	6	5	4	3	2	1	0
	TP31_PIXEL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	TP31_PIXEL_1	TP31 toggle point. Defines the pixel-counter value for TP31. If PO10 is configured for direct control and second pulse is enabled, this field configures the falling edge of the second pulse; TP31 is not supported in this case. Bits[15:8] of a 16-bit field.

8.5.190 TG_OUTMUX_CFG0_0

Address: 0x000 04D8
BANK3 Address: 0x58

RW	7	6	5	4	3	2	1	0
	PCK1_PO_SEL				PCK1_DLY		CLKOUT1_POL	CLKOUT1_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PCK1_PO_SEL	CLKOUT1 pulse signal selection from PO0 to PO10 0x0 = (Default) Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved
3:2	PCK1_DLY	Toggle Pulse Delay for CLKOUT1 00 = (Default) No delay 01 = 1 ns 10 = 2 ns 11 = 3 ns
1	CLKOUT1_POL	Clock Inversion Control for CLKOUT1 0 = (Default) Disabled 1 = Enabled
0	CLKOUT1_EN	Clock Output Enable for CLKOUT1 0 = (Default) Disabled 1 = Enabled

8.5.191 TG_OUTMUX_CFG0_1

Address: 0x000 04D9
BANK3 Address: 0x59

RW	7	6	5	4	3	2	1	0
	PCK2_PO_SEL				PCK2_DLY		CLKOUT2_POL	CLKOUT2_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PCK2_PO_SEL	CLKOUT2 pulse signal selection from PO0 to PO10 0x0 = (Default) Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved
3:2	PCK2_DLY	Toggle Pulse Delay for CLKOUT2 00 = (Default) No delay 01 = 1 ns 10 = 2 ns 11 = 3 ns
1	CLKOUT2_POL	Clock Inversion Control for CLKOUT2 0 = (Default) Disabled 1 = Enabled
0	CLKOUT2_EN	Clock Output Enable for CLKOUT2 0 = (Default) Disabled 1 = Enabled

8.5.192 TG_OUTMUX_CFG0_2

Address: 0x000 04DA
BANK3 Address: 0x5A

RW	7	6	5	4	3	2	1	0
	PCK3_PO_SEL				PCK3_DLY		CLKOUT3_POL	CLKOUT3_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PCK3_PO_SEL	CLKOUT3 pulse signal selection from PO0 to PO10 0x0 = (Default) Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved
3:2	PCK3_DLY	Toggle Pulse Delay for CLKOUT3 00 = (Default) No delay 01 = 1 ns 10 = 2 ns 11 = 3 ns
1	CLKOUT3_POL	Clock Inversion Control for CLKOUT3 0 = (Default) Disabled 1 = Enabled
0	CLKOUT3_EN	Clock Output Enable for CLKOUT3 0 = (Default) Disabled 1 = Enabled

8.5.193 TG_OUTMUX_CFG0_3

Address: 0x000 04DB
BANK3 Address: 0x5B

RW	7	6	5	4	3	2	1	0
	PCK4_PO_SEL				PCK4_DLY		CLKOUT4_POL	CLKOUT4_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PCK4_PO_SEL	CLKOUT4 pulse signal selection from PO0 to PO10 0x0 = (Default) Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved
3:2	PCK4_DLY	Toggle Pulse Delay for CLKOUT4 00 = (Default) No delay 01 = 1 ns 10 = 2 ns 11 = 3 ns
1	CLKOUT4_POL	Clock Inversion Control for CLKOUT4 0 = (Default) Disabled 1 = Enabled
0	CLKOUT4_EN	Clock Output Enable for CLKOUT4 0 = (Default) Disabled 1 = Enabled

8.5.194 TG_OUTMUX_CFG1_0

Address: 0x000 04DC
BANK3 Address: 0x5C

RW	7	6	5	4	3	2	1	0
	PCK5_PO_SEL				PCK5_DLY		CLKOUT5_POL	CLKOUT5_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PCK5_PO_SEL	CLKOUT5 pulse signal selection from PO0 to PO10 0x0 = (Default) Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved

Bits	Name	Description
3:2	PCK5_DLY	Toggle Pulse Delay for CLKOUT5 00 = (Default) No delay 01 = 1 ns 10 = 2 ns 11 = 3 ns
1	CLKOUT5_POL	Clock Inversion Control for CLKOUT5 0 = (Default) Disabled 1 = Enabled
0	CLKOUT5_EN	Clock Output Enable for CLKOUT5 0 = (Default) Disabled 1 = Enabled

8.5.195 TG_OUTMUX_CFG1_1

Address: 0x000 04DD
BANK3 Address: 0x5D

RW	7	6	5	4	3	2	1	0
	PCK6_PO_SEL				PCK6_DLY		CLKOUT6_POL	CLKOUT6_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PCK6_PO_SEL	CLKOUT6 pulse signal selection from PO0 to PO10 0x0 = (Default) Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved
3:2	PCK6_DLY	Toggle Pulse Delay for CLKOUT6 00 = (Default) No delay 01 = 1 ns 10 = 2 ns 11 = 3 ns
1	CLKOUT6_POL	Clock Inversion Control for CLKOUT6 0 = (Default) Disabled 1 = Enabled
0	CLKOUT6_EN	Clock Output Enable for CLKOUT6 0 = (Default) Disabled 1 = Enabled

8.5.196 TG_OUTMUX_CFG1_2

Address: 0x000 04DE
BANK3 Address: 0x5E

RW	7	6	5	4	3	2	1	0
	PCK7_PO_SEL				PCK7_DLY		CLKOUT7_POL	CLKOUT7_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PCK7_PO_SEL	CLKOUT7 pulse signal selection from PO0 to PO10 0x0 = (Default) Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved
3:2	PCK7_DLY	Toggle Pulse Delay for CLKOUT7 00 = (Default) No delay 01 = 1 ns 10 = 2 ns 11 = 3 ns
1	CLKOUT7_POL	Clock Inversion Control for CLKOUT7 0 = (Default) Disabled 1 = Enabled
0	CLKOUT7_EN	Clock Output Enable for CLKOUT7 0 = (Default) Disabled 1 = Enabled

8.5.197 TG_OUTMUX_CFG1_3

Address: 0x000 04DF
BANK3 Address: 0x5F

RW	7	6	5	4	3	2	1	0
	PCK8_PO_SEL				PCK8_DLY		CLKOUT8_POL	CLKOUT8_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PCK8_PO_SEL	CLKOUT8 pulse signal selection from PO0 to PO10 0x0 = (Default) Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved
3:2	PCK8_DLY	Toggle Pulse Delay for CLKOUT8 00 = (Default) No delay 01 = 1 ns 10 = 2 ns 11 = 3 ns
1	CLKOUT8_POL	Clock Inversion Control for CLKOUT8 0 = (Default) Disabled 1 = Enabled
0	CLKOUT8_EN	Clock Output Enable for CLKOUT8 0 = (Default) Disabled 1 = Enabled

8.5.198 TG_OUTMUX_CFG2_0

Address: 0x000 04E0
BANK3 Address: 0x60

RW	7	6	5	4	3	2	1	0
	PCK9_PO_SEL				PCK9_DLY		CLKOUT9_POL	CLKOUT9_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PCK9_PO_SEL	CLKOUT9 pulse signal selection from PO0 to PO10 0x0 = (Default) Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved
3:2	PCK9_DLY	Toggle Pulse Delay for CLKOUT9 00 = (Default) No delay 01 = 1 ns 10 = 2 ns 11 = 3 ns
1	CLKOUT9_POL	Clock Inversion Control for CLKOUT9 0 = (Default) Disabled 1 = Enabled
0	CLKOUT9_EN	Clock Output Enable for CLKOUT9 0 = (Default) Disabled 1 = Enabled

8.5.199 TG_OUTMUX_CFG2_1

Address: 0x000 04E1
BANK3 Address: 0x61

RW	7	6	5	4	3	2	1	0
	PCK10_PO_SEL				PCK10_DLY		CLKOUT10_POL	CLKOUT10_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PCK10_PO_SEL	CLKOUT10 pulse signal selection from PO0 to PO10 0x0 = (Default) Pulse Output PO0 0x1 = Pulse Output PO1 0x2 = Pulse Output PO2 0x3 = Pulse Output PO3 0x4 = Pulse Output PO4 0x5 = Pulse Output PO5 0x6 = Pulse Output PO6 0x7 = Pulse Output PO7 0x8 = Pulse Output PO8 0x9 = Pulse Output PO9 0xA = Pulse Output PO10 0xB–0xF = Reserved

Bits	Name	Description
3:2	PCK10_DLY	Toggle Pulse Delay for CLKOUT10 00 = (Default) No delay 01 = 1 ns 10 = 2 ns 11 = 3 ns
1	CLKOUT10_POL	Clock Inversion Control for CLKOUT10 0 = (Default) Disabled 1 = Enabled
0	CLKOUT10_EN	Clock Output Enable for CLKOUT10 0 = (Default) Disabled 1 = Enabled

8.5.200 TG_OUTMUX_CFG2_3

Address: 0x000 04E3
BANK3 Address: 0x63

RW	7	6	5	4	3	2	1	0
	—		CLKOUT6_SRC	CLKOUT5_SRC	CLKOUT4_SRC	CLKOUT3_SRC	CLKOUT2_SRC	CLKOUT1_SRC
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	CLKOUT6_SRC	Clock/Pulse Signal Selection for CLKOUT6 0 = (Default) C_CK6 pulse from DLL1 1 = P_CK6 pulse waveform from POn
4	CLKOUT5_SRC	Clock/Pulse Signal Selection for CLKOUT5 0 = (Default) C_CK5 pulse from DLL1 1 = P_CK5 pulse waveform from POn
3	CLKOUT4_SRC	Clock/Pulse Signal Selection for CLKOUT4 0 = (Default) C_CK4 pulse from DLL1 1 = P_CK4 pulse waveform from POn
2	CLKOUT3_SRC	Clock/Pulse Signal Selection for CLKOUT3 0 = (Default) C_CK3 pulse from DLL1 1 = P_CK3 pulse waveform from POn
1	CLKOUT2_SRC	Clock/Pulse Signal Selection for CLKOUT2 0 = (Default) C_CK2 pulse from DLL1 1 = P_CK2 pulse waveform from POn
0	CLKOUT1_SRC	Clock/Pulse Signal Selection for CLKOUT1 0 = (Default) C_CK1 pulse from DLL1 1 = P_CK1 pulse waveform from POn

8.5.201 DLL_CFG1_0

Address: 0x000 04E4
BANK3 Address: 0x64

RW	7	6	5	4	3	2	1	0
	—		DLL_RSMP_RISE					
Default	0	0	1	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	DLL_RSMP_RISE	RSMP rise timing 0x00 = 0 tap 0x01 = 1 tap … 0x20 = (Default) 32 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.202 DLL_CFG1_1

Address: 0x000 04E5
BANK3 Address: 0x65

RW	7	6	5	4	3	2	1	0
	—		DLL_RSMP_FALL					
Default	0	0	1	0	0	1	1	0

Bits	Name	Description
7:6	—	Reserved
5:0	DLL_RSMP_FALL	RSMP fall timing 0x00 = 0 tap 0x01 = 1 tap … 0x26 = (Default) 38 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.203 DLL_CFG1_2

Address: 0x000 04E6
BANK3 Address: 0x66

RW	7	6	5	4	3	2	1	0
	—		DLL_VSMP_RISE					
Default	0	0	1	0	1	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	DLL_VSMP_RISE	VSMP rise timing 0x00 = 0 tap 0x01 = 1 tap … 0x28 = (Default) 40 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.204 DLL_CFG1_3

Address: 0x000 04E7
BANK3 Address: 0x67

RW	7	6	5	4	3	2	1	0
	—		DLL_VSMP_FALL					
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	DLL_VSMP_FALL	VSMP fall timing 0x00 = 0 tap 0x01 = 1 tap … 0x08 = (Default) 8 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.205 DLL_CFG2_0

Address: 0x000 04E8
BANK3 Address: 0x68

RW	7	6	5	4	3	2	1	0
	—		DLL_CK1_RISE					
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:6	—	Reserved
5:0	DLL_CK1_RISE	C_CK1 rise timing 0x00 = 0 tap 0x01 = 1 tap … 0x0A = (Default) 10 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.206 DLL_CFG2_1

Address: 0x000 04E9
BANK3 Address: 0x69

RW	7	6	5	4	3	2	1	0
	DLL_CK1_DIV	—	DLL_CK1_FALL					
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	DLL_CK1_DIV	C_CK1 divide by two 0 = (Default) no division 1 = div2
6	—	Reserved
5:0	DLL_CK1_FALL	C_CK1 fall timing 0x00 = 0 tap 0x01 = 1 tap … 0x19 = (Default) 25 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.207 DLL_CFG2_2

Address: 0x000 04EA
BANK3 Address: 0x6A

RW	7	6	5	4	3	2	1	0
	—		DLL_CK2_RISE					
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7:6	—	Reserved
5:0	DLL_CK2_RISE	C_CK2 rise timing 0x00 = 0 tap 0x01 = 1 tap … 0x19 = (Default) 25 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.208 DLL_CFG2_3

Address: 0x000 04EB
BANK3 Address: 0x6B

RW	7	6	5	4	3	2	1	0
	DLL_CK2_DIV	—	DLL_CK2_FALL					
Default	0	0	1	0	1	0	0	0

Bits	Name	Description
7	DLL_CK2_DIV	C_CK2 divide by two 0 = (Default) no division 1 = div2
6	—	Reserved
5:0	DLL_CK2_FALL	C_CK2 fall timing 0x00 = 0 tap 0x01 = 1 tap … 0x28 = (Default) 40 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.209 DLL_CFG3_0

Address: 0x000 04EC
BANK3 Address: 0x6C

RW	7	6	5	4	3	2	1	0
	—		DLL_CK3_RISE					
Default	0	0	1	0	1	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	DLL_CK3_RISE	C_CK3 rise timing 0x00 = 0 tap 0x01 = 1 tap … 0x28 = (Default) 40 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.210 DLL_CFG3_1

Address: 0x000 04ED
BANK3 Address: 0x6D

RW	7	6	5	4	3	2	1	0
	DLL_CK3_DIV	—	DLL_CK3_FALL					
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7	DLL_CK3_DIV	C_CK3 divide by two 0 = (Default) no division 1 = div2
6	—	Reserved
5:0	DLL_CK3_FALL	C_CK3 fall timing 0x00 = 0 tap 0x01 = 1 tap … 0x0A = (Default) 10 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.211 DLL_CFG3_2

Address: 0x000 04EE
BANK3 Address: 0x6E

RW	7	6	5	4	3	2	1	0
	—		DLL_CK4_RISE					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	DLL_CK4_RISE	C_CK4 rise timing 0x00 = (Default) 0 tap 0x01 = 1 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.212 DLL_CFG3_3

Address: 0x000 04EF
BANK3 Address: 0x6F

RW	7	6	5	4	3	2	1	0
	DLL_CK4_DIV	—	DLL_CK4_FALL					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	DLL_CK4_DIV	C_CK4 divide by two 0 = (Default) no division 1 = div2
6	—	Reserved
5:0	DLL_CK4_FALL	C_CK4 fall timing 0x00 = (Default) 0 tap 0x01 = 1 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.213 DLL_CFG4_0

Address: 0x000 04F0
BANK3 Address: 0x70

RW	7	6	5	4	3	2	1	0
	—		DLL_CK5_RISE					
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:6	—	Reserved
5:0	DLL_CK5_RISE	C_CK5 rise timing 0x00 = 0 tap 0x01 = 1 tap … 0x0A = (Default) 10 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.214 DLL_CFG4_1

Address: 0x000 04F1
BANK3 Address: 0x71

RW	7	6	5	4	3	2	1	0
	DLL_CK5_DIV	—	DLL_CK5_FALL					
Default	0	0	1	0	1	0	0	0

Bits	Name	Description
7	DLL_CK5_DIV	C_CK5 divide by two 0 = (Default) no division 1 = div2
6	—	Reserved
5:0	DLL_CK5_FALL	C_CK5 fall timing 0x00 = 0 tap 0x01 = 1 tap … 0x28 = (Default) 40 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.215 DLL_CFG4_2

Address: 0x000 04F2
BANK3 Address: 0x72

RW	7	6	5	4	3	2	1	0
	—		DLL_CK6_RISE					
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:6	—	Reserved
5:0	DLL_CK6_RISE	C_CK6 rise timing 0x00 = 0 tap 0x01 = 1 tap … 0x0A = (Default) 10 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.216 DLL_CFG4_3

Address: 0x000 04F3
BANK3 Address: 0x73

RW	7	6	5	4	3	2	1	0
	DLL_CK6_DIV	—	DLL_CK6_FALL					
Default	0	0	1	0	1	0	0	0

Bits	Name	Description
7	DLL_CK6_DIV	C_CK6 divide by two 0 = (Default) no division 1 = div2
6	—	Reserved
5:0	DLL_CK6_FALL	C_CK6 fall timing 0x00 = 0 tap 0x01 = 1 tap … 0x28 = (Default) 40 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.217 DLL_CFG5_0

Address: 0x000 04F4
BANK3 Address: 0x74

RW	7	6	5	4	3	2	1	0
	—		DLL_TGCKO_RISE					
Default	0	0	1	1	0	1	1	1

Bits	Name	Description
7:6	—	Reserved
5:0	DLL_TGCKO_RISE	TGCKO rise timing. Configures the rise/fall edge timing of the POn pulse outputs. 0x00 = 0 tap 0x01 = 1 tap … 0x37 = (Default) 55 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.5.218 DLL_CFG5_1

Address: 0x000 04F5
BANK3 Address: 0x75

RW	7	6	5	4	3	2	1	0
	—		DLL_AFECK_DUR					
Default	0	0	0	1	0	1	1	0

Bits	Name	Description
7:6	—	Reserved
5:0	DLL_AFECK_DUR	AFECK pulse duration 0x00 = 0 tap 0x01 = 1 tap … 0x16 = (Default) 22 tap … 0x3B = 59 tap 0x3C–0x3F = Reserved

8.6 OP_FORMAT—Output Formatter

8.6.1 OP_FORMAT_CFG0_0

Address: 0x000 0500
BANK0 Address: 0x4C

RW	7	6	5	4	3	2	1	0
	FORMAT_LOAD	FORMAT_SEL						
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7	FORMAT_LOAD	Output format load. If this bit is set, the FORMAT_SEL output format is loaded. This bit is cleared automatically when the selected format has been loaded. 0 = (Default) No action 1 = Load format
6:0	FORMAT_SEL	Output format selection. Set to the corresponding format ID value to select the data-output format.

8.6.2 OP_FORMAT_CFG0_1

Address: 0x000 0501
BANK0 Address: 0x4D

RW	7	6	5	4	3	2	1	0
	—				LVDS_POL	LVDS_REVERSE	CMOS_EXT_POL	LVDS_BIT_ORDER
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:4	—	Reserved
3	LVDS_POL	LVDS output polarity. If this bit is set, the LVDS data output is inverted. 0 = (Default) Normal 1 = Inverted
2	LVDS_REVERSE	LVDS format reverse. If this bit is set, each LVDS data block is time-reversed. 0 = (Default) Normal 1 = Reverse
1	CMOS_EXT_POL	CMOS (External) phase control. Selects which MCLK edge the output format is synchronized to. 0 = (Default) Rising edge 1 = Falling edge
0	LVDS_BIT_ORDER	LVDS bit order. If this bit is 0, the bit order (MSB/LSB) is swapped. 0 = Swapped 1 = (Default) Normal

8.6.3 OP_FORMAT_CFG0_2

Address: 0x000 0502
BANK0 Address: 0x4E

RW	7	6	5	4	3	2	1	0
	—						TDM_GAP	TDM_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1	TDM_GAP	TDM gap. If this bit is set in TDM Mode, a gap of one MCLK cycle is inserted after each data-output phase. 0 = (Default) Disabled 1 = Enabled
0	TDM_EN	TDM Mode enable. Allows two devices to output data on a single data bus. 0 = (Default) Disabled 1 = Enabled

8.6.4 OP_FORMAT_CFG0_3

Address: 0x000 0503
BANK0 Address: 0x4F

RW	7	6	5	4	3	2	1	0
	—			TDM_OFFSET				
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4:0	TDM_OFFSET	TDM output timing control. This field is used to offset the data-output timing in TDM Mode. 0x00 = (Default) 0 bit 0x01 = 1 bit … 0x1F = 31 bit

8.6.5 OP_FORMAT_CFG1_0

Address: 0x000 0504
BANK0 Address: 0x50

RW	7	6	5	4	3	2	1	0
	FLAG_S1_FN				FLAG_S0_FN			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	FLAG_S1_FN	Status Flag S1 function select 0x0 = (Default) Logic 0 0x1 = Sequence State[0] 0x2 = Sequence State[1] 0x3 = FLAG_PIX1 0x4 = FLAG_PIX2 0x5 = FLAG_DEN1 0x6 = FLAG_DEN2 0x7 = Channel ID[0] 0x8 = Channel ID[1] 0x9 = Channel ID[2] 0xA–0xE = Reserved 0xF = Logic 1
3:0	FLAG_S0_FN	Status Flag S0 function select 0x0 = (Default) Logic 0 0x1 = Sequence State[0] 0x2 = Sequence State[1] 0x3 = FLAG_PIX1 0x4 = FLAG_PIX2 0x5 = FLAG_DEN1 0x6 = FLAG_DEN2 0x7 = Channel ID[0] 0x8 = Channel ID[1] 0x9 = Channel ID[2] 0xA–0xE = Reserved 0xF = Logic 1

8.6.6 OP_FORMAT_CFG1_1

Address: 0x000 0505
BANK0 Address: 0x51

RW	7	6	5	4	3	2	1	0
	FLAG_S3_FN				FLAG_S2_FN			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	FLAG_S3_FN	Status Flag S3 function select 0x0 = (Default) Logic 0 0x1 = Sequence State[0] 0x2 = Sequence State[1] 0x3 = FLAG_PIX1 0x4 = FLAG_PIX2 0x5 = FLAG_DEN1 0x6 = FLAG_DEN2 0x7 = Channel ID[0] 0x8 = Channel ID[1] 0x9 = Channel ID[2] 0xA–0xE = Reserved 0xF = Logic 1
3:0	FLAG_S2_FN	Status Flag S2 function select 0x0 = (Default) Logic 0 0x1 = Sequence State[0] 0x2 = Sequence State[1] 0x3 = FLAG_PIX1 0x4 = FLAG_PIX2 0x5 = FLAG_DEN1 0x6 = FLAG_DEN2 0x7 = Channel ID[0] 0x8 = Channel ID[1] 0x9 = Channel ID[2] 0xA–0xE = Reserved 0xF = Logic 1

8.6.7 OP_FORMAT_CFG1_2

Address: 0x000 0506
BANK0 Address: 0x52

RW	7	6	5	4	3	2	1	0
	—				FLAG_S4_FN			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	FLAG_S4_FN	Status Flag S4 function select 0x0 = (Default) Logic 0 0x1 = Sequence State[0] 0x2 = Sequence State[1] 0x3 = FLAG_PIX1 0x4 = FLAG_PIX2 0x5 = FLAG_DEN1 0x6 = FLAG_DEN2 0x7 = Channel ID[0] 0x8 = Channel ID[1] 0x9 = Channel ID[2] 0xA–0xE = Reserved 0xF = Logic 1

8.7 PAD_INTF—Pad Interface I/O Control

8.7.1 CLKOUT_SEL_1_0

Address: 0x000 0600
BANK0 Address: 0x54

RW	7	6	5	4	3	2	1	0
	CLKOUT4_FN	CLKOUT3_FN			CLKOUT2_FN		CLKOUT1_FN	
Default	0	0	0	1	0	1	0	1

Bits	Name	Description
7	CLKOUT4_FN	CLKOUT4 pin function select 0 = (Default) General purpose input/output (GPIO4) 1 = CLKOUT4 output
6:4	CLKOUT3_FN	CLKOUT3 pin function select 000 = Blue LED control input 001 = (Default) RSMP input for reset sampling in External Mode 010 = General purpose input/output (GPIO3) 011 = CLKOUT3 output 100 = Monitor/test output 101–111 = Reserved

Bits	Name	Description
3:2	CLKOUT2_FN	CLKOUT2 pin function select 00 = Green LED control input 01 = (Default) External LED Start input for use in synchronising internal LED enables 10 = General purpose input/output (GPIO2) 11 = CLKOUT2 output
1:0	CLKOUT1_FN	CLKOUT1 pin function select 00 = Red LED control input 01 = (Default) External TGSYNC input for use in generating timing signals in External Mode 10 = General purpose input/output (GPIO1) 11 = CLKOUT1 output

8.7.2 CLKOUT_SEL_1_1

Address: 0x000 0601
BANK0 Address: 0x55

RW	7	6	5	4	3	2	1	0
	—		CLKOUT10_FN	CLKOUT9_FN	CLKOUT8_FN	CLKOUT7_FN	CLKOUT6_FN	CLKOUT5_FN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	CLKOUT10_FN	CLKOUT10 pin function select 0 = (Default) General purpose input/output (GPIO10) 1 = CLKOUT10 output o/p
4	CLKOUT9_FN	CLKOUT9 pin function select 0 = (Default) General purpose input/output (GPIO9) 1 = CLKOUT9 output
3	CLKOUT8_FN	CLKOUT8 pin function select 0 = (Default) General purpose input/output (GPIO8) 1 = CLKOUT8 output
2	CLKOUT7_FN	CLKOUT7 pin function select 0 = (Default) General purpose input/output (GPIO7) 1 = CLKOUT7 output
1	CLKOUT6_FN	CLKOUT6 pin function select 0 = (Default) General purpose input (GPI6) 1 = CLKOUT6 output
0	CLKOUT5_FN	CLKOUT5 pin function select 0 = (Default) General purpose input (GPI5) 1 = CLKOUT5 output

8.7.3 CLKOUT_SEL_1_2

Address: 0x000 0602
BANK0 Address: 0x56

RW	7	6	5	4	3	2	1	0
	—			MON_SEL			TGSYNC1_VSMP_FN	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4:2	MON_SEL	MON pin function select 000 = (Default) VSMP output 001 = RSMP output 010 = AFECK output 011 = Data clock output 100 = PLL clock output 101–111 = Reserved
1:0	TGSYNC1_VSMP_FN	TGSYNC1/VMSMP_EXT pin function select 00 = (Default) VSMP input for video sampling in External Mode 01 = TGSYNC1 input 10 = Reserved 11 = TGSYNC output

8.7.4 CLKOUT_SEL_1_3

Address: 0x000 0603
BANK0 Address: 0x57

RW	7	6	5	4	3	2	1	0
	—				TDM_DOUT_DLY_SEL		TDM_DOUT_DLY_EN	MCLK_EXT_LVDS
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7:4	—	Reserved
3:2	TDM_DOUT_DLY_SEL	Selects output delay in TDM Mode. Only valid if TDM_DOUT_DLY_EN=1. 00 = 0.5 nsec 01 = (Default) 1.0 nsec 10 = 1.5 nsec 11 = 2.0 nsec
1	TDM_DOUT_DLY_EN	Enables output delay in TDM Mode. The delay is configured using TDM_DOUT_DLY_SEL. 0 = (Default) Disabled 1 = Enabled
0	MCLK_EXT_LVDS	MCLK input selection. In CMOS Mode, general-purpose input GP12 is supported on the MCLK_EXT_N pin. 0 = (Default) CMOS (MCLK_EXT) 1 = LVDS (MCLK_EXT_P/N)

8.7.5 GPI_VAL_0

Address: 0x000 060C
BANK6 Address: 0x0C

RO	7	6	5	4	3	2	1	0
	GP7_IN_STS	GP6_IN_STS	GP5_IN_STS	GP4_IN_STS	GP3_IN_STS	GP2_IN_STS	GP1_IN_STS	GP12_IN_STS
Default	X	X	X	X	X	X	X	X

Bits	Name	Description
7	GP7_IN_STS	GP7 input status 0 = Low 1 = High
6	GP6_IN_STS	GP6 input status 0 = Low 1 = High
5	GP5_IN_STS	GP5 input status 0 = Low 1 = High
4	GP4_IN_STS	GP4 input status 0 = Low 1 = High
3	GP3_IN_STS	GP3 input status 0 = Low 1 = High
2	GP2_IN_STS	GP2 input status 0 = Low 1 = High
1	GP1_IN_STS	GP1 input status 0 = Low 1 = High
0	GP12_IN_STS	GP12 input status 0 = Low 1 = High

8.7.6 GPI_VAL_1

Address: 0x000 060D
BANK6 Address: 0x0D

RO	7	6	5	4	3	2	1	0
	—					GP10_IN_STS	GP9_IN_STS	GP8_IN_STS
Default	0	0	0	0	X	X	X	X

Bits	Name	Description
7:3	—	Reserved
2	GP10_IN_STS	GP10 input status 0 = Low 1 = High
1	GP9_IN_STS	GP9 input status 0 = Low 1 = High
0	GP8_IN_STS	GP8 input status 0 = Low 1 = High

8.7.7 GPI_VAL_2

Address: 0x000 060E
BANK6 Address: 0x0E

RW	7	6	5	4	3	2	1	0
	GP10_DIR	GP9_DIR	GP8_DIR	GP7_DIR	GP4_DIR	GP3_DIR	GP2_DIR	GP1_DIR
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	GP10_DIR	GPIO10 pin direction 0 = (Default) Input 1 = Output
6	GP9_DIR	GPIO9 pin direction 0 = (Default) Input 1 = Output
5	GP8_DIR	GPIO8 pin direction 0 = (Default) Input 1 = Output
4	GP7_DIR	GPIO7 pin direction 0 = (Default) Input 1 = Output
3	GP4_DIR	GPIO4 pin direction 0 = (Default) Input 1 = Output
2	GP3_DIR	GPIO3 pin direction 0 = (Default) Input 1 = Output
1	GP2_DIR	GPIO2 pin direction 0 = (Default) Input 1 = Output
0	GP1_DIR	GPIO1 pin direction 0 = (Default) Input 1 = Output

8.7.8 GPI_VAL_3

Address: 0x000 060F
BANK6 Address: 0x0F

RW	7	6	5	4	3	2	1	0
	GP10_OUT_LVL	GP9_OUT_LVL	GP8_OUT_LVL	GP7_OUT_LVL	GP4_OUT_LVL	GP3_OUT_LVL	GP2_OUT_LVL	GP1_OUT_LVL
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	GP10_OUT_LVL	GP10 output level 0 = (Default) Low 1 = High
6	GP9_OUT_LVL	GP9 output level 0 = (Default) Low 1 = High
5	GP8_OUT_LVL	GP8 output level 0 = (Default) Low 1 = High
4	GP7_OUT_LVL	GP7 output level 0 = (Default) Low 1 = High
3	GP4_OUT_LVL	GP4 output level 0 = (Default) Low 1 = High
2	GP3_OUT_LVL	GP3 output level 0 = (Default) Low 1 = High
1	GP2_OUT_LVL	GP2 output level 0 = (Default) Low 1 = High
0	GP1_OUT_LVL	GP1 output level 0 = (Default) Low 1 = High

8.7.9 LVDS_CFG

Address: 0x000 0610
BANK6 Address: 0x10

RW	7	6	5	4	3	2	1	0
	—						LVDS_VREF_SEL	
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:2	—	Reserved
1:0	LVDS_VREF_SEL	LVDS pad voltage selection 00 = From internal resistor divider on VDD-0.9 V 01 = (Default) From internal resistor divider on VDD-1.2 V 10 = Not supported 11 = From external reference voltage on VREF VDD-1.2 V or 0.9 V

8.7.10 CMOS_CFG_0

Address: 0x000 0618
BANK6 Address: 0x18

RW	7	6	5	4	3	2	1	0
	—	SPI_SDO_I2C_SCL_DRV_STR			SPI_SDO_I2C_SCL_PULL		SPI_MISO_I2C_SCL_HIZ_EN	SPI_MISO_I2C_SCL_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	SPI_SDO_I2C_SCL_DRV_STR	SPI_SDO/I2C_SCL output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved

Bits	Name	Description
3:2	SPI_SDO_I2C_SCL_PULL	SPI_SDO/I2C_SCL pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	SPI_MISO_I2C_SCL_HIZ_EN	SPI_SDO/I2C_SCL High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	SPI_MISO_I2C_SCL_IE	SPI_SDO/I2C_SCL input enable 0 = Disabled 1 = (Default) Enabled

8.7.11 CMOS_CFG_1

Address: 0x000 0619
BANK6 Address: 0x19

RW	7	6	5	4	3	2	1	0
	—	SPI_MOSI_I2C_SDA_DRV_STR			SPI_MOSI_I2C_SDA_PULL		SPI_MOSI_I2C_SDA_HIZ_EN	SPI_MOSI_I2C_SDA_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	SPI_MOSI_I2C_SDA_DRV_STR	SPI_SDI_I2C_SDA output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	SPI_MOSI_I2C_SDA_PULL	SPI_SDI_I2C_SDA pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	SPI_MOSI_I2C_SDA_HIZ_EN	SPI_SDI_I2C_SDA High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	SPI_MOSI_I2C_SDA_IE	SPI_SDI_I2C_SDA input enable 0 = Disabled 1 = (Default) Enabled

8.7.12 CMOS_CFG_2

Address: 0x000 061A
BANK6 Address: 0x1A

RW	7	6	5	4	3	2	1	0
	—				SPI_SCK_PULL		—	SPI_SCK_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7:4	—	Reserved
3:2	SPI_SCK_PULL	SPI_SCK pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	—	Reserved
0	SPI_SCK_IE	SPI_SCK input enable 0 = Disabled 1 = (Default) Enabled

8.7.13 CMOS_CFG_3

Address: 0x000 061B
BANK6 Address: 0x1B

RW	7	6	5	4	3	2	1	0
	—				SPI_CS_PULL		—	SPI_CS_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7:4	—	Reserved
3:2	SPI_CS_PULL	SPI_CS pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	—	Reserved
0	SPI_CS_IE	SPI_CS input enable 0 = Disabled 1 = (Default) Enabled

8.7.14 MCLK_CFG_0

Address: 0x000 061C
BANK6 Address: 0x1C

RW	7	6	5	4	3	2	1	0
	—	MCLK_LVDS_RT_EN	—					
Default	0	0	1	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6	MCLK_LVDS_RT_EN	MCLK LVDS resistor termination 0 = (Default) Disabled 1 = Enabled
5:0	—	Reserved

8.7.15 MCLK_CFG_1

Address: 0x000 061D
BANK6 Address: 0x1D

RW	7	6	5	4	3	2	1	0
	—				MCLK_EXT_MCLK_EXT_P_PULL		MCLK_EXT_MCLK_EXT_P_HIZ_EN	MCLK_EXT_MCLK_EXT_P_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7:4	—	Reserved
3:2	MCLK_EXT_MCLK_EXT_P_PULL	MCLK_P pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	MCLK_EXT_MCLK_EXT_P_HIZ_EN	MCLK_P High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	MCLK_EXT_MCLK_EXT_P_IE	MCLK_P input enable 0 = Disabled 1 = (Default) Enabled

8.7.16 MCLK_CFG_2

Address: 0x000 061E
BANK6 Address: 0x1E

RW	7	6	5	4	3	2	1	0
	—				MCLK_EXT_N_GPI12_PULL		MCLK_EXT_N_GPI12_HIZ_EN	MCLK_EXT_N_GPI12_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7:4	—	Reserved
3:2	MCLK_EXT_N_GPI12_PULL	MCLK_N/GPI12 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper

Bits	Name	Description
1	MCLK_EXT_N_GPI12_HIZ_EN	MCLK_N/GPI12 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	MCLK_EXT_N_GPI12_IE	MCLK_N/GPI12 input enable 0 = Disabled 1 = (Default) Enabled

8.7.17 CLKOUT1_4_CFG_0

Address: 0x000 0620
BANK6 Address: 0x20

RW	7	6	5	4	3	2	1	0
	—	CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_DRV_STR			CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_PULL		CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_HIZ_EN	CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_DRV_STR	CLKOUT1/LEDR_EN/TGSYNC2/GPIO1 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_PULL	CLKOUT1/LEDR_EN/TGSYNC2/GPIO1 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_HIZ_EN	CLKOUT1/LEDR_EN/TGSYNC2/GPIO1 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	CLKOUT1_LEDR_EN_TGSYNC2_GPIO1_IE	CLKOUT1/LEDR_EN/TGSYNC2/GPIO1 input enable 0 = Disabled 1 = (Default) Enabled

8.7.18 CLKOUT1_4_CFG_1

Address: 0x000 0621
BANK6 Address: 0x21

RW	7	6	5	4	3	2	1	0
	—	CLKOUT2_LEDG_EN_LEDSTART_GPIO2_DRV_STR			CLKOUT2_LEDG_EN_LEDSTART_GPIO2_PULL		CLKOUT2_LEDG_EN_LEDSTART_GPIO2_HIZ_EN	CLKOUT2_LEDG_EN_LEDSTART_GPIO2_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	CLKOUT2_LEDG_EN_LEDSTART_GPIO2_DRV_STR	CLKOUT2/LEDG_EN/LED_START/GPIO2 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	CLKOUT2_LEDG_EN_LEDSTART_GPIO2_PULL	CLKOUT2/LEDG_EN/LED_START/GPIO2 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	CLKOUT2_LEDG_EN_LEDSTART_GPIO2_HIZ_EN	CLKOUT2/LEDG_EN/LED_START/GPIO2 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	CLKOUT2_LEDG_EN_LEDSTART_GPIO2_IE	CLKOUT2/LEDG_EN/LED_START/GPIO2 input enable 0 = Disabled 1 = (Default) Enabled

8.7.19 CLKOUT1_4_CFG_2

Address: 0x000 0622
BANK6 Address: 0x22

RW	7	6	5	4	3	2	1	0
	—	CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_DRV_STR			CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_PULL		CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_HIZ_EN	CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_DRV_STR	CLKOUT3/LEDB_EN/MON/RSMP_EXT/GPIO3 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_PULL	CLKOUT3/LEDB_EN/MON/RSMP_EXT/GPIO3 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_HIZ_EN	CLKOUT3/LEDB_EN/MON/RSMP_EXT/GPIO3 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	CLKOUT3_LEDB_EN_MON_RSMP_EXT_GPIO3_IE	CLKOUT3/LEDB_EN/MON/RSMP_EXT/GPIO3 input enable 0 = Disabled 1 = (Default) Enabled

8.7.20 CLKOUT1_4_CFG_3

Address: 0x000 0623
BANK6 Address: 0x23

RW	7	6	5	4	3	2	1	0
	—	CLKOUT4_GPIO4_DRV_STR			CLKOUT4_GPIO4_PULL		CLKOUT4_GPIO4_HIZ_EN	CLKOUT4_GPIO4_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	CLKOUT4_GPIO4_DRV_STR	CLKOUT4/GPIO4 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	CLKOUT4_GPIO4_PULL	CLKOUT4/GPIO4 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	CLKOUT4_GPIO4_HIZ_EN	CLKOUT4/GPIO4 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	CLKOUT4_GPIO4_IE	CLKOUT4/GPIO4 input enable 0 = Disabled 1 = (Default) Enabled

8.7.21 CLKOUT5_GPI5_CFG_0

Address: 0x000 0624
BANK6 Address: 0x24

RW	7	6	5	4	3	2	1	0
	—	CLKOUT5_GPI5_DRV_STR			CLKOUT5_GPI5_PULL		CLKOUT5_GPI5_HIZ_EN	CLKOUT5_GPI5_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	CLKOUT5_GPI5_DRV_STR	CLKOUT5/GPI5 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved

Bits	Name	Description
3:2	CLKOUT5_GPI5_PULL	CLKOUT5/GPI5 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	CLKOUT5_GPI5_HIZ_EN	CLKOUT5/GPI5 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	CLKOUT5_GPI5_IE	CLKOUT5/GPI5 input enable 0 = Disabled 1 = (Default) Enabled

8.7.22 CLKOUT5_GPI5_CFG_1

Address: 0x000 0625
BANK6 Address: 0x25

RW	7	6	5	4	3	2	1	0
	—	CLKOUT6_GPI6_DRV_STR			CLKOUT6_GPI6_PULL		CLKOUT6_GPI6_HIZ_EN	CLKOUT6_GPI6_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	CLKOUT6_GPI6_DRV_STR	CLKOUT6/GPI6 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	CLKOUT6_GPI6_PULL	CLKOUT6/GPI6 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	CLKOUT6_GPI6_HIZ_EN	CLKOUT6/GPI6 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	CLKOUT6_GPI6_IE	CLKOUT6/GPI6 input enable 0 = Disabled 1 = (Default) Enabled

8.7.23 CLKOUT5_GPI5_CFG_2

Address: 0x000 0626
BANK6 Address: 0x26

RW	7	6	5	4	3	2	1	0
	—	CLKOUT7_GPIO7_DRV_STR			CLKOUT7_GPIO7_PULL		CLKOUT7_GPIO7_HIZ_EN	CLKOUT7_GPIO7_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	CLKOUT7_GPIO7_DRV_STR	CLKOUT7/GPIO7 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	CLKOUT7_GPIO7_PULL	CLKOUT7/GPIO7 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	CLKOUT7_GPIO7_HIZ_EN	CLKOUT7/GPIO7 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	CLKOUT7_GPIO7_IE	CLKOUT7/GPIO7 input enable 0 = Disabled 1 = (Default) Enabled

8.7.24 CLKOUT5_GPI5_CFG_3

Address: 0x000 0627
BANK6 Address: 0x27

RW	7	6	5	4	3	2	1	0
	—	CLKOUT8_GPIO8_DRV_STR			CLKOUT8_GPIO8_PULL		CLKOUT8_GPIO8_HIZ_EN	CLKOUT8_GPIO8_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	CLKOUT8_GPIO8_DRV_STR	CLKOUT8/GPIO8 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	CLKOUT8_GPIO8_PULL	CLKOUT8/GPIO8 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	CLKOUT8_GPIO8_HIZ_EN	CLKOUT8/GPIO8 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	CLKOUT8_GPIO8_IE	CLKOUT8/GPIO8 input enable 0 = Disabled 1 = (Default) Enabled

8.7.25 CLKOUT9_GPI9_CFG_0

Address: 0x000 0628
BANK6 Address: 0x28

RW	7	6	5	4	3	2	1	0
	—	CLKOUT9_GPIO9_DRV_STR			CLKOUT9_GPIO9_PULL		CLKOUT9_GPIO9_HIZ_EN	CLKOUT9_GPIO9_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	CLKOUT9_GPIO9_DRV_STR	CLKOUT9/GPIO9 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	CLKOUT9_GPIO9_PULL	CLKOUT9/GPIO9 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	CLKOUT9_GPIO9_HIZ_EN	CLKOUT9/GPIO9 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	CLKOUT9_GPIO9_IE	CLKOUT9/GPIO9 input enable 0 = Disabled 1 = (Default) Enabled

8.7.26 CLKOUT9_GPI9_CFG_1

Address: 0x000 0629
BANK6 Address: 0x29

RW	7	6	5	4	3	2	1	0
	—	CLKOUT10_GPIO10_DRV_STR			CLKOUT10_GPIO10_PULL		CLKOUT10_GPIO10_HIZ_EN	CLKOUT10_GPIO10_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	CLKOUT10_GPIO10_DRV_STR	CLKOUT10/GPIO10 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	CLKOUT10_GPIO10_PULL	CLKOUT10/GPIO10 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper

Bits	Name	Description
1	CLKOUT10_ GPIO10_HIZ_EN	CLKOUT10/GPIO10 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	CLKOUT10_ GPIO10_IE	CLKOUT10/GPIO10 input enable 0 = Disabled 1 = (Default) Enabled

8.7.27 TGSYNC1_VSMP_EXT_CFG

Address: 0x000 062C
BANK6 Address: 0x2C

RW	7	6	5	4	3	2	1	0
	—	TGSYNC1_VSMP_EXT_DRV_STR			TGSYNC1_VSMP_EXT_PULL		TGSYNC1_VSMP_ EXT_HIZ_EN	TGSYNC1_VSMP_ EXT_IE
Default	0	0	0	1	1	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	TGSYNC1_VSMP_ EXT_DRV_STR	TGSYNC1/VSMP_EXT output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	TGSYNC1_VSMP_ EXT_PULL	TGSYNC1/VSMP_EXT pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	TGSYNC1_VSMP_ EXT_HIZ_EN	TGSYNC1/VSMP_EXT High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	TGSYNC1_VSMP_ EXT_IE	TGSYNC1/VSMP_EXT input enable 0 = Disabled 1 = (Default) Enabled

8.7.28 DOUT_CH1_CFG_0

Address: 0x000 0630
BANK6 Address: 0x30

RW	7	6	5	4	3	2	1	0
	—	DOUT1_P_DOUT1_DRV_STR			DOUT1_P_DOUT1_PULL		DOUT1_P_DOUT1_ HIZ_EN	DOUT1_P_DOUT1_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DOUT1_P_DOUT1_ DRV_STR	DOUT1_P/DOUT1 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DOUT1_P_DOUT1_ PULL	DOUT1_P/DOUT1 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DOUT1_P_DOUT1_ HIZ_EN	DOUT1_P/DOUT1 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT1_P_DOUT1_ IE	DOUT1_P/DOUT1 input enable 0 = (Default) Disabled 1 = Enabled

8.7.29 DOUT_CH1_CFG_1

Address: 0x000 0631
BANK6 Address: 0x31

RW	7	6	5	4	3	2	1	0
	—	DOUT1_N_DOUT2_DRV_STR			DOUT1_N_DOUT2_PULL		DOUT1_N_DOUT2_HIZ_EN	DOUT1_N_DOUT2_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DOUT1_N_DOUT2_DRV_STR	DOUT1_N/DOUT2 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DOUT1_N_DOUT2_PULL	DOUT1_N/DOUT2 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DOUT1_N_DOUT2_HIZ_EN	DOUT1_N/DOUT2 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT1_N_DOUT2_IE	DOUT1_N/DOUT2 input enable 0 = (Default) Disabled 1 = Enabled

8.7.30 DCLKOUT_CFG_2

Address: 0x000 0632
BANK6 Address: 0x32

RW	7	6	5	4	3	2	1	0
	—				DCLKOUT_LVDS_TXDRV		DCLKOUT_LVDS_TRIM	
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:4	—	Reserved
3:2	DCLKOUT_LVDS_TXDRV	DCLKOUT_LVDS drive current control The reference voltage is selected using LVDS_VREF_SEL. 00 = 0 mA 01 = 1.1 mA (Vref=1.2V), 0.85 mA (Vref=0.9V) 10 = (Default) 2.2 mA (Vref=1.2V), 1.7 mA (Vref=0.9V) 11 = 3.3 mA (Vref=1.2V), 2.5 mA (Vref=0.9V)
1:0	DCLKOUT_LVDS_TRIM	DCLKOUT_LVDS bias resistor trim 00–01 = Reserved 10 = (Default) 0% 11 = Reserved

8.7.31 DOUT_CH2_CFG_0

Address: 0x000 0634
BANK6 Address: 0x34

RW	7	6	5	4	3	2	1	0
	—	DOUT2_P_DOUT3_DRV_STR			DOUT2_P_DOUT3_PULL		DOUT2_P_DOUT3_HIZ_EN	DOUT2_P_DOUT3_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DOUT2_P_DOUT3_DRV_STR	DOUT2_P/DOUT3 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DOUT2_P_DOUT3_PULL	DOUT2_P/DOUT3 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper

Bits	Name	Description
1	DOUT2_P_DOUT3_ HIZ_EN	DOUT2_P/DOUT3 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT2_P_DOUT3_ IE	DOUT2_P/DOUT3 input enable 0 = (Default) Disabled 1 = Enabled

8.7.32 DOUT_CH2_CFG_1

Address: 0x000 0635
BANK6 Address: 0x35

RW	7	6	5	4	3	2	1	0
	—	DOUT2_N_DOUT4_DRV_STR			DOUT2_N_DOUT4_PULL		DOUT2_N_DOUT4_ HIZ_EN	DOUT2_N_DOUT4_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DOUT2_N_DOUT4_ DRV_STR	DOUT2_N/DOUT4 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DOUT2_N_DOUT4_ PULL	DOUT2_N/DOUT4 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DOUT2_N_DOUT4_ HIZ_EN	DOUT2_N/DOUT4 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT2_N_DOUT4_ IE	DOUT2_N/DOUT4 input enable 0 = (Default) Disabled 1 = Enabled

8.7.33 DOUT_CH1_CFG_2

Address: 0x000 0636
BANK6 Address: 0x36

RW	7	6	5	4	3	2	1	0
	—				DOUT1_LVDS_TXDRV		DOUT1_LVDS_TRIM	
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:4	—	Reserved
3:2	DOUT1_LVDS_ TXDRV	DOUT1_LVDS drive current control The reference voltage is selected using LVDS_VREF_SEL. 00 = 0 mA 01 = 1.1 mA (Vref=1.2V), 0.85 mA (Vref=0.9V) 10 = (Default) 2.2 mA (Vref=1.2V), 1.7 mA (Vref=0.9V) 11 = 3.3 mA (Vref=1.2V), 2.5 mA (Vref=0.9V)
1:0	DOUT1_LVDS_TRIM	DOUT1_LVDS bias resistor trim 00–01 = Reserved 10 = (Default) 0% 11 = Reserved

8.7.34 DOUT_CH3_CFG_0

Address: 0x000 0638
BANK6 Address: 0x38

RW	7	6	5	4	3	2	1	0
	—	DOUT3_P_DOUT5_DRV_STR			DOUT3_P_DOUT5_PULL		DOUT3_P_DOUT5_ HIZ_EN	DOUT3_P_DOUT5_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DOUT3_P_DOUT5_ DRV_STR	DOUT3_P/DOUT5 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved

Bits	Name	Description
3:2	DOUT3_P_DOUT5_PULL	DOUT3_P/DOUT5 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DOUT3_P_DOUT5_HIZ_EN	DOUT3_P/DOUT5 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT3_P_DOUT5_IE	DOUT3_P/DOUT5 input enable 0 = (Default) Disabled 1 = Enabled

8.7.35 DOUT_CH3_CFG_1

Address: 0x000 0639
BANK6 Address: 0x39

RW	7	6	5	4	3	2	1	0
	—	DOUT3_N_DOUT6_DRV_STR			DOUT3_N_DOUT6_PULL		DOUT3_N_DOUT6_HIZ_EN	DOUT3_N_DOUT6_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DOUT3_N_DOUT6_DRV_STR	DOUT3_N/DOUT6 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DOUT3_N_DOUT6_PULL	DOUT3_N/DOUT6 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DOUT3_N_DOUT6_HIZ_EN	DOUT3_N/DOUT6 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT3_N_DOUT6_IE	DOUT3_N/DOUT6 input enable 0 = (Default) Disabled 1 = Enabled

8.7.36 DOUT_CH2_CFG_2

Address: 0x000 063A
BANK6 Address: 0x3A

RW	7	6	5	4	3	2	1	0
	—				DOUT2_LVDS_TXDRV		DOUT2_LVDS_TRIM	
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:4	—	Reserved
3:2	DOUT2_LVDS_TXDRV	DOUT2_LVDS drive current control The reference voltage is selected using LVDS_VREF_SEL. 00 = 0 mA 01 = 1.1 mA (Vref=1.2V), 0.85 mA (Vref=0.9V) 10 = (Default) 2.2 mA (Vref=1.2V), 1.7 mA (Vref=0.9V) 11 = 3.3 mA (Vref=1.2V), 2.5 mA (Vref=0.9V)
1:0	DOUT2_LVDS_TRIM	DOUT2_LVDS bias resistor trim 00–01 = Reserved 10 = (Default) 0% 11 = Reserved

8.7.37 DOUT_CH4_CFG_0

Address: 0x000 063C
BANK6 Address: 0x3C

RW	7	6	5	4	3	2	1	0
	—	DOUT4_P_DOUT7_DRV_STR			DOUT4_P_DOUT7_PULL		DOUT4_P_DOUT7_HIZ_EN	DOUT4_P_DOUT7_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DOUT4_P_DOUT7_DRV_STR	DOUT4_P/DOUT7 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DOUT4_P_DOUT7_PULL	DOUT4_P/DOUT7 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DOUT4_P_DOUT7_HIZ_EN	DOUT4_P/DOUT7 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT4_P_DOUT7_IE	DOUT4_P/DOUT7 input enable 0 = (Default) Disabled 1 = Enabled

8.7.38 DOUT_CH4_CFG_1

Address: 0x000 063D
BANK6 Address: 0x3D

RW	7	6	5	4	3	2	1	0
	—	DOUT4_N_DOUT8_DRV_STR			DOUT4_N_DOUT8_PULL		DOUT4_N_DOUT8_HIZ_EN	DOUT4_N_DOUT8_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DOUT4_N_DOUT8_DRV_STR	DOUT4_N/DOUT8 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DOUT4_N_DOUT8_PULL	DOUT4_N/DOUT8 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DOUT4_N_DOUT8_HIZ_EN	DOUT4_N/DOUT8 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT4_N_DOUT8_IE	DOUT4_N/DOUT8 input enable 0 = (Default) Disabled 1 = Enabled

8.7.39 DOUT_CH3_CFG_2

Address: 0x000 063E
BANK6 Address: 0x3E

RW	7	6	5	4	3	2	1	0
	—				DOUT3_LVDS_TXDRV		DOUT3_LVDS_TRIM	
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:4	—	Reserved

Bits	Name	Description
3:2	DOUT3_LVDS_TXDRV	DOUT3_LVDS drive current control The reference voltage is selected using LVDS_VREF_SEL. 00 = 0 mA 01 = 1.1 mA (Vref=1.2V), 0.85 mA (Vref=0.9V) 10 = (Default) 2.2 mA (Vref=1.2V), 1.7 mA (Vref=0.9V) 11 = 3.3 mA (Vref=1.2V), 2.5 mA (Vref=0.9V)
1:0	DOUT3_LVDS_TRIM	DOUT3_LVDS bias resistor trim 00–01 = Reserved 10 = (Default) 0% 11 = Reserved

8.7.40 DOUT_CH5_CFG_0

Address: 0x000 0640
BANK6 Address: 0x40

RW	7	6	5	4	3	2	1	0
	—	DOUT5_P_DOUT9_DRV_STR			DOUT5_P_DOUT9_PULL		DOUT5_P_DOUT9_HIZ_EN	DOUT5_P_DOUT9_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DOUT5_P_DOUT9_DRV_STR	DOUT5_P/DOUT9 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DOUT5_P_DOUT9_PULL	DOUT5_P/DOUT9 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DOUT5_P_DOUT9_HIZ_EN	DOUT5_P/DOUT9 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT5_P_DOUT9_IE	DOUT5_P/DOUT9 input enable 0 = (Default) Disabled 1 = Enabled

8.7.41 DOUT_CH5_CFG_1

Address: 0x000 0641
BANK6 Address: 0x41

RW	7	6	5	4	3	2	1	0
	—	DOUT5_N_DOUT10_DRV_STR			DOUT5_N_DOUT10_PULL		DOUT5_N_DOUT10_HIZ_EN	DOUT5_N_DOUT10_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DOUT5_N_DOUT10_DRV_STR	DOUT5_N/DOUT10 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DOUT5_N_DOUT10_PULL	DOUT5_N/DOUT10 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DOUT5_N_DOUT10_HIZ_EN	DOUT5_N/DOUT10 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DOUT5_N_DOUT10_IE	DOUT5_N/DOUT10 input enable 0 = (Default) Disabled 1 = Enabled

8.7.42 DOUT_CH4_CFG_2

Address: 0x000 0642
BANK6 Address: 0x42

RW	7	6	5	4	3	2	1	0
	—				DOUT4_LVDS_TXDRV		DOUT4_LVDS_TRIM	
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:4	—	Reserved
3:2	DOUT4_LVDS_TXDRV	DOUT4_LVDS drive current control The reference voltage is selected using LVDS_VREF_SEL. 00 = 0 mA 01 = 1.1 mA (Vref=1.2V), 0.85 mA (Vref=0.9V) 10 = (Default) 2.2 mA (Vref=1.2V), 1.7 mA (Vref=0.9V) 11 = 3.3 mA (Vref=1.2V), 2.5 mA (Vref=0.9V)
1:0	DOUT4_LVDS_TRIM	DOUT4_LVDS bias resistor trim 00–01 = Reserved 10 = (Default) 0% 11 = Reserved

8.7.43 DCLKOUT_CFG_0

Address: 0x000 0644
BANK6 Address: 0x44

RW	7	6	5	4	3	2	1	0
	—	DCLKOUT_P_DCLKOUT1_DRV_STR			DCLKOUT_P_DCLKOUT1_PULL		DCLKOUT_P_ DCLKOUT1_HIZ_EN	DCLKOUT_P_ DCLKOUT1_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DCLKOUT_P_ DCLKOUT1_DRV_ STR	DCLKOUT_P/DCLKOUT1 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DCLKOUT_P_ DCLKOUT1_PULL	DCLKOUT_P/DCLKOUT1 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper
1	DCLKOUT_P_ DCLKOUT1_HIZ_EN	DCLKOUT_P/DCLKOUT1 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DCLKOUT_P_ DCLKOUT1_IE	DCLKOUT_P/DCLKOUT1 input enable 0 = (Default) Disabled 1 = Enabled

8.7.44 DCLKOUT_CFG_1

Address: 0x000 0645
BANK6 Address: 0x45

RW	7	6	5	4	3	2	1	0
	—	DCLKOUT_N_DCLKOUT2_DRV_STR			DCLKOUT_N_DCLKOUT2_PULL		DCLKOUT_N_ DCLKOUT2_HIZ_EN	DCLKOUT_N_ DCLKOUT2_IE
Default	0	0	0	1	1	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	DCLKOUT_N_ DCLKOUT2_DRV_ STR	DCLKOUT_N/DCLKOUT2 output drive strength 000 = 1.6 mA 001 = (Default) 3.1 mA 010 = 4.5 mA 011 = 5.8 mA 100–111 = Reserved
3:2	DCLKOUT_N_ DCLKOUT2_PULL	DCLKOUT_N/DCLKOUT2 pull resistor and bus-keeper configuration 00 = Disabled 01 = Pull-up 10 = (Default) Pull-down 11 = Bus keeper

Bits	Name	Description
1	DCLKOUT_N_ DCLKOUT2_HIZ_EN	DCLKOUT_N/DCLKOUT2 High-Z enable 0 = (Default) Normal 1 = Hi-Z
0	DCLKOUT_N_ DCLKOUT2_IE	DCLKOUT_N/DCLKOUT2 input enable 0 = (Default) Disabled 1 = Enabled

8.7.45 DOUT_CH5_CFG_2

Address: 0x000 0646
BANK6 Address: 0x46

RW	7	6	5	4	3	2	1	0
	—				DOUT5_LVDS_TXDRV		DOUT5_LVDS_TRIM	
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:4	—	Reserved
3:2	DOUT5_LVDS_ TXDRV	DOUT5_LVDS drive current control The reference voltage is selected using LVDS_VREF_SEL. 00 = 0 mA 01 = 1.1 mA (Vref=1.2V), 0.85 mA (Vref=0.9V) 10 = (Default) 2.2 mA (Vref=1.2V), 1.7 mA (Vref=0.9V) 11 = 3.3 mA (Vref=1.2V), 2.5 mA (Vref=0.9V)
1:0	DOUT5_LVDS_TRIM	DOUT5_LVDS bias resistor trim 00–01 = Reserved 10 = (Default) 0% 11 = Reserved

8.8 DAC_CTRL—DAC_CTRL

8.8.1 DAC_CTRL_OFS01_CH1_0

Address: 0x000 0704
BANK0 Address: 0x5C

RW	7	6	5	4	3	2	1	0
	CH1_SEQ0_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ0_ OFFSET_0	DAC offset for Channel 1, State 0 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.2 DAC_CTRL_OFS01_CH1_1

Address: 0x000 0705
BANK0 Address: 0x5D

RW	7	6	5	4	3	2	1	0
	—							CH1_SEQ0_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH1_SEQ0_ OFFSET_1	DAC offset for Channel 1, State 0 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.3 DAC_CTRL_OFS01_CH1_2

Address: 0x000 0706
BANK0 Address: 0x5E

RW	7	6	5	4	3	2	1	0
	CH1_SEQ1_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ1_ OFFSET_0	DAC offset for Channel 1, State 1 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.4 DAC_CTRL_OFS01_CH1_3

Address: 0x000 0707
BANK0 Address: 0x5F

RW	7	6	5	4	3	2	1	0
	—							CH1_SEQ1_OFFSET_ 1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH1_SEQ1_ OFFSET_1	DAC offset for Channel 1, State 1 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.5 DAC_CTRL_OFS23_CH1_0

Address: 0x000 0708
BANK0 Address: 0x60

RW	7	6	5	4	3	2	1	0
	CH1_SEQ2_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ2_ OFFSET_0	DAC offset for Channel 1, State 2 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.6 DAC_CTRL_OFS23_CH1_1

Address: 0x000 0709
BANK0 Address: 0x61

RW	7	6	5	4	3	2	1	0
	—							CH1_SEQ2_OFFSET_ 1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH1_SEQ2_ OFFSET_1	DAC offset for Channel 1, State 2 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.7 DAC_CTRL_OFS23_CH1_2

Address: 0x000 070A
BANK0 Address: 0x62

RW	7	6	5	4	3	2	1	0
	CH1_SEQ3_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ3_ OFFSET_0	DAC offset for Channel 1, State 3 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.8 DAC_CTRL_OFS23_CH1_3

Address: 0x000 070B
BANK0 Address: 0x63

RW	7	6	5	4	3	2	1	0
	—							CH1_SEQ3_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH1_SEQ3_ OFFSET_1	DAC offset for Channel 1, State 3 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.9 DAC_CTRL_OFS0_CH2_3_0

Address: 0x000 070C
BANK0 Address: 0x64

RW	7	6	5	4	3	2	1	0
	CH2_SEQ0_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH2_SEQ0_ OFFSET_0	DAC offset for Channel 2, State 0 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.10 DAC_CTRL_OFS0_CH2_3_1

Address: 0x000 070D
BANK0 Address: 0x65

RW	7	6	5	4	3	2	1	0
	—							CH2_SEQ0_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH2_SEQ0_ OFFSET_1	DAC offset for Channel 2, State 0 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.11 DAC_CTRL_OFS0_CH2_3_2

Address: 0x000 070E
BANK0 Address: 0x66

RW	7	6	5	4	3	2	1	0
	CH3_SEQ0_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH3_SEQ0_ OFFSET_0	DAC offset for Channel 3, State 0 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.12 DAC_CTRL_OFS0_CH2_3_3

Address: 0x000 070F
BANK0 Address: 0x67

RW	7	6	5	4	3	2	1	0
	—							CH3_SEQ0_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH3_SEQ0_ OFFSET_1	DAC offset for Channel 3, State 0 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.13 DAC_CTRL_OFS0_CH4_5_0

Address: 0x000 0710
BANK0 Address: 0x68

RW	7	6	5	4	3	2	1	0
	CH4_SEQ0_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH4_SEQ0_ OFFSET_0	DAC offset for Channel 4, State 0 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.14 DAC_CTRL_OFS0_CH4_5_1

Address: 0x000 0711
BANK0 Address: 0x69

RW	7	6	5	4	3	2	1	0
	—							CH4_SEQ0_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH4_SEQ0_ OFFSET_1	DAC offset for Channel 4, State 0 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.15 DAC_CTRL_OFS0_CH4_5_2

Address: 0x000 0712
BANK0 Address: 0x6A

RW	7	6	5	4	3	2	1	0
	CH5_SEQ0_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH5_SEQ0_OFFSET_0	DAC offset for Channel 5, State 0 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.16 DAC_CTRL_OFS0_CH4_5_3

Address: 0x000 0713
BANK0 Address: 0x6B

RW	7	6	5	4	3	2	1	0
	—							CH5_SEQ0_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH5_SEQ0_OFFSET_1	DAC offset for Channel 5, State 0 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.17 DAC_CTRL_OFS0_CH6_0

Address: 0x000 0714
BANK0 Address: 0x6C

RW	7	6	5	4	3	2	1	0
	CH6_SEQ0_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH6_SEQ0_OFFSET_0	DAC offset for Channel 6, State 0 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.18 DAC_CTRL_OFS0_CH6_1

Address: 0x000 0715
BANK0 Address: 0x6D

RW	7	6	5	4	3	2	1	0
	—							CH6_SEQ0_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH6_SEQ0_OFFSET_1	DAC offset for Channel 6, State 0 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.19 DAC_CTRL_OFS1_CH2_2

Address: 0x000 071A
BANK1 Address: 0x0E

RW	7	6	5	4	3	2	1	0
	CH2_SEQ1_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH2_SEQ1_ OFFSET_0	DAC offset for Channel 2, State 1 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.20 DAC_CTRL_OFS1_CH2_3

Address: 0x000 071B
BANK1 Address: 0x0F

RW	7	6	5	4	3	2	1	0
	—							CH2_SEQ1_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH2_SEQ1_ OFFSET_1	DAC offset for Channel 2, State 1 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.21 DAC_CTRL_OFS1_CH3_2

Address: 0x000 071E
BANK1 Address: 0x12

RW	7	6	5	4	3	2	1	0
	CH3_SEQ1_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH3_SEQ1_ OFFSET_0	DAC offset for Channel 3, State 1 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.22 DAC_CTRL_OFS1_CH3_3

Address: 0x000 071F
BANK1 Address: 0x13

RW	7	6	5	4	3	2	1	0
	—							CH3_SEQ1_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH3_SEQ1_ OFFSET_1	DAC offset for Channel 3, State 1 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.23 DAC_CTRL_OFS1_CH4_2

Address: 0x000 0722
BANK1 Address: 0x16

RW	7	6	5	4	3	2	1	0
	CH4_SEQ1_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH4_SEQ1_ OFFSET_0	DAC offset for Channel 4, State 1 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.24 DAC_CTRL_OFS1_CH4_3

Address: 0x000 0723
BANK1 Address: 0x17

RW	7	6	5	4	3	2	1	0
	—							CH4_SEQ1_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH4_SEQ1_ OFFSET_1	DAC offset for Channel 4, State 1 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.25 DAC_CTRL_OFS01_CH5_2

Address: 0x000 0726
BANK1 Address: 0x1A

RW	7	6	5	4	3	2	1	0
	CH5_SEQ1_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH5_SEQ1_ OFFSET_0	DAC offset for Channel 5, State 1 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.26 DAC_CTRL_OFS01_CH5_3

Address: 0x000 0727
BANK1 Address: 0x1B

RW	7	6	5	4	3	2	1	0
	—							CH5_SEQ1_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH5_SEQ1_ OFFSET_1	DAC offset for Channel 5, State 1 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.27 DAC_CTRL_OFS1_CH6_2

Address: 0x000 072A
BANK1 Address: 0x1E

RW	7	6	5	4	3	2	1	0
	CH6_SEQ1_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH6_SEQ1_ OFFSET_0	DAC offset for Channel 6, State 1 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.28 DAC_CTRL_OFS1_CH6_3

Address: 0x000 072B
BANK1 Address: 0x1F

RW	7	6	5	4	3	2	1	0
	—							CH6_SEQ1_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH6_SEQ1_ OFFSET_1	DAC offset for Channel 6, State 1 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.29 DAC_CTRL_OFS23_CH2_0

Address: 0x000 072C
BANK1 Address: 0x20

RW	7	6	5	4	3	2	1	0
	CH2_SEQ2_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH2_SEQ2_ OFFSET_0	DAC offset for Channel 2, State 2 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.30 DAC_CTRL_OFS23_CH2_1

Address: 0x000 072D
BANK1 Address: 0x21

RW	7	6	5	4	3	2	1	0
	—							CH2_SEQ2_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH2_SEQ2_ OFFSET_1	DAC offset for Channel 2, State 2 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.31 DAC_CTRL_OFS23_CH2_2

Address: 0x000 072E
BANK1 Address: 0x22

RW	7	6	5	4	3	2	1	0
	CH2_SEQ3_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH2_SEQ3_ OFFSET_0	DAC offset for Channel 2, State 3 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.32 DAC_CTRL_OFS23_CH2_3

Address: 0x000 072F
BANK1 Address: 0x23

RW	7	6	5	4	3	2	1	0
	—							CH2_SEQ3_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH2_SEQ3_ OFFSET_1	DAC offset for Channel 2, State 3 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.33 DAC_CTRL_OFS23_CH3_0

Address: 0x000 0730
BANK1 Address: 0x24

RW	7	6	5	4	3	2	1	0
	CH3_SEQ2_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH3_SEQ2_ OFFSET_0	DAC offset for Channel 3, State 2 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.34 DAC_CTRL_OFS23_CH3_1

Address: 0x000 0731
BANK1 Address: 0x25

RW	7	6	5	4	3	2	1	0
	—							CH3_SEQ2_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH3_SEQ2_ OFFSET_1	DAC offset for Channel 3, State 2 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.35 DAC_CTRL_OFS23_CH3_2

Address: 0x000 0732
BANK1 Address: 0x26

RW	7	6	5	4	3	2	1	0
	CH3_SEQ3_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH3_SEQ3_ OFFSET_0	DAC offset for Channel 3, State 3 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.36 DAC_CTRL_OFS23_CH3_3

Address: 0x000 0733
BANK1 Address: 0x27

RW	7	6	5	4	3	2	1	0
	—							CH3_SEQ3_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH3_SEQ3_ OFFSET_1	DAC offset for Channel 3, State 3 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.37 DAC_CTRL_OFS23_CH4_0

Address: 0x000 0734
BANK1 Address: 0x28

RW	7	6	5	4	3	2	1	0
	CH4_SEQ2_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH4_SEQ2_ OFFSET_0	DAC offset for Channel 4, State 2 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.38 DAC_CTRL_OFS23_CH4_1

Address: 0x000 0735
BANK1 Address: 0x29

RW	7	6	5	4	3	2	1	0
	—							CH4_SEQ2_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH4_SEQ2_ OFFSET_1	DAC offset for Channel 4, State 2 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.39 DAC_CTRL_OFS23_CH4_2

Address: 0x000 0736
BANK1 Address: 0x2A

RW	7	6	5	4	3	2	1	0
	CH4_SEQ3_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH4_SEQ3_ OFFSET_0	DAC offset for Channel 4, State 3 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.40 DAC_CTRL_OFS23_CH4_3

Address: 0x000 0737
BANK1 Address: 0x2B

RW	7	6	5	4	3	2	1	0
	—							CH4_SEQ3_OFFSET_ 1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH4_SEQ3_ OFFSET_1	DAC offset for Channel 4, State 3 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.41 DAC_CTRL_OFS23_CH5_0

Address: 0x000 0738
BANK1 Address: 0x2C

RW	7	6	5	4	3	2	1	0
	CH5_SEQ2_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH5_SEQ2_ OFFSET_0	DAC offset for Channel 5, State 2 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.42 DAC_CTRL_OFS23_CH5_1

Address: 0x000 0739
BANK1 Address: 0x2D

RW	7	6	5	4	3	2	1	0
	—							CH5_SEQ2_OFFSET_ 1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH5_SEQ2_ OFFSET_1	DAC offset for Channel 5, State 2 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.43 DAC_CTRL_OFS23_CH5_2

Address: 0x000 073A
BANK1 Address: 0x2E

RW	7	6	5	4	3	2	1	0
	CH5_SEQ3_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH5_SEQ3_ OFFSET_0	DAC offset for Channel 5, State 3 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.44 DAC_CTRL_OFS23_CH5_3

Address: 0x000 073B
BANK1 Address: 0x2F

RW	7	6	5	4	3	2	1	0
	—							CH5_SEQ3_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH5_SEQ3_ OFFSET_1	DAC offset for Channel 5, State 3 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.45 DAC_CTRL_OFS23_CH6_0

Address: 0x000 073C
BANK1 Address: 0x30

RW	7	6	5	4	3	2	1	0
	CH6_SEQ2_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH6_SEQ2_ OFFSET_0	DAC offset for Channel 6, State 2 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.46 DAC_CTRL_OFS23_CH6_1

Address: 0x000 073D
BANK1 Address: 0x31

RW	7	6	5	4	3	2	1	0
	—							CH6_SEQ2_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH6_SEQ2_ OFFSET_1	DAC offset for Channel 6, State 2 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.47 DAC_CTRL_OFS23_CH6_2

Address: 0x000 073E
BANK1 Address: 0x32

RW	7	6	5	4	3	2	1	0
	CH6_SEQ3_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH6_SEQ3_ OFFSET_0	DAC offset for Channel 6, State 3 This field contains bits [7:0] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.8.48 DAC_CTRL_OFS23_CH6_3

Address: 0x000 073F
BANK1 Address: 0x33

RW	7	6	5	4	3	2	1	0
	—							CH6_SEQ3_OFFSET_1
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	CH6_SEQ3_ OFFSET_1	DAC offset for Channel 6, State 3 This field contains bit [8] of the 9-bit code. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.9 PGA_CTRL—PGA_CTRL

8.9.1 PGA_CTRL_AGAIN_CH1_0

Address: 0x000 0804
BANK0 Address: 0x74

RW	7	6	5	4	3	2	1	0
	—		CH1_SEQ0_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH1_SEQ0_AGAIN	Analog gain for Channel 1, State 0 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.2 PGA_CTRL_AGAIN_CH1_1

Address: 0x000 0805
BANK0 Address: 0x75

RW	7	6	5	4	3	2	1	0
	—		CH1_SEQ1_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH1_SEQ1_AGAIN	Analog gain for Channel 1, State 1 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.3 PGA_CTRL_AGAIN_CH1_2

Address: 0x000 0806
BANK0 Address: 0x76

RW	7	6	5	4	3	2	1	0
	—		CH1_SEQ2_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH1_SEQ2_AGAIN	Analog gain for Channel 1, State 2 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.4 PGA_CTRL_AGAIN_CH1_3

Address: 0x000 0807
BANK0 Address: 0x77

RW	7	6	5	4	3	2	1	0
	—		CH1_SEQ3_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH1_SEQ3_AGAIN	Analog gain for Channel 1, State 3 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.5 PGA_CTRL_AGAIN_CH2_0

Address: 0x000 0808
BANK0 Address: 0x78

RW	7	6	5	4	3	2	1	0
	—		CH2_SEQ0_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH2_SEQ0_AGAIN	Analog gain for Channel 2, State 0 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.6 PGA_CTRL_AGAIN_CH3_0

Address: 0x000 0809
BANK0 Address: 0x79

RW	7	6	5	4	3	2	1	0
	—		CH3_SEQ0_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH3_SEQ0_AGAIN	Analog gain for Channel 3, State 0 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.7 PGA_CTRL_AGAIN_CH4_0

Address: 0x000 080A
BANK0 Address: 0x7A

RW	7	6	5	4	3	2	1	0
	—		CH4_SEQ0_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH4_SEQ0_AGAIN	Analog gain for Channel 4, State 0 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.8 PGA_CTRL_AGAIN_CH5_0

Address: 0x000 080B
BANK0 Address: 0x7B

RW	7	6	5	4	3	2	1	0
	—		CH5_SEQ0_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH5_SEQ0_AGAIN	Analog gain for Channel 5, State 0 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.9 PGA_CTRL_AGAIN_CH6_0

Address: 0x000 080C
BANK0 Address: 0x7C

RW	7	6	5	4	3	2	1	0
	—		CH6_SEQ0_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH6_SEQ0_AGAIN	Analog gain for Channel 6, State 0 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.10 PGA_CTRL_AGAIN_CH2_1

Address: 0x000 0811
BANK1 Address: 0x35

RW	7	6	5	4	3	2	1	0
	—		CH2_SEQ1_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH2_SEQ1_AGAIN	Analog gain for Channel 2, State 1 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.11 PGA_CTRL_AGAIN_CH2_2

Address: 0x000 0812
BANK1 Address: 0x36

RW	7	6	5	4	3	2	1	0
	—		CH2_SEQ2_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH2_SEQ2_AGAIN	Analog gain for Channel 2, State 2 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.12 PGA_CTRL_AGAIN_CH2_3

Address: 0x000 0813
BANK1 Address: 0x37

RW	7	6	5	4	3	2	1	0
	—		CH2_SEQ3_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH2_SEQ3_AGAIN	Analog gain for Channel 2, State 3 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.13 PGA_CTRL_AGAIN_CH3_1

Address: 0x000 0815
BANK1 Address: 0x39

RW	7	6	5	4	3	2	1	0
	—		CH3_SEQ1_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH3_SEQ1_AGAIN	Analog gain for Channel 3, State 1 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.14 PGA_CTRL_AGAIN_CH3_2

Address: 0x000 0816
BANK1 Address: 0x3A

RW	7	6	5	4	3	2	1	0
	—		CH3_SEQ2_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH3_SEQ2_AGAIN	Analog gain for Channel 3, State 2 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.15 PGA_CTRL_AGAIN_CH3_3

Address: 0x000 0817
BANK1 Address: 0x3B

RW	7	6	5	4	3	2	1	0
	—		CH3_SEQ3_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH3_SEQ3_AGAIN	Analog gain for Channel 3, State 3 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.16 PGA_CTRL_AGAIN_CH4_1

Address: 0x000 0819
BANK1 Address: 0x3D

RW	7	6	5	4	3	2	1	0
	—		CH4_SEQ1_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH4_SEQ1_AGAIN	Analog gain for Channel 4, State 1 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.17 PGA_CTRL_AGAIN_CH4_2

Address: 0x000 081A
BANK1 Address: 0x3E

RW	7	6	5	4	3	2	1	0
	—		CH4_SEQ2_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH4_SEQ2_AGAIN	Analog gain for Channel 4, State 2 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.18 PGA_CTRL_AGAIN_CH4_3

Address: 0x000 081B
BANK1 Address: 0x3F

RW	7	6	5	4	3	2	1	0
	—		CH4_SEQ3_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH4_SEQ3_AGAIN	Analog gain for Channel 4, State 3 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.19 PGA_CTRL_AGAIN_CH5_1

Address: 0x000 081D
BANK1 Address: 0x41

RW	7	6	5	4	3	2	1	0
	—		CH5_SEQ1_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH5_SEQ1_AGAIN	Analog gain for Channel 5, State 1 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.20 PGA_CTRL_AGAIN_CH5_2

Address: 0x000 081E
BANK1 Address: 0x42

RW	7	6	5	4	3	2	1	0
	—		CH5_SEQ2_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH5_SEQ2_AGAIN	Analog gain for Channel 5, State 2 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.21 PGA_CTRL_AGAIN_CH5_3

Address: 0x000 081F
BANK1 Address: 0x43

RW	7	6	5	4	3	2	1	0
	—		CH5_SEQ3_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH5_SEQ3_AGAIN	Analog gain for Channel 5, State 3 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.22 PGA_CTRL_AGAIN_CH6_1

Address: 0x000 0821
BANK1 Address: 0x45

RW	7	6	5	4	3	2	1	0
	—		CH6_SEQ1_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH6_SEQ1_AGAIN	Analog gain for Channel 6, State 1 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.23 PGA_CTRL_AGAIN_CH6_2

Address: 0x000 0822
BANK1 Address: 0x46

RW	7	6	5	4	3	2	1	0
	—		CH6_SEQ2_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH6_SEQ2_AGAIN	Analog gain for Channel 6, State 2 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.9.24 PGA_CTRL_AGAIN_CH6_3

Address: 0x000 0823
BANK1 Address: 0x47

RW	7	6	5	4	3	2	1	0
	—		CH6_SEQ3_AGAIN					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	CH6_SEQ3_AGAIN	Analog gain for Channel 6, State 3 0x00 = (Default) 1.0 V/V 0x01 = 1.125 V/V … 0x1F = 4.875 V/V 0x20 = 5.0 V/V 0x21 = 5.25 V/V … 0x33 = 9.75 V/V 0x34–0x3F = 9.75 V/V

8.10 BLC_CTRL—BLC_CTRL

8.10.1 BLC_CTRL1_0

Address: 0x000 0900
BANK1 Address: 0x48

RW	7	6	5	4	3	2	1	0
	—	BLC_FINE_EVERYLINE	BLC_FINE_ACCUM	BLC_FINE_EN	—	BLC_COARSE_CYCLES		
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6	BLC_FINE_EVERYLINE	Enables BLC fine adjust on every line 0 = (Default) Fine adjust on the first line of a frame only 1 = Fine adjust on every line
5	BLC_FINE_ACCUM	Selects whether the fine adjust result is accumulated over multiple lines 0 = (Default) Fine adjust is recalculated for each line 1 = Fine adjust is accumulated over multiple lines
4	BLC_FINE_EN	Enables the BLC fine adjustment 0 = (Default) Disabled 1 = Enabled
3	—	Reserved
2:0	BLC_COARSE_CYCLES	Selects the number of BLC course adjust iterations 000 = (Default) 0 iteration 001 = 1 iteration … 111 = 7 iteration

8.10.2 BLC_CTRL1_1

Address: 0x000 0901
BANK1 Address: 0x49

	7	6	5	4	3	2	1	0
	BLC_TRACKING				—			BLC_FRAME_START
Access	RW				—			WO
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	BLC_TRACKING	Configures DC tracking for BLC. 0000 = Worst DC tracking, best noise suppression 0001 … 1110 1111 = Best DC tracking, worst noise suppression
3:1	—	Reserved
0	BLC_FRAME_START	Setting this bit indicates the next start-of-line is the first line in a frame. This bit is automatically cleared at the end of the BLC operation on the first line. 0 = (Default) Null 1 = Frame Start

8.10.3 BLC_CTRL1_2

Address: 0x000 0902
BANK1 Address: 0x4A

RW	7	6	5	4	3	2	1	0
	BLC_LENGTH_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	BLC_LENGTH_0	Number of pixels available for BLC (coarse and/or fine adjust calibration), valid from 18..1023. This field contains bits [7:0] of the 10-bit code.

8.10.4 BLC_CTRL1_3

Address: 0x000 0903
BANK1 Address: 0x4B

RW	7	6	5	4	3	2	1	0
	—			BLC_TARGET_RANGE	—		BLC_LENGTH_1	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4	BLC_TARGET_RANGE	Select BLC target range 0 = (Default) Normal range (0-63 in 10-bit output format) 1 = Extended range (0-255 in 10-bit output format)
3:2	—	Reserved
1:0	BLC_LENGTH_1	Number of pixels available for BLC (coarse and/or fine adjust calibration), valid from 18..1023. This field contains bits [9:8] of the 10-bit code.

8.10.5 BLC_TARGET_CH1_0

Address: 0x000 0908
BANK1 Address: 0x50

RW	7	6	5	4	3	2	1	0
	CH1_SEQ0_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ0_BLC_TARGET	BLC target level for Channel 1, State 0

8.10.6 BLC_TARGET_CH1_1

Address: 0x000 0909
BANK1 Address: 0x51

RW	7	6	5	4	3	2	1	0
	CH1_SEQ1_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ1_BLC_TARGET	BLC target level for Channel 1, State 1

8.10.7 BLC_TARGET_CH1_2

Address: 0x000 090A
BANK1 Address: 0x52

RW	7	6	5	4	3	2	1	0
	CH1_SEQ2_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ2_BLC_TARGET	BLC target level for Channel 1, State 2

8.10.8 BLC_TARGET_CH1_3

Address: 0x000 090B
BANK1 Address: 0x53

RW	7	6	5	4	3	2	1	0
	CH1_SEQ3_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ3_BLC_TARGET	BLC target level for Channel 1, State 3

8.10.9 BLC_TARGET_CH2_0

Address: 0x000 090C
BANK1 Address: 0x54

RW	7	6	5	4	3	2	1	0
	CH2_SEQ0_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH2_SEQ0_BLC_TARGET	BLC target level for Channel 2, State 0

8.10.10 BLC_TARGET_CH2_1

Address: 0x000 090D
BANK1 Address: 0x55

RW	7	6	5	4	3	2	1	0
	CH2_SEQ1_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH2_SEQ1_BLC_TARGET	BLC target level for Channel 2, State 1

8.10.11 BLC_TARGET_CH2_2

Address: 0x000 090E
BANK1 Address: 0x56

RW	7	6	5	4	3	2	1	0
	CH2_SEQ2_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH2_SEQ2_BLC_TARGET	BLC target level for Channel 2, State 2

8.10.12 BLC_TARGET_CH2_3

Address: 0x000 090F
BANK1 Address: 0x57

RW	7	6	5	4	3	2	1	0
	CH2_SEQ3_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH2_SEQ3_BLC_ TARGET	BLC target level for Channel 2, State 3

8.10.13 BLC_TARGET_CH3_0

Address: 0x000 0910
BANK1 Address: 0x58

RW	7	6	5	4	3	2	1	0
	CH3_SEQ0_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH3_SEQ0_BLC_ TARGET	BLC target level for Channel 3, State 0

8.10.14 BLC_TARGET_CH3_1

Address: 0x000 0911
BANK1 Address: 0x59

RW	7	6	5	4	3	2	1	0
	CH3_SEQ1_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH3_SEQ1_BLC_ TARGET	BLC target level for Channel 3, State 1

8.10.15 BLC_TARGET_CH3_2

Address: 0x000 0912
BANK1 Address: 0x5A

RW	7	6	5	4	3	2	1	0
	CH3_SEQ2_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH3_SEQ2_BLC_ TARGET	BLC target level for Channel 3, State 2

8.10.16 BLC_TARGET_CH3_3

Address: 0x000 0913
BANK1 Address: 0x5B

RW	7	6	5	4	3	2	1	0
	CH3_SEQ3_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH3_SEQ3_BLC_ TARGET	BLC target level for Channel 3, State 3

8.10.17 BLC_TARGET_CH4_0

Address: 0x000 0914
BANK1 Address: 0x5C

RW	7	6	5	4	3	2	1	0
	CH4_SEQ0_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH4_SEQ0_BLC_ TARGET	BLC target level for Channel 4, State 0

8.10.18 BLC_TARGET_CH4_1

Address: 0x000 0915
BANK1 Address: 0x5D

RW	7	6	5	4	3	2	1	0
	CH4_SEQ1_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH4_SEQ1_BLC_ TARGET	BLC target level for Channel 4, State 1

8.10.19 BLC_TARGET_CH4_2

Address: 0x000 0916
BANK1 Address: 0x5E

RW	7	6	5	4	3	2	1	0
	CH4_SEQ2_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH4_SEQ2_BLC_ TARGET	BLC target level for Channel 4, State 2

8.10.20 BLC_TARGET_CH4_3

Address: 0x000 0917
BANK1 Address: 0x5F

RW	7	6	5	4	3	2	1	0
	CH4_SEQ3_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH4_SEQ3_BLC_ TARGET	BLC target level for Channel 4, State 3

8.10.21 BLC_TARGET_CH5_0

Address: 0x000 0918
BANK1 Address: 0x60

RW	7	6	5	4	3	2	1	0
	CH5_SEQ0_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH5_SEQ0_BLC_ TARGET	BLC target level for Channel 5, State 0

8.10.22 BLC_TARGET_CH5_1

Address: 0x000 0919
BANK1 Address: 0x61

RW	7	6	5	4	3	2	1	0
	CH5_SEQ1_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH5_SEQ1_BLC_ TARGET	BLC target level for Channel 5, State 1

8.10.23 BLC_TARGET_CH5_2

Address: 0x000 091A
BANK1 Address: 0x62

RW	7	6	5	4	3	2	1	0
	CH5_SEQ2_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH5_SEQ2_BLC_ TARGET	BLC target level for Channel 5, State 2

8.10.24 BLC_TARGET_CH5_3

Address: 0x000 091B
BANK1 Address: 0x63

RW	7	6	5	4	3	2	1	0
	CH5_SEQ3_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH5_SEQ3_BLC_ TARGET	BLC target level for Channel 5, State 3

8.10.25 BLC_TARGET_CH6_0

Address: 0x000 091C
BANK1 Address: 0x64

RW	7	6	5	4	3	2	1	0
	CH6_SEQ0_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH6_SEQ0_BLC_ TARGET	BLC target level for Channel 6, State 0

8.10.26 BLC_TARGET_CH6_1

Address: 0x000 091D
BANK1 Address: 0x65

RW	7	6	5	4	3	2	1	0
	CH6_SEQ1_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH6_SEQ1_BLC_ TARGET	BLC target level for Channel 6, State 1

8.10.27 BLC_TARGET_CH6_2

Address: 0x000 091E
BANK1 Address: 0x66

RW	7	6	5	4	3	2	1	0
	CH6_SEQ2_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH6_SEQ2_BLC_ TARGET	BLC target level for Channel 6, State 2

8.10.28 BLC_TARGET_CH6_3

Address: 0x000 091F
BANK1 Address: 0x67

RW	7	6	5	4	3	2	1	0
	CH6_SEQ3_BLC_TARGET							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH6_SEQ3_BLC_ TARGET	BLC target level for Channel 6, State 3

8.10.29 BLC_OFFSET_CH1_0

Address: 0x000 0928

RO	7	6	5	4	3	2	1	0
	CH1_BLC_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_BLC_OFFSET_0	BLC offset level for Channel 1 This field contains bits [7:0] of the 9-bit code. Not valid during the first line in the BLC frame. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.10.30 BLC_OFFSET_CH1_1

Address: 0x000 0929

RO	7	6	5	4	3	2	1	0
	—							CH1_BLC_OFFSET_1
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	CH1_BLC_OFFSET_1	BLC offset level for Channel 1 This field contains bit [8] of the 9-bit code. Not valid during the first line in the BLC frame. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.10.31 BLC_OFFSET_CH2_0

Address: 0x000 092C

RO	7	6	5	4	3	2	1	0
	CH2_BLC_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH2_BLC_OFFSET_0	BLC offset level for Channel 2 This field contains bits [7:0] of the 9-bit code. Not valid during the first line in the BLC frame. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.10.32 BLC_OFFSET_CH2_1

Address: 0x000 092D

RO	7	6	5	4	3	2	1	0
	—							CH2_BLC_OFFSET_1
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	CH2_BLC_OFFSET_1	BLC offset level for Channel 2 This field contains bit [8] of the 9-bit code. Not valid during the first line in the BLC frame. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.10.33 BLC_OFFSET_CH3_0

Address: 0x000 0930

RO	7	6	5	4	3	2	1	0
	CH3_BLC_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH3_BLC_OFFSET_0	BLC offset level for Channel 3 This field contains bits [7:0] of the 9-bit code. Not valid during the first line in the BLC frame. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.10.34 BLC_OFFSET_CH3_1

Address: 0x000 0931

RO	7	6	5	4	3	2	1	0
	—							CH3_BLC_OFFSET_1
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	CH3_BLC_OFFSET_1	BLC offset level for Channel 3 This field contains bit [8] of the 9-bit code. Not valid during the first line in the BLC frame. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.10.35 BLC_OFFSET_CH4_0

Address: 0x000 0934

RO	7	6	5	4	3	2	1	0
	CH4_BLC_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH4_BLC_OFFSET_0	BLC offset level for Channel 4 This field contains bits [7:0] of the 9-bit code. Not valid during the first line in the BLC frame. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.10.36 BLC_OFFSET_CH4_1

Address: 0x000 0935

RO	7	6	5	4	3	2	1	0
	—							CH4_BLC_OFFSET_1
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	CH4_BLC_OFFSET_1	BLC offset level for Channel 4 This field contains bit [8] of the 9-bit code. Not valid during the first line in the BLC frame. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.10.37 BLC_OFFSET_CH5_0

Address: 0x000 0938

RO	7	6	5	4	3	2	1	0
	CH5_BLC_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH5_BLC_OFFSET_0	BLC offset level for Channel 5 This field contains bits [7:0] of the 9-bit code. Not valid during the first line in the BLC frame. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.10.38 BLC_OFFSET_CH5_1

Address: 0x000 0939

RO	7	6	5	4	3	2	1	0
	—							CH5_BLC_OFFSET_1
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	CH5_BLC_OFFSET_1	BLC offset level for Channel 5 This field contains bit [8] of the 9-bit code. Not valid during the first line in the BLC frame. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.10.39 BLC_OFFSET_CH6_0

Address: 0x000 093C

RO	7	6	5	4	3	2	1	0
	CH6_BLC_OFFSET_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH6_BLC_OFFSET_0	BLC offset for Channel 6 This field contains bits [7:0] of the 9-bit code. Not valid during the first line in the BLC frame. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.10.40 BLC_OFFSET_CH6_1

Address: 0x000 093D

RO	7	6	5	4	3	2	1	0
	—							CH6_BLC_OFFSET_1
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	CH6_BLC_OFFSET_1	BLC offset level for Channel 6 This field contains bit [8] of the 9-bit code. Not valid during the first line in the BLC frame. 0 = –333 mV 256 = 0 mV 511 = 331.7 mV

8.11 SARADC_1—SARADC_1

8.11.1 SAR1_CTRL_1

Address: 0x000 0A01
BANK1 Address: 0x69

RW	7	6	5	4	3	2	1	0
	—					CH1_POL	—	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	CH1_POL	Signal polarity selection 0 = (Default) Positive signalling (CIS waveform) 1 = Negative signalling (CCD waveform)
1:0	—	Reserved

8.11.2 SAR1_CTRL_3

Address: 0x000 0A03
BANK1 Address: 0x6B

RW	7	6	5	4	3	2	1	0
	—						CH1_AFE_POWER	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1:0	CH1_AFE_POWER	AFE power mode selection. 00 = Low Power 01–10 = Reserved 11 = (Default) High Performance

8.12 SARADC_2—SARADC_2

8.12.1 SAR2_CTRL_1

Address: 0x000 0B01
BANK1 Address: 0x6D

RW	7	6	5	4	3	2	1	0
	—					CH2_POL	—	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	CH2_POL	Signal polarity selection 0 = (Default) Positive signalling (CIS waveform) 1 = Negative signalling (CCD waveform)
1:0	—	Reserved

8.12.2 SAR2_CTRL_3

Address: 0x000 0B03
BANK1 Address: 0x6F

RW	7	6	5	4	3	2	1	0
	—						CH2_AFE_POWER	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1:0	CH2_AFE_POWER	AFE power mode selection. 00 = Low Power 01–10 = Reserved 11 = (Default) High Performance

8.13 SARADC_3—SARADC_3

8.13.1 SAR3_CTRL_1

Address: 0x000 0C01
BANK1 Address: 0x71

RW	7	6	5	4	3	2	1	0
	—					CH3_POL	—	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	CH3_POL	Signal polarity selection 0 = (Default) Positive signalling (CIS waveform) 1 = Negative signalling (CCD waveform)
1:0	—	Reserved

8.13.2 SAR3_CTRL_3

Address: 0x000 0C03
BANK1 Address: 0x73

RW	7	6	5	4	3	2	1	0
	—						CH3_AFE_POWER	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1:0	CH3_AFE_POWER	AFE power mode selection. 00 = Low Power 01–10 = Reserved 11 = (Default) High Performance

8.14 SARADC_4—SARADC_4

8.14.1 SAR4_CTRL_1

Address: 0x000 0D01
BANK1 Address: 0x75

RW	7	6	5	4	3	2	1	0
	—					CH4_POL	—	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	CH4_POL	Signal polarity selection 0 = (Default) Positive signalling (CIS waveform) 1 = Negative signalling (CCD waveform)
1:0	—	Reserved

8.14.2 SAR4_CTRL_3

Address: 0x000 0D03
BANK1 Address: 0x77

RW	7	6	5	4	3	2	1	0
	—						CH4_AFE_POWER	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1:0	CH4_AFE_POWER	AFE power mode selection. 00 = Low Power 01–10 = Reserved 11 = (Default) High Performance

8.15 SARADC_5—SARADC_5

8.15.1 SAR5_CTRL_1

Address: 0x000 0E01
BANK1 Address: 0x79

RW	7	6	5	4	3	2	1	0
	—					CH5_POL	—	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	CH5_POL	Signal polarity selection 0 = (Default) Positive signalling (CIS waveform) 1 = Negative signalling (CCD waveform)
1:0	—	Reserved

8.15.2 SAR5_CTRL_3

Address: 0x000 0E03
BANK1 Address: 0x7B

RW	7	6	5	4	3	2	1	0
	—						CH5_AFE_POWER	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1:0	CH5_AFE_POWER	AFE power mode selection. 00 = Low Power 01–10 = Reserved 11 = (Default) High Performance

8.16 SARADC_6—SARADC_6

8.16.1 SAR6_CTRL_1

Address: 0x000 0F01
BANK1 Address: 0x7D

RW	7	6	5	4	3	2	1	0
	—					CH6_POL	—	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	CH6_POL	Signal polarity selection 0 = (Default) Positive signalling (CIS waveform) 1 = Negative signalling (CCD waveform)
1:0	—	Reserved

8.16.2 SAR6_CTRL_3

Address: 0x000 0F03
BANK1 Address: 0x7F

RW	7	6	5	4	3	2	1	0
	—						CH6_AFE_POWER	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1:0	CH6_AFE_POWER	AFE power mode selection. 00 = Low Power 01–10 = Reserved 11 = (Default) High Performance

8.17 AGC_TOP—Digital Gain Control

8.17.1 DGAIN_SEQ01_CH1_0

Address: 0x000 108C
BANK7 Address: 0x0C

RW	7	6	5	4	3	2	1	0
	CH1_SEQ0_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ0_DGAIN_0	Digital gain for Channel 1, State 0 Gain = [DGAIN/2048]. Valid from 1024 to 4095. This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.2 DGAIN_SEQ01_CH1_1

Address: 0x000 108D
BANK7 Address: 0x0D

RW	7	6	5	4	3	2	1	0
	—				CH1_SEQ0_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH1_SEQ0_DGAIN_1	Digital gain for Channel 1, State 0 Gain = [DGAIN/2048]. Valid from 1024 to 4095. This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.3 DGAIN_SEQ01_CH1_2

Address: 0x000 108E
BANK7 Address: 0x0E

RW	7	6	5	4	3	2	1	0
	CH1_SEQ1_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ1_DGAIN_0	Digital gain for Channel 1, State 1 Gain = [DGAIN/2048]. Valid from 1024 to 4095. This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.4 DGAIN_SEQ01_CH1_3

Address: 0x000 108F
BANK7 Address: 0x0F

RW	7	6	5	4	3	2	1	0
	—				CH1_SEQ1_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH1_SEQ1_DGAIN_1	Digital gain for Channel 1, State 1 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.5 DGAIN_SEQ23_CH1_0

Address: 0x000 1090
BANK7 Address: 0x10

RW	7	6	5	4	3	2	1	0
	CH1_SEQ2_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ2_DGAIN_0	Digital gain for Channel 1, State 2 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.6 DGAIN_SEQ23_CH1_1

Address: 0x000 1091
BANK7 Address: 0x11

RW	7	6	5	4	3	2	1	0
	—				CH1_SEQ2_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH1_SEQ2_DGAIN_1	Digital gain for Channel 1, State 2 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.7 DGAIN_SEQ23_CH1_2

Address: 0x000 1092
BANK7 Address: 0x12

RW	7	6	5	4	3	2	1	0
	CH1_SEQ3_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH1_SEQ3_DGAIN_0	Digital gain for Channel 1, State 3 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.8 DGAIN_SEQ23_CH1_3

Address: 0x000 1093
BANK7 Address: 0x13

RW	7	6	5	4	3	2	1	0
	—				CH1_SEQ3_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH1_SEQ3_DGAIN_1	Digital gain for Channel 1, State 3 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.9 DGAIN_SEQ01_CH2_0

Address: 0x000 1094
BANK7 Address: 0x14

RW	7	6	5	4	3	2	1	0
	CH2_SEQ0_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH2_SEQ0_DGAIN_0	Digital gain for Channel 2, State 0 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.10 DGAIN_SEQ01_CH2_1

Address: 0x000 1095
BANK7 Address: 0x15

RW	7	6	5	4	3	2	1	0
	—				CH2_SEQ0_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH2_SEQ0_DGAIN_1	Digital gain for Channel 2, State 0 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.11 DGAIN_SEQ01_CH2_2

Address: 0x000 1096
BANK7 Address: 0x16

RW	7	6	5	4	3	2	1	0
	CH2_SEQ1_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH2_SEQ1_DGAIN_0	Digital gain for Channel 2, State 1 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.12 DGAIN_SEQ01_CH2_3

Address: 0x000 1097
BANK7 Address: 0x17

RW	7	6	5	4	3	2	1	0
	—				CH2_SEQ1_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH2_SEQ1_DGAIN_1	Digital gain for Channel 2, State 1 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.13 DGAIN_SEQ23_CH2_0

Address: 0x000 1098
BANK7 Address: 0x18

RW	7	6	5	4	3	2	1	0
	CH2_SEQ2_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH2_SEQ2_DGAIN_0	Digital gain for Channel 2, State 2 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.14 DGAIN_SEQ23_CH2_1

Address: 0x000 1099
BANK7 Address: 0x19

RW	7	6	5	4	3	2	1	0
	—				CH2_SEQ2_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH2_SEQ2_DGAIN_1	Digital gain for Channel 2, State 2 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.15 DGAIN_SEQ23_CH2_2

Address: 0x000 109A
BANK7 Address: 0x1A

RW	7	6	5	4	3	2	1	0
	CH2_SEQ3_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH2_SEQ3_DGAIN_0	Digital gain for Channel 2, State 3 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.16 DGAIN_SEQ23_CH2_3

Address: 0x000 109B
BANK7 Address: 0x1B

RW	7	6	5	4	3	2	1	0
	—				CH2_SEQ3_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH2_SEQ3_DGAIN_1	Digital gain for Channel 2, State 3 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.17 DGAIN_SEQ01_CH3_0

Address: 0x000 109C
BANK7 Address: 0x1C

RW	7	6	5	4	3	2	1	0
	CH3_SEQ0_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH3_SEQ0_DGAIN_0	Digital gain for Channel 3, State 0 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.18 DGAIN_SEQ01_CH3_1

Address: 0x000 109D
BANK7 Address: 0x1D

RW	7	6	5	4	3	2	1	0
	—				CH3_SEQ0_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH3_SEQ0_DGAIN_1	Digital gain for Channel 3, State 0 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.19 DGAIN_SEQ01_CH3_2

Address: 0x000 109E
BANK7 Address: 0x1E

RW	7	6	5	4	3	2	1	0
	CH3_SEQ1_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH3_SEQ1_DGAIN_0	Digital gain for Channel 3, State 1 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.20 DGAIN_SEQ01_CH3_3

Address: 0x000 109F
BANK7 Address: 0x1F

RW	7	6	5	4	3	2	1	0
	—				CH3_SEQ1_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH3_SEQ1_DGAIN_1	Digital gain for Channel 3, State 1 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.21 DGAIN_SEQ23_CH3_0

Address: 0x000 10A0
BANK7 Address: 0x20

RW	7	6	5	4	3	2	1	0
	CH3_SEQ2_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH3_SEQ2_DGAIN_0	Digital gain for Channel 3, State 2 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.22 DGAIN_SEQ23_CH3_1

Address: 0x000 10A1
BANK7 Address: 0x21

RW	7	6	5	4	3	2	1	0
	—				CH3_SEQ2_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH3_SEQ2_DGAIN_1	Digital gain for Channel 3, State 2 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.23 DGAIN_SEQ23_CH3_2

Address: 0x000 10A2
BANK7 Address: 0x22

RW	7	6	5	4	3	2	1	0
	CH3_SEQ3_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH3_SEQ3_DGAIN_0	Digital gain for Channel 3, State 3 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.24 DGAIN_SEQ23_CH3_3

Address: 0x000 10A3
BANK7 Address: 0x23

RW	7	6	5	4	3	2	1	0
	—				CH3_SEQ3_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH3_SEQ3_DGAIN_1	Digital gain for Channel 3, State 3 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.25 DGAIN_SEQ01_CH4_0

Address: 0x000 10A4
BANK7 Address: 0x24

RW	7	6	5	4	3	2	1	0
	CH4_SEQ0_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH4_SEQ0_DGAIN_0	Digital gain for Channel 4, State 0 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.26 DGAIN_SEQ01_CH4_1

Address: 0x000 10A5
BANK7 Address: 0x25

RW	7	6	5	4	3	2	1	0
	—				CH4_SEQ0_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH4_SEQ0_DGAIN_1	Digital gain for Channel 4, State 0 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.27 DGAIN_SEQ01_CH4_2

Address: 0x000 10A6
BANK7 Address: 0x26

RW	7	6	5	4	3	2	1	0
	CH4_SEQ1_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH4_SEQ1_DGAIN_0	Digital gain for Channel 4, State 1 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.28 DGAIN_SEQ01_CH4_3

Address: 0x000 10A7
BANK7 Address: 0x27

RW	7	6	5	4	3	2	1	0
	—				CH4_SEQ1_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH4_SEQ1_DGAIN_1	Digital gain for Channel 4, State 1 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.29 DGAIN_SEQ23_CH4_0

Address: 0x000 10A8
BANK7 Address: 0x28

RW	7	6	5	4	3	2	1	0
	CH4_SEQ2_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH4_SEQ2_DGAIN_0	Digital gain for Channel 4, State 2 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.30 DGAIN_SEQ23_CH4_1

Address: 0x000 10A9
BANK7 Address: 0x29

RW	7	6	5	4	3	2	1	0
	—				CH4_SEQ2_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH4_SEQ2_DGAIN_1	Digital gain for Channel 4, State 2 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.31 DGAIN_SEQ23_CH4_2

Address: 0x000 10AA
BANK7 Address: 0x2A

RW	7	6	5	4	3	2	1	0
	CH4_SEQ3_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH4_SEQ3_DGAIN_0	Digital gain for Channel 4, State 3 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.32 DGAIN_SEQ23_CH4_3

Address: 0x000 10AB
BANK7 Address: 0x2B

RW	7	6	5	4	3	2	1	0
	—				CH4_SEQ3_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH4_SEQ3_DGAIN_1	Digital gain for Channel 4, State 3 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.33 DGAIN_SEQ01_CH5_0

Address: 0x000 10AC
BANK7 Address: 0x2C

RW	7	6	5	4	3	2	1	0
	CH5_SEQ0_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH5_SEQ0_DGAIN_0	Digital gain for Channel 5, State 0 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.34 DGAIN_SEQ01_CH5_1

Address: 0x000 10AD
BANK7 Address: 0x2D

RW	7	6	5	4	3	2	1	0
	—				CH5_SEQ0_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH5_SEQ0_DGAIN_1	Digital gain for Channel 5, State 0 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.35 DGAIN_SEQ01_CH5_2

Address: 0x000 10AE
BANK7 Address: 0x2E

RW	7	6	5	4	3	2	1	0
	CH5_SEQ1_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH5_SEQ1_DGAIN_0	Digital gain for Channel 5, State 1 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.36 DGAIN_SEQ01_CH5_3

Address: 0x000 10AF
BANK7 Address: 0x2F

RW	7	6	5	4	3	2	1	0
	—				CH5_SEQ1_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH5_SEQ1_DGAIN_1	Digital gain for Channel 5, State 1 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.37 DGAIN_SEQ23_CH5_0

Address: 0x000 10B0
BANK7 Address: 0x30

RW	7	6	5	4	3	2	1	0
	CH5_SEQ2_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH5_SEQ2_DGAIN_0	Digital gain for Channel 5, State 2 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.38 DGAIN_SEQ23_CH5_1

Address: 0x000 10B1
BANK7 Address: 0x31

RW	7	6	5	4	3	2	1	0
	—				CH5_SEQ2_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH5_SEQ2_DGAIN_1	Digital gain for Channel 5, State 2 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.39 DGAIN_SEQ23_CH5_2

Address: 0x000 10B2
BANK7 Address: 0x32

RW	7	6	5	4	3	2	1	0
	CH5_SEQ3_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH5_SEQ3_DGAIN_0	Digital gain for Channel 5, State 3 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.40 DGAIN_SEQ23_CH5_3

Address: 0x000 10B3
BANK7 Address: 0x33

RW	7	6	5	4	3	2	1	0
	—				CH5_SEQ3_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH5_SEQ3_DGAIN_1	Digital gain for Channel 5, State 3 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.41 DGAIN_SEQ01_CH6_0

Address: 0x000 10B4
BANK7 Address: 0x34

RW	7	6	5	4	3	2	1	0
	CH6_SEQ0_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH6_SEQ0_DGAIN_0	Digital gain for Channel 6, State 0 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.42 DGAIN_SEQ01_CH6_1

Address: 0x000 10B5
BANK7 Address: 0x35

RW	7	6	5	4	3	2	1	0
	—				CH6_SEQ0_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH6_SEQ0_DGAIN_1	Digital gain for Channel 6, State 0 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.43 DGAIN_SEQ01_CH6_2

Address: 0x000 10B6
BANK7 Address: 0x36

RW	7	6	5	4	3	2	1	0
	CH6_SEQ1_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH6_SEQ1_DGAIN_0	Digital gain for Channel 6, State 1 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.44 DGAIN_SEQ01_CH6_3

Address: 0x000 10B7
BANK7 Address: 0x37

RW	7	6	5	4	3	2	1	0
	—				CH6_SEQ1_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH6_SEQ1_DGAIN_1	Digital gain for Channel 6, State 1 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.45 DGAIN_SEQ23_CH6_0

Address: 0x000 10B8
BANK7 Address: 0x38

RW	7	6	5	4	3	2	1	0
	CH6_SEQ2_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH6_SEQ2_DGAIN_0	Digital gain for Channel 6, State 2 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.46 DGAIN_SEQ23_CH6_1

Address: 0x000 10B9
BANK7 Address: 0x39

RW	7	6	5	4	3	2	1	0
	—				CH6_SEQ2_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH6_SEQ2_DGAIN_1	Digital gain for Channel 6, State 2 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.47 DGAIN_SEQ23_CH6_2

Address: 0x000 10BA
BANK7 Address: 0x3A

RW	7	6	5	4	3	2	1	0
	CH6_SEQ3_DGAIN_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CH6_SEQ3_DGAIN_0	Digital gain for Channel 6, State 3 This field contains bits [7:0] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.17.48 DGAIN_SEQ23_CH6_3

Address: 0x000 10BB
BANK7 Address: 0x3B

RW	7	6	5	4	3	2	1	0
	—				CH6_SEQ3_DGAIN_1			
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	CH6_SEQ3_DGAIN_1	Digital gain for Channel 6, State 3 This field contains bits [11:8] of the 12-bit code. 1024 = 0.5 V/V 2048 = 1.0 V/V 3072 = 1.5 V/V 4095 = 1.9995 V/V

8.18 PAT_GEN—Test pattern generator

8.18.1 PGCONFIG_0

Address: 0x000 1100
BANK3 Address: 0x78

RW	7	6	5	4	3	2	1	0
	PGEN_MARCH	PGEN_PATT_SEL		PGEN_INV	—			PGEN_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	PGEN_MARCH	Pattern generator march enable. If this bit is set, the marching pattern overrides PGEN_PATT_SEL selection. 0 = (Default) No override 1 = March enabled
6:5	PGEN_PATT_SEL	Pattern generator select 00 = (Default) Constant level 01 = Vertical ramp 10 = Horizontal ramp 11 = Patch pattern
4	PGEN_INV	Pattern generator invert 0 = (Default) Non-inverted 1 = Inverted
3:1	—	Reserved
0	PGEN_EN	Pattern generator enable 0 = (Default) Disabled 1 = Enabled

8.18.2 PGCONFIG_2

Address: 0x000 1102
BANK3 Address: 0x7A

RW	7	6	5	4	3	2	1	0
	PGEN_LVL_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PGEN_LVL_0	Pattern generator intensity This field contains bits [7:0] of the 16-bit code, valid from 0-65535.

8.18.3 PGCONFIG_3

Address: 0x000 1103
BANK3 Address: 0x7B

RW	7	6	5	4	3	2	1	0
	PGEN_LVL_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PGEN_LVL_1	Pattern generator intensity This field contains bits [15:8] of the 16-bit code, valid from 0-65535.

8.18.4 PGWIDTH_0

Address: 0x000 1104
BANK3 Address: 0x7C

RW	7	6	5	4	3	2	1	0
	PGEN_WIDTH1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PGEN_WIDTH1	Pattern generator width1. Configures the dimensions of the vertical ramp, horizontal ramp, and patch pattern.

8.18.5 PGWIDTH_1

Address: 0x000 1105
BANK3 Address: 0x7D

RW	7	6	5	4	3	2	1	0
	PGEN_WIDTH2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PGEN_WIDTH2	Pattern generator width2. Configures the dimensions of the patch pattern (gap between patches).

8.19 LED_CTRL—LED Control

8.19.1 LED_CTRL_CONFIG_0

Address: 0x000 1500
BANK6 Address: 0x48

RW	7	6	5	4	3	2	1	0
	—				LED_CTRL_SRC	LEDB_EN	LEDG_EN	LEDR_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3	LED_CTRL_SRC	Select control source for LED drivers 0 = (Default) Internal (POn) 1 = External (HW pin)
2	LEDB_EN	LEDB driver control 0 = (Default) Disabled 1 = Enabled
1	LEDG_EN	LEDG driver control 0 = (Default) Disabled 1 = Enabled
0	LEDR_EN	LEDR driver control 0 = (Default) Disabled 1 = Enabled

8.19.2 LED_CTRL_CONFIG_1

Address: 0x000 1501
BANK6 Address: 0x49

RW	7	6	5	4	3	2	1	0
	—				LED_RAMP_TIME			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	LED_RAMP_TIME	LED ramp time. Time taken to ramp fine current (LEDn_FINE) from 0-255. 0x0–0x7 = (Default) 8 us 0x8 = 9 us 0x9 = 10 us … 0xF = 16 us

8.19.3 LED_CTRL_CONFIG_2

Address: 0x000 1502
BANK6 Address: 0x4A

RW	7	6	5	4	3	2	1	0
	LED_RAMP_BOOST		LEDB_COARSE		LEDG_COARSE		LEDR_COARSE	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	LED_RAMP_BOOST	LED ramp boost. Shortens the ramp time by a factor of 2 or 4. Boost by 2 is only valid if pixel sample rate >= 4MHz. Boost by 4 is only valid if pixel sample rate >= 12MHz and LED_RAMP_TIME >= 0xB. If an invalid selection is made, the boost is disabled and the unmodified LED_RAMP_TIME is used. 00 = (Default) No boost 01 = Boost by 2 10 = Boost by 4 11 = Reserved
5:4	LEDB_COARSE	LEDB coarse current control. This is the output current if LEDB_FINE=255. 00 = (Default) 33 mA 01 = 41 mA 10 = 49 mA 11 = 66 mA
3:2	LEDG_COARSE	LEDG coarse current control. This is the output current if LEDG_FINE=255. 00 = (Default) 33 mA 01 = 41 mA 10 = 49 mA 11 = 66 mA
1:0	LEDR_COARSE	LEDR coarse current control. This is the output current if LEDR_FINE=255. 00 = (Default) 33 mA 01 = 41 mA 10 = 49 mA 11 = 66 mA

8.19.4 LEDX_FINE_0

Address: 0x000 1504
BANK6 Address: 0x4C

RW	7	6	5	4	3	2	1	0
	LEDR_FINE							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LEDR_FINE	LEDR fine current control. Selects the output current from 0 to LEDR_COARSE. If the LEDR output is enabled, the current ramps to (LEDR_FINE/255 * LEDR_COARSE)

8.19.5 LEDX_FINE_1

Address: 0x000 1505
BANK6 Address: 0x4D

RW	7	6	5	4	3	2	1	0
	LEDG_FINE							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LEDG_FINE	LEDG fine current control. Selects the output current from 0 to LEDG_COARSE. If the LEDG output is enabled, the current ramps to (LEDG_FINE/255 * LEDG_COARSE)

8.19.6 LEDX_FINE_2

Address: 0x000 1506
BANK6 Address: 0x4E

RW	7	6	5	4	3	2	1	0
	LEDB_FINE							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	LEDB_FINE	LEDB fine current control. Selects the output current from 0 to LEDB_COARSE. If the LEDB output is enabled, the current ramps to (LEDB_FINE/255 * LEDB_COARSE)

8.19.7 LED_CTRL_STATUS

Address: 0x000 1508
BANK6 Address: 0x50

RO	7	6	5	4	3	2	1	0
	—			LED_MAX_ CURRENT_ERR	LED_CTRL_SHORT_ ERR	—		
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4	LED_MAX_ CURRENT_ERR	Maximum current error. Indicates the sum of LEDR_COARSE, LEDG_COARSE, and LEDB_COARSE for the active LED channels exceeds 0b11. Only applies to active channels (enabled using LEDx_EN and by an asserted hardware pin or pulse waveform). If this bit is set, the fine current selections are restricted to a maximum of 45 mA. In most configurations, the error indicates a sum exceeding 135 mA. The combination of 33mA + 49mA + 49mA (total 131 mA) also triggers the maximum-current response. 0 = (Default) Normal 1 = Max current error
3	LED_CTRL_ SHORT_ERR	Short circuit detection on LED control resistor. Indicates a short circuit in the ILED_CTRL external resistor. 0 = (Default) Normal 1 = Short detected
2:0	—	Reserved

8.20 DPLL1—DPLL1

8.20.1 DPLL1_DFLL_DIVIDER_CTRL_0

Address: 0x000 1700
BANK6 Address: 0x60

RW	7	6	5	4	3	2	1	0
	PLL1_OUTPUT1_DIV_0							—
Default	0	0	1	0	0	0	0	0

Bits	Name	Description
7:1	PLL1_OUTPUT1_ DIV_0	Divider ratio for main output (ADC clock output). This field contains bits [6:0] of the 9-bit integer.
0	—	Reserved

8.20.2 DPLL1_DFLL_DIVIDER_CTRL_1

Address: 0x000 1701
BANK6 Address: 0x61

RW	7	6	5	4	3	2	1	0
	PLL1_VCO_RANGE				—		PLL1_OUTPUT1_DIV_1	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	PLL1_VCO_RANGE	VCO frequency range 0x0 = (Default) 150-182 MHz 0x1 = 182-189 MHz 0x2 = 189-197 MHz 0x3 = 197-203 MHz 0x4 = 203-214 MHz 0x5 = 214-225 MHz 0x6 = 225-234 MHz 0x7 = 234-245 MHz 0x8 = 245-253 MHz 0x9 = 253-261 MHz 0xA = 261-269 MHz 0xB = 269-278 MHz 0xC = 278-285 MHz 0xD = 285-294 MHz 0xE = 294-298 MHz 0xF = 298-300 MHz
3:2	—	Reserved
1:0	PLL1_OUTPUT1_ DIV_1	Divider ratio for main output (ADC clock output). This field contains bits [8:7] of the 9-bit integer.

8.20.3 DPLL1_DFLL_DIVIDER_CTRL_2

Address: 0x000 1702
BANK6 Address: 0x62

RW	7	6	5	4	3	2	1	0
	PLL1_OUTPUT2_DIV_0							PLL1_OUTPUT2_EN
Default	0	0	1	0	0	0	0	0

Bits	Name	Description
7:1	PLL1_OUTPUT2_DIV_0	Divider ratio for secondary output (data output clock). This field contains bits [6:0] of the 9-bit integer.
0	PLL1_OUTPUT2_EN	PLL secondary output control (data output clock) 0 = (Default) Disabled 1 = Enabled

8.20.4 DPLL1_DFLL_DIVIDER_CTRL_3

Address: 0x000 1703
BANK6 Address: 0x63

RW	7	6	5	4	3	2	1	0
	PLL1_REFCLK_DIV_RATIO				PLL1_REFCLK_DIV_BYPASS	—	PLL1_OUTPUT2_DIV_1	
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:4	PLL1_REFCLK_DIV_RATIO	MCLK input divider ratio 0x0 = (Default) Divide by 1 0x1 = Divide by 2 … 0xF = Divide by 16
3	PLL1_REFCLK_DIV_BYPASS	MCLK input divider bypass 0 = Divider enabled 1 = (Default) Divider bypass
2	—	Reserved
1:0	PLL1_OUTPUT2_DIV_1	Divider ratio for secondary output (data output clock). This field contains bits [8:7] of the 9-bit integer.

8.20.5 DPLL1_DFLL_FEEDBACK_RATIO_0

Address: 0x000 1704
BANK6 Address: 0x64

RW	7	6	5	4	3	2	1	0
	PLL1_RATIO_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL1_RATIO_0	PLL frequency ratio. Sets the ratio of the VCO to the MCLK reference. 9 integer bits, 20 fractional bits. This field contains bits [7:0] of the 29-bit code.

8.20.6 DPLL1_DFLL_FEEDBACK_RATIO_1

Address: 0x000 1705
BANK6 Address: 0x65

RW	7	6	5	4	3	2	1	0
	PLL1_RATIO_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL1_RATIO_1	PLL frequency ratio. Sets the ratio of the VCO to the MCLK reference. 9 integer bits, 20 fractional bits. This field contains bits [15:8] of the 29-bit code.

8.20.7 DPLL1_DFLL_FEEDBACK_RATIO_2

Address: 0x000 1706
BANK6 Address: 0x66

RW	7	6	5	4	3	2	1	0
	PLL1_RATIO_2							
Default	0	0	0	1	0	0	0	0

Bits	Name	Description
7:0	PLL1_RATIO_2	PLL frequency ratio. Sets the ratio of the VCO to the MCLK reference. 9 integer bits, 20 fractional bits. This field contains bits [23:16] of the 29-bit code.

8.20.8 DPLL1_DFLL_FEEDBACK_RATIO_3

Address: 0x000 1707
BANK6 Address: 0x67

RW	7	6	5	4	3	2	1	0
	—		PLL1_MODE	PLL1_RATIO_3				
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	PLL1_MODE	PLL Mode select. In Integer Mode, only the integer bits of the PLL ratio are used. 0 = (Default) Fractional Mode 1 = Integer Mode
4:0	PLL1_RATIO_3	PLL frequency ratio. Sets the ratio of the VCO to the MCLK reference. 9 integer bits, 20 fractional bits. This field contains bits [28:24] of the 29-bit code.

8.20.9 DPLL1_DFLL_FEATURES_0

Address: 0x000 1708
BANK6 Address: 0x68

RW	7	6	5	4	3	2	1	0
	PLL1_VCO_GAIN				PLL1_CP_IBIAS			PLL1_PHASE_DET_PAUSE_EN
Default	1	0	0	0	0	1	0	0

Bits	Name	Description
7:4	PLL1_VCO_GAIN	PLL VCO gain
3:1	PLL1_CP_IBIAS	PLL current bias
0	PLL1_PHASE_DET_PAUSE_EN	Phase detect control. If enabled, the phase detection is paused when MCLK phase change is indicated. 0 = (Default) Disabled 1 = Enabled

8.20.10 DPLL1_DFLL_FEATURES_1

Address: 0x000 1709
BANK6 Address: 0x69

RW	7	6	5	4	3	2	1	0
	—				PLL1_FILT			
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:4	—	Reserved
3:0	PLL1_FILT	PLL loop filter cut-off frequency

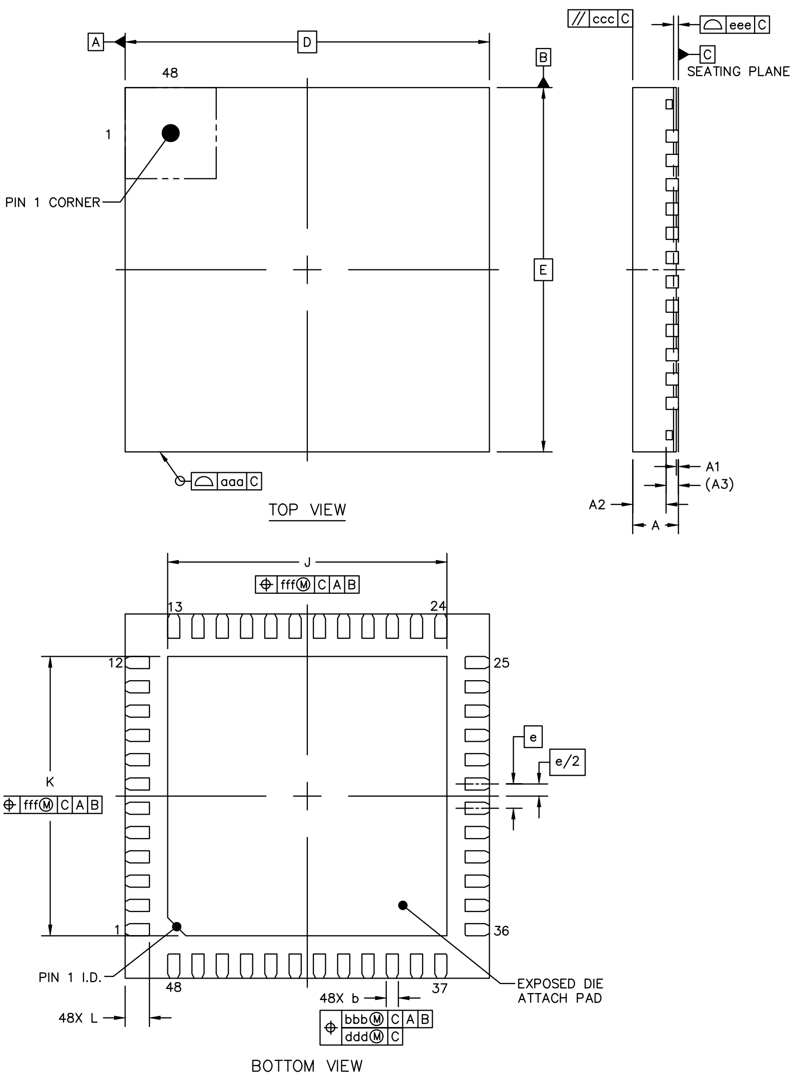
9 Thermal Characteristics

Table 9-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	QFN	Units
Junction-to-ambient thermal resistance	θ_{JA}	24.16	°C/W
Junction-to-board thermal resistance	θ_{JB}	11.84	°C/W
Junction-to-case (top) thermal resistance	θ_{JC}	31.94	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	11.16	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	1.02	°C/W

Notes:
- Natural convection at the maximum recommended operating temperature T_A (see Table 3-1)
- Four-layer, 2s2p PCB as specified by JESD51–9 and JESD51–11; dimensions: 101.5 x 114.5 x 1.6 mm
- Exposed pad is connected to the PCB ground layer through a 4 x 4 thermal via array; vias are 0.3 mm diameter, plated.
- Thermal parameters as defined by JESD51–12

10 Package Dimensions

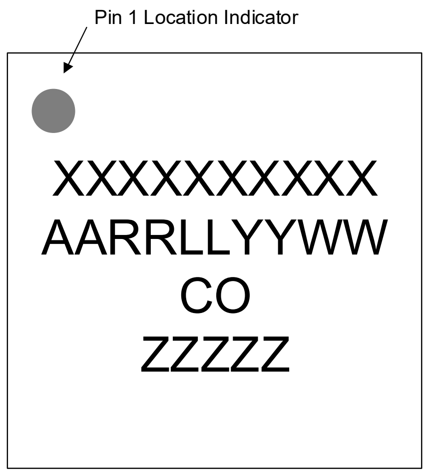


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203	REF
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6	BSC
	Y	E		6	BSC
LEAD PITCH		e		0.4	BSC
EP SIZE	X	J	4.5	4.6	4.7
	Y	K	4.5	4.6	4.7
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
2.0 TOTAL THICKNESS NOT INCLUDE SAW BURR.

Figure 10-1. QFN 48-pin Package Drawing

11 Package Marking



Top Side Brand
Line 1: Part number
Line 2: Package mark
Line 3: Country of origin (CO)
Line 4: Encoded wafer/device ID

Package Mark Fields
AA = Assembly site code
RR = Device revision code
LL = Lot sequence code
YY = Year of manufacture
WW = Work week of manufacture

Figure 11-1. Package Marking

12 Ordering Information

Table 12-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number #
CS82L46	Six-channel AFE with sensor timing generation and LVDS/CMOS data output	48-pin QFN	Yes	Commercial	–40 to +85°C	Tape and Reel	CS82L46–DNR
CS82L46	Six-channel AFE with sensor timing generation and LVDS/CMOS data output	48-pin QFN	Yes	Commercial	–40 to +85°C	Tray	CS82L46–DN

13 Revision History

Table 13-1. Revision History

Revision	Changes
F1 JAN 2026	• Initial production release

Important: Please check www.cirrus.com or with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.