CDB42L56

Evaluation Board for CS42L56

Features

- Analog Line and Microphone Level Inputs
  - 6 RCA and 3 Stereo 1/8" Jacks
  - Compatible with Single-Ended and Pseudo-Diff. Input Configurations
- Analog Line and Headphone Outputs
  - Stereo 1/8" Headphone Jack w/Input Detection
  - 4 RCA Jacks for Headphone/Line Outputs
- 8 to 96 kHz S/PDIF Interface
  - CS8416 Digital Audio Receiver
  - CS8406 Digital Audio Transmitter
- I/O Stake Header Accessibility
  - External Control Port Headers
  - External Direct and Buffered Serial Audio I/O Headers
- Multiple Power Supply options via USB, Battery or External Power Supplies.
- 1.8 V to 3.3 V Selectable Logic Interface
- FlexGUI S/W Control - Windows® Compatible
  - Pre-Defined & User-Configurable Scripts

Description

The CDB42L56 is the ideal evaluation platform solution to test and evaluate the CS42L56.The CS42L56 is a highly integrated, 24-bit, ultra-low power stereo codec based on multi-bit delta-sigma modulation suitable for low power portable applications. Use of the board requires an analog/digital signal source, an analyzer and power supplies. A Windows PC-compatible computer is also needed in order to configure the CS42L56 and the board.

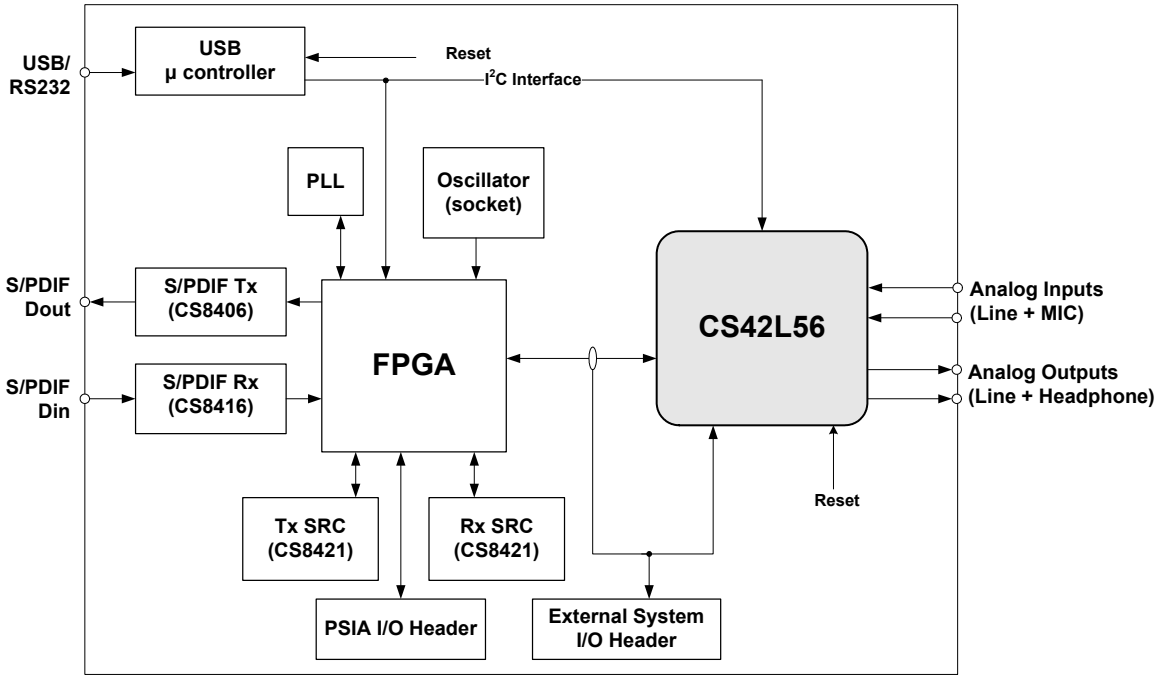
System timing can be provided by the CS8416 (on-board), by the CS42L56 supplied with a master clock, by the on-board crystal oscillator or via an I/O stake header with a DSP connected.

RCA phono connectors and stereo 1/8th inch audio jacks are provided for CS42L56 analog inputs and HP/Line outputs. Digital I/O connections are provided via RCA phono or optical connectors to the CS8416 and CS8406 (S/PDIF Rx and Tx).

The CDB42L56 is programmed via the PC's USB using Cirrus Logic's Microsoft® Windows®-based software (FlexGUI). The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB42L56 Evaluation Board



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1. SYSTEM OVERVIEW

The CDB42L56 evaluation platform provides analog and digital interfaces to the CS42L56 and allows for external DSP and I²C interconnects to the board. On-board peripherals are powered either from the USB connection or from an external +5 V supply. On-board voltage regulators provide power to the digital and analog cores of the CS42L56. The CDB42L56 is configured using Cirrus Logic's Windows-compatible FlexGUI software to read/write to device registers.

This section describes the various components on the CDB42L56 and how they are used with the CS42L56. Section 2 on page 8 is a simplified quick connect guide provided for user convenience and may be used to quickly configure the CS42L56. Section 3 on page 9 describes some of the configurations available for transmitting and receiving audio signals. Section 4 on page 11 provides software configuration details. Section 5 on page 18 provides a description of all stake headers and connectors, including the default factory settings of all jumpers. Section 6 on page 21 provides typical performance plots. The CDB42L56 schematic and layout set is shown in Figures 35 through 44.

1.1 Control Port and Board Configuration

The CDB42L56 evaluation board must be programmed using the Windows compatible software (Cirrus Logic FlexGUI) provided. This software allows the user to program the registers of all the programmable components on the board using an I²C interface.

The GUI interfaces with an on-board micro controller through either the USB or the serial port connector. For a detailed explanation on software controls, refer to Section 4 on page 11.

Alternatively, the I²C interface to the CS42L56 can be directly accessed through an I/O header (J109) to accept external timing and signals in a user application during system development.

1.2 Power

Power is supplied to the evaluation board through either the +5.0 V test points or the VBUS supply from the USB. NOTE: The minimum current required for board operation is approximately 300 mA. It may therefore be necessary to connect the CDB42L56 directly to the USB port on the PC as opposed to a hub or keyboard port where the current might be limited.

Jumpers connect the CS42L56's supplies to a low dropout regulated voltage of +1.8 V, +2.5 V or +3.3 V for VL and +1.8 V or +2.5 V for VLDO, VA and VCP. A selection for a 1.8 V supply from a buck regulator is also available, providing a more efficient means of evaluating the CS42L56's performance when powered from batteries (3 AAA battery connectors are available on the bottom side of the CDB).

For current measurement purposes only, a 1 Ω ohm series resistor is connected to each supply. The current is easily calculated by measuring the voltage drop across this resistor. NOTE: The stake headers connected in parallel with these resistors must be shunted with the supplied jumper during normal operation.

WARNING: Please refer to the CS42L56 data sheet for allowable voltage levels.

1.3 Digital Input

1.3.1 CS8416 S/PDIF Digital Audio Receiver

The CS8416 S/PDIF receiver converts an incoming S/PDIF data input stream into PCM data for the CS42L56 (through the "Transmit" (Tx) Sample Rate Converter (SRC)).

A complete description of the CS8416 (Figure 36 on page 29) and a discussion of the digital audio interface can be found in the CS8416 data sheet.

Configuration of the CS8416 is made using controls in the “Board Configuration” tab of the Cirrus FlexGUI software. Section 3. “Configuration Options” on page 9 and Section 4. “Software Mode Control” on page 11 provide configuration examples and software details.

1.3.1.1 CS8421 Sample Rate Converter (Tx SRC to CS42L56)

The CS8421 Tx SRC receives PCM digital audio data from either the CS8416 S/PDIF receiver or the AP PSIA header and synchronizes this data with the CS42L56, regardless of the CS42L56’s master and audio clocks.

A complete description of the CS8421 (Figure 36 on page 29) and a discussion of the digital audio interface can be found in the CS8421 data sheet.

Configuration and routing selections for the CS8421 are made using controls in the “Board Configuration” tab of the Cirrus FlexGUI software. Section 3. “Configuration Options” on page 9 and Section 4. “Software Mode Control” on page 11 provide configuration examples and software details.

1.4 Digital Output

1.4.1 CS8406 S/PDIF Digital Audio Transmitter

The CS8406 converts the PCM data generated from the CS42L56 (through the “Receive” (Rx) SRC) to the standard S/PDIF data stream.

A complete description of the CS8406 (Figure 36 on page 29) and a discussion of the digital audio interface can be found in the CS8406 data sheet.

Configuration of the CS8406 is made using controls in the “Board Configuration” tab of the Cirrus FlexGUI software. Section 3. “Configuration Options” on page 9 and Section 4. “Software Mode Control” on page 11 provide configuration examples and software details.

1.4.2 CS8421 Sample Rate Converter (Rx SRC from CS42L56)

The CS8421 Rx SRC receives PCM digital audio data from the CS42L56 and synchronizes this data with either the CS8406 S/PDIF transmitter or the AP PSIA headers, regardless of the CS42L56’s master and audio clocks.

A complete description of the CS8421 (Figure 36 on page 29) and a discussion of the digital audio interface can be found in the CS8421 data sheet.

Configuration and routing selections for the CS8421 are made using controls in the “Board Configuration” tab of the Cirrus FlexGUI software.Section 3. “Configuration Options” on page 9 and Section 4. “Software Mode Control” on page 11 provide configuration examples and software details.

1.5 FPGA

The FPGA controls the digital signal routing between the CS42L56, CS8406, CS8416, CS8421 (Tx SRC and Rx SRC), PLL and the I/O stake header. It also provides a divider for the system master clock from an on-board oscillator to the required devices. Figures 2 and 3 in Section 3 show how the FPGA can route clocks and data in order to allow the user to test the CS42L56 in various setups.

Configuration and routing selections for the FPGA are made using controls in the “Board Configuration” tab of the Cirrus FlexGUI software. Section 4 on page 11 provides software configuration details.

1.6 Oscillator

The socketed on-board oscillator (Y1) can be selected as the system master clock source by using the selections on the “Board Configuration” tab of the Cirrus FlexGUI. Section 4 on page 11 provides software configuration details.

The oscillator is mounted in pin sockets, allowing easy removal or replacement. The device footprint on the board will accommodate half-can or full-can sized oscillators.

1.7 PLL

An on-board PLL is used with the FPGA to generate the serial port sub-clocks for the CS42L56’s serial port when the CS42L56 is set to slave mode. The sub-clocks’ frequencies are selected on the “Board Configuration” tab of the Cirrus FlexGUI. Section 4 on page 11 provides software configuration details.

1.8 I/O Stake Headers

Headers J104 and J109 (Figure 35 on page 28) provide unbuffered bidirectional access to the CS42L56 serial port and control port, respectively. For regular operation, the left two pins on all rows should be shunted to allow the CS42L56 to receive serial and control port data and clocks from the on-board FPGA.

Alternatively, the stake headers provide access to the CS42L56 from external systems simply by removing all the shunt jumpers from the “USB” and “CDB I/O” positions. The user may then connect a ribbon cable connector to the “Ext. Sys. Connect” pins for external control of board functions. A single row of “GND” pins is provided to maintain signal ground integrity. Two unpopulated pull-up resistors are also available should the user choose to use the CDB42L56 logic supply (VL) externally.

If an external system is used to interface with the CS42L56 through headers J104 and J109, the digital I/O logic voltage levels must be selected cautiously since the lines between the headers and the device are not buffered. Please refer to the CS42L56 product data sheet for a detailed explanation on digital I/O interface specifications. Selections are made using the “Board Configuration” tab of the Cirrus FlexGUI software. Section 4 on page 11 provides software configuration details.

1.9 CS42L56 Audio Codec

A complete description of the CS42L56 (U3 - Figure 35 on page 28) can be found in the CS42L56 product data sheet.

The CS42L56 is configured using the Cirrus Logic Windows compatible software FlexGUI. The device configuration registers are directly accessible via the “Register Maps” tab of the Cirrus FlexGUI software. This tab provides low-level control of each bit. For easier configuration, additional tabs provide high-level control. Section 4 on page 11 provides software configuration details.

1.10 Analog Inputs

The analog input circuitry on the CDB42L56 has been designed to allow for testing of the CS42L56 in all its possible analog input configurations. Line or microphone level analog input signals can be provided to the analog inputs on the CS42L56 through RCA or microphone input jacks (Figure 35 on page 28). Stake header J6 allows the user to select (with jumpers installed) the CS42L56 as the microphone bias source for each microphone input (**CAUTION:** Only 2 jumpers may be installed at a time).

Headers J19 and J20 are used to select the desired input for pins AIN3A/AIN1REF and AIN3B/AIN2REF on the CS42L56. These headers can be used to select between either a single-ended or a pseudo-differential analog input setup. Table 1 provides jumper and resistor settings for the various analog input configurations allowed on the CS42L56. The shaded rows in the table indicate the most commonly used configurations and do not require any extra resistor modifications.

No.	Analog Input 1		Analog Input 2		Analog Input 3		Jumper Settings		Resistors to Populate	Resistors to Unpopulate
	AIN1A	AIN1B	AIN2A	AIN2B	AIN3A	AIN3B	J19	J20		
1.	S.E.	S.E.	S.E.	S.E.	S.E.	S.E.	1-2	2-3	-	-
2.	S.E.	P.Diff.	S.E.	S.E.	-	S.E.	2-3	2-3	R86	R12
3.	P.Diff.	S.E.	S.E.	S.E.	-	S.E.	2-3	2-3	R41	R58
4.	S.E.	S.E.	S.E.	P.Diff.	S.E.	-	1-2	1-2	R109	R78
5.	S.E.	S.E.	P.Diff.	S.E.	S.E.	-	1-2	1-2	R51	R43
6.	S.E.	P.Diff.	P.Diff.	S.E.	-	-	2-3	1-2	R86 R51	R12 R43
7.	S.E.	P.Diff.	S.E.	P.Diff.	-	-	2-3	1-2	R86 R109	R12 R78
8.	P.Diff.	S.E.	S.E.	P.Diff.	-	-	2-3	1-2	R41 R109	R58 R78
9.	P.Diff.	S.E.	P.Diff.	S.E.	-	-	2-3	1-2	R41 R51	R58 R43
10.	S.E.	S.E.	P.Diff.	P.Diff.	S.E.	-	1-2	1-2	-	-
11.	P.Diff.	P.Diff.	S.E.	S.E.	-	S.E.	2-3	2-3	-	-
12.	S.E.	P.Diff.	P.Diff.	P.Diff.	-	-	2-3	1-2	R86	R12
13.	P.Diff.	S.E.	P.Diff.	P.Diff.	-	-	2-3	1-2	R41	R58
14.	P.Diff.	P.Diff.	S.E.	P.Diff.	-	-	2-3	1-2	R109	R78
15.	P.Diff.	P.Diff.	P.Diff.	S.E.	-	-	2-3	1-2	R51	R43
16.	P.Diff.	P.Diff.	P.Diff.	P.Diff.	-	-	2-3	1-2	-	-

Table 1. Analog Input Configuration Jumper and Resistor Settings

Notes:

1. Use headers J7 and J11 to select input signal ground reference (in pseudo-differential mode) as either the CDB42L56 board ground or the signal ground reference from the external system which the CDB42L56 receives through the shield of the analog input cable.
2. Resistor modifications are only required if single-ended and pseudo-differential input configurations need to be used simultaneously on the “A” and “B” inputs of the same analog input channel.
3. Resistor population settings for resistors not shown in the table should be the same as factory defaults.

Figure 35 on page 28 illustrates how the analog inputs are connected and routed. Table 3 on page 19 details the jumper selections.

1.11 Analog Outputs

The CS42L56 analog outputs can be monitored on RCA jacks J15 and J17 for line and J37 and J38 for headphone outputs. Additionally, the CS42L56 headphone outputs can also be monitored on stereo headphone jack J1 which also allows the user to test the CS42L56’s headphone detect functionality. The CDB42L56 on-board circuitry drives the headphone detect pin low when a headphone is inserted in J1.

Headers J12 and J4 can be used to select optional 16 Ω or 32 Ω resistive loads for headphone outputs. Headers J2 and J3 give users the option of receiving filtered or unfiltered outputs on the RCA headphone output jacks.

Figure 35 on page 28 illustrates how the analog outputs are connected and routed. Table 3 on page 19 provides details on jumper selections for filtered or unfiltered outputs.

2. QUICK-START GUIDE

The following figure is a simplified quick-start guide made for user convenience. The guide configures the board with a 1.8 V power supply to VLDO, VA and VCP and a 3.3 V power supply to VL. The user may choose from steps 7 through 10 depending on the desired measurement. Refer to Section 3 on page 9 for details on how the various components on the board interface with each other in different board configuration modes. Refer to Section 4 on page 11 for descriptions on control settings in the Cirrus FlexGUI software.

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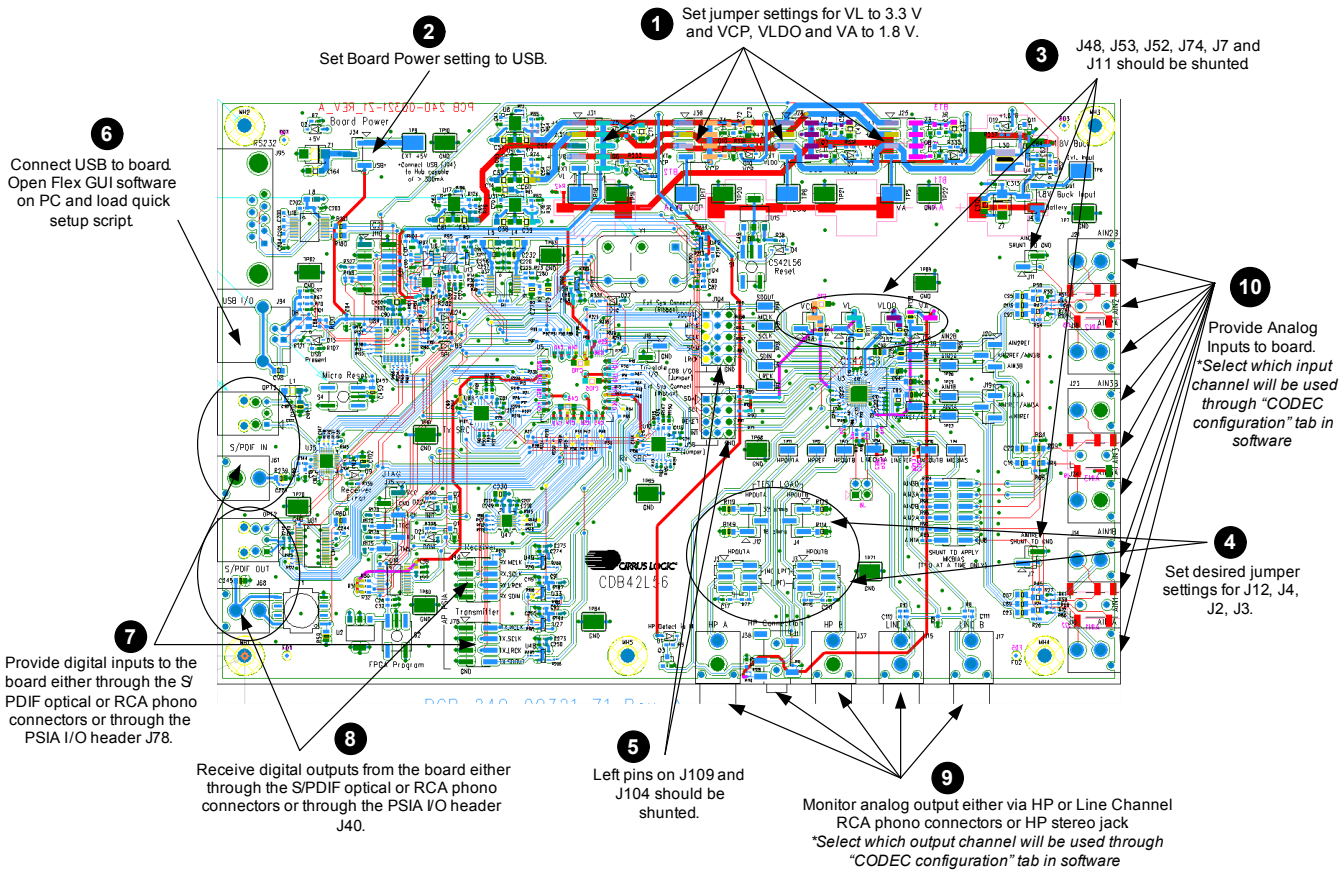


Figure 1. Quick-Start Board Layout

3. CONFIGURATION OPTIONS

This section shows two common configurations of the CDB42L56.

3.1 S/PDIF In to Analog Out and Analog In to S/PDIF Out

The CS42L56 ADC and DAC performance can be tested by loading the **"SPDIF In to Analog Out -- Analog In to S/PDIF Out"** quick setup file provided with the software package. The script configures the digital clock and data signal routing on the board as shown in Figure 2. The quick setup scripts provided in the software assume that a 24.000 MHz on-board oscillator is populated in Y1.

A S/PDIF input must be provided as the S/PDIF Tx (CS8406) uses the RMCK signal from the S/PDIF Rx (CS8416) for synchronization in this configuration, as shown in the Figure 2.

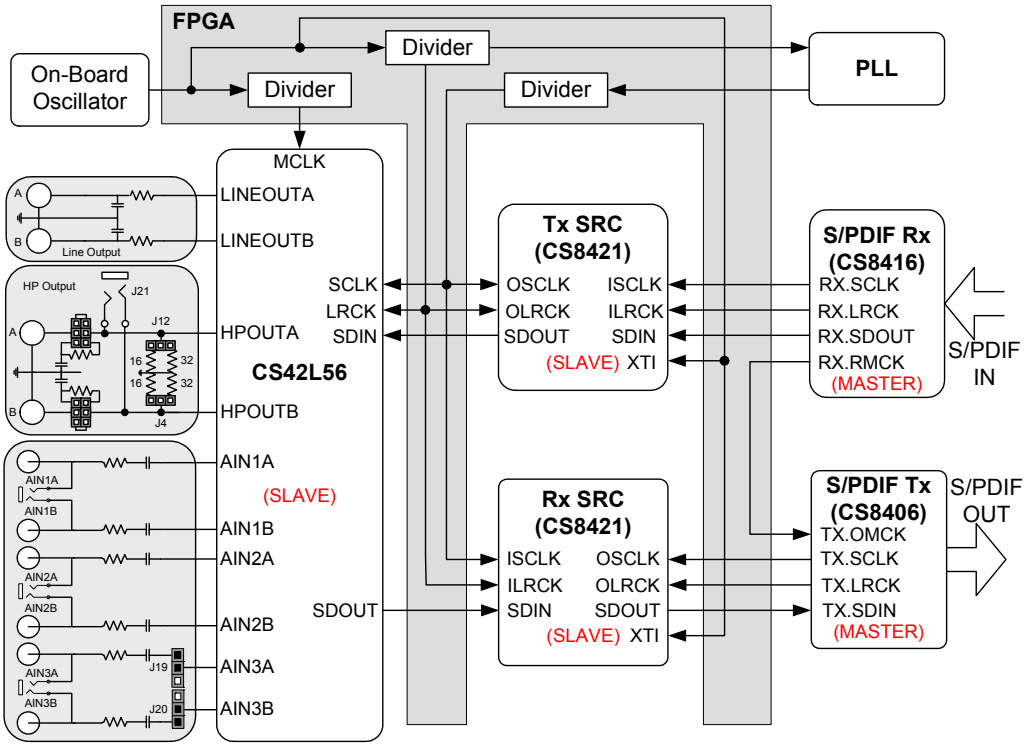


Figure 2. S/PDIF In to Analog Out and Analog In to S/PDIF Out

3.2 PSIA In to Analog Out and Analog In to PSIA Out

The CS42L56 ADC and DAC performance can be tested by loading the **"PSIA In to Analog Out -- Analog In to PSIA Out"** quick setup file provided with the software package. The script configures the digital clock and data signal routing on the board as shown in Figure 2. The quick setup scripts provided in the software assume that a 24.000 MHz on-board oscillator is populated in Y1.

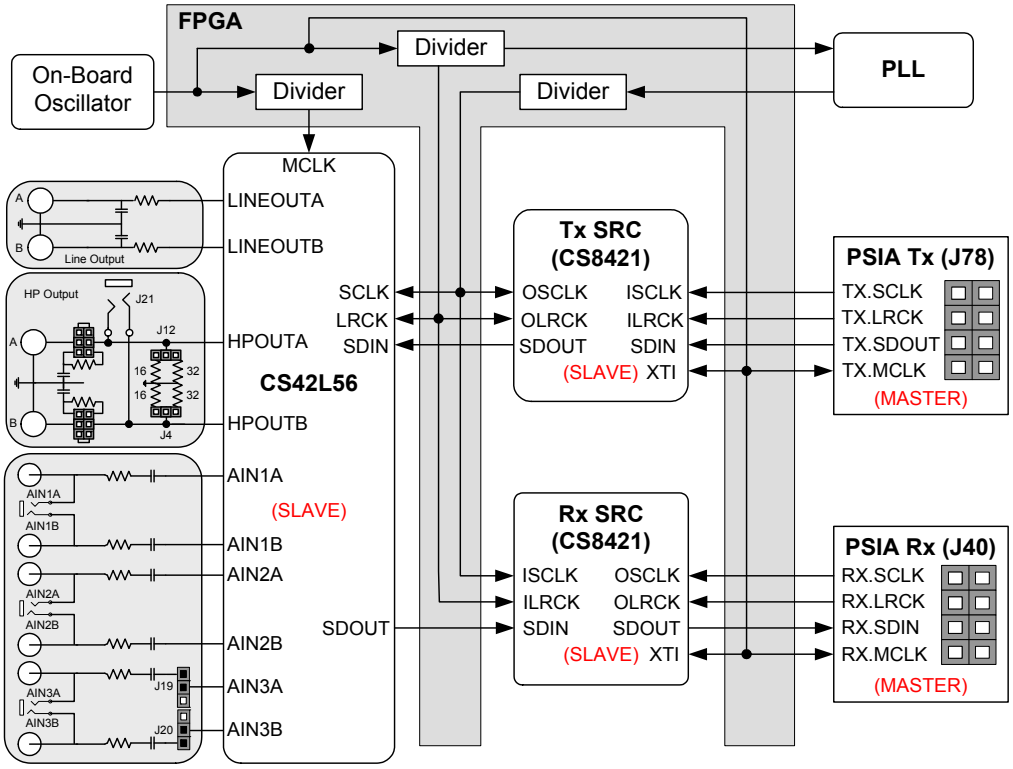


Figure 3. PSIA In to Analog Out and Analog In to PSIA Out

4. SOFTWARE MODE CONTROL

The CDB42L56 may be used with the Microsoft® Windows®-based FlexGUI graphical user interface, allowing software control of the CS42L56, FPGA, CS8421, CS8416 and CS8406 registers. The latest control software may be downloaded from www.cirrus.com/msasoftware. Step-by-step instructions for setting up the FlexGUI are provided as follows:

1. Download and install the FlexGUI software as instructed on the web site.
2. Connect the CDB to the host PC using a USB cable.
3. Launch the Cirrus FlexGUI. *Once the GUI is launched successfully, all registers are set to their default reset state.*
4. Refresh the GUI by clicking on the “Update” button. *The default state of all registers are now visible.*

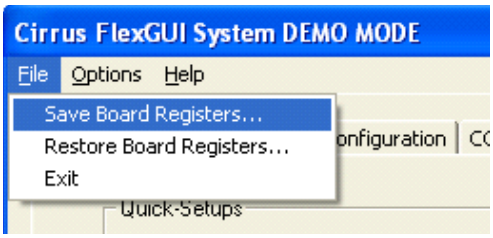
For standard set-up:

5. Set up the signal routing in the “Board Configuration” tab as desired.
6. Set up the CS42L56 in the “Codec Configuration”, “Codec Analog Input Volume”, “Codec DSP Engine”, “Codec Analog Output Volume” and “Register Maps” tabs as desired.
7. Begin evaluating the CS42L56.

For quick set-up, the CDB42L56 may, alternatively, be configured by loading a predefined sample script file:

8. On the File menu, click "Restore Board Registers..."
9. Browse to Boards\CDB42L56\Scripts\.
10. Choose any one of the provided scripts to begin evaluation.

To create personal scripts files:



11. On the File menu, click “Save Board Registers...”
12. Enter any name that sufficiently describes the created setup.
13. Choose the desired location and save the script.
14. To load this script, follow the instructions from step 8 above.

4.1 Board Configuration Tab

The “Board Configuration” tab provides high-level control of signal routing on the CDB42L56. The controls in this tab are used to setup the CS8416, CS8406, Tx SRC, Rx SRC and the FPGA routing and are divided into separate control groups for each of these individual devices. A description of each control group is outlined below. This tab also includes a drop down menu with a list of quick-setup configurations. Selecting a quick-setup from the drop down box, the software loads a predefined configuration for the different devices on the board. Section 3 on page 9 provides details on some quick-setup configurations.

FPGA Routing - Includes controls to setup the FPGA for using the S/PDIF or the PSIA test interface and for setting up clock and signal routing for CS42L56 in master/slave mode. This group also has controls for selecting SCLK and LRCK frequencies, perform divide operations on the oscillator.

CS8416 S/PDIF Receiver Control - Controls for the CS8416.

CS8406 S/PDIF Transmitter Control - Controls for the CS8406.

CS8421 SRC Control - Controls for the receive and transmit SRCs. To configure, select the desired SRC from the drop down menu and then click the update button.

Update - Reads all registers in the FPGA, CS42L56, CS8416, CS8406 and CS8421 and shows the current values in the GUI.

Reset - Resets FPGA to default routing configuration.

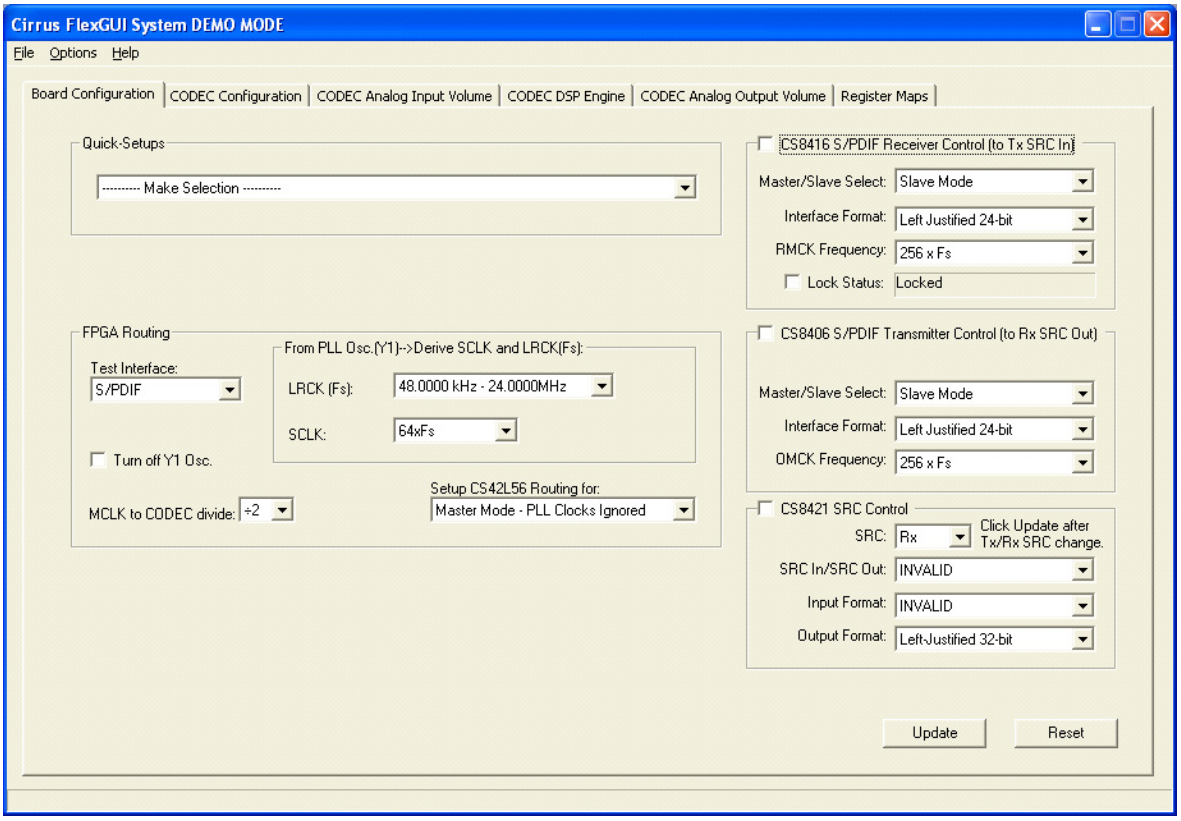


Figure 4. Board Configuration Tab

4.2 Codec Configuration Tab

The “Codec Configuration” tab provides high-level control of the CS42L56 register settings. Status text detailing the CS42L56’s specific configuration is shown in parenthesis or appears directly below the associated control. This text will change depending on the setting of the associated control. A description of each control group is outlined below. See the CS42L56 data sheet for complete register descriptions.

Power Control - Controls for powering all devices.

ADC Input Configuration - Controls for input configuration and routing/mixing.

Serial Port Configuration - Controls for all settings related to the serial I/O data and clocks on the board.

Status - Displays status of interrupt bits.

Update - Reads all registers in the CS42L56 and reflects the current values in the GUI.

Reset - Resets the CS42L56.

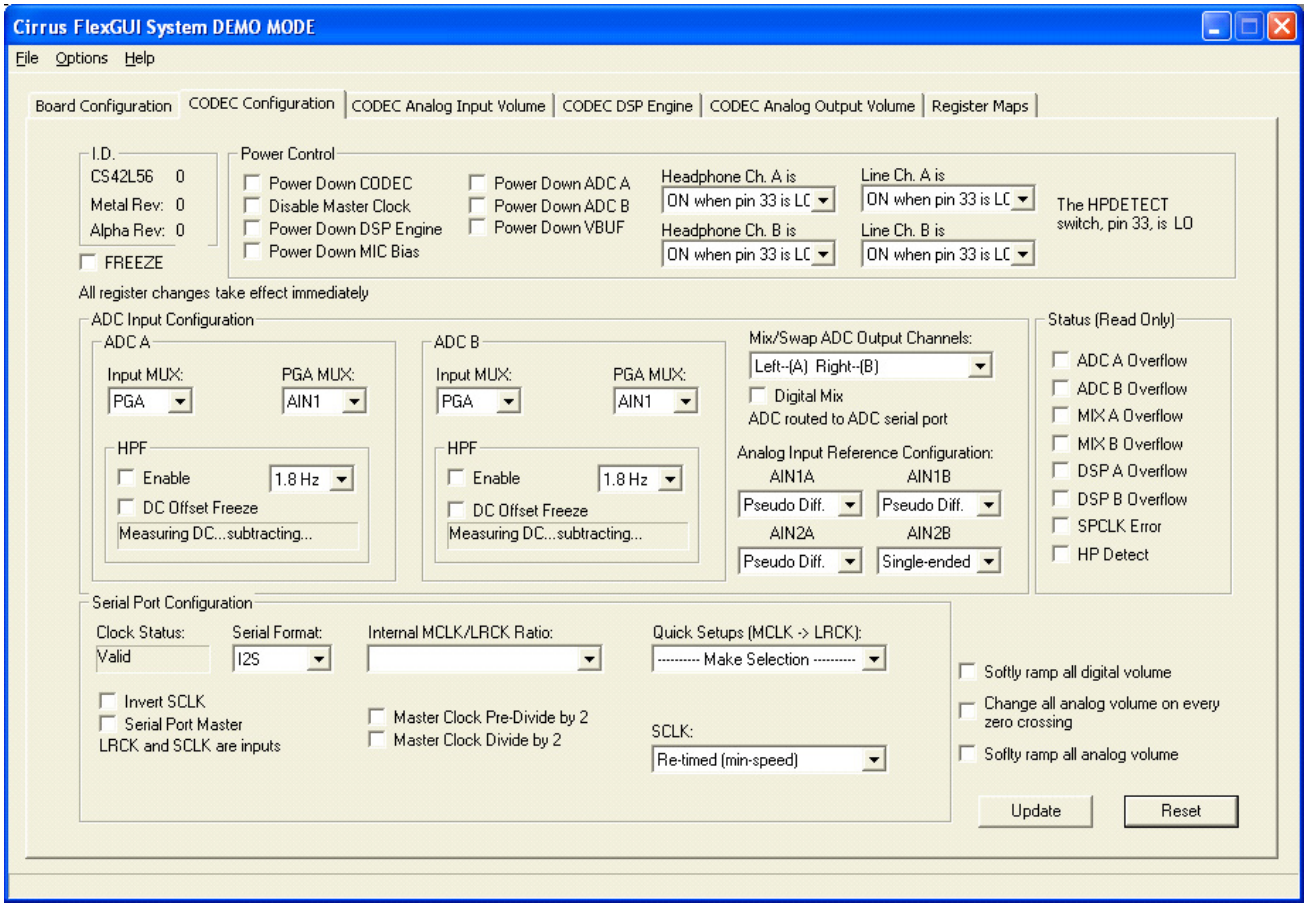


Figure 5. Codec Configuration Tab

4.3 Codec Analog Input Volume Tab

The “Codec Analog Input Volume” tab provides high-level control of all volume settings in the ADC of the CS42L56. Status text detailing the CS42L56’s specific configuration is shown in parenthesis or inside the control group of the affected control. This text will change depending on the setting of the associated control. A description of each control group is outlined below.

Digital Volume Control - Digital volume controls and adjustments (ADC output).

ALC Configuration - Configuration settings for the Automatic Level Control (ALC).

Analog Volume Control - Analog volume controls and adjustments for the PGA and MIC amps.

Noise Gate Configuration - Configuration settings for the noise gate.

Update - Reads all registers in the CS42L56 and reflects the current values in the GUI.

Reset - Resets the CS42L56.

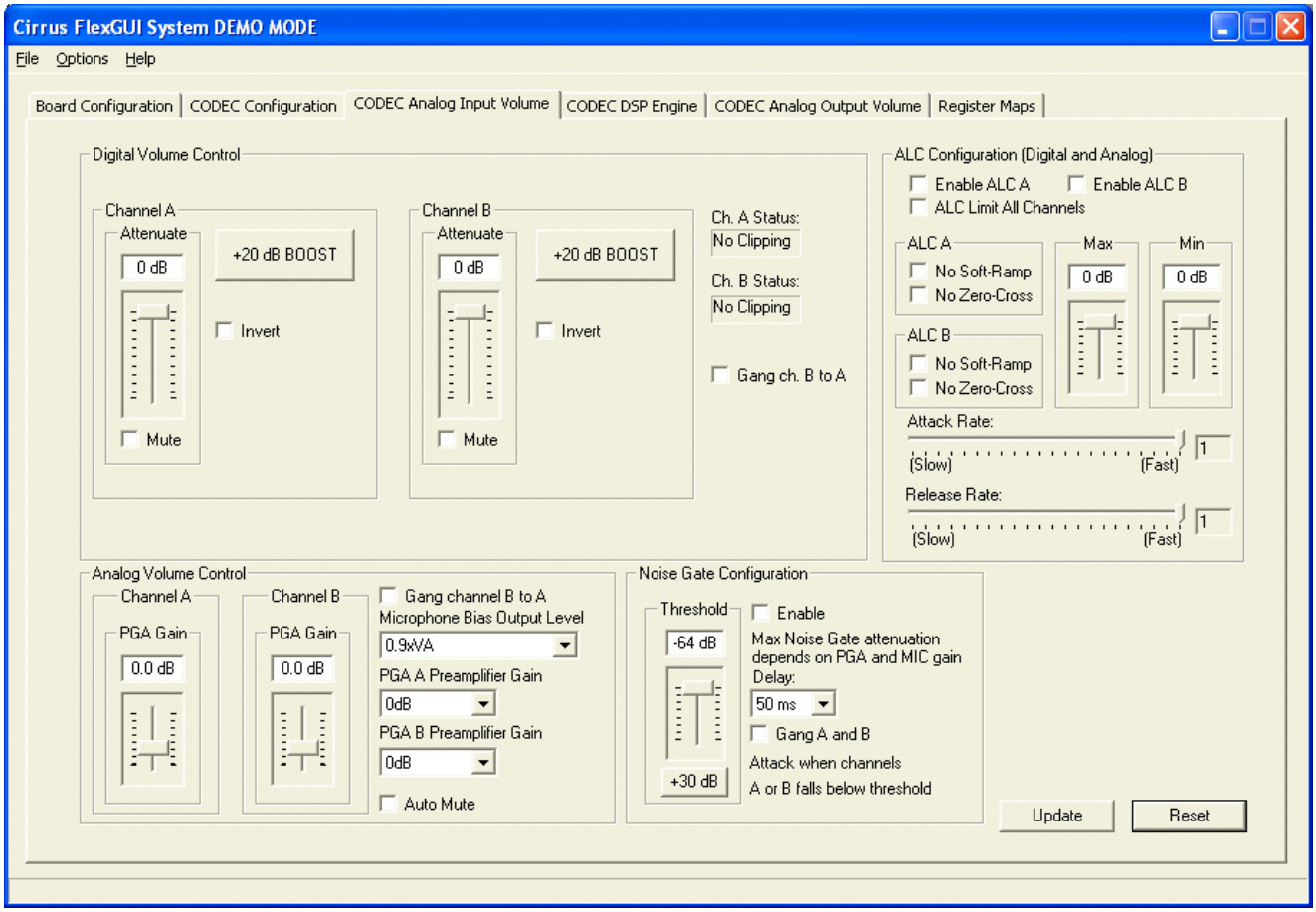


Figure 6. Codec Analog Input Volume Tab

4.4 Codec DSP Engine Tab

The “Codec DSP Engine” tab provides high-level control functions to modify the SDIN (PCM) data volume level, the ADC output/SDIN mix volume level, the Tone Control and the Beep Generator. Status text detailing the CS42L56’s specific configuration is shown inside the control group of the affected control. This text will change depending on the setting of the associated control. A description of each control group is outlined below.

Digital Volume Control - Controls for mutes or inverts and the volume/gain of the ADC mix or the PCM mix.

Tone Control - Controls for the corner frequencies and the volume/gain of the treble and bass shelving filters.

Beep Generator - Controls for setting the on/off time, frequency, volume, mix and repeat beep functions.

Update - Reads all registers in the CS42L56 and reflects the current values in the GUI.

Reset - Resets the CS42L56.

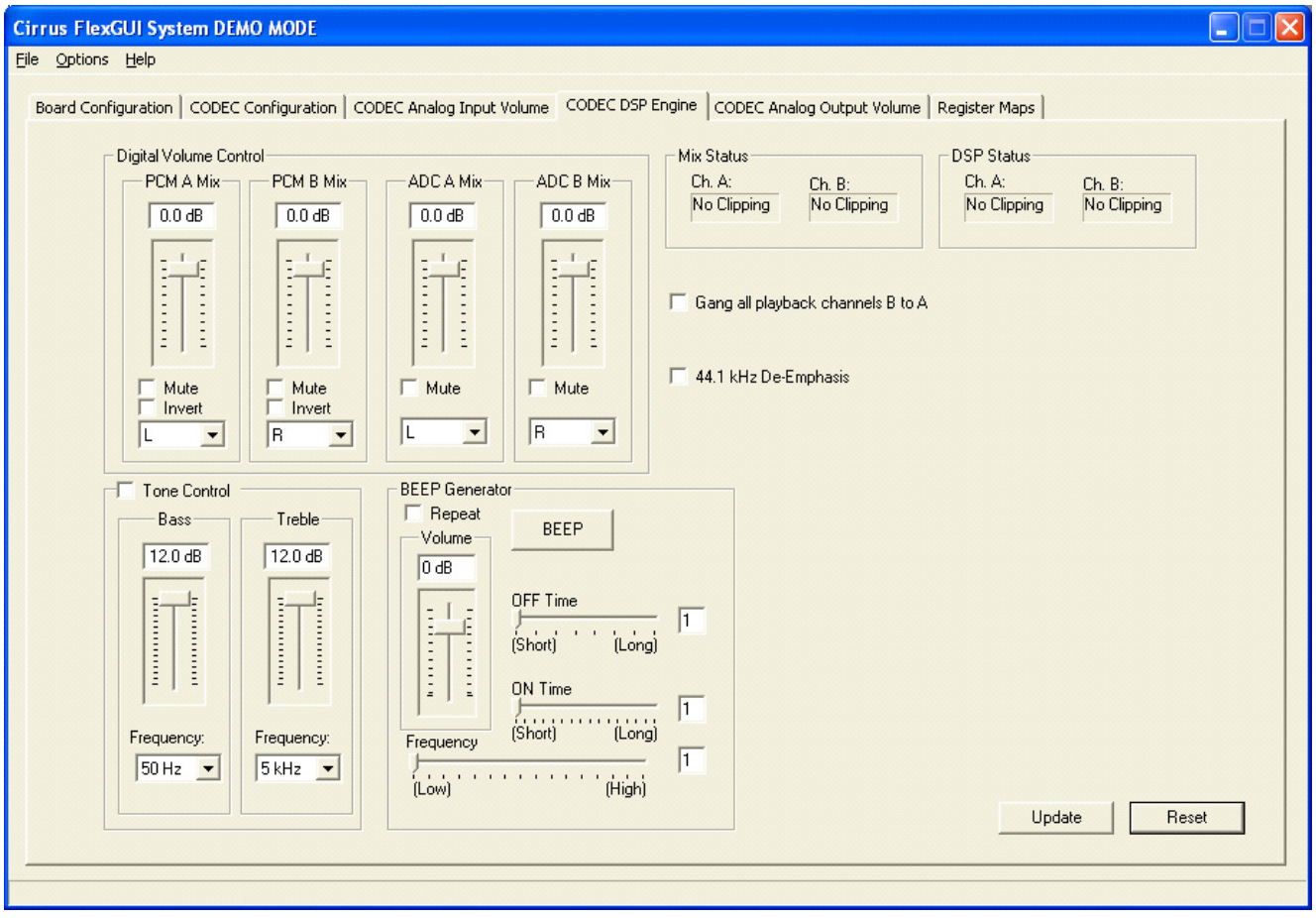


Figure 7. Codec DSP Engine Tab

4.5 Codec Analog Output Volume Tab

The “Codec Analog Output Volume” tab provides high-level control of the CS42L56 class H output amplifier, HP/Line output volume levels, charge pump frequency, DAC channel limiter, and overall master volume level. A description of each control group is outlined below.

Class H Controls - Controls for defining the digital and analog advisory volume, charge pump frequency, and adaptive power supply mode for the class H control to determine the appropriate power supply for the HP/Line amplifiers.

Headphone/Line Amplifiers - Controls for configuring mutes and for setting the volume of the signal from the headphone/line amplifier and controls for the HP/Line mux.

Limiter - Configuration settings for the peak detect and limiter in the CS42L56.

Master Volume Control - Sets the volume of the signal out of the DSP.

Update - Reads all registers in the CS42L56 and reflects the current values in the GUI.

Reset - Resets the CS42L56.

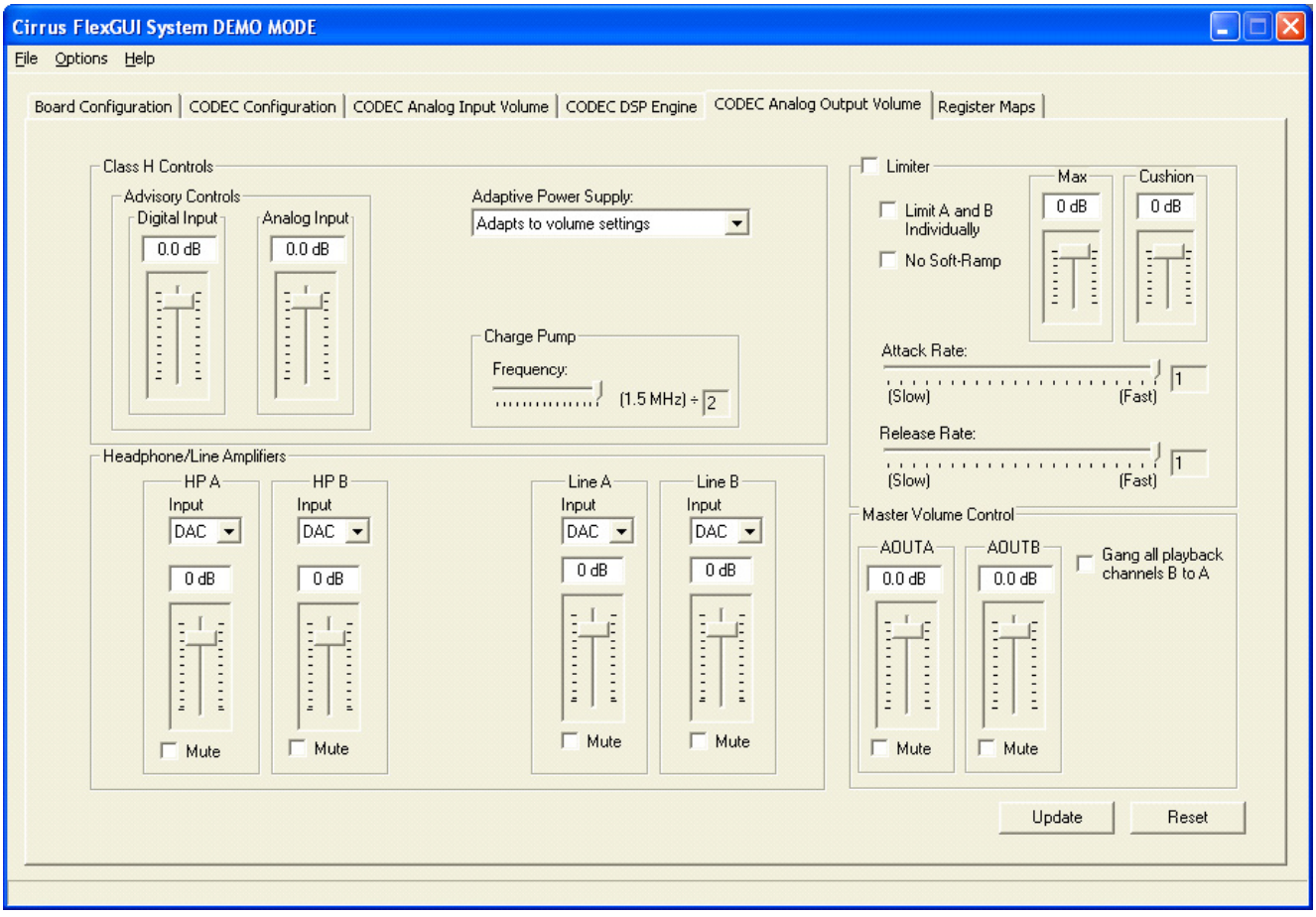


Figure 8. Codec Analog Output Volume Tab

4.6 Register Maps Tab

The Register Maps tab provides low-level control of the CS42L56, CS8416, CS8406, CS8421, FPGA and GPIO register settings. Register values can be modified bit-wise or byte-wise. “Left-clicking” on a particular register accesses that register and shows its contents at the bottom. The user can change the register contents by using the push-buttons, by selecting a particular bit and typing in the new bit value or by selecting the register in the map and typing in a new hex value.

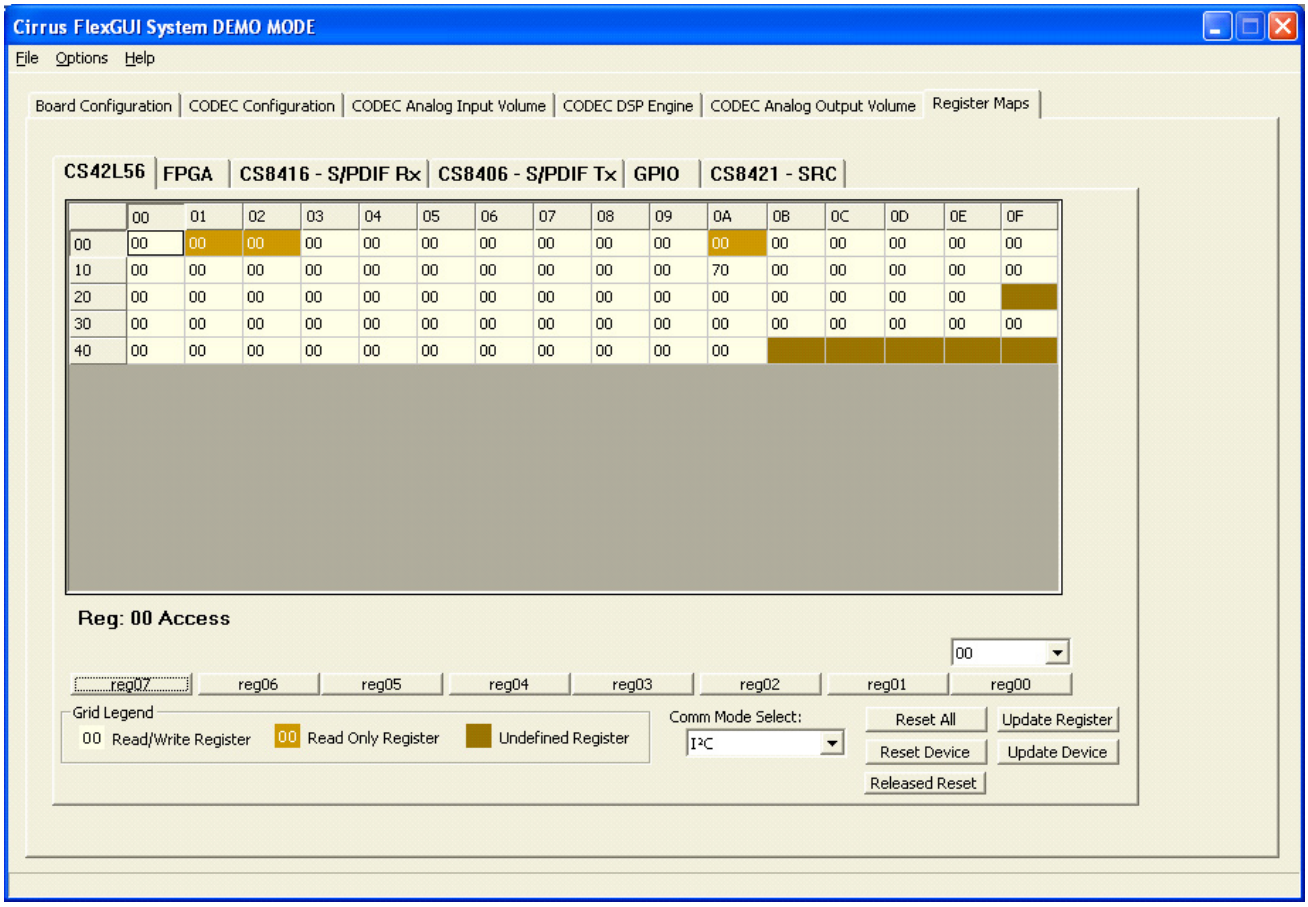


Figure 9. Register Maps Tab - CS42L56

5. JUMPER SETTINGS AND SYSTEM CONNECTIONS

CONNECTOR	REF	INPUT/OUTPUT	SIGNAL PRESENT
EXT. +5V	TP9	Input	+5V power supply for evaluation board
GND	TP10	Input	GND reference from power supply
Ext. Input	TP6	Input	+4.5V external power supply for buck converter
GND	TP7	Input	GND reference from power supply
AAA	BT1 BT2 BT3	Input Input Input	Socket for +1.5 V AAA batteries for buck converter
RS232	J95	Input/Output	RS232 serial port connection to PC for I²C control port signals
USB I/O	J94	Input/Output	USB connection to PC for I²C control port signals
S/PDIF Optical IN	OPT3	Input	CS8416 digital audio input via optical cable
S/PDIF Optical OUT	OPT2	Output	CS8406 digital audio output via optical cable
S/PDIF COAX IN	J61	Input	CS8416 digital audio input via coaxial cable
S/PDIF COAX OUT	J68	Output	CS8406 digital audio input via coaxial cable
MICRO RESET	S4	Input	Reset for microcontroller (U84)
CS42L56 RESET	S1	Input	Reset for CS42L56 (U3)
FPGA Program	S2	Input	Reload Xilinx program into the FPGA from Flash (U14)
FPGA JTAG	J75	Input/Output	I/O for programming the FPGA (U5)
MICRO JTAG	J110	Input/Output	I/O for programming the microcontroller (U84)
AP PSIA Transmitter	J78	Input/Output	Digital Data and Clocks to CS42L56
AP PSIA Receiver	J40	Input/Output	Digital Data and Clocks from CS42L56
AIN1B AIN1A AIN2B AIN2A AIN3B AIN3A	J14 J10 J21 J18 J23 J24	Input Input Input Input Input Input	RCA connectors for analog inputs to CS42L56
AIN1 AIN2 AIN3	J22 J13 J9	Input Input Input	Stereo jacks for analog inputs to CS42L56
HP Channel A HP Channel B	J38 J37	Output Output	RCA connector for headphone analog output from CS42L56
Line Channel A Line Channel B	J15 J17	Output Output	RCA connector for line analog output from CS42L56
HP Stereo Connection	J1	Output	Stereo jack for headphone stereo output from CS42L56
Oscillator	Y1	Input	Oscillator for providing master clock for system timing
I/O Header	J104	Input/Output	I/O for Clocks and Data
S/W CONTROL	J109	Input/Output	I/O for external I²C control port signals
Test Points	TP1-TP2, TP34-TP36, TP11-TP16, TP23, TP25, TP26, TP28	Outputs	Test Points for monitoring signals to and from CS42L56

Table 2. System Connections

JMP	LABEL	PURPOSE	POSITION	FUNCTION SELECTED
J31	VL	Selects source of voltage for the VL supply	*+1.8V	Voltage source is +1.8 V regulator.
			+2.5V	Voltage source is +2.5 V regulator.
			+3.3V	Voltage source is +3.3 V regulator.
			+1.8VB	Voltage source is +1.8 V from battery.
			EXT. VL	Voltage source from TP18.
J36	VCP	Selects source of voltage for the VCP supply	*+1.8V	Voltage source is +1.8 V regulator.
			+2.5V	Voltage source is +2.5 V regulator.
			+1.8VB	Voltage source is +1.8V from battery.
			EXT. VCP	Voltage source from TP17.
J25	VA	Selects source of voltage for the VA supply	*+1.8V	Voltage source is +1.8 V regulator.
			+2.5V	Voltage source is +2.5 V regulator.
			+1.8VB	Voltage source is +1.8 V from battery.
			EXT. VA	Voltage source from TP5.
J28	VLDO	Selects source of voltage for the VLDO supply	*+1.8V	Voltage source is +1.8 V regulator.
			+2.5V	Voltage source is +2.5 V regulator.
			+1.8VB	Voltage source is +1.8 V from battery.
			EXT. VLDO	Voltage source from TP8.
J52 J74 J53 J48	VLDO VA VL VCP	Current Measurement	*SHUNTED	1 Ω series resistor is shorted.
			OPEN	1 Ω series resistor in power supply path.
J11	Shunt to RCA	Provides RCA reference to GND	*SHUNTED	AIN2REF and RCAs for AIN2A and AIN2B given a board ground reference.
			OPEN	AIN2REF is given AIN2A and AIN2B ground reference on RCA shield.
J7	Shunt to RCA	Provides RCA reference to GND	*SHUNTED	AIN1REF and RCAs for AIN1A and AIN1B given a board ground reference.
			OPEN	AIN1REF is given AIN1A and AIN1B ground reference on RCA shield.
J5	1.8 V Buck Input	Selects power supply source for +1.8VB	1 - 2	1.8VB is derived from external input TP6.
			*2 - 3	1.8VB is derived from AAA batteries.
J19	AIN3A/AIN1REF Input	Selects input source for pin AIN3A/AIN1REF	*1 - 2	AIN3A/AIN1REF is given AIN3A input.
			2 - 3	AIN3A/AIN1REF is given AIN1 ground reference as input.
J20	AIN3B/AIN2REF Input	Selects input source for pin AIN3B/AIN2REF	*1 - 2	AIN3B/AIN2REF is given AIN3B input.
			2 - 3	AIN3B/AIN2REF is given AIN2 ground reference as input.
J6	SHUNT TO APPLY MICBIAS	Selects MICBIAS for analog inputs	1 - 3	MICBIAS applied to AIN1A.
			2 - 4	MICBIAS applied to AIN1B.
			5 - 6	MICBIAS applied to AIN2A.
			7 - 8	MICBIAS applied to AIN2B.
			9 - 10	MICBIAS applied to AIN3A.
			11 - 12	MICBIAS applied to AIN3B.
J12	HPOUTA	Selects test load from HPOUTA	1 - 2	32 Ω load selected for HPOUTA.
			*2 - 3	16 Ω load selected for HPOUTA.
J4	HPOUTB	Selects test load from HPOUTB	1 - 2	32 Ω load selected for HPOUTB.
			*2 - 3	16 Ω load selected for HPOUTB.

Table 3. Jumper Settings

J2	HPOUTA FLT/NOFLT	Selects filtered or unfiltered output for HPOUTA	*2 - 4, *1 - 3	Unfiltered output selected for HPOUTA.
			4 - 6, 3 - 5	RC filtered output selected for HPOUTA.
J3	HPOUTB FLT/NOFLT	Selects filtered or unfiltered output for HPOUTB	*2 - 4, *1 - 3	Unfiltered output selected for HPOUTB.
			4 - 6, 3 - 5	RC filtered output selected for HPOUTB.
J34	Board Power	Selects source of Board Power	1 - 2	Board powered from external +5 V source connected to TP9/TP10.
			*2 - 3	Board powered from USB.
J16	Tri-state I/O	Tri-states FGPA I/O	SHUNTED	FGPA I/O pins are tri-stated.
			*OPEN	FGPA I/O pins in normal operation.

*Default factory settings

Table 3. Jumper Settings

6. PERFORMANCE PLOTS

Test conditions (unless otherwise specified): T_A = 25°C; VA=VCP=VLDO=VL=1.8 V; input test signal is a full-scale 997 Hz sine wave; dB values relative to full-scale output; measurement bandwidth 20 Hz to 20 kHz (un-weighted); Sample Frequency = 48 kHz; +2 dB analog gain for Line Output path; -4 dB analog gain for Headphone Output path; Headphone test load: R_L = 16 Ω; no LPF option for Headphone Output path.

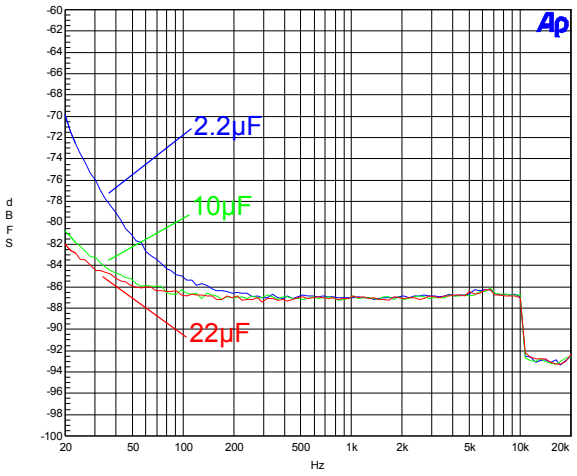


Figure 10. THD+N vs. Freq. - Analog In to Digital Out

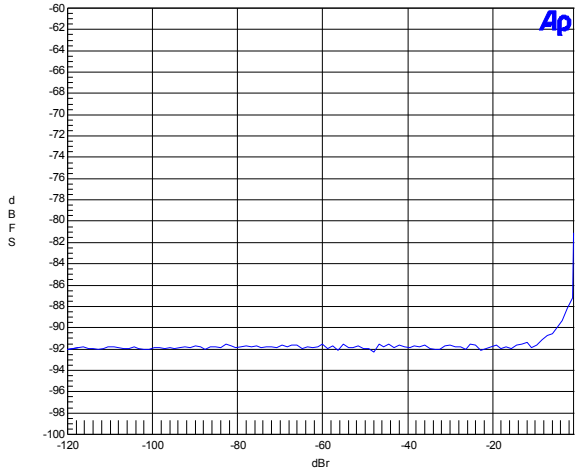


Figure 11. THD+N vs. Amplitude - Analog In to Digital Out

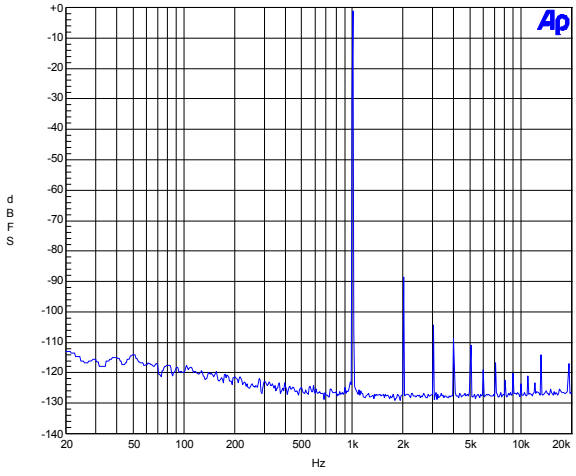


Figure 12. FFT - Analog In to Digital Out @ -1 dBFS

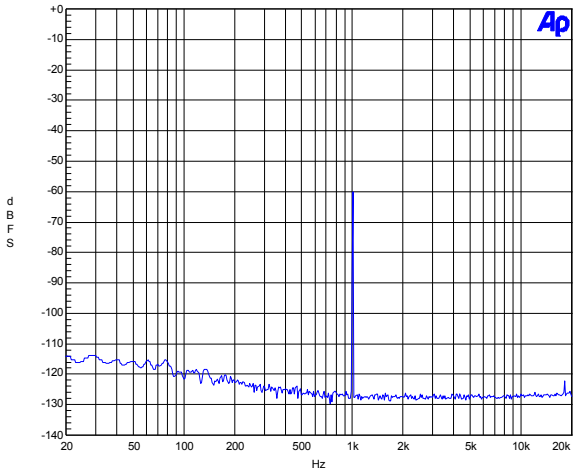


Figure 13. FFT - Analog In to Digital Out @ -60 dBFS

Note: The total harmonic distortion + noise (THD+N) performance of the ADC in the CS42L56 is determined by the value of the capacitor on the FILT+ pin. Larger capacitor values yield significant improvement in THD+N at low frequencies. Fig. 10 shows the THD+N vs. frequency performance measured with several FILT+ capacitor values.

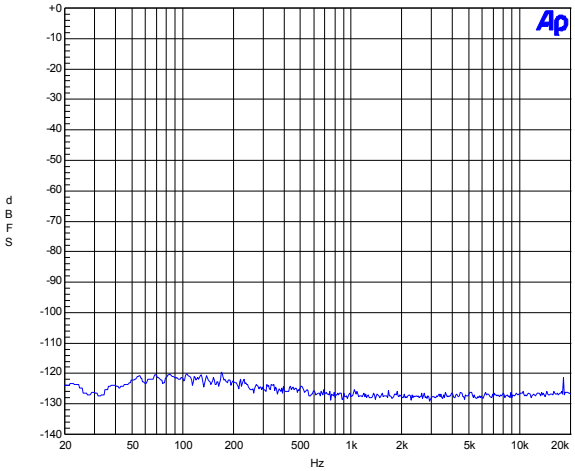


Figure 14. FFT - Analog In to Digital Out - No Input

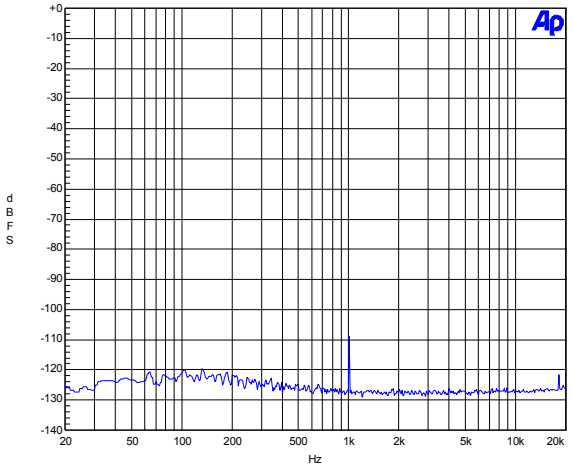


Figure 15. FFT Crosstalk - Analog In to Digital Out @ -1 dBFS

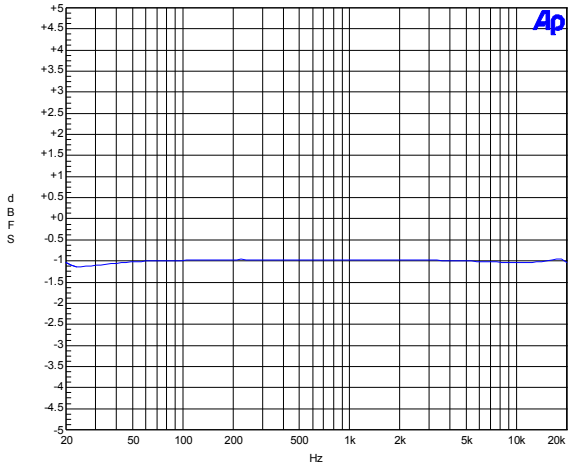


Figure 16. Freq. Response - Analog In to Digital Out

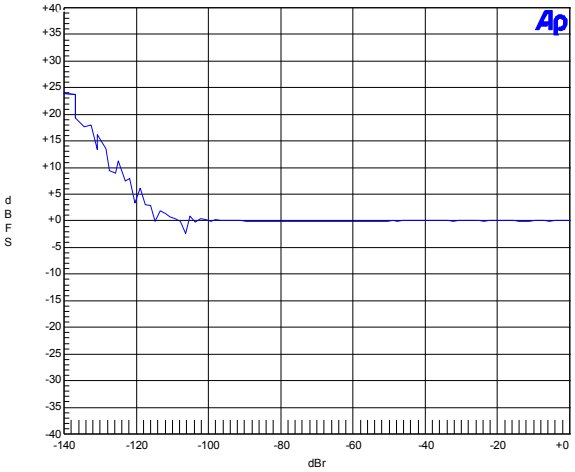


Figure 17. Fade-to-Noise Linearity - Analog In to Digital Out

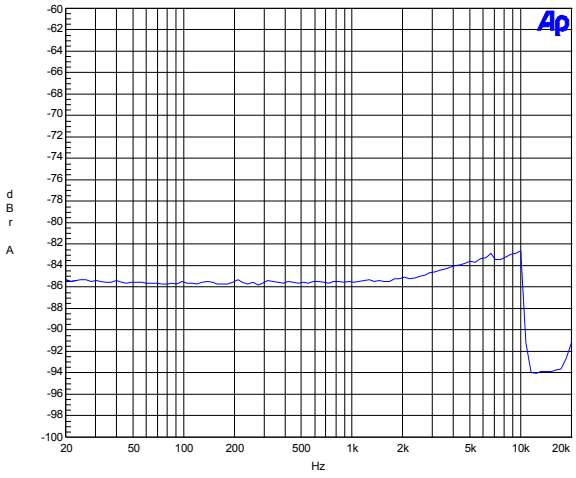


Figure 18. THD+N vs. Freq. - Digital In to HP Out

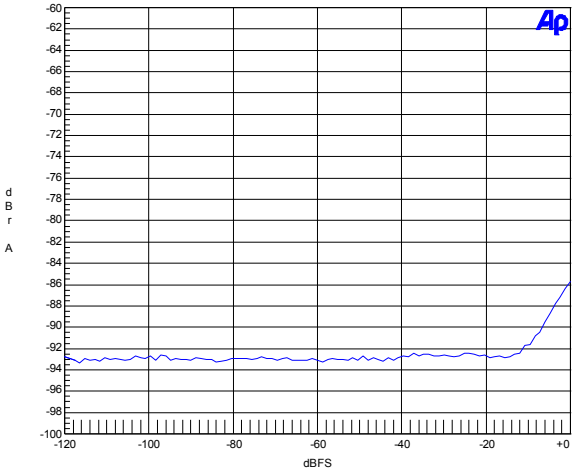


Figure 19. THD+N vs. Amplitude - Digital In to HP Out

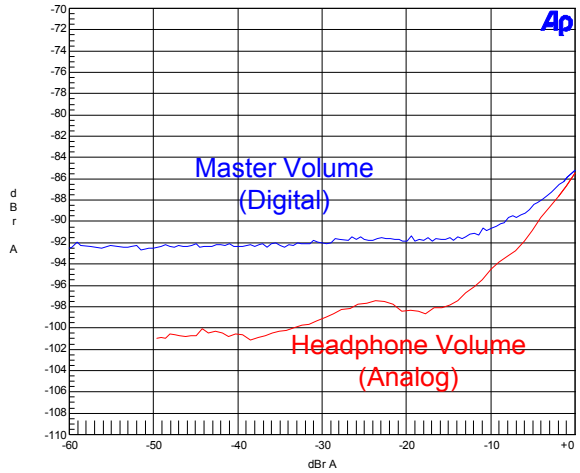


Figure 20. THD+N vs. Volume - Digital In to HP Out

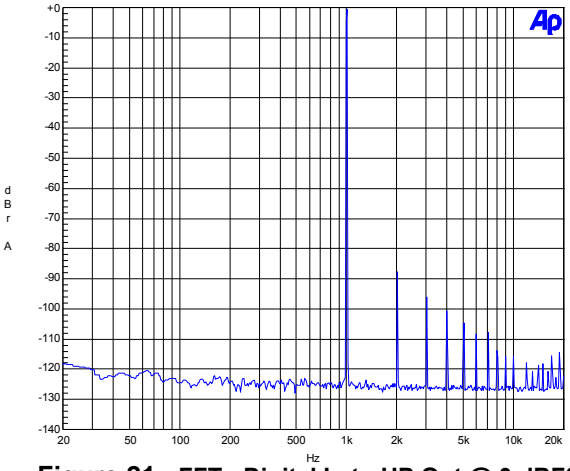


Figure 21. FFT - Digital In to HP Out @ 0 dBFS

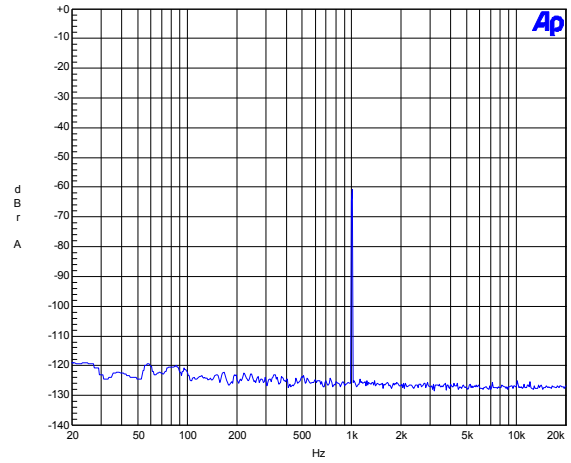


Figure 20. FFT - Digital In to HP Out @ -60 dBFS

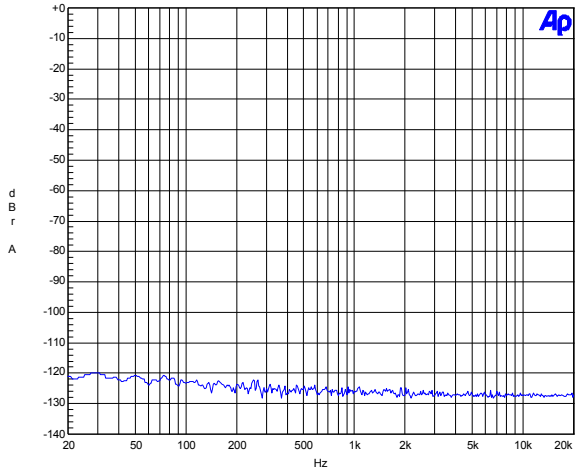


Figure 21. FFT - Digital In to HP Out - No Input

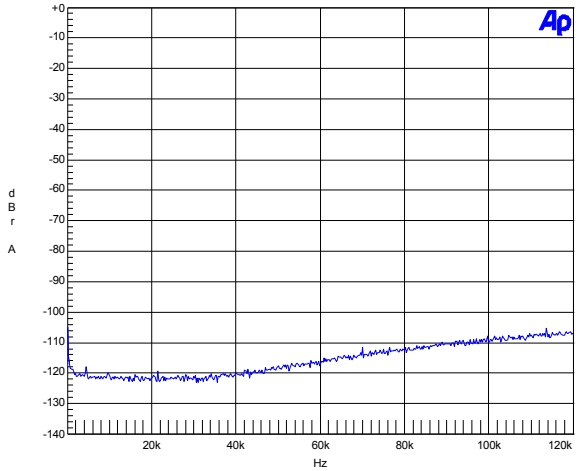


Figure 22. FFT - Digital In to HP Out - No Input Wideband

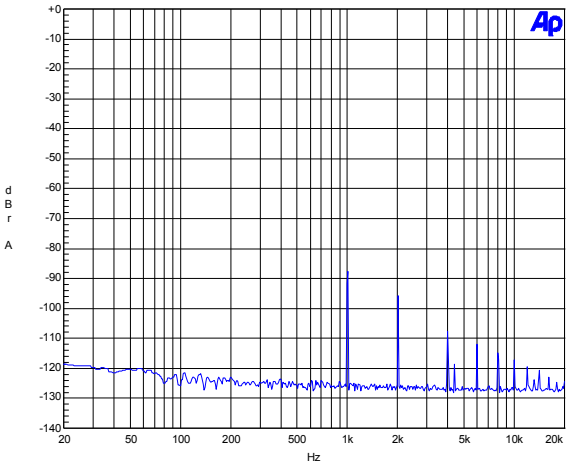


Figure 23. FFT Crosstalk - Digital In to HP Out @ 0 dBFS

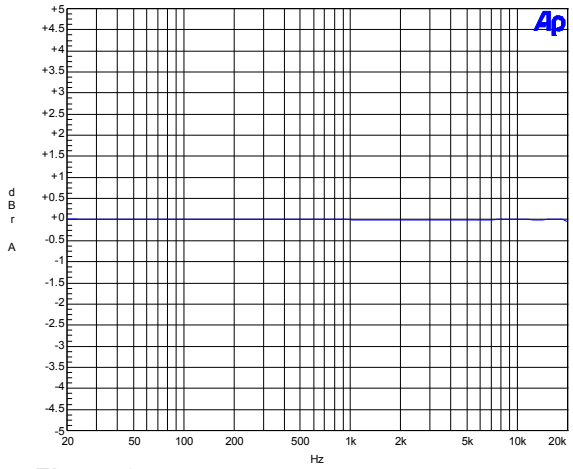


Figure 24. Freq. Response - Digital In to HP Out

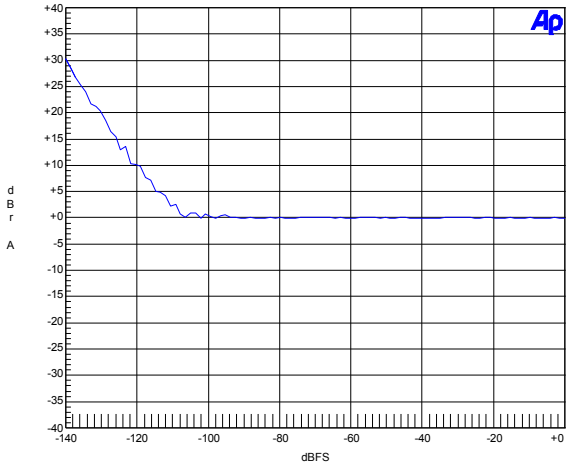


Figure 25. Fade-to-Noise Linearity- Digital In to HP Out

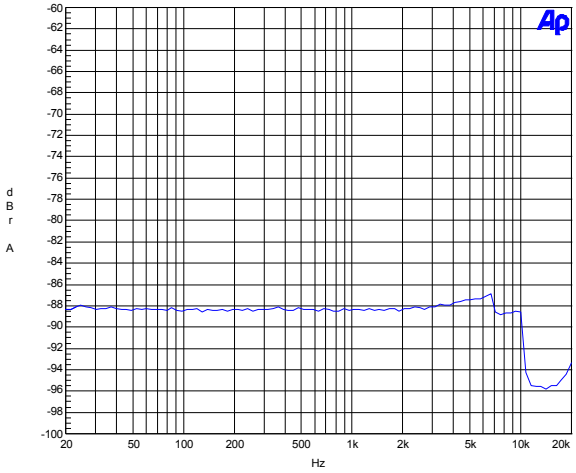


Figure 26. THD+N vs. Freq. - Digital In to Line Out

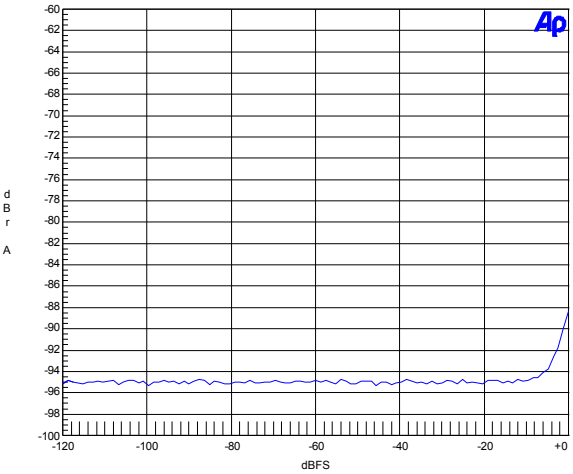


Figure 27. THD+N vs. Amplitude - Digital In to Line Out

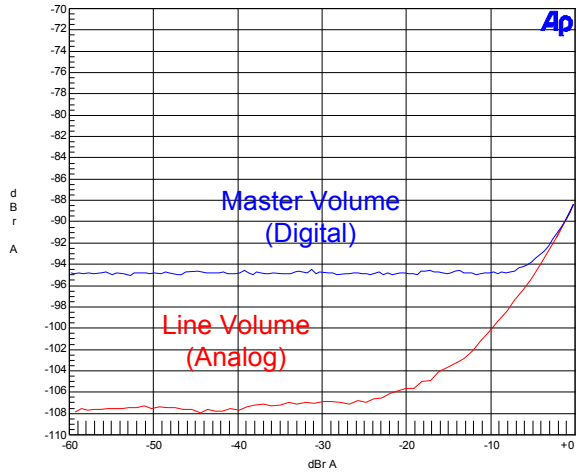


Figure 28. THD+N vs. Volume - Digital In to Line Out

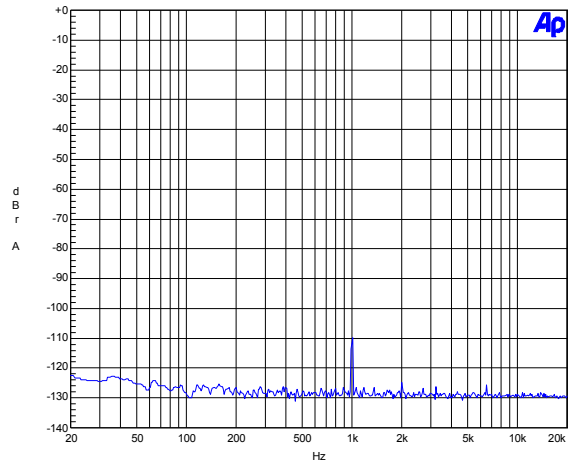


Figure 29. FFT Crosstalk - Digital In to Line Out @ 0 dBFS

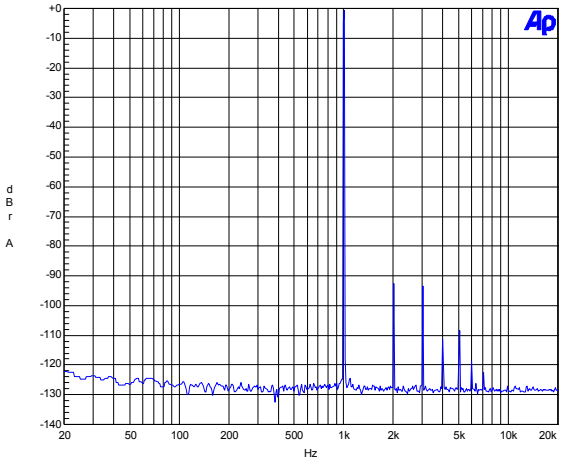


Figure 28. FFT - Digital In to Line Out @ 0 dBFS

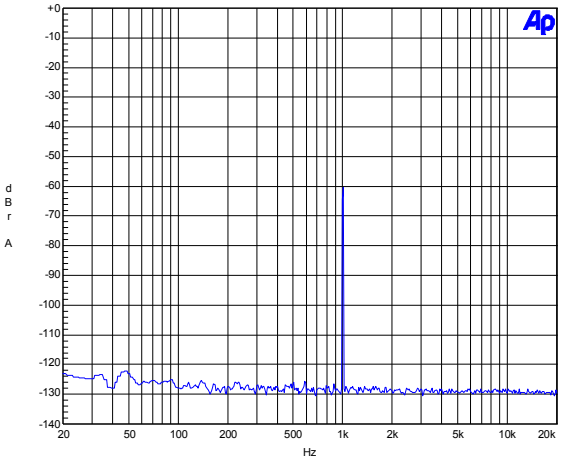


Figure 29. FFT - Digital In to Line Out @ -60 dBFS

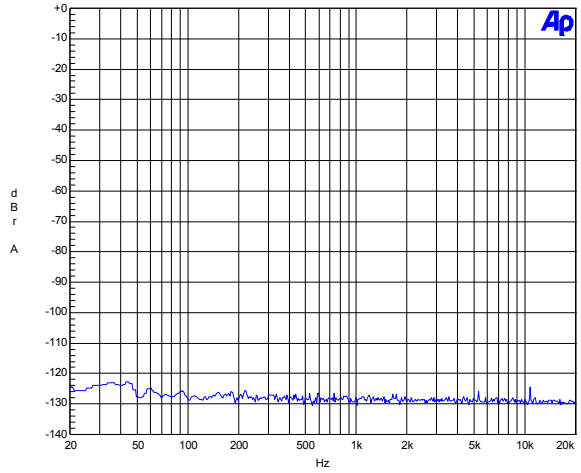


Figure 30. FFT - Digital In to Line Out - No Input

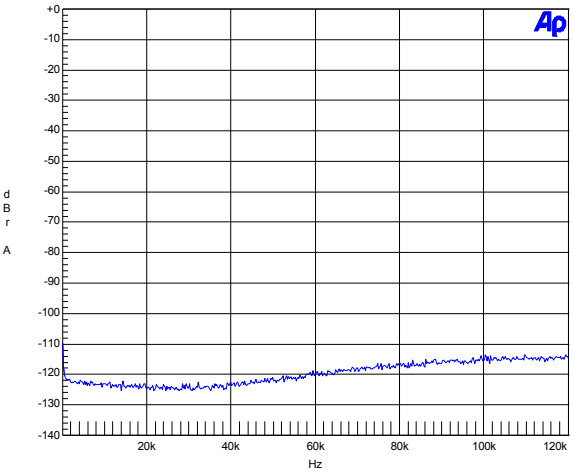


Figure 31. FFT - Digital In to Line Out - No Input Wideband

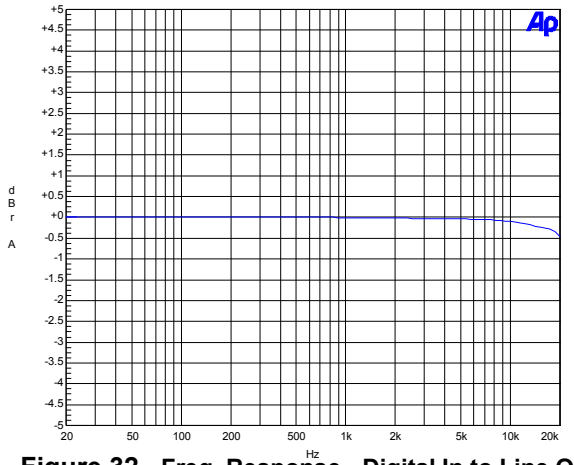


Figure 32. Freq. Response - Digital In to Line Out

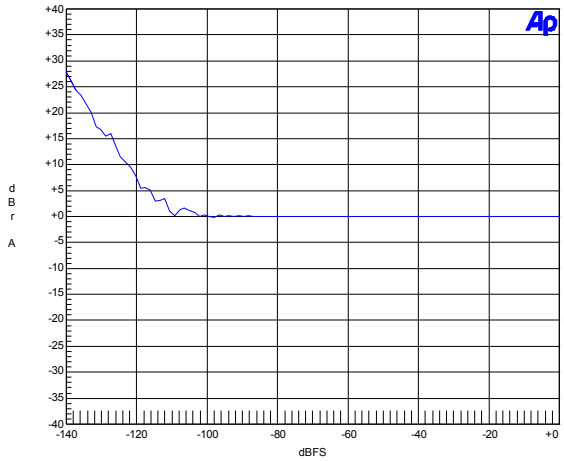


Figure 33. Fade-to-Noise Linearity- Digital In to Line Out

7. CDB42L56 BLOCK DIAGRAM

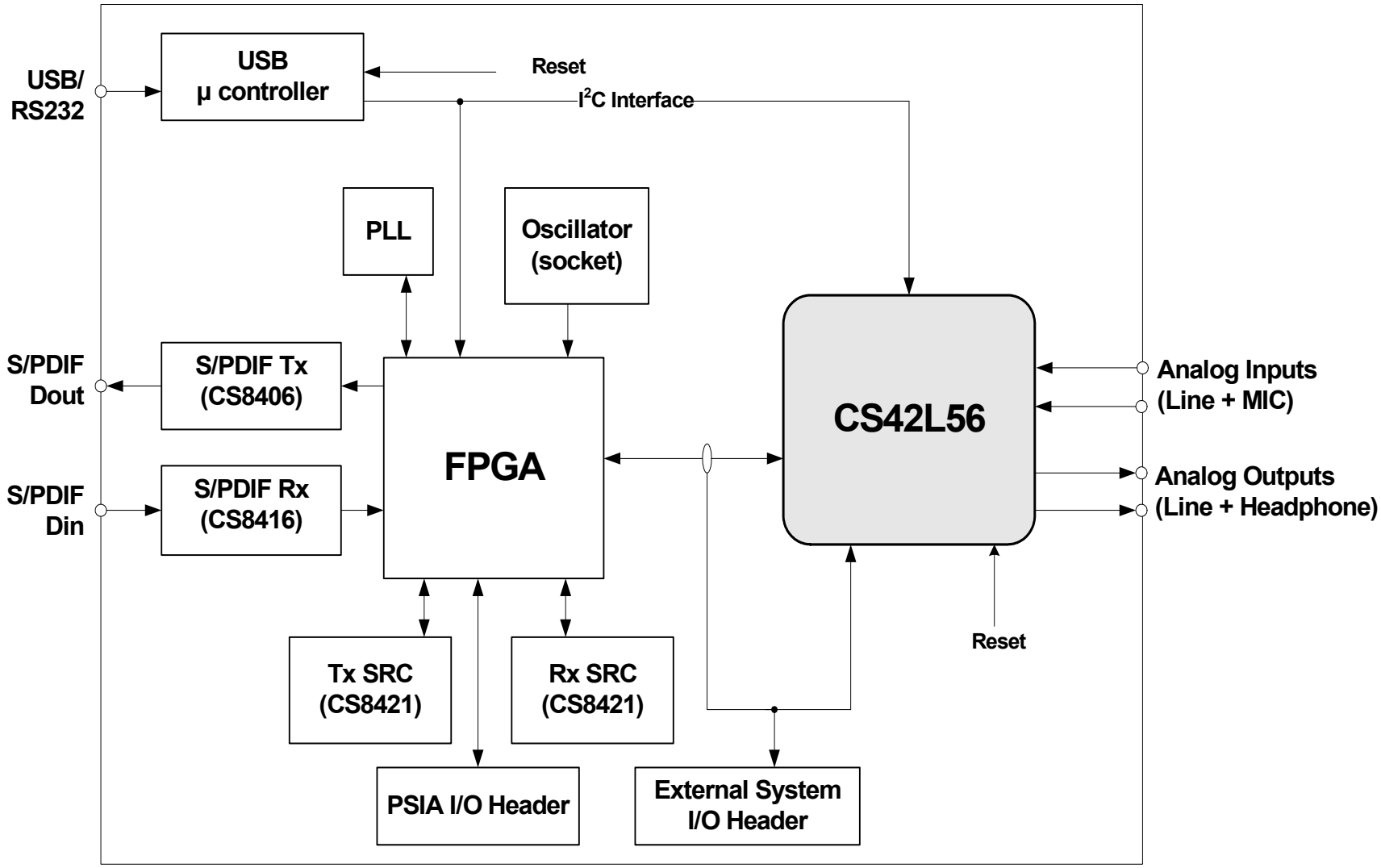
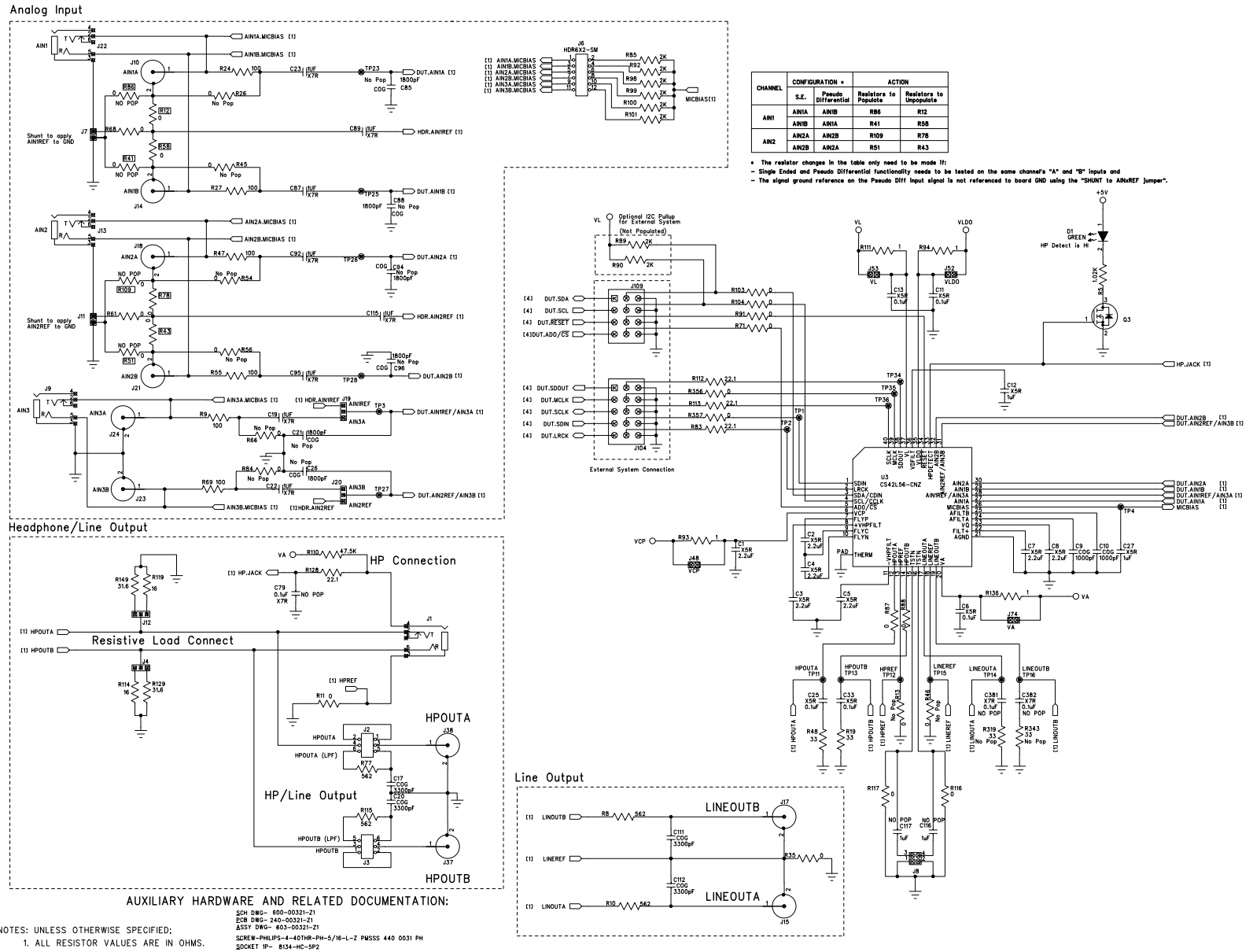


Figure 34. Block Diagram

8. CDB42L56 SCHEMATICS



CHANNEL	CONFIGURATION *		ACTION	
	S.E.	Pseudo Differential	Resistors to Populate	Resistors to Unpopulate
AIN1	AIN1A	AIN1B	RB6	R12
	AIN1B	AIN1A	R41	R58
AIN2	AIN2A	AIN2B	R109	R78
	AIN2B	AIN2A	R51	R43

* The resistor changes in the table only need to be made if:
– Single Ended and Pseudo Differential functionality needs to be tested on the same channel's "A" and "B" inputs and
– The signal ground reference on the Pseudo Diff input signal is not referenced to board GND using the "SHUNT to AINxREF jumper".

Figure 35. CS42L56 & Analog I/O (Schematic Sheet 1)

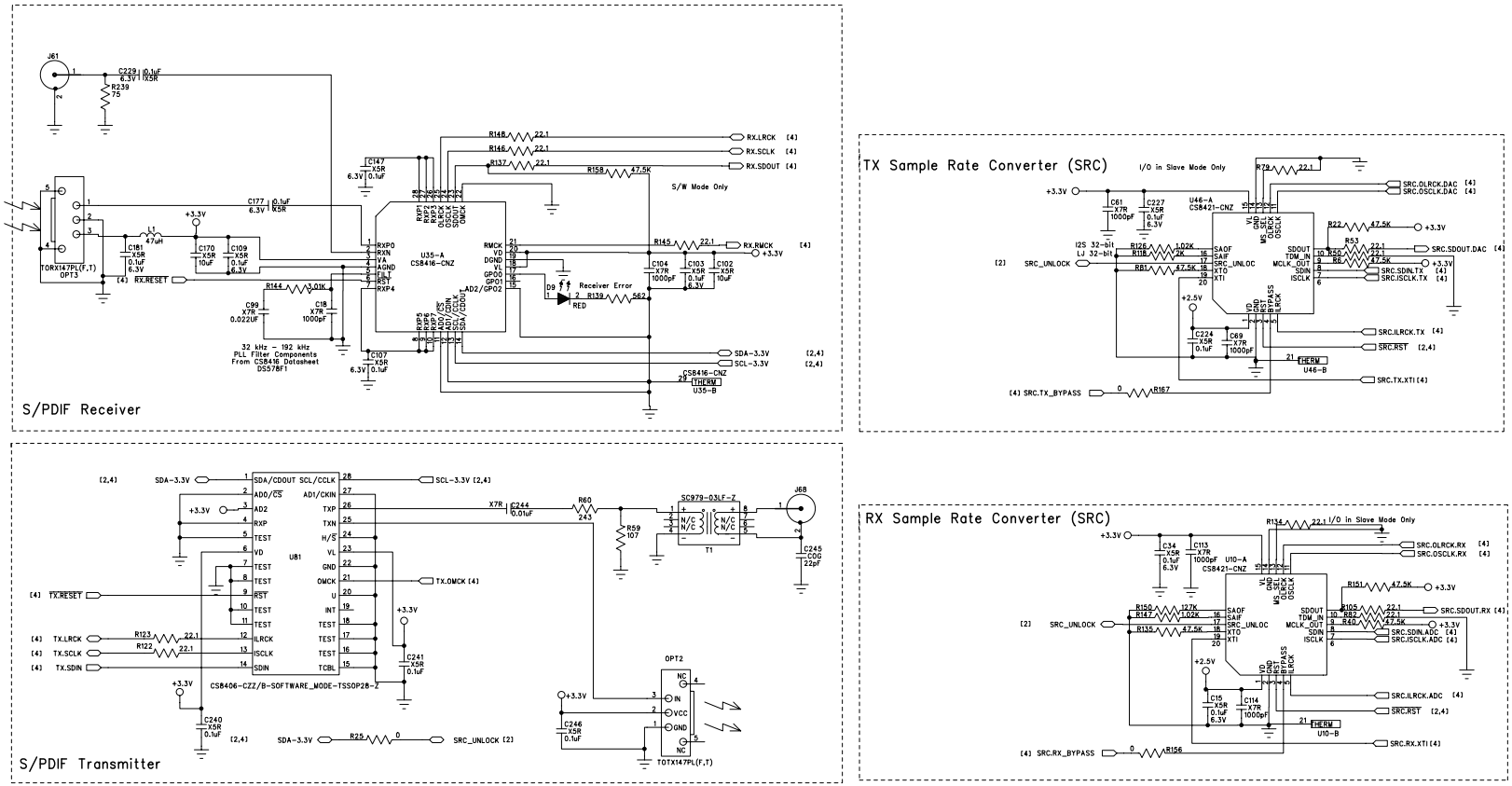


Figure 36. S/PDIF & Digital Interface (Schematic Sheet 2)

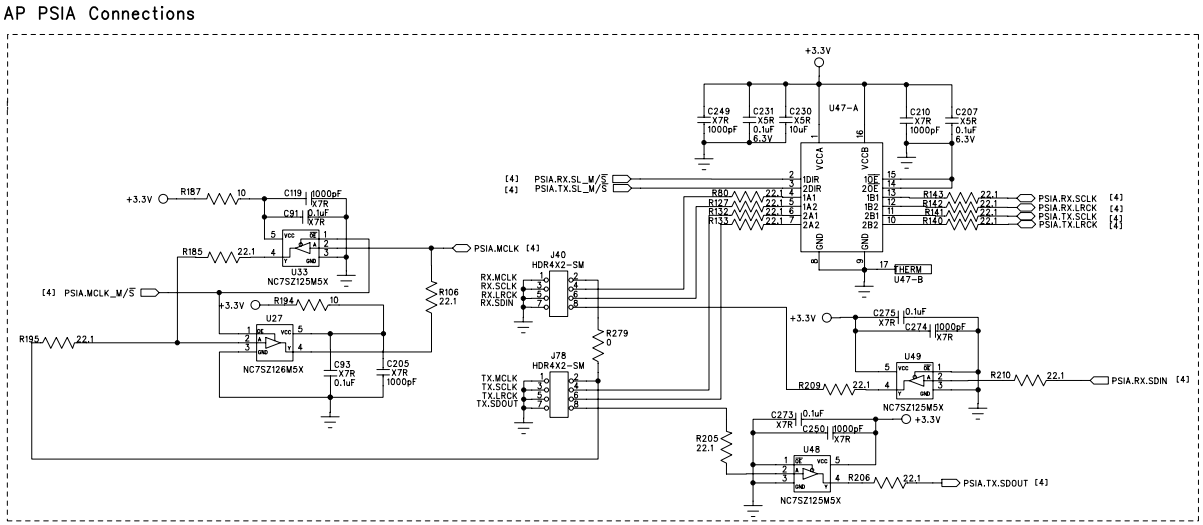


Figure 37. PLL, oscillator and external I/O connections (Schematic Sheet 3)

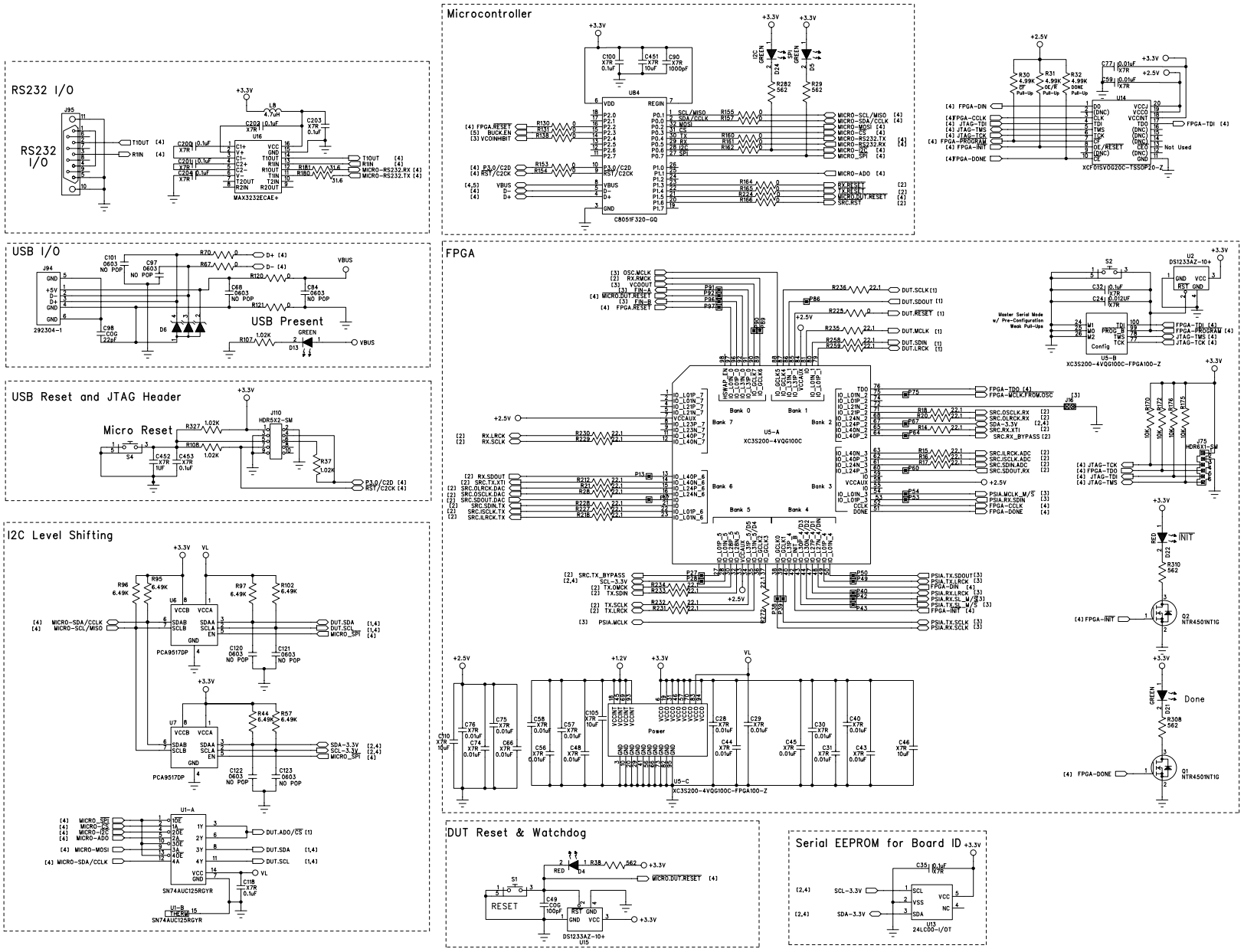


Figure 38. Microcontroller and FPGA (Schematic Sheet 4)

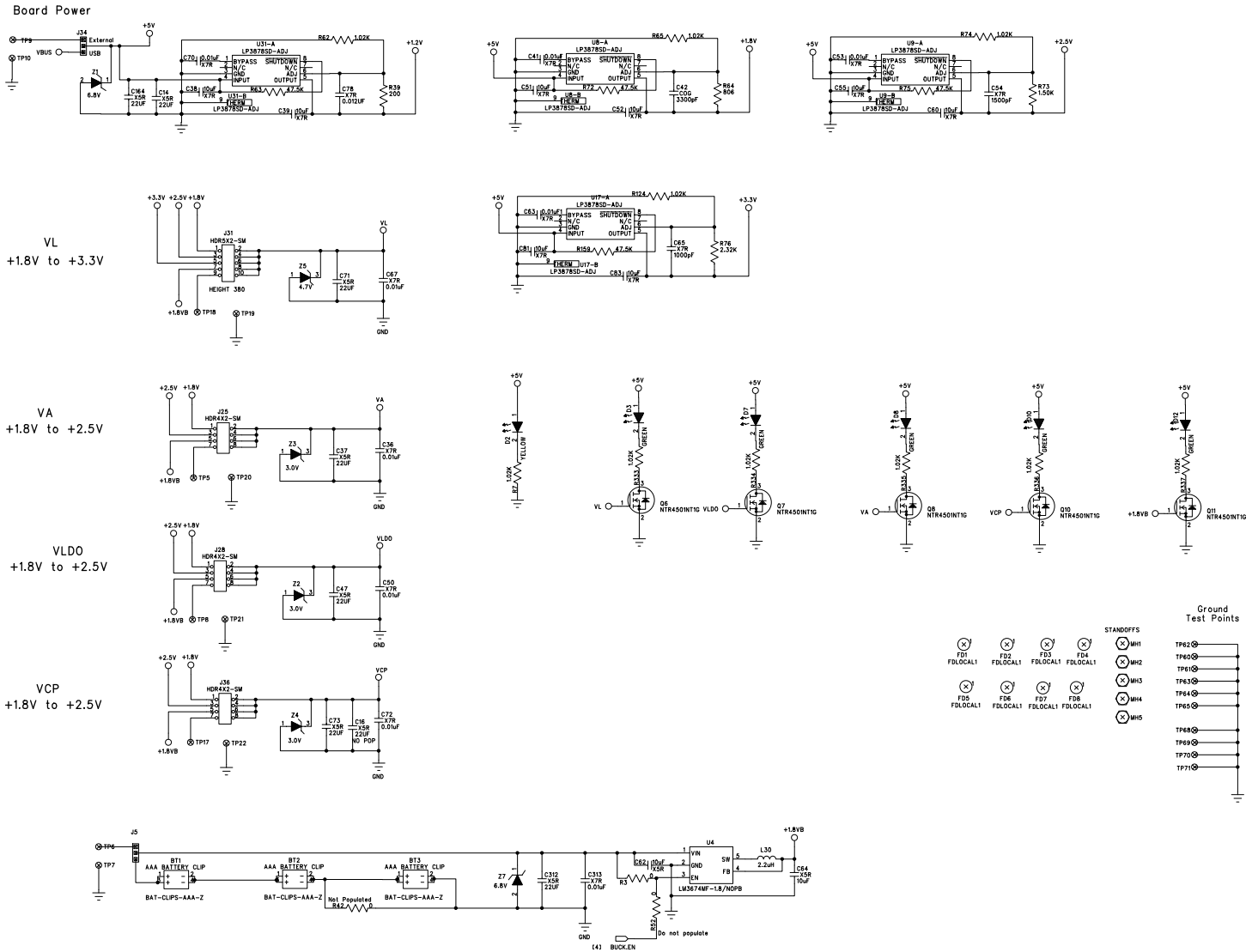


Figure 39. Power (Schematic Sheet 5)

9. CDB42L56 LAYOUT

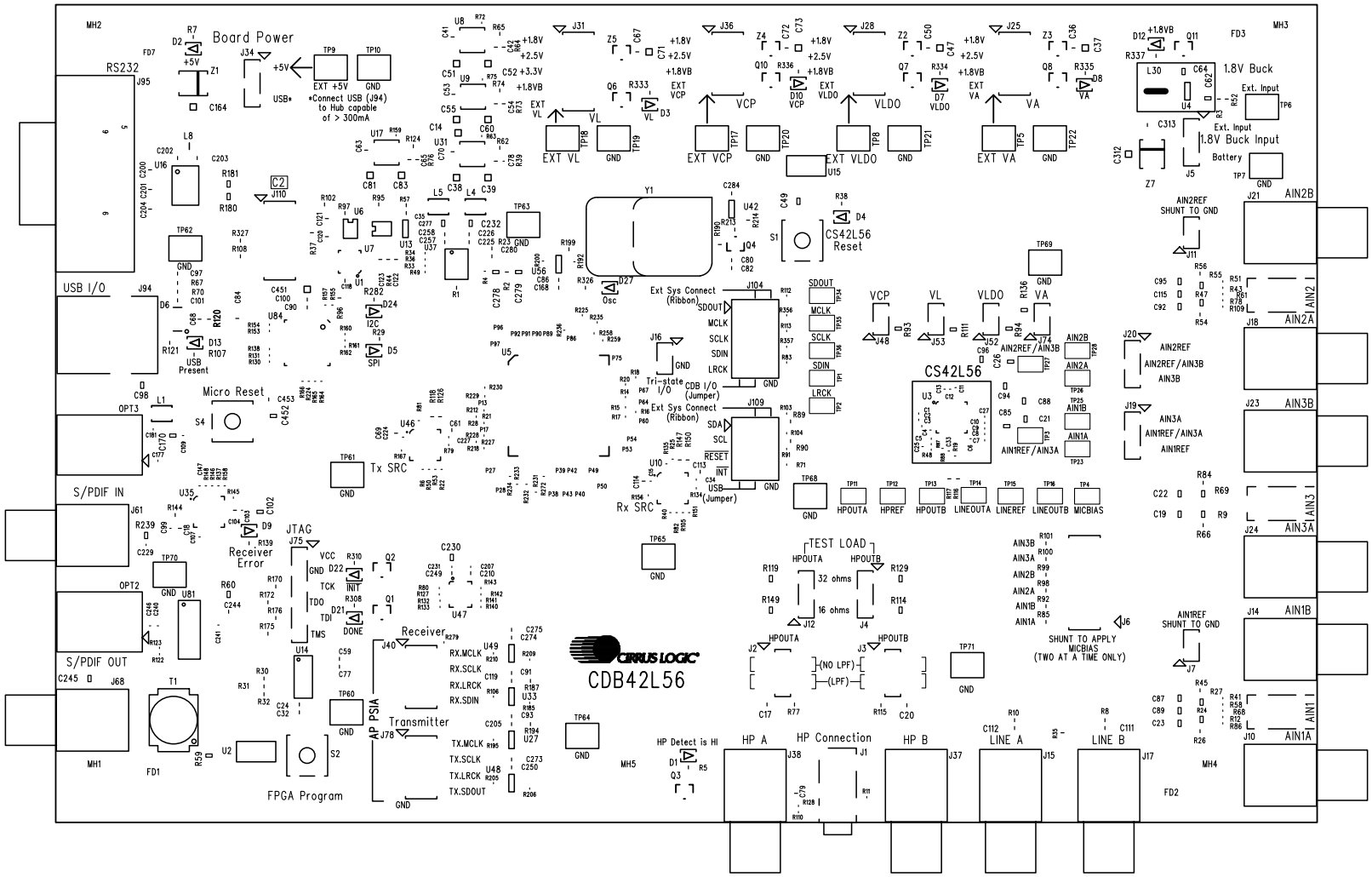


Figure 40. Silk Screen

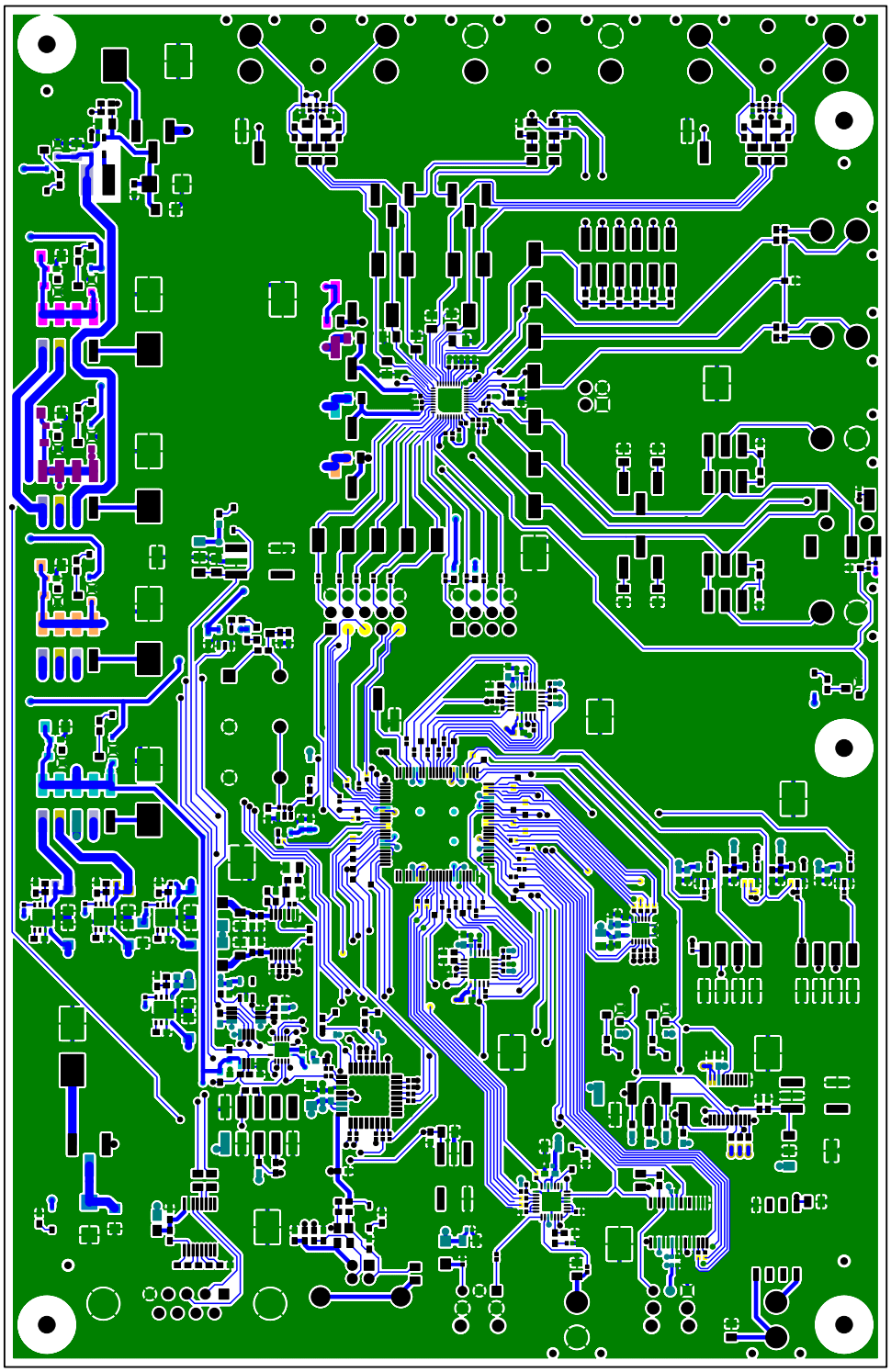


Figure 41. Top-Side Layer

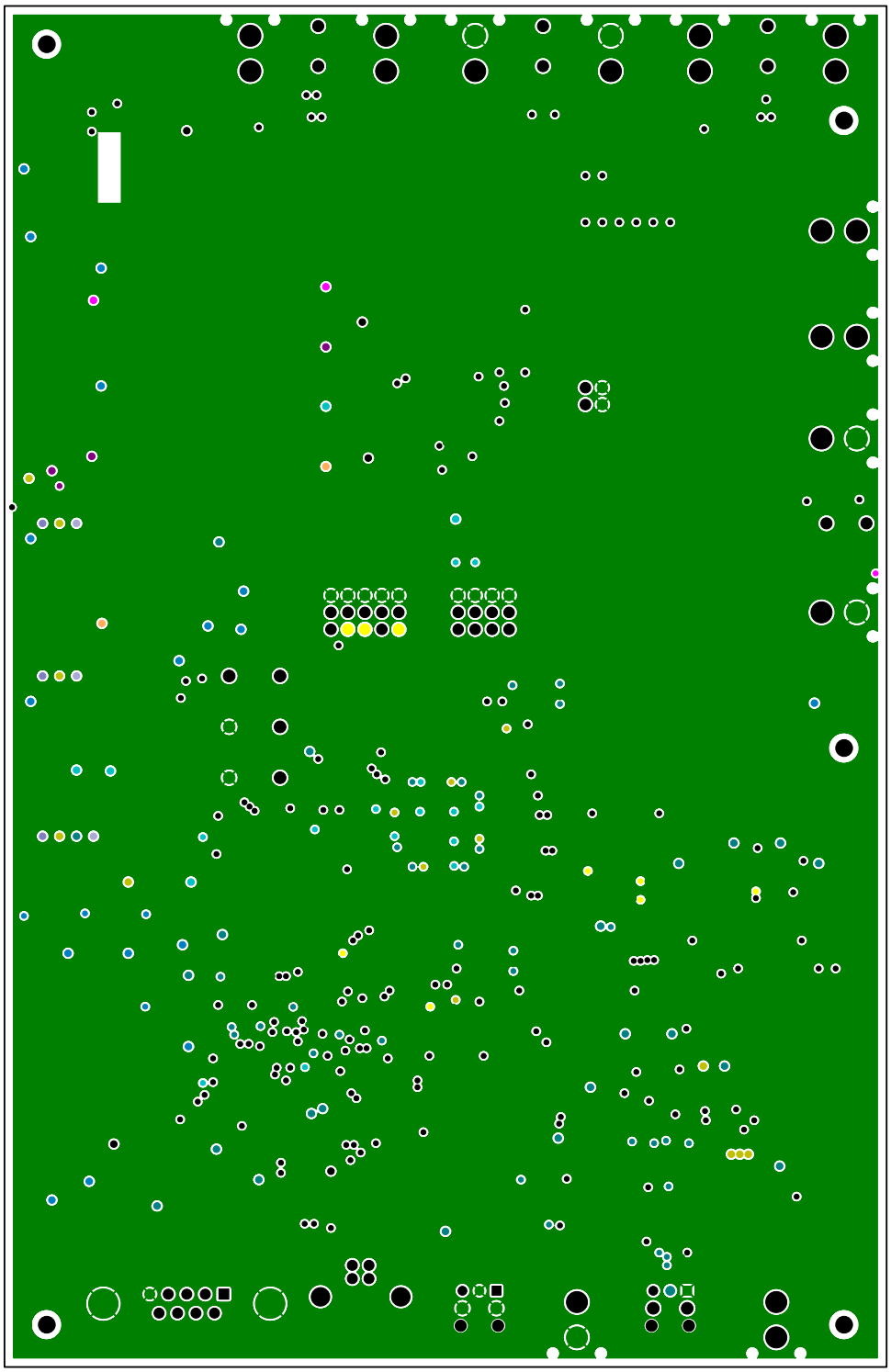


Figure 42. GND (Layer 2)

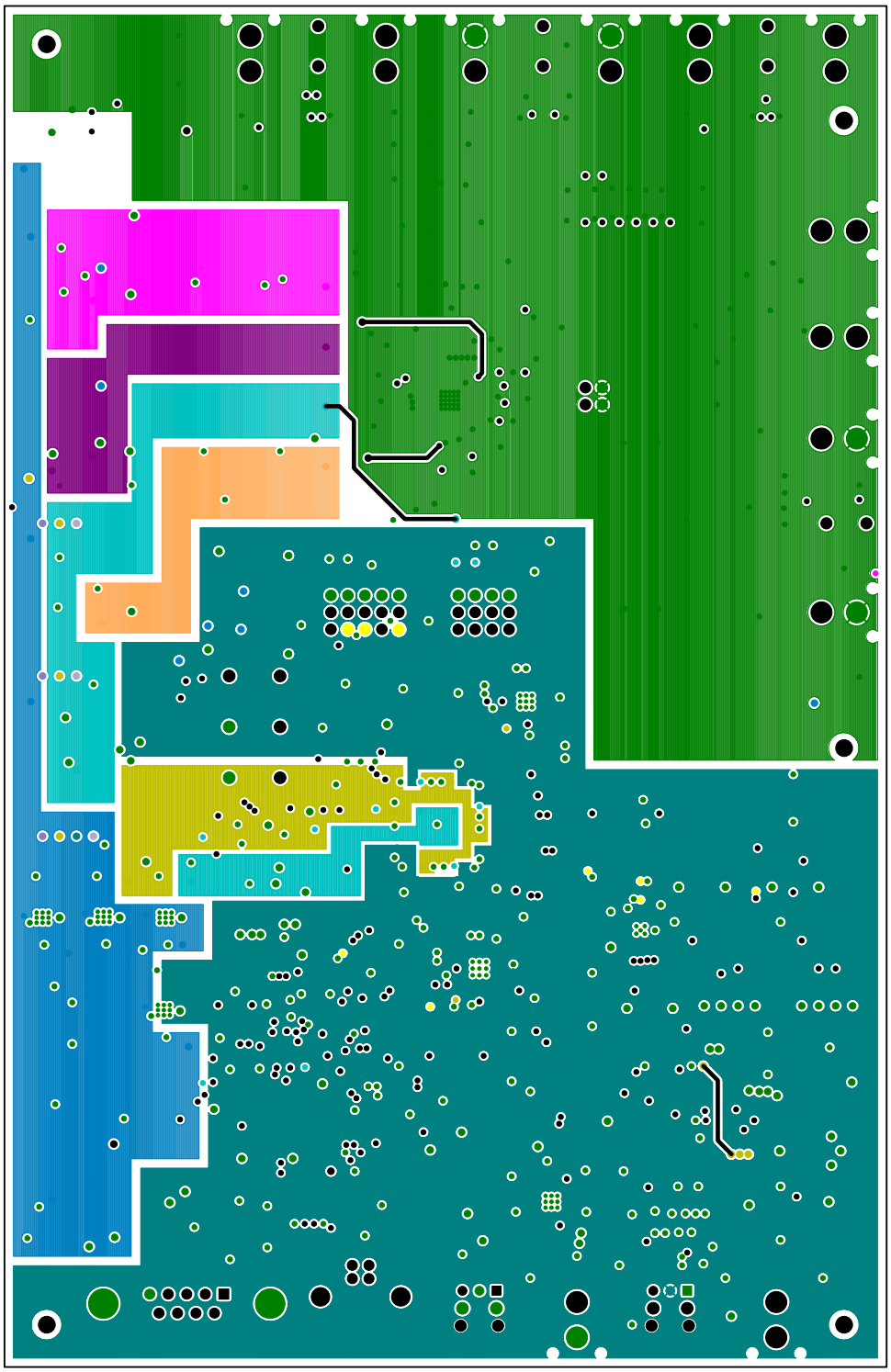


Figure 43. Power (Layer 3)

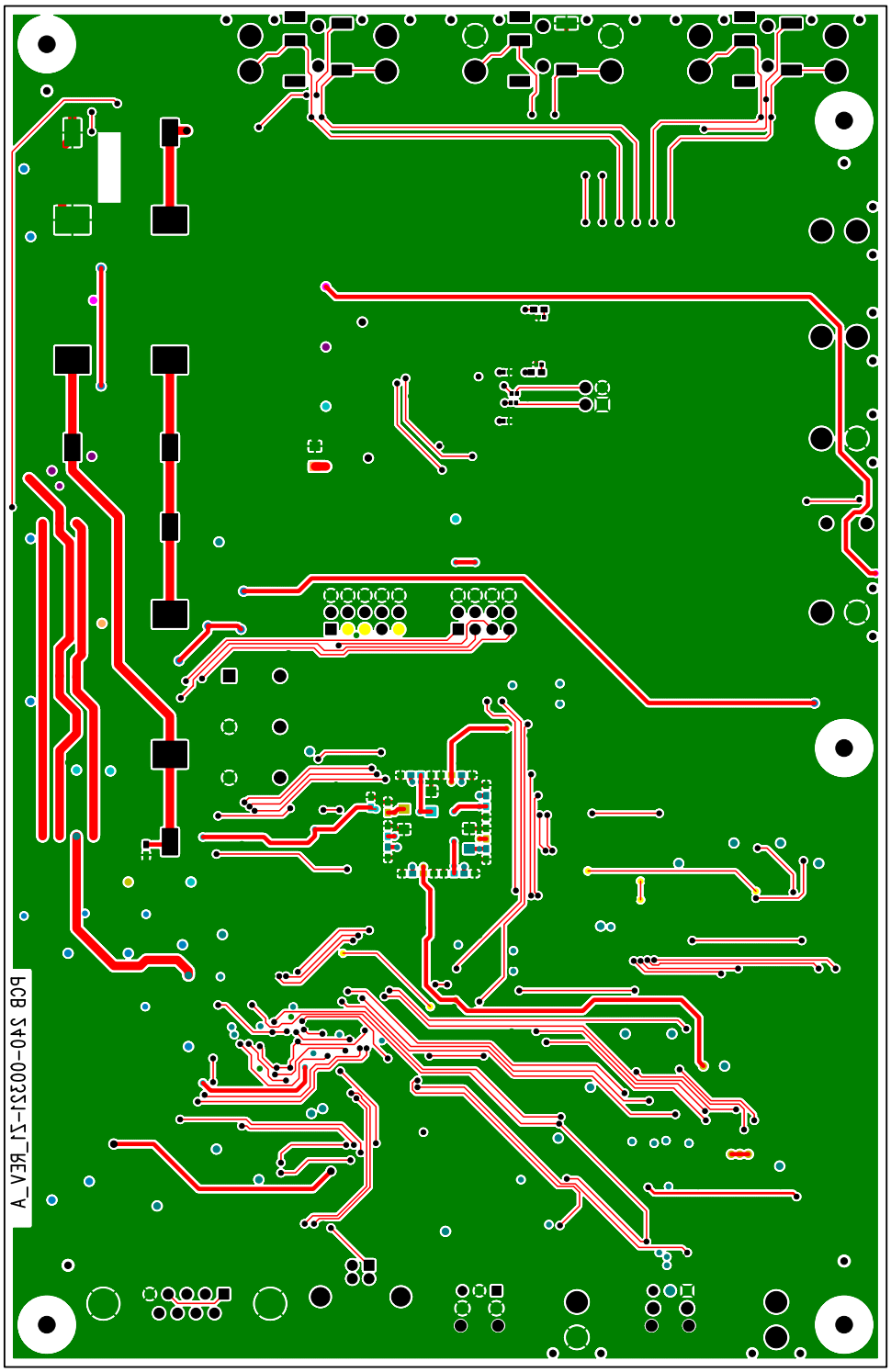


Figure 44. Bottom Side Layer

10.REVISION HISTORY

Revision	Changes
DB1	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.