Evaluation Board for CS4344

Features
- Demonstrates recommended layout and grounding arrangements
- CS8416 receives S/PDIF, & EIAJ-340 compatible digital audio
- Header for external PCM audio
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

Description
The CDB4344 evaluation board is an excellent means for quickly evaluating the CS4344 24-bit, 10 pin stereo D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, and a power supply. Analog line level outputs are provided via RCA phono jacks.

The CS8416 digital audio receiver I.C. provides the system timing necessary to operate the Digital-to-Analog converter and will accept S/PDIF, and EIAJ-340-compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION
CDB4344  Evaluation Board
TABLE OF CONTENTS

1. CS4344 DIGITAL TO ANALOG CONVERTER ........................................ 3
2. CS8416 DIGITAL AUDIO RECEIVER ............................................... 3
3. INPUT FOR CLOCKS AND DATA .................................................. 3
4. POWER SUPPLY CIRCUITRY ...................................................... 3
5. GROUNDING AND POWER SUPPLY DECOUPLING ............................ 4
6. ANALOG OUTPUT FILTERING ...................................................... 4
7. ERRATA ..................................................................................... 5

LIST OF FIGURES

Figure 1. System Block Diagram and Signal Flow ................................. 6
Figure 2. CS4344 and outputs .......................................................... 7
Figure 3. CS8416 S/PDIF Input .......................................................... 8
Figure 4. PCM Input Header .............................................................. 9
Figure 5. Power Supply Connections ............................................... 10
Figure 6. Silkscreen Top ................................................................. 11
Figure 7. Top Side ........................................................................... 12
Figure 8. Bottom Side ..................................................................... 13
CDB4344 SYSTEM OVERVIEW

The CDB4344 evaluation board is an excellent means of quickly evaluating the CS4344. The CS8416 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply external PCM clocks and data through a header for system development.

The CDB4344 schematic has been partitioned into 4 schematics shown in Figures 2 through 5. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

1. CS4344 DIGITAL TO ANALOG CONVERTER
A description of the CS4344 is included in the CS4344 datasheet.

2. CS8416 DIGITAL AUDIO RECEIVER
The system receives and decodes the standard S/PDIF data format using a CS8416 Digital Audio Receiver, Figure 3. The outputs of the CS8416 include a serial bit clock, serial data, left-right clock, and a 128/256 Fs master clock. The CS8416 data format is fixed to I²S (can be changed with R42 and R47). The operation of the CS8416 and a discussion of the digital audio interface is included in the CS8416 datasheet.

The evaluation board has been designed such that the input can be either optical or coax, see Figure 3. However, both inputs cannot be driven simultaneously.

The right hand switch of S2 sets the output MCLK to LRCK ratio of the CS8416. This switch should be set to 256 (closed) for inputs Fs\leq96 \text{ kHz} and 128 (open) for Fs\geq64 \text{ kHz}. The 8416 must be manually reset using RX_RST (S1) when this switch is changed.

3. INPUT FOR CLOCKS AND DATA
The evaluation board has been designed to allow interfacing to external systems via the header J9. Header J9 allows the evaluation board to accept externally generated PCM clocks and data. The schematic for the clock/data input is shown in Figure 4. The left hand switch of S2 selects the source as either CS8416 (closed) or header J9 (open).

Please see the CS4344 datasheet for more information.

4. POWER SUPPLY CIRCUITRY
Power is supplied to the evaluation board by three binding posts (GND, +5V, and ‘+3.3V to +5V’), see Figure 5. The ‘+3.3V to +5V’ which supplies VA can be jumpered to a +3.3 V regulator or the +5V binding post. The VA supply should be set to the recommended values stated in the CS4344 datasheet.

**WARNING:** Refer to the CS4344 datasheet for maximum allowable voltages levels. Operation outside of this range can cause permanent damage to the device.
5. GROUNDING AND POWER SUPPLY DECOUPLING

As with any high performance converter, the CS4344 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 2 details the connections to the CS4344 and Figures 6, 7, and 8 show the component placement and top and bottom layout. The decoupling capacitors are located as close to the CS4344 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

6. ANALOG OUTPUT FILTERING

The analog output on the CDB4344 has been designed according to the CS4344 datasheet. This output circuit includes an AC coupling cap and a single pole R and C. An additional load resistance may be added by stuffing R10 and R26 to test the CS4344’s load driving capability.

<table>
<thead>
<tr>
<th>CONNECTOR</th>
<th>INPUT/OUTPUT</th>
<th>SIGNAL PRESENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5V</td>
<td>Input</td>
<td>+ 5 V power</td>
</tr>
<tr>
<td>GND</td>
<td>Input</td>
<td>Ground connection from power supply</td>
</tr>
<tr>
<td>+3.3V to +5V</td>
<td>Input</td>
<td>+3.3 V to +5 V positive supply for the CS4344 VA power</td>
</tr>
<tr>
<td>S/PDIF INPUT - J5</td>
<td>Input</td>
<td>Digital audio interface input via coax</td>
</tr>
<tr>
<td>S/PDIF INPUT - OPT1</td>
<td>Input</td>
<td>Digital audio interface input via optical</td>
</tr>
<tr>
<td>PCM INPUT - J9</td>
<td>Input</td>
<td>Input for master, serial, left/right clocks and serial data</td>
</tr>
<tr>
<td>LEFT_OUT and RIGHT_OUT</td>
<td>Output</td>
<td>RCA line level analog outputs</td>
</tr>
</tbody>
</table>

Table 1. System Connections
## 7. ERRATA

### CDB4344 Revision B.0

Switch S2 is oriented incorrectly on some boards (if open is away from binding posts) and thus the 0 and 1 labels above and below are incorrect. Using closed for 0 and open for 1, the table next to the switch will be correct.
Figure 1. System Block Diagram and Signal Flow

CS4344

Left Channel Output

Right Channel Output

Figure 2

Figure 5

Power

Figure 2

8416 Digital Audio Receiver

Figure 3

PCM Inputs

Figure 4

Reset Circuit

Figure 2
Figure 2. CS4344 and outputs

- Single pole -3dB at 103kHz.
  - 0.1dB at 16kHz.
  - 0.18dB at 20kHz.

Substitute with 2.2nF
- Single pole -3dB at 126kHz.
  - 0.1dB at 20kHz.
Figure 3. CS8416 S/PDIF Input

<table>
<thead>
<tr>
<th>CS4345</th>
<th>CS4344</th>
<th>CS4346</th>
<th>Notes:</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX_SSEL0</td>
<td>RX_SSEL1</td>
<td>RX_JWCLK</td>
<td>Left Justified 24bit</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>RX_JWCLK must be 1 for 96kHz and 192kHz S/PDIF</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CS4345</th>
<th>CS4346</th>
<th>Notes:</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>d</td>
<td>d</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Right Justified 24bit</td>
</tr>
</tbody>
</table>

d = don't care
0 = 0 Ohm
1 = No Pop
Figure 4. PCM Input Header

*Internal SCLK mode supported only through EXT DAI
Figure 5. Power Supply Connections
Figure 6. Silkscreen Top
Figure 7. Top Side
Figure 8. Bottom Side
## REVISION HISTORY

<table>
<thead>
<tr>
<th>Release</th>
<th>Date</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB1</td>
<td>DEC 2003</td>
<td>Initial Release</td>
</tr>
<tr>
<td>DB2</td>
<td>JUN 2004</td>
<td>Changed C29 in Figure 2 on page 7 from 3.3 to 10 $\mu$F to improve popguard performance</td>
</tr>
</tbody>
</table>

---

**Contacting Cirrus Logic Support**

For all product questions and inquiries contact a Cirrus Logic Sales Representative. To find one nearest you go to www.cirrus.com

---

**IMPORTANT NOTICE**

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN AIRCRAFT SYSTEMS, MILITARY APPLICATIONS, PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS (INCLUDING MEDICAL DEVICES, AIRCRAFT SYSTEMS OR COMPONENTS AND PERSONAL OR AUTOMOTIVE SAFETY OR SECURITY DEVICES). INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERstood TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.