# Evaluation Board for CS4352

## Features
- Demonstrates Recommended Layout And Grounding Arrangements
- CS8416 Receives S/PDIF, & EIAJ-340- Compatible Digital Audio
- Headers for External PCM Audio
- Requires Only a Digital Signal Source and Power Supplies for a Complete Digital-to-Analog Converter System

## Description
The CDB4352 evaluation board is an excellent means for quickly evaluating the CS4352 24-bit, high-performance stereo D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, and a power supply. Analog line-level outputs are provided via RCA phono jacks.

The CS8416 digital audio receiver IC provides the system timing necessary to operate the Digital-to-Analog converter and will accept S/PDIF and EIAJ-340-compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

## Ordering Information
- CDB4352 Evaluation Board
CDB4352

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1. CDB4352 SYSTEM OVERVIEW

The CDB4352 evaluation board is an excellent means of quickly evaluating the CS4352. The CS8416 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply external PCM clocks and data through a header for system development.

The CDB4352 schematic has been partitioned into five schematics, as shown in Figures 32 through 36. Each partitioned schematic is represented in the system diagram shown in Figure 31. Notice that the system diagram also includes the interconnections between the partitioned schematics.

2. CS4352 DIGITAL-to-ANALOG CONVERTER

A description of the CS4352 is included in the CS4352 datasheet.

3. CS8416 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8416 Digital Audio Receiver, Figure 35. The outputs of the CS8416 include a serial bit clock, serial data, left-right clock, and a 128/256 Fs master clock. The CS8416 data format is fixed to I²S. The operation of the CS8416 and a discussion of the digital audio interface is included in the CS8416 datasheet.

The evaluation board has been designed such that the input can be either optical or coaxial, see Figure 35. However, both inputs cannot be driven simultaneously.

Position 2 of S1 sets the output MCLK to LRCK ratio of the CS8416. This switch should be set to 256 (LO) for input Fs<=48 kHz and can be either 256 (LO) or 128 (HI) for Fs>48 kHz.

4. INPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the header J13. Header J13 allows the evaluation board to accept externally generated PCM clocks and data. The schematic for the clock/data input is shown in Figure 34. Switch position 1 of S1 selects the source as either CS8416 or header J13.

Please see the CS4352 datasheet for more information.

5. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by three binding posts (GND, VL, and VA_H), see Figure 36. The VL supply can be jumpered to a +3.3 V regulator or provided externally through the VL binding post. VD and VA is normally supplied by the 3.3 V regulator but can be disconnected using J4 and J6 and then have external voltage applied to the VD and VA test points. The +5 V supply (which powers the regulators for this board) is normally supplied by a 5 V regulator but can be supplied externally by removing J7 and applying 5 V to TP8.

Power consumption of the CS4352 can be measured through the voltage drop at J8, J9, J10, and J11 when the shunts are removed.

**WARNING:** Refer to the CS4352 datasheet for maximum allowable voltages levels. Operation outside of this range can cause permanent damage to the device.
6. GROUNDING AND POWER SUPPLY DECOUPLING

As with any high-performance converter, the CS4352 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 32 details the connections to the CS4352 and Figures 37, 38, and 39 show the component placement and top and bottom layout. The decoupling capacitors are located as close to the CS4352 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

7. HARDWARE CONTROL

The CDB4352 is controlled through settings on switch S1. This allows for configuration of the board without a PC. A switch is provided for CS8416 MCLK speed, clock and data source for the board, and the hardware mode configuration of the CS4352.

8. ANALOG OUTPUT FILTERING

The analog output on the CDB4352 has been designed according to the CS4352 datasheet. This output circuit includes an AC coupling cap, the BJT mute circuit, and a single-pole R and C.

<table>
<thead>
<tr>
<th>CONNECTOR</th>
<th>INPUT/OUTPUT</th>
<th>SIGNAL PRESENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VL</td>
<td>Input</td>
<td>+ 1.5 V to +3.3 V power for the CS4352 serial interface</td>
</tr>
<tr>
<td>VA_H</td>
<td>Input</td>
<td>+9 V to +12 V positive supply for the CS4352 high-voltage analog and the CDB4352 regulators</td>
</tr>
<tr>
<td>GND</td>
<td>Input</td>
<td>Ground connection from power supply</td>
</tr>
<tr>
<td>SPDIF INPUT - J16</td>
<td>Input</td>
<td>Digital audio interface input via coaxial cable</td>
</tr>
<tr>
<td>SPDIF INPUT - OPT1</td>
<td>Input</td>
<td>Digital audio interface input via optical cable</td>
</tr>
<tr>
<td>PCM INPUT - J13</td>
<td>Input</td>
<td>Input for master, serial, left/right clocks and serial data</td>
</tr>
<tr>
<td>AOUTA and AOUTB</td>
<td>Output</td>
<td>RCA line-level analog outputs</td>
</tr>
</tbody>
</table>

Table 1. System Connections
9. PERFORMANCE PLOTS

Figure 1. FFT (48 kHz, 0 dB)

Figure 2. FFT (48 kHz, -60 dB)

Figure 3. FFT (48 kHz, No Input)

Figure 4. FFT (48 kHz Out-of-Band, No Input)

Figure 5. 48 kHz, THD+N vs. Input Freq

Figure 6. 48 kHz, THD+N vs. Level
Figure 7. 48 kHz, Fade-to-Noise Linearity

Figure 8. 48 kHz, Frequency Response

Figure 9. 48 kHz, Crosstalk

Figure 10. 48 kHz, Impulse Response

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Figure 22. FFT (192 kHz, -60 dB)

Figure 23. FFT (192 kHz, No Input)

Figure 24. FFT (192 kHz Out-of-Band, No Input)
Figure 25. 192 kHz, THD+N vs. Input Freq

Figure 26. 192 kHz, THD+N vs. Level

Figure 27. 192 kHz, Fade-to-Noise Linearity

Figure 28. 192 kHz, Frequency Response

Figure 29. 192 kHz, Crosstalk

Figure 30. 192 kHz, Impulse Response
Table 2. CDB4352 Jumper Settings

<table>
<thead>
<tr>
<th>JUMPER / SWITCH</th>
<th>PURPOSE</th>
<th>POSITION</th>
<th>FUNCTION SELECTED</th>
</tr>
</thead>
<tbody>
<tr>
<td>J7</td>
<td>Selects source of voltage for the +5V supplies</td>
<td>+5 V</td>
<td>Voltage source is +5 V test point (TP8) Voltage source is +5 V regulator *+5V_REG</td>
</tr>
<tr>
<td>J4</td>
<td>Selects source of voltage for the VD supplies</td>
<td>VD</td>
<td>Voltage source is VD test point (TP2) Voltage source is +3.3 V regulator *+3.3V_REG</td>
</tr>
<tr>
<td>J5</td>
<td>Selects source of voltage for the VL supply</td>
<td>VL</td>
<td>Voltage source is VL binding post Voltage source is +3.3 V regulator *+3.3V_REG</td>
</tr>
<tr>
<td>J6</td>
<td>Selects source of voltage for the VA supply</td>
<td>VA</td>
<td>Voltage source is VA test point (TP7) Voltage source is +3.3 V regulator *+3.3V_REG</td>
</tr>
<tr>
<td>J8</td>
<td>Current measure for VD</td>
<td>*shunted</td>
<td>When shunt is removed, the voltage can be measured across a fixed resistance to determine current.</td>
</tr>
<tr>
<td>J9</td>
<td>Current measure for VL</td>
<td>*shunted</td>
<td>When shunt is removed, the voltage can be measured across a fixed resistance to determine current.</td>
</tr>
<tr>
<td>J10</td>
<td>Current measure for VA</td>
<td>*shunted</td>
<td>When shunt is removed, the voltage can be measured across a fixed resistance to determine current.</td>
</tr>
<tr>
<td>J11</td>
<td>Current measure for VA_H</td>
<td>*shunted</td>
<td>When shunt is removed, the voltage can be measured across a fixed resistance to determine current.</td>
</tr>
<tr>
<td>S1</td>
<td>Sets clock source, CS8416 clock speed, and CS4352 settings</td>
<td>*1 = open position 1: 0 = external clock source, 1 = CS8416 *2, 3, 4, 5 = closed position 2: 0 = 8416 MCLK is 256xFs, 1 = 128xFs Position 3,4,5: see CS4352 datasheet</td>
<td></td>
</tr>
<tr>
<td>S2</td>
<td>Reset</td>
<td>-</td>
<td>Enables reset for CS4352 and CS8416 when pressed</td>
</tr>
<tr>
<td>J12, J17</td>
<td>Mute Disable</td>
<td>*LED MUTE</td>
<td>Bypasses muting to turn on LED Normal muting circuit</td>
</tr>
</tbody>
</table>

*Default Factory Settings.

10. DESIGN NOTE

10.1 CDB4352 Revision A.0

D2 has been removed and shorted and R2 has been removed.
The serial audio decode table for S1 is incorrect. ‘01’ should be RJ-24 and ‘10’ should be LJ
The polarity of the silkscreen for Z1, Z2, Z3, Z4, and Z5 is incorrect
The CS4352 revision is A1

10.2 CDB4352 Revision B.0

No errors at this time
11. SCHEMATICS

Figure 31. System Block Diagram and Signal Flow

- 8416 Digital Audio Receiver
  - MCLK
  - SCLK
  - LRCK
  - SDIN
  Figure 35

- PCM Inputs
  Figure 34

- CS4352
  Figure 32

- Hardware Switch
  Figure 34

- Power
  Figure 36

- Reset Circuit

- Channel A Outputs and Mute
  Figure 33

- Channel B Outputs and Mute
  Figure 33

Figure 34

Figure 33
Figure 33. Analog Outputs
Figure 34. PCM Input Headers
Figure 35. CS8416 S/PDIF Input
Figure 36. Power
Figure 37. Silkscreen Top
### Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

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